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Excalibur Development Kit

with the Nios Embedded Processor

June 2000, ver. 1.0 Data Sheet

Introduction

Altera® users now have a single system-on-a-programmable-chip (SOPC) solution. The Excalibur™ development kit, featuring the Nios™ soft core embedded processor, contains all the tools that hardware and software engineers need to create high-performance systems in Altera programmable logic devices (PLDs). This kit provides a PLD-optimized processor that designers can implement immediately, improving design workflow and speeding time-to-market.

As shown in Figure 1, the Excalibur development kit contains:

Figure 1. Excalibur Development Kit, with the Nios Embedded Processor



- Nios configurable RISC processor core and peripherals
- GNUPro® compiler and debugger from Cygnus®, a Red Hat® company
- The Quartus™ development software
- ByteBlasterMV™ download cable
- Development board populated with the APEX™ EP20K200E device
- SOPC reference design

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Nios Embedded Processor

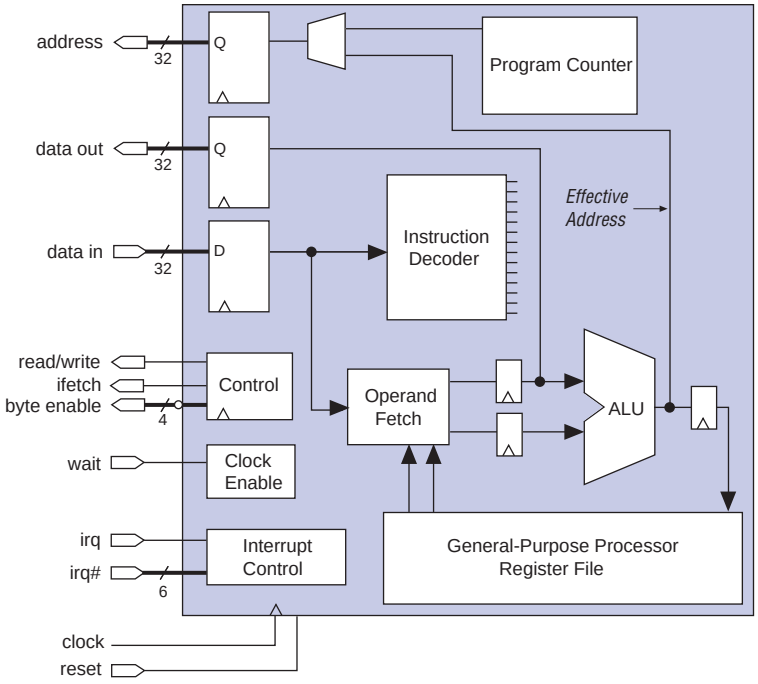
The Nios embedded processor is a fully-integrated soft core processor developed to take advantage of Altera's PLD architecture. This section describes the Nios embedded processor and peripherals included in the Excalibur development kit. Figure 2 on page 3 shows a diagram of the Nios processor.

- Nios embedded processor core
  - 16-bit instruction set
  - Data width of 16 or 32 bits
  - One instruction per clock cycle
  - Support for on-chip and off-chip memory
  - Up to 50 million instructions per second (MIPS) performance
  - Windowed register access for fast interrupt handling
  - Register file with up to 512 32-bit registers
  - Shift depth from 8 to 32 bits
  - Register access to peripherals
- Nios microperipherals
  - Universal asynchronous receiver/transmitter (UART)
  - Parallel input/output (PIO)
  - Timer
  - Memory interfaces to SRAM and FLASH
- Low-cost accessibility
  - Free licensing from the Altera web site
  - Royalty-free
- MegaWizard™ Plug-In interface, which creates and configures the Nios embedded processor core
- SOPC Builder software
  - Generates on-chip peripheral bus
  - Configures peripherals and generates C header files

For more information on the Nios embedded processor, see the *Nios Soft Core Embedded Processor Data Sheet*.

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Figure 2. Nios Embedded Processor



GNUPro Compiler & Debugger

The GNUPro compiler and debugger from Cygnus, a Red Hat company, is an industry-standard compiler and debugger tool suite in use by software developers worldwide. It is an open-source C/C++ development tool suite. Optimized for the Nios embedded processor, the GNUPro compiler and debugger delivers an environment familiar to design engineers, including:

- Optimized C/C++ compiler
- GNU assembler
- Insite debugger
- Binary utilities

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Quartus Programmable Logic Development Tools

The Excalibur development kit, with the Nios embedded processor, includes the Quartus development software. This software allows designers to process multi-million gate designs with advancements never before seen in PLD development tools. To streamline development flows and decrease time-to-market, the Quartus software supports system-level solutions with block-level editing, workgroup computing, and expanded support for megafunctions. In addition, an embedded logic analysis feature allows engineers to verify chip functionality and timing by observing internal and I/O signal values at system clock speeds.

State-of-the-art features make the Quartus software the ideal platform for SOPC designs:

- SOPC methodology with block-level editing, workgroup computing, and expanded support for megafunctions streamlines the development flow and increases productivity.
- An embedded logic analysis solution reduces verification time by enabling engineers to view internal chip signal values while the system is running at speed.
- Seamless interface with third-party electronic design automation (EDA) software tools allows designers to use familiar tools to design for Altera devices.
- The industry's first "Internet-aware" development tool provides up-to-the-minute information and file exchanges, including software updates, license file delivery, and support services across the Internet.
- An unmatched level of technical support effectively makes Altera a member of the design team.
- Support for the APEX 20K device family offers design flexibility and high-performance system-integration functionality.



For more information on the Quartus development software, see the *Quartus Programmable Logic Development System & Software Data Sheet*.

ByteBlasterMV Download Cable

To connect to the development board, the Excalibur development kit includes the ByteBlasterMV parallel port download cable. The ByteBlasterMV download cable is a hardware interface to a standard PC parallel port (known as an LPT port) and drives configuration data to the APEX device. Because design changes are downloaded directly to the APEX device, prototyping is easy and multiple design iterations are accomplished quickly.

The ByteBlasterMV download cable performs the following functions:

- Configures APEX devices
- Supports V_{CC} operation at 3.3 V or 5.0 V

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- Provides a fast and low-cost method for in-system programming
- Interfaces with a standard 25-pin parallel port on PCs
- Uses a 10-pin connector, which is located on the development board

For more information on the ByteBlaster MV Download Cable, see the *ByteBlaster Parallel Port Download Cable Data Sheet*.

Development Board

The Excalibur development kit also includes a comprehensive development board that gives engineers a hardware platform on which they can immediately start developing a system on a programmable chip. Figure 3 shows a diagram of the development board, which incorporates the following components and features:

- APEX EP20K200E device
- Memory
  - On-board FLASH RAM (8M bits)
  - On-board SRAM (256 Kbytes)
  - SDRAM connector
- Communications ports
  - RS-232
  - JTAG
  - Processor trace port
- Expansion ports
  - 32-bit PMC host connector
  - 5.0 V prototype connector
  - 3.3 V prototype connector
- User-configurable LEDs
  - Two seven-segment LEDs
  - Two single-segment LEDs
- User-configurable switches
  - One dual in-line package-8 (DIP-8) switch
  - Four momentary contacts/switches

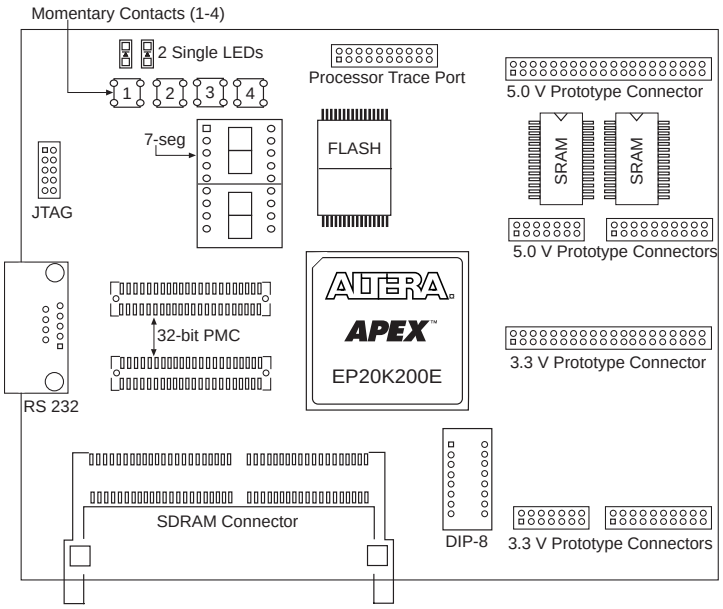
The Nios processor and serial port monitor are pre-loaded in FLASH and boot on power-up. The monitor provides the interface to the GNUPro debugger, as well as facilities for user code download to SRAM or FLASH. The Nios embedded processor core is supported by 256 Kbytes of zero-wait-state SRAM, providing a complete software development environment. Using the JTAG port, custom SOPC solutions can also be loaded in FLASH to create a stand-alone custom application. The development board comes with an international power supply, and software debug facilities are provided by the on-board processor trace port.

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The development board can be expanded to support a wide range of interfaces through the prototype connectors, PCI mezzanine connectors, or the SDRAM connectors. Altera provides solution packages from the IP MegaStore at **http://www.altera.com/IPmegastore**.

For more information on the development board, see *The Nios Development Board User Guide.*

Figure 3. Excalibur Development Board



SOPC Reference Design

The Excalibur development kit includes a reference design that is a complete SOPC configuration, including a processor core, peripherals, and an on-chip bus. The reference design is pre-loaded in on-board FLASH, and boots on power-up, allowing software engineers to begin developing their code immediately. It also comes as a Quartus project that can be customized by the user. Peripherals included in the reference design are:

- UART
- Timer
- External memory interface (SRAM, FLASH)
- Internal memory interface (ESB)
- PIO

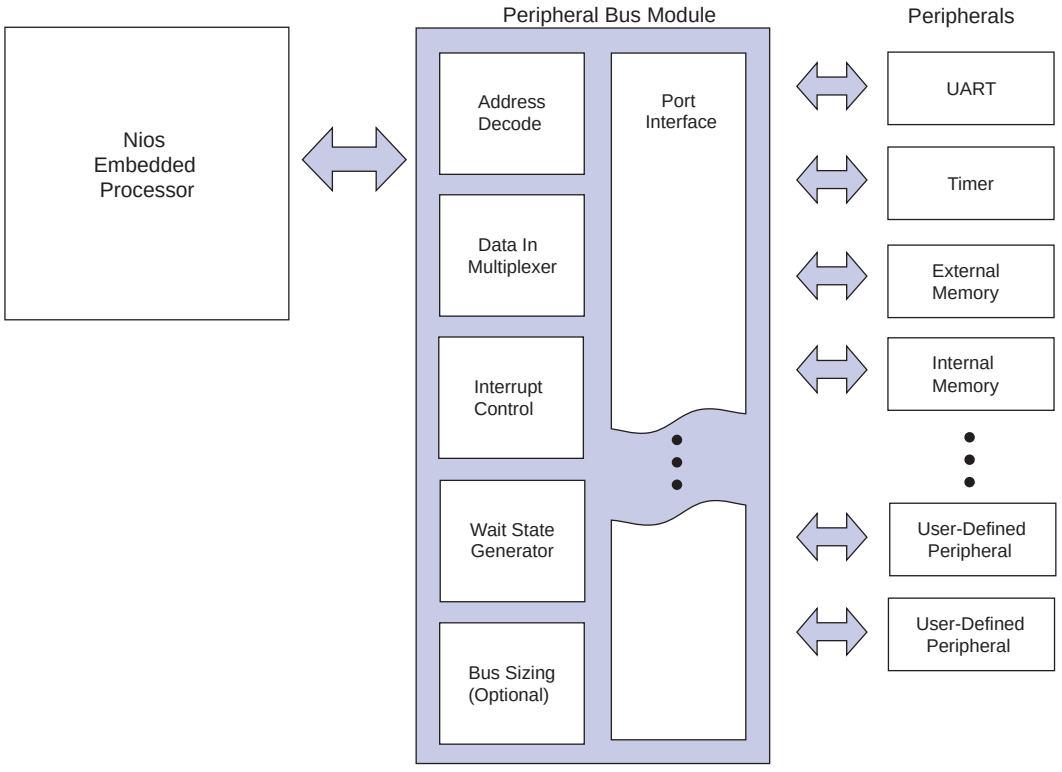
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The Nios processor communicates with the peripheral devices through the peripheral bus module (PBM). The PBM is automatically generated by the SOPC builder software based on peripheral requirements supplied by the user. These include:

- Address decode—Maps the address for each peripheral and generates the chip select signals
- Data in multiplexer—Provides data bus connection between each peripheral and the Nios core. Provides read-only, read-write, and write-only access for each peripheral
- Interrupt control—Allows the user to assign a hardware interrupt to each peripheral
- Wait state generator—Assigns the number of wait states required by each peripheral
- Bus sizing—An optional dynamic bus sizing module provides direct interface to 8-, 16-, and 32-bit peripherals

Figure 4 shows a block diagram of the reference design.

Figure 4. SOPC Reference Design Peripherals



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Conclusion

The Excalibur development kit, with the Nios embedded processor, gives designers the flexibility they need and provides the familiarity of the industry-standard GNUPro compiler and debugger. By integrating the Nios embedded processor onto the APEX device and offering the feature-rich Excalibur development kits, Altera provides the flexibility and time-to-market needed for system integration in SOPC designs.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
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lit_req@altera.com

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