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Evaluation Board

UDTech Taishan440GX

User's Manual

Technical Support: taishansupport@amcc.com

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2007-07-18	Modified PLB clock to 200MHz.
2007-8-20	Modified the 200MHz parameter of DDR controller
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1 Board Architecture

The PPC440GX contains a high-performance RISC processor core, DDR SDRAM controller, PCI-X bus interface, Ethernet interface, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O. Utilizing this processor, features of the board include 256MB SDRAM, 64MB flash for boot and application, an IIC serial EEPROM stored the strap configuration data, two 64-bit PCIX slots, a expansion interface connector (EBC connector), built-in Ethernet support, a 16X2 character LCD module, a CPLD, two serial ports, and a IIC serial Temperature sensor.

Figure 1-1 illustrates the board architecture, Subsequent paragraphs discuss aspects of the diagram in more detail.

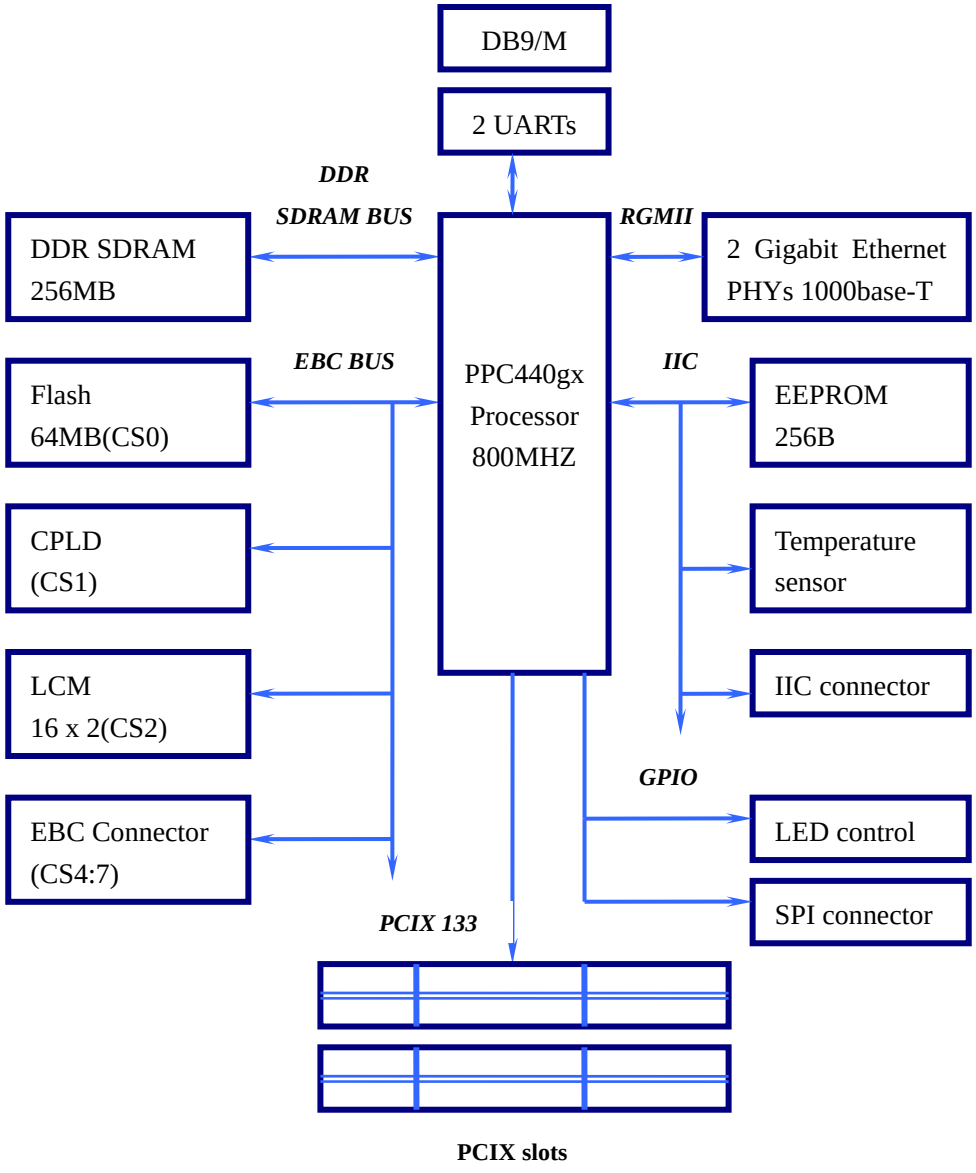


Figure 1-1. Board architecture

Figure 1-2 shows the top view board layout, the figure shows the headers unpopulated.

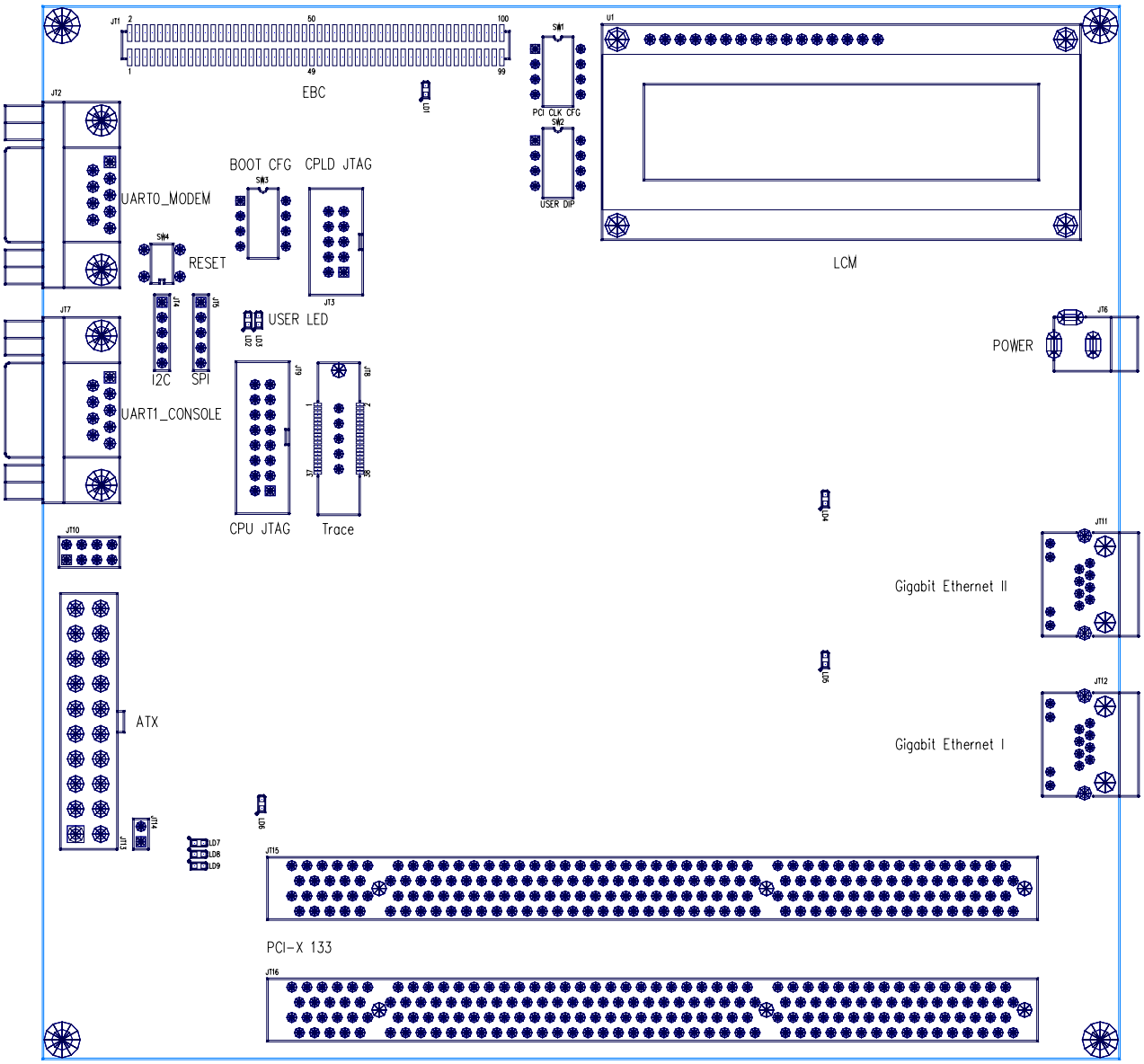


Figure 1-2. Top view board layout

1.1 Board Clocking

The clock architecture of the board is illustrated in figure 1-3. Note that the clock PLL is reset only at board power-on, not by any other reset source.

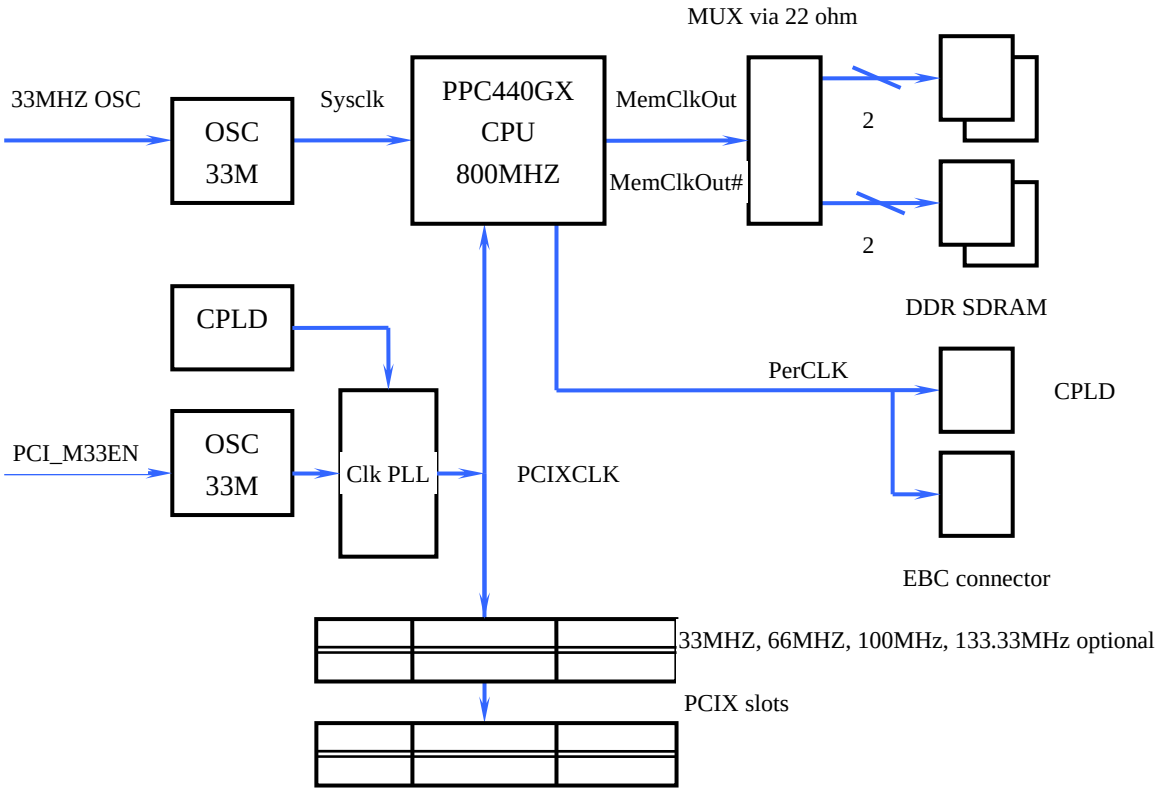


Figure 1-3. Clock architecture of the board

During power-on reset, the CPLD will detect the PCIX card capability automatically. And then it will set the corresponding PCI clock frequency.

1.2 Strapping Options

The PPC440GX processor configures itself at reset based on strapping options. On the board, these options can be selected using slide switch SW3.

The strapping options for the board are shown in Table 1-1. Table 1-2 shows the switch settings for each option. Figure 1-4 shows SW3 Factory Default Setting.

Table 1-1. Board Strapping Options

UART0_DCD#	UART0_DSR#	GMC1TXCTL	Option
0	**0**	**0**	Strapping Option A SysClk - 33 MHz VCO - 1000 MHz CPU - 500 MHz PLB - 166 MHz OPB - 83 MHz PerClk - 83 MHz Boot ROM Location - EBC Boot width - 16 bit
0	**X**	**1**	Strapping Option B SysClk - 33 MHz VCO - 933MHz CPU - 466 MHz PLB - 133 MHz OPB - 66 MHz PerClk - 66 MHz Boot ROM Location - EBC Boot width - 8 bit The PPC440GX defaults to bootstrap option B if the IIC bootstrap controller is unable to read the serial ROM.
0	**1**	**0**	Strapping Option C SysClk - 33 MHz VCO - 1000 MHz CPU - 500 MHz PLB - 166 MHz OPB - 83 MHz PerClk - 83 MHz Boot ROM Location - EBC Boot width - 32 bit
1	**0**	**0**	Strapping Option D SysClk - 33 MHz VCO - 1000 MHz CPU - 500 MHz PLB - 166 MHz OPB - 83 MHz PerClk -83 MHz Boot ROM Location - PCI
1	**0**	**1**	Strapping Option E IIC Bootstrap controller enabled, serial ROM address 0b1010100
1	**1**	**0**	Reserved.

1	**1**	**1**	Strapping Option F IIC Bootstrap controller enabled, serial ROM address 0b1010000; The default configuration is 800MHz CPU and 200MHz PLB. Please refer to the table 3-1.

Table 1-2. SW3 switch settings

Switch	OFF	ON	Description
1	**1**	**0**	BOOT_CFG0, the CPU strapping pin UART0_DCD#
2	**1**	**0**	BOOT_CFG1, the CPU strapping pin UART0_DSR#
3	**1**	**0**	BOOT_CFG2, the CPU strapping pin GMC1TXCTL
4	**1**	**0**	Unused

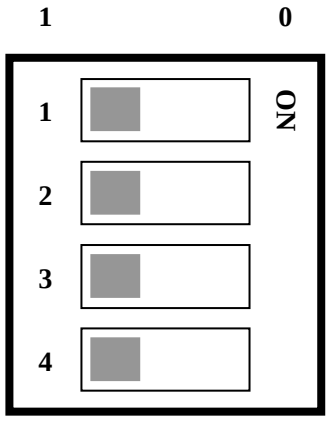


Figure 1-4. SW3 Factory Default Setting (Strapping Option F)

1.3 DDR SDRAM Design

The double data rate (DDR) SDRAM memory controller of PPC440GX supports x8, x16, x32, and x64 registered and unregistered DDR SDRAMs, and discrete devices, for chips that support 1 DQS per byte. The controller supports page mode operation with bank interleaving always active and can maintain up to eight open pages. The controller supports up to four 512 MB logical banks in limited configurations, providing memory up to 2 GB. Global memory timings, address and bank sizes, and memory addressing modes are programmable. The DDR SDRAM controller supports 100, 133, 166, and 200 MHz.

On this board, SDRAM is provided by four chips which are addressed by one chip select. Size of chip is 64MB.

1.4 PCI BUS

The PCI-X interface allows connection of PCI and PCI-X devices to the PowerPC processor and local memory. This interface is designed to Version 1.0a of the PCI-X Specification and supports 32- and 64-bit PCI-X buses. PCI 32/64-bit conventional mode, compatible with PCI Version 2.3, is also supported.
The PCI-X interface can be the PCI Host Bus Bridge or an Adapter Device's PCI interface. But on this board the PCI Host Bus Bridge is only supported.

On the board, the IDSEL signal of PCI slot 0 is AD17, and the IDSEL signal of PCI slot 1 is AD18.

During power-on reset, the CPLD will detect the PCI card capability automatically. And then it will set the corresponding PCI clock frequency. 33.33MHz, 66.66MHz, 100MHz, and 133.33MHz frequency are supported. The switch SW1 will influence the behavior of CPLD when detecting the PCI card capability. Table 1-3 shows the switch SW1 settings. Figure 1-5 shows SW1 Factory Default Setting.

Table 1-3. SW1 switch settings

Switch	OFF	ON	Description
1	**1**	**0**	AUTO_DETECT_EN, PCI clock auto-detect enable. When this bit is '1', CPLD will auto-detect the clock range of PCI card and set the PCI clock frequency during reset. When this bit is '0', user can set PCI clock frequency manually.
2	**1**	**0**	Unused.
3	**1**	**0**	PCI_CLK_S1_CFG, see PCI_CLK_S0_CFG.
4	**1**	**0**	PCI_CLK_S0_CFG When AUTO_DETECT_EN = '0' PCI_CLK_S1_CFG PCI_CLK_S0_CFG PCI clock frequency 0 0 33.33MHz 0 1 66.66MHz 1 0 100MHz 1 1 133MHz When AUTO_DETECT_EN = '1', the following list derived from bootstrap configuration SDR0_SDSTP1[PXFS]. That is when CPLD detecting the PCI cards support PCI-X133, the corresponding clock frequency select for the PCI card. PCI_CLK_S1_CFG PCI_CLK_S0_CFG PCI clock frequency 0 0 133MHz 0 1 100MHz 1 0 66.66MHz 1 1 reserved

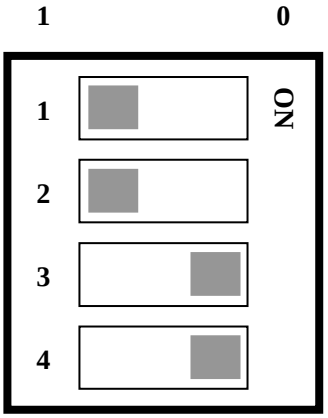


Figure 1-5. SW1 Factory Default Setting

1.5 Ethernet Design

The board provides two 10/100/1000Base-T Ethernet ports, with auto negotiation to 10/100Base-T when connected to networks not capable of 1000Mbps operation.

Ethernet support through the Media Access Control (MAC) layer is provided in the PPC440GX chip. The Physical Layer Device (PHY) and the Physical Medium Dependent sublayer and interface (PMD) are provided on the board. The connections between the MAC and the PHY conform to the Reduced Gigabit Medium Independent Interface (RGMII) specification.

The PHY and PMD sublayer are provided by a Agere Semiconductor ET1011C. There are two PHYs, PHY0 and PHY1, provided. PHY0 is connected with address PHYAD=0b00001, and PHY1 is connected with address PHYAD=0b00011.

The supported media is Category 5 Unshielded Twisted Pair cable (UTP), accessed by means of RJ45 connectors on the board.

1.6 Flash Memory

32-bit flash is used on the board. There are 64MB (2 pieces) flash provided on the board. The PPC440GX boots from the 64MB flash which can be access by chip select PerCS0. Table 1-4 shows the chip select usage.

Table 1-4. Chip Select Usage

CS[4:0]	Usage	Comment
PerCS0	**Flash**	64MB
PerCS1	**CPLD**	-
PerCS2	**LCM**	LCD module
PerCS4 **…** **PerCS7**	**EBC connector**	2 x 50 Header

1.7 16x2 Character LCD module

The 16X2 character LCD module (LCM) is provided on the board. It supports 16 columns by 2-line text display. And it includes a built-in 5 x 7 dot matrix font with the full range of ASCII characters. Backlighting may be turned on or off under program control.

The LCM communicates with the system processor over the general purpose parallel interface. It has 8-bit data bus and 1 address bit (occupying 2 locations) and uses PerCS2. See *Table 1-4, "Chip Select Usage"*, for more details.

1.8 CPLD

The CPLD is provided to read 4-position slide switch (SW2) status and detect the capability of the PCIX card. It furnishes some distributed logic on the board. It communicates with the PPC440GX over the peripheral bus. See *Table 1-4 "Chip Select Usage"*, for more details.
Table 1-5 shows CPLD registers address assignment. Table 1-6 shows CPLD register VER(0:7) usage. Table 1-7 shows CPLD register SWITCH(0:7) usage. Table 1-8 shows CPLD register CTL(0:7) usage. Table 1-9 shows CPLD register STS(0:7) usage.

Table 1-5. CPLD Registers Address Assignment

A[29:31]	register	R/W	Comment
000	**VER(0:7)**	**R**	CPLD version register
001	**SWITCH(0:7)**	**R**	User switch status register
010	**CTL(0:7)**	**R/W**	CPLD control register
011	**STS(0:7)**	**R**	CPLD status register

Table 1-6. CPLD Register VER(0:7) Usage

D[0:7]	R/W	usage	Default	Comment
0:3	**-**	**Reserved**	-	-
4:7	**R**	**Ver**	0100	The board version number

Table 1-7. CPLD Register SWITCH(0:7) Usage

D[7:0]	R/W	usage	Default	Comment
0:3	**-**	**Reserved**	-	-
4	**R**	**User switch 1**	0	SW2
5	**R**	**User switch 2**	0	SW2
6	**R**	**User switch 3**	0	SW2
7	**R**	**User switch 4**	0	SW2

Table 1-8. CPLD Register CTL(0:7) Usage

D[7:0]	R/W	usage	Default	Comment
0:3	**-**	**Reserved**	-	-
4	**R/W**	**Flow control enable**	0	UART1 hardware flow control enabled, default 0, active 1
5	**R/W**	**EBC master enable**	0	EBC master enable, default 0, active 1
6	**R/W**	**LCM backlight enable**	0	LCM backlight control, default 0, active 1
7	**R/W**	**UART1 signals multiplexing**	0	UART1 signals multiplexing, default 0, enable UART1DSR/CTS as DSR and UART1DTR/RTS as DTR

Table 1-9. CPLD Register STS(0:7) Usage

D[7:0]	R/W	usage	Default	Comment
0:3	**-**	**Reserved**	-	-
4:6	**R**	**Reserved**	000	
7	**R**	**PCI clock locked**	0	PCI clock locked, active 0

1.9 GPIO Usage

The PPC440GX has one 32-bit GPIO controller. GPIO provides 32 user-programmable external signals, multiplexed with system-related signal groups including trace outputs, external interrupt inputs, UART interface signals, IIC bus interface signals, and Ethernet MAC interface signals. Table 1-10 shows the GPIO usage.

Table 1-10. GPIO Usage

GPIO[31:0]	Usage	Comment
GPIO0/IRQ0	**IRQ0**	PCI slot interrupt request INTA
GPIO1/IRQ1	**IRQ1**	PCI slot interrupt request INTB
GPIO2/IRQ2	**IRQ2**	PCI slot interrupt request INTC
GPIO3/IRQ3	**IRQ3**	PCI slot interrupt request INTD
GPIO4/IRQ4	**IRQ4**	Gigabit Ethernet PHY I interrupt request
GPIO5/IRQ5	**IRQ5**	Gigabit Ethernet PHY II interrupt request
GPIO6/IRQ6	**IRQ6**	EBC connector interrupt request
GPIO7/IRQ7	**GPIO7**	SPI port DO signal
GPIO8/IRQ8	**GPIO8**	SPI port DI signal
GPIO9/IRQ9	**GPIO9**	SPI port SCLK signal
GPIO10/IRQ10	**GPIO10**	User programmable LED1 control signal
GPIO11/GMCTxClk	**GPIO11**	User programmable LED2 control signal
GPIO12/UART1RX	**UART1RX**	UART1
GPIO13/UART1TX	**UART1TX**	UART1
GPIO14/UART1DSR_CTS	**UART1DSR_CTS**	UART1
GPIO15/UART1RTS_DTR	**UART1RTS_DTR**	UART1
GPIO16/IIC1SCL	**IIC1SCL**	IIC1
GPIO17/IIC1SDA	**IIC1SDA**	IIC1
GPIO18/TrcBS0	**TrcBS0**	RISCTrace port **TrcBS0** signal
GPIO19/TrcBS1	**TrcBS1**	RISCTrace port **TrcBS1** signal
GPIO20/TrcBS2	**TrcBS2**	RISCTrace port **TrcBS2** signal
GPIO21/TrcES0	**TrcES0**	RISCTrace port **TrcES0** signal
GPIO22/TrcES1	**TrcES1**	RISCTrace port **TrcES1** signal
GPIO23/TrcES2	**TrcES2**	RISCTrace port **TrcES2** signal
GPIO24/TrcES3	**TrcES3**	RISCTrace port **TrcES3** signal
GPIO25/TrcES4	**TrcES4**	RISCTrace port **TrcES4** signal
GPIO26/TrcTS0	**TrcTS0**	RISCTrace port **TrcTS0** signal
GPIO27/GMC1RXCLK	**GMC1RXCLK**	RGMII interface signal
GPIO28/GMC1RXD0	**GMC1RXD0**	RGMII interface signal
GPIO29/GMC1RXD1	**GMC1RXD1**	RGMII interface signal
GPIO30/GMC1RXD2	**GMC1RXD2**	RGMII interface signal
GPIO31/GMC1RXD3	**GMC1RXD3**	RGMII interface signal

1.10 Serial EEPROM

The Serial EEPROM (sEEPROM) used on the board is the ATMEL semiconductor AT24C02B. The AT24C02B provides 2048 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 256 words of 8 bits each. It is accessed via a Two-Wire (I2C) serial interface. The IIC address is 0x50. So the PPC440GX can read configuration data from the serial EEPROM after reset. Table 1-11 shows the IIC address usage on this board.

Table 1-11. IIC Address Usage

Device	IIC address	Comment
sEEPROM	**0x50**	
Temperature sensor	**0x48**	
IIC Connector	**User defined**	

1.11 Temperature sensor

The temperature sensor used on the board is the fairchild semiconductor FM75. The FM75 Digital Thermometer and Thermostat provides temperature readings which indicate the temperature of the device. It measures temperatures from －40℃ to ＋125℃. Thermometer accuracy is ±2℃. It communicates with the PPC440GX over a Two-Wire (I2C) serial interface. The IIC address is 0x48. See *Table 1-11, "IIC Address Usage"*, for more detail.

1.12 Expansion Interface Support

A 2x50 header connector is provided to facilitate the attachment of customer prototyping logic. Some primary lines of External Peripheral interface are presented. See *Table 7-2 Expansion Interface Connector Pin Assignment*.

1.13 IIC Port Support

A 1x5 header connector is provided to connect to customer IIC devices. See *Table 7-3 IIC Connector Pin Assignment*.

1.14 SPI Port Support

A 1x5 header connector is provided on GPIOs. See *Table 1-10, "GPIO Usage"* and *Table 7-4 SPI Connector Pin Assignment*, for more details.

1.15 Serial Port

Two serial ports, software compatible with 16750, are included in the PPC440GX chip.
UART 0 provides a full set of modem control lines.
UART 1 provides only Tx, Rx, and optional hardware flow control signals. These lines are multiplexed with GPIO signals. See *Table 7-7 Serial port ConnectorPin List.*

1.16 Power Supply

There are two kinds of power supply. One is standard ATX power supply; another is 120/240V IN 5V/4A OUT power adapter. The PCIX interface is powered by ATX. And other parts are powered by the adapter. Figure 1-6 shows the power architecture on the board.

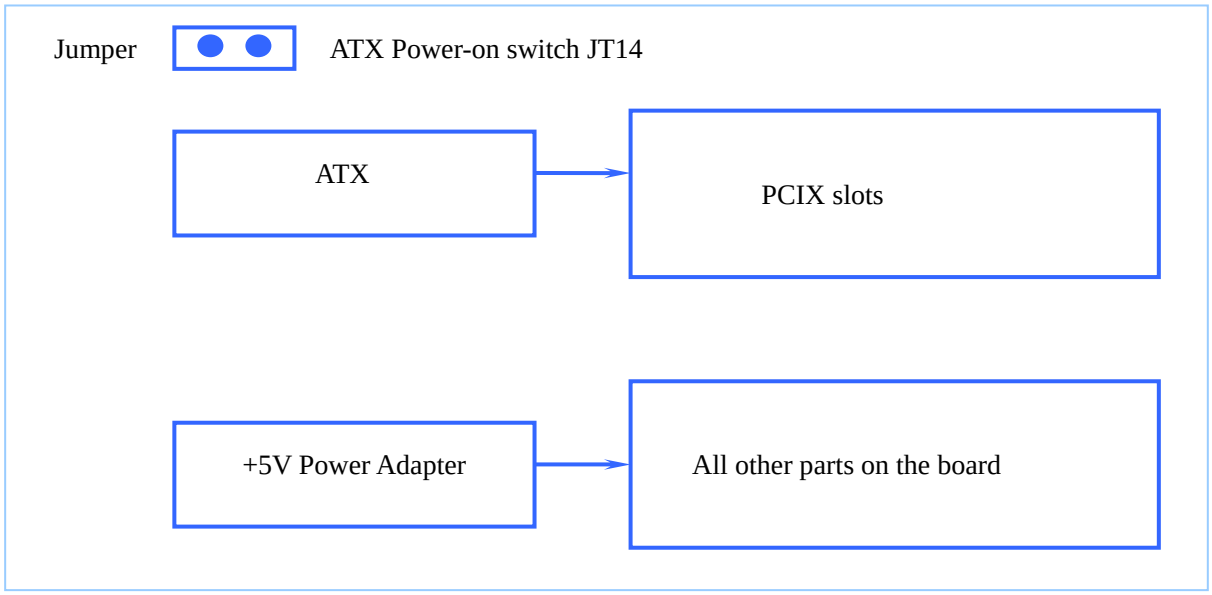


Figure 1-6 the power architecture

Note:
When testing PCIX interface, you must use the ATX power supply, and assemble the jumper, and the power adapter must be installed.

1.17PPC440GX Processor Power

The PPC440GX chip requires four voltages, +1.55V, +3.3V, +2.5V, +1.25V. In this board design, all voltages are derived from the +5V input (+5V input of ATX or +5V power adapter). There are separate DC-DC voltage regulators for each voltage.

2 Memory Map

Table 2-1 summarizes address space assignment on the board.

Table 2-1. PPC440GX Address Space assignment

Function	Subfunction	Start Address	End Address	Size
Local Memory	DDR SDRAM	0x0 0000 0000	0x0 0FFF FFFF	256MB
	DDR SDRAM (Unused)	0x0 1000 0000	0x0 7FFF FFFF	
	SRAM	0x0 8000 0000	0x0 8000 3FFF	256KB
	Reserved	0x0 8000 4000	0x0 FFFE FFFF	
	IMU	0x0 FFFF 0000	0x0 FFFF FFFF	64KB
Internal Peripherals	Reserved	0x1 4000 0000	0x1 4000 01FF	
	UART0	0x1 4000 0200	0x1 4000 0207	8B
	Reserved	0x1 4000 0208	0x1 4000 02FF	
	UART1	0x1 4000 0300	0x1 4000 0307	8B
	Reserved	0x1 4000 0308	0x1 4000 03FF	
	IIC0	0x1 4000 0400	0x1 4000 041F	32B
	Reserved	0x1 4000 0420	0x1 4000 04FF	
	IIC1	0x1 4000 0500	0x1 4000 051F	32B
	Reserved	0x1 4000 0520	0x1 4000 05FF	
	OPB Arbiter	0x1 4000 0600	0x1 4000 063F	64B
	Reserved	0x1 4000 0640	0x1 4000 06FF	
	GPIO Controller	0x1 4000 0700	0x1 4000 077F	128B
	Ethernet PHY ZMII	0x1 4000 0780	0x1 4000 078F	16B
	Ethernet PHY GMII	0x1 4000 0790	0x1 4000 079F	16B
	Reserved	0x1 4000 07A0	0x1 4000 07FF	
	Ethernet 0 Controller	0x1 4000 0800	0x1 4000 08FF	256B
	Ethernet 1 Controller	0x1 4000 0900	0x1 4000 09FF	256B
	General Purpose Timer	0x1 4000 0A00	0x1 4000 0AFF	256B
	TCPIP Accelerator 0	0x1 4000 0B00	0x1 4000 0BFF	256B
	Ethernet 2 Controller	0x1 4000 0C00	0x1 4000 0CFF	256B
	TCPIP Accelerator 1	0x1 4000 0D00	0x1 4000 0DFF	256B
	Ethernet 3 Controller	0x1 4000 0E00	0x1 4000 0EFF	256B
	EBC_CPLD (CS1)	0x1 4100 0000	0x1 410F FFFF	1MB
	EBC_LCM (CS2)	0x1 4200 0000	0x1 420F FFFF	1MB
	EBC connector (CS4:7)	0x1 4800 0000	0x1 4FFF FFFF	128M
	Reserved	0x1 5000 0000	0x1 EFFF FFFF	
Expansion ROM (Boot ROM)	Unused	0x1 F000 0000	0x1 FBFF FFFF	
	Boot ROM (CS0)	0x1 FC00 0000	0x1 FFFF FFFF	64MB

Table 2-1. PPC440GX Address Space assignment (continued)

Function	Subfunction	Start Address	End Address	Size
PCI-X	**Reserved**	0x2 0000 0000	0x2 07FF FFFF	
	PCI-X I/O	0x2 0800 0000	0x2 0BFF FFFF	64MB
	Reserved	0x2 0C00 0000	0x2 0EBF FFFF	
	PCI-X External Configuration Registers	0x 2 0EC0 0000	0x 2 0EC0 0007	8B
	Reserved	0x2 0EC8 0100	0x2 0EC8 00FF	
	PCI-X Special Cycle	0x2 0ED0 0000	0x2 0EDF FFFF	1MB
	PCI-X Memory	0x2 0EE0 0000	0xF FFFF FFFF	55.76GB

3 Programming the PPC440GX

This chapter provides guidance on programming the PPC440GX to work with the board design.

3.1 PLL Configuration

On this board, the PCI clock is determined by the CPLD during power-on reset. The input reference clock, SysCLk, derives from 33.33MHz OSC. And the UART clock, UARTSERCLK, derives from 11.0592MHz OSC. Table 3-1 shows the clock configuration on the board.

Table 3-1. Clock Shipping Configuration

Core Clock	**800MHz**
PLB clock	**200MHz**
DDR SDRAM Clock	**200MHz**
OPB Clock	**66MHz**
Peripheral clock	**66MHz**

3.2 Bootstrap Configuration

Table 3-2 shows the shipping bootstrap configuration when PPC440GX reading strapping Options from the EEPROM.

Table 3-2. Bootstrap Configuration

Serial Device Strap Register bit field	Strapping option (EEPROM)	Description
SDR0_SDSTP0[ENG]	**1**	**Engage** **1 PLL's VCO is the source for the PLL forward dividers**
SDR0_SDSTP0[SRC]	**0**	**PLL Feedback Source** **0 Feedback originates from PLLOutA**
SDR0_SDSTP0[SEL]	**000**	**Feedback Selection** **000 PLL output (A or B)**
SDR0_SDSTP0[TUNE]	**1100111100**	**PLL Tune bits** **1100111100 - 22<M<=40**
SDR0_SDSTP0[FBDV]	**01100**	**PLL Feedback Divisor** **01100 PLL Feedback Divisor = 12**
SDR0_SDSTP0[FWDVA]	**0001**	**PLL Forward Divisor A** **0001 PLL Forward Divisor A = 1**

Table 3-2. Bootstrap Configuration (continued)

Serial Device Strap Register bit field	Strapping option (EEPROM)	Description
SDR0_SDSTP0[FWDVB]	100	PLL Forward Divisor B 101 PLL Forward Divisor B = 4
SDR0_SDSTP0[PRBDV0]	001	PLL Primary Divisor B 001 PLL Primary Divisor B = 1 Note: Reset value for PLL Primary Divisor A is 1.
SDR0_SDSTP0[OPBDV0]	11	OPB Clock Divisor 0 10 OPB clock divisor 0 = 3
SDR0_SDSTP1[LFBDV]	000010	PLL Local Feedback Divisor 000010 PLL local feedback divisor = 2
SDR0_SDSTP1[PERDV0]	01	Peripheral Clock Divisor 0 01 Peripheral clock divisor = 1
SDR0_SDSTP1[MALDV0]	01	MAL Clock Divisor 0 01 MAL clock divisor 0 = 1
SDR0_SDSTP1[RW]	10	EBC ROM Width 10 EBC ROM Width = 32 bit
SDR0_SDSTP1[EARV]	0	ERPN Address Reset Vector 0 ROM connected to EBC0 1 ROM connected to PCI
SDR0_SDSTP1[PAE]	1	PCI arbiter enable 1 PCI arbiter enabled
SDR0_SDSTP1[PHCE]	1	PCI host configuration enable 1 PCI host configuration enabled
SDR0_SDSTP1[PISE]	1	PCI initial sequence enable 1 PCI initial sequence enabled
SDR0_SDSTP1[PCWE]	0	PCI local CPU wait enable 0 PCI local CPU wait disabled
SDR0_SDSTP1[PPIM]	0000	PCI inbound map (PIM) settings 0000 PIM0 off, PIM1 off, PIM2 off
SDR0_SDSTP1[PR64E]	1	PCI initialize Req64 enable 1 PCI initialize Req64 enabled
SDR0_SDSTP1[PXFS]	00	PCIX frequency selection 00 100 - 133MHz frequency selection
SDR0_SDSTP1[24]	0	Reserved
SDR0_SDSTP1[PDM]	0	PCIX driver mode control 0 PCIX driver mode Multipoint
SDR0_SDSTP1[EPS]	100	Ethernet Pin Selection 100 (SMII0, SMII1, RGMII0/RTBI0, RGMII1/RTBI0)

Table 3-2. Bootstrap Configuration (continued)

Serial Device Strap Register bit field	Strapping option (EEPROM)	Description
SDR0_SDSTP1[RMII]	1	RMII Mode 1 RMII 10 Mb
SDR0_SDSTP1[TRE]	1	GPIO Trace Enable 1 GPIO 18-31 are disabled
SDR0_SDSTP1[Nto1]	1	CPU:PLB N to 1 clock ratio 0 CPU:PLB ratio N to X where X is 1
SDR0_SDTP2	0x00000000	Custom Configuration Register 0
SDR0_SDTP3	0x00000000	Custom Configuration Register 1

3.3 DDR SDRAM Bank 0

The DDR SDRAM used on this board is the MICRON semiconductor MT46V32M16. It is organized as 8,192 (13 bits) rows by 1024 (10 bits) columns by 4 bits. On the board, there are four pieces of chip, or 256MB totally. The bank 0 is only used. Table 3-3 to Table 3-10 show the SDRAM registers configuration.

Table 3-3. DDR SDRAM Clock Timing Register - SDRAM0_CLKTR (offset 0x82) 200MHz

Initial	Bit	Field	Value	Description
0x4000 0000	0:1	CLKP	01	Write clock phase (advance 90 degrees).
	2:22	-	xxxxxxxxxx xxxxxxxxxx x	Reserved.
	23:31	DCDT	000000000	DDR clock delay tuning.

Table 3-4. DDR SDRAM Timing Register 0 - SDRAM0_TR0 (offset 0x80) 200MHz

Initial	Bit	Field	Value	Description
0xC18A 40BE (0xC10A 401A 166MHz)	0	SDWR	1	Write recovery (3 CLK).
	1	SDWD	1	Write to wrote delay when crossing a chip select boundary (1 CLK).
	2:6	-	xxxxx	Reserved.
	7:8	SDCL	11	CAS latency (3 CLK).
	9:11	-	xxx	Reserved.
	12:13	SDPA	10	CBR precharge command to next activate command minimum (3 CLK).
	14:15	SDCP	10	Read/write command to precharge command (4 CLK).

Table 3-4. DDR SDRAM Timing Register 0 - SDRAM0_TR0 (offset 0x80) 200MHz (continued)

Initial	Bit	Field	Value	Description
0xC18A 40BE (0xC10A 401A 166MHz)	16:17	SDLD	01	Command leadoff (2 CLK).
	18:23	-	xxxxxx	Reserved.
	24	TWTR	1	Write-to-read command (1 selects Twtr of 2 clock).
	25:26	RFTA	01	Refresh-to-activate command (Adds 1 clocks to SD_RFTA value programmed in SDTR0 [27:29]).
	27:29	SDRA	111	CBR refresh command to next activate command minimum (13 CLK).
	30:31	SDRD	10	RAS to CAS delay (3 CLK).

Table 3-5. DDR SDRAM Timing Register 1 - SDRAM0_TR1 (offset 0x81) 200MHz

Initial	Bit	Field	Value	Description
0x4040 0198 (0x8080 0819 166MHz)	0:1	RDSS	01	Read sample cycle select (T1 sample).
	2:7	-	xxxxxx	Reserved.
	8:9	RDSL	01	Read sample stage select (stage 2).
	10:19	-	xxxxxxxxxx	Reserved.
	20	RDCD	0	Read clock delay - stage 2 (0 clock delay).
	21:22	-	xx	Reserved.
	23:31	RDCT	110011000	Read clock delay tuning bits(2ns).

Table 3-6. Write Data/DM/DQS Clock Timing Register - SDRAM0_WDDCTR (offset 0x83) 200MHz

Initial	Bit	Field	Value	Description
0x0000 0000	0:1	WRCP	00	Write clock phase (advance 0 degrees).
	2:22	-	xxxxxxxxxx xxxxxxxxxx x	Reserved.
	23:31	DCD	000000000	DDR write Data/DM/DQS clock delay tuning bits

Table 3-7. DDR SDRAM Bank 0 Configuration Register - SDRAM0_B0CR (offset 0x40) 200MHz

Initial	Bit	Field	Value	Description
0x000C 4001	0:8	SDBA	000000000	Base address (128M first bank, start 0x0, 13x10).
	9:11	-	xxx	Reserved.
	12:14	SDSZ	110	Size (256MB).

Table 3-7. DDR SDRAM Bank 0 Configuration Register - SDRAM0_B0CR (offset 0x40) 200MHz (continued)

Initial	Bit	Field	Value	Description
0x000C 4001	15	-	x	Reserved.
	16:18	SDAM	010	Addressing mode (mode 3).
	19:30	-	xxxxxxxxxx xx	Reserved.
	31	SDBE	1	Memory bank enable.

Table 3-8. Refresh Timer Register - SDRAM0_RTR (offset 0x30) 200MHz

Initial	Bit	Field	Value	Description
0x0618 0000 (0x04E0 0000 166MHz)	0:1	-	xx	Reserved.
	2:12	RINT	00011000011	Refresh Interval.
	13:31	-	xxxxxxxxxx xxxxxxxxx	Reserved.

Table 3-9. PLB UA Bus Base Address - SDRAM0_UABBA (offset 0x38) 200MHz

Initial	Bit	Field	Value	Description
0x0000 0000	0:27	-	xxxxxxxxxx xxxxxxxxxx xxxxxxxx	Reserved.
	28:31	UBBA	0000	PLB UABus Base Address.

Table 3-10. DDR SDRAM Controller Options 0 Register - SDRAM0_CFG0 (offset 0x20) 200MHz

Initial	Bit	Field	Value	Description
0x8620 0000	0	DCEN	1	DDR SDRAM Controller Enable.
	1	-	x	Reserved.
	2:3	MCHK	00	Memory data error checking (none).
	4	RDEN	0	Registered DIMM disable.
	5	PMUD	1	Page management unit (enabled).
	6	DMWD	1	Width (64-bit).
	7	-	x	Reserved.
	8:9	UIOS	00	Unused I/O state (active [high-z on read, driven on write] - switching DQS).
	10	PDP	1	Page deallocation policy (Least recently used).
	11:31	-	xxxxxxxxxx xxxxxxxxxx x	Reserved.

3.4 Peripheral Bus Timings

The following timings all assume that the peripheral bus frequency is 83MHz. At lower bus frequencies, these timings should still work, though with sub-optimum throughput.
The EBC0_CFG register is same setting for eight Peripheral banks. Table 3-11 shows register EBC0_CFG setting.

Table 3-11. EBC Configuration Register EBC0_CFG (offset 0x23)

Initial	Bit	Field	Value	Description
0x07C0 0000	0	LE	0	Lock error 0 Do not lock error.
	1	PTD	0	Device-Paced time-out disable 0 Enabled time-outs.
	2:4	RTC	000	Ready timeout count 000 16 PerClk cycles.
	5	ATC	1	Address bus high impedance control 1 External address bus drive previous value when EBC is idle and has ownership of the peripheral Interface.
	6	DTC	1	Data bus high impedance control 1 External data bus drive previous write data value when EBC is idle and has ownership of the peripheral interface.
	7	CTC	1	Control signal high impedance control 1 External bus Control Signals are driven inactive and held when EBC is idle and has ownership of the peripheral interface
	8	OEO	1	External bus override high impedance control 1 External Bus Output Enable Override Enabled.
	9	EMC	1	External master high impedance control 1 High impedance all EBC outputs when HOLD_ACK = 1 except PerCS0:7 are always driven.
	10:13	-	xxxx	Reserved.
	14	PME	0	Power management disable
	15:19	PMT	00000	Power management timer (32*PMT)
	20:21	PR	00	Pending request timer 00 -16
	22:31	-	xxxxxxxxxx	Reserved.

3.4.1 Peripheral Bank 0

The flash, 64MB, is attached to bank 0. Table 3-12 shows Peripheral bank 0 register **EBC0_B0CR** settings. Table 3-13 shows Peripheral bank 0 register **EBC0_B0AP** settings.

Table 3-12. Peripheral Bank 0 Configuration Register EBC0_B0CR (offset 0x00)

Initial	Bit	Field	Value	Description
0xFC0D E000	0:11	BAS	0xFC0	The bank 0 base address is 0xFC0.
	12:14	BS	110	The bank 0 size is 64MB.
	15:16	BU	11	Read/write can be allowed for the bank 0.
	17:18	BW	11	The bank 0 bus width is 32-bit.
	19:31	-	xxxxxxxxxxxxx	Reserved.

Table 3-13. Peripheral Bank 0 Access Parameter Register EBC0_B0AP (offset 0x10)

Initial	Bit	Field	Value	Description
0x0785 5600	0	BME	0	Burst mode disable.
	1:8	TWT	00001111	Transfer waits 15 PerCLK cycles.
	9	BCE	0	Fixed length burst reads disabled.
	10:11	BCT	00	Fixed length burst count (2 transfers).
	12:13	CSN	01	Number of cycles from peripheral address driven to PerCS0 low.
	14:15	OEN	01	Number of cycles from PerCS0 low to PerOE low.
	16:17	WBN	01	Number of cycles from PerCS0 low to PerWBE0:1 active.
	18:19	WBF	01	Number of cycles PerWBE0:1 becomes inactive prior to PerCS0 inactive.
	20:22	TH	011	Contains the number of hold cycles inserted at the end of a transfer.
	23	RE	0	PerReady is disabled.
	24	SOR	0	Data transfer occurs one PerClk cycle after PerReady is sampled active.
	25	BEM	0	PerWBE0:1 is only active for write cycles.
	26	PEN	0	Disable Parity checking.
	27:31	-	xxxxx	Reserved.

3.4.2 Peripheral Bank 1

The CPLD is attached to bank 1. Table 3-14 shows Peripheral bank 1 register **EBC0_B1CR** settings. Table 3-15 shows Peripheral bank 1 register **EBC0_B1AP** settings.

Table 3-14. Peripheral Bank 1 Configuration Register EBC0_B1CR (offset 0x01)

Initial	Bit	Field	Value	Description
0x4101 8000	0:11	BAS	0x410	The bank 1 base address is 0x410.
	12:14	BS	000	The bank 1 size is 1MB.
	15:16	BU	11	Read/write can be allowed for the bank 1.
	17:18	BW	00	The bank 1 bus width is 8-bit.
	19:31	-	xxxxxxxxxx xxx	Reserved.

Table 3-15. Peripheral Bank 1 Access Parameter Register EBC0_B1AP (offset 0x11)

Initial	Bit	Field	Value	Description
0x0285 5600	0	BME	0	Burst mode disable.
	1:8	TWT	00000101	Transfer waits 5 PerCLK cycles.
	9	BCE	0	Fixed length burst reads disabled.
	10:11	BCT	00	Fixed length burst count (2 transfers).
	12:13	CSN	01	Number of cycles from peripheral address driven to PerCS0 low.
	14:15	OEN	01	Number of cycles from PerCS0 low to PerOE low.
	16:17	WBN	01	Number of cycles from PerCS0 low to PerWBE0:1 active.
	18:19	WBF	01	Number of cycles PerWBE0:1 becomes inactive prior to PerCS0 inactive.
	20:22	TH	011	Contains the number of hold cycles inserted at the end of a transfer.
	23	RE	0	PerReady is disabled.
	24	SOR	0	Data transfer occurs one PerClk cycle after PerReady is sampled active.
	25	BEM	0	PerWBE0:1 is only active for write cycles.
	26	PEN	0	Disable Parity checking.
	27:31	-	xxxxx	Reserved.

3.4.3 Peripheral Bank 2

The LCM is attached to bank 2. Table 3-16 show Peripheral bank 2 register **EBC0_B2CR** settings. Table 3-17 show Peripheral bank 2 register **EBC0_B2AP** settings.

Table 3-16. Peripheral Bank 2 Configuration Register EBC0_B2CR (offset 0x02)

Initial	Bit	Field	Value	Description
0x4201 8000	0:11	BAS	0x420	The bank 2 base address is 0x420.
	12:14	BS	000	The bank 2 size is 1MB.
	15:16	BU	11	Read/write can be allowed for the bank 2.
	17:18	BW	00	The bank 2 bus width is 8-bit.
	19:31	-	xxxxxxxxxxxxx	Reserved.

Table 3-17. Peripheral Bank 2 Access Parameter Register EBC0_B2AP (offset 0x12)

Initial	Bit	Field	Value	Description
0x2007 FE00	0	BME	0	Burst mode disable.
	1:8	TWT	01000000	Transfer waits 64 PerCLK cycles.
	9	BCE	0	Fixed length burst reads disabled.
	10:11	BCT	00	Fixed length burst count (2 transfers).
	12:13	CSN	01	Number of cycles from peripheral address driven to PerCS0 low.
	14:15	OEN	11	Number of cycles from PerCS0 low to PerOE low.
	16:17	WBN	11	Number of cycles from PerCS0 low to PerWBE0:1 active.
	18:19	WBF	11	Number of cycles PerWBE0:1 becomes inactive prior to PerCS0 inactive.
	20:22	TH	111	Contains the number of hold cycles inserted at the end of a transfer.
	23	RE	0	PerReady is disabled.
	24	SOR	0	Data transfer occurs one PerClk cycle after PerReady is sampled active.
	25	BEM	0	PerWBE0:1 is only active for write cycles.
	26	PEN	0	Disable Parity checking.
	27:31	-	xxxxx	Reserved.

4 Reset and Interrupts

Reset is generated at power-on, by the reset pushbutton, by system-reset from the PPC440GX or by under voltage on either the +5V or +3.3V supplies.

There are 11 external interrupt inputs to the PPC440GX. They are multiplexed with GPIOs. More detail about these interrupts is given in *Table 1-10, "GPIO Usage"*.

5 Switches

The board contains a reset switch and a 4-position slide switch for testing. Additionally, the board contains two 4-position slide switches for CPU strapping and PCI clock configuration. Table 5-1 shows the switch list.

Table 5-1. Switch List

Location	Function	Page No.
SW1	**PCI clock configuration switch**	**P.14**
SW2	**User switch**	**P.17**
SW3	**CPU strapping switch**	**P.12**
SW4	**Reset pushbutton switch**	**P.33**

6 Displays

The LED displays provided on the board are described in Table 6-1.

Table 6-1. Displays

Name	Location	Color	Description
System error	**LD1**	**Red**	Lights when the PPC440GX SYS_ERROR signal is asserted.
User LED1	**LD2**	**Green**	User programmable LED1.
User LED2	**LD3**	**Red**	User programmable LED2.
Ethernet II 1000M status	**LD4**	**Green**	Ethernet II 1000M status indicator.
Ethernet I 1000M status	**LD5**	**Green**	Ethernet I 1000M status indicator.
Flash Status Power Good	**LD6**	**Red**	Lights when the flash is busy.
+2.5V power good LED	**LD7**	**Green**	Lights when the +2.5V voltage is supplied.
+3.3V power good LED	**LD8**	**Red**	Lights when the +3.3V voltage is supplied.
+5V_PCI power good LED	**LD9**	**Red**	Lights when the +5V_PCI voltage is supplied.
Ethernet I Status	**JT12**	**Yellow–Link Status Green–Tx/Rx Activity**	Dual LEDs, part of the RJ-45 PHY1 Ethernet connector assembly, indicating Tx/Rx Activity and Link Status.
Ethernet II Status	**JT11**	**Yellow–Link Status Green–Tx/Rx Activity**	Dual LEDs, part of the RJ-45 PHY1 Ethernet connector assembly, indicating Tx/Rx Activity and Link Status.

7 Connectors

The connector types and pin usage for board connectors are described in the following sections. Table 7-1 shows the connector list.

Table 7-1. Connector List

Location	Description
JT1	**EBC connector**
JT2	**Serial port 0 connector**
JT3	**CPLD JTAG Port**
JT4	**IIC connector**
JT5	**SPI connector**
JT6	**The +5V power adapter connector**
JT7	**Serial port 1 connector**
JT8	**RISCTrace connector**
JT9	**JTAG Debugger connector**
JT10	**+5V ATX and +5V adapter connector (not installed)**
JT11	**Ethernet II RJ45 connector**
JT12	**Ethernet I RJ45 connector**
JT13	**ATX connector**
JT14	**ATX power-on jumper**
JT15	**PCI connector 0**
JT16	**PCI connector 1**

7.1 Expansion Interface Connector

User logic may be placed on a daughter card attached to the Expansion Interface connector. The pin usage of the connector is described in Table 7-2. Refer to the board schematic for the definitions of each of the signal names in the table.

Table 7-2. Expansion Interface Connector Pin Assignment

Pin	Signal name	Pin	Signal name
1	EBC_D15	2	EBC_A15
3	EBC_D14	4	EBC_A14
5	EBC_D13	6	EBC_A13
7	EBC_D12	8	EBC_A12
9	EBC_D11	10	EBC_A11
11	EBC_D10	12	EBC_A10
13	EBC_D9	14	EBC_A9
15	EBC_D8	16	EBC_A8
17	+3.3V	18	+3.3V
19	GND	20	GND
21	EBC_D7	22	EBC_A7
23	EBC_D6	24	EBC_A6
25	EBC_D5	26	EBC_A5
27	EBC_D4	28	EBC_A4
29	EBC_D3	30	EBC_A3
31	EBC_D2	32	EBC_A2
33	EBC_D1	34	EBC_A1
35	EBC_D0	36	EBC_A0
37	+3.3V	38	+3.3V
39	GND	40	GND
41	EBC_D31	42	PER_CS3#
43	EBC_D30	44	PER_CS4#
45	EBC_D29	46	PER_CS5#
47	EBC_D28	48	PER_CS6#
49	EBC_D27	50	PER_CS7#
51	EBC_D26	52	PER_R/W
53	EBC_D25	54	PER_OE#
55	EBC_D24	56	PER_WE#
57	+3.3V	58	+3.3V
59	GND	60	GND
61	EBC_D23	62	PER_BE0#
63	EBC_D22	64	PER_BE1#
65	EBC_D21	66	PER_BE2#

Table 7-2. Expansion Interface Connector Pin Assignment (continued)

Pin	Signal name	Pin	Signal name
67	EBC_D20	68	PER_BE3#
69	EBC_D19	70	PER_PAR0
71	EBC_D18	72	PER_ PAR1
73	EBC_D17	74	PER_ PAR2
75	EBC_D16	76	PER_ PAR3
77	+5V	78	+5V
79	GND	80	GND
81	PER_ERR	82	DMAREQ0
83	HOLDREQ	84	DMAACK0
85	HOLDACK	86	EOT0
87	EXTREQ#	88	PER_READY
89	EXTACK#	90	PER_BLAST#
91	BUSREQ	92	IRQ6
93	+5V	94	+5V
95	GND	96	GND
97	PER_RESET#	98	PER_CLK
99	GND	100	GND

7.2 IIC Connector

The IIC connects to a 1x5 header connector. The pin assignment of the connector is described in Table 7-3.

Table 7-3. IIC Connector Pin Assignment

Pin	Signal name
1	IIC1SCLK
2	+3.3V
3	IIC1SDA
4	GND
5	-

7.3 SPI Connector

The SPI connects to a 1x5 header connector. The pin assignment of the connector is described in Table 7-4.

Table 7-4. SPI Connector Pin Assignment

Pin	Signal name
1	SPI_SCLK
2	+3.3V
3	SPI_DI
4	GND
5	SPI_DO

7.4 JTAG Debugger Connector

The JTAG debugger connects to the board through a 2x8-pin header. Pin usage is described in Table 7-5.

Table 7-5. JTAG Debugger Connector Pin Assignment

Pin	Signal name
1	TDO
2	Unused
3	TDI
4	TRST, from BDI2000
5	Unused
6	Power, This is a status signal, not a power source.
7	TCK
8	Unused
9	TMS
10	Unused
11	HALT, from BDI2000
12	Unused
13	Unused
14	Unused
15	Unused
16	GND

7.5 RISCTrace Connector

The RISCTrace feature connects to the board through a 2x10-pin header. Pin usage is described in Table 7-6.

Table 7-6. RISCTrace Connector Pin Assignment

Pin	Signal name	Pin	Signal name
1	Capacitor to GND	2	GND
3	GND	4	GND
5	GND	6	TRCCLK
7	HALT#	8	GND
9	GND	10	GND
11	TDO	12	JTAG_VREF
13	GND	14	GND
15	TCK	16	GND
17	TMS	18	GND
19	TDI	20	GND
21	TRST#	22	GND
23	GND	24	TRCES4
25	TRCBS0	26	TRCTS0
27	TRCBS1	28	TRCTS1
29	TRCBS2	30	TRCTS2
31	TRCES0	32	TRCTS3
33	TRCES1	34	TRCTS4
35	TRCES2	36	TRCTS5
37	TRCES3	38	TRCTS6

7.6 Serial Port Connector

Two serial ports are included on the board. Pin usage is described in Table 7-7.

Table 7-7. Serial port Connector Pin List

Pin	Signal name	Serial 1	Serial 0	Comment
1	**DCD#**		√	Carrier Detect
2	**RXD**	√	√	Receive Data
3	**TXD**	√	√	Transmit Data
4	**DTR#**	√	√	Data Terminal Ready
5	**GND**	√	√	System Ground
6	**DSR#**	√	√	Data Set Ready
7	**RTS#**	√	√	Request to Send
8	**CTS#**	√	√	Clear to Send
9	**RI#**		√	Ring Indicator

7.7 CPLD JTAG Connector

The CPLD may be programmed in place on the board via this JTAG connector and appropriate downloading software. It is a 2x5 header connector. The pin assignment of the connector is described in Table 7-8.

Table 7-8. CPLD JTAG Connector Pin Assignment

Pin	Signal name
1	**TCK**
2	**GND**
3	**TDO**
4	**3.3V**
5	**TMS**
6	**Unused**
7	**Unused**
8	**Unused**
9	**TDI**
10	**GND**

7.8 PCIX Connector

PCIX slot is a standard connector as defined by the +3.3VDC, 64-bit, 184-pin, PCI edge specification. This interface allows PCIX cards to be interfaced to the evaluation board. The pin assignment of the connector is described in Table 7-9.

Table 7-9. PCIX Connector Pin Assignment

Pin	Signal name	Pin	Signal name
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	GND	A3	TMS
B4	TDO	A4	TDI
B5	+5V	A5	+5V
B6	+5V	A6	INTA#
B7	INTB#	A7	INTC#
B8	INTD#	A8	+5V
B9	PRSNT1#	A9	Reserved
B10	Reserved	A10	+3.3V(I/O)
B11	PRSNT2#	A11	Reserved
B12	KEY	A12	KEY
B13	KEY	A13	KEY
B14	Reserved	A14	3.3Vaux
B15	GND	A15	RST#
B16	CLK	A16	+3.3V(I/O)
B17	GND	A17	GNT#
B18	REQ#	A18	GND
B19	+3.3V(I/O)	A19	PME#
B20	AD31	A20	AD30
B21	AD29	A21	+3.3V
B22	GND	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	GND
B25	+3.3V	A25	AD24
B26	C/BE3#	A26	IDSEL
B27	AD23	A27	+3.3V
B28	GND	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	GND
B31	+3.3V	A31	AD18
B32	AD17	A32	AD16

B33	**C/BE2#**	**A33**	**+3.3V**
B34	**GND**	**A34**	**FRAME#**
B35	**IRDY#**	**A35**	**GND**
B36	**+3.3V**	**A36**	**TRDY#**
B37	**DEVSEL#**	**A37**	**GND**
B38	**PCIXCAP**	**A38**	**STOP**
B39	**LOCK#**	**A39**	**+3.3V**
B40	**PERR#**	**A40**	**+3.3V**
B41	**+3.3V**	**A41**	**+3.3V**
B42	**SERR#**	**A42**	**GND**
B43	**+3.3V**	**A43**	**PAR**
B44	**C/BE1#**	**A44**	**AD15**
B45	**AD14**	**A45**	**+3.3V**
B46	**GND**	**A46**	**AD13**
B47	**AD12**	**A47**	**AD11**
B48	**AD10**	**A48**	**GND**
B49	**M66EN**	**A49**	**AD9**
B50	**GND**	**A50**	**GND**
B51	**GND**	**A51**	**GND**
B52	**AD8**	**A52**	**C/BE0#**
B53	**AD7**	**A53**	**+3.3V**
B54	**+3.3V**	**A54**	**AD6**
B55	**AD5**	**A55**	**AD4**
B56	**AD3**	**A56**	**GND**
B57	**GND**	**A57**	**AD2**
B58	**AD1**	**A58**	**AD0**
B59	**+3.3V(I/O)**	**A59**	**+3.3V(I/O)**
B60	**ACK64#**	**A60**	**REQ64#**
B61	**+5V**	**A61**	**+5V**
B62	**+5V**	**A62**	**+5V**
B63	**Reserved**	**A63**	**GND**
B64	**GND**	**A64**	**C/BE7#**
B65	**C/BE6#**	**A65**	**C/BE5#**
B66	**C/BE4#**	**A66**	**+3.3V(I/O)**
B67	**GND**	**A67**	**PAR64**
B68	**AD63**	**A68**	**AD62**
B69	**AD61**	**A69**	**GND**
B70	**+3.3V(I/O)**	**A70**	**AD60**
B71	**AD59**	**A71**	**AD58**
B72	**AD57**	**A72**	**GND**
B73	**GND**	**A73**	**AD56**
B74	**AD55**	**A74**	**AD54**

B75	**AD53**	**A75**	**+3.3V(I/O)**
B76	**GND**	**A76**	**AD52**
B77	**AD51**	**A77**	**AD50**
B78	**AD49**	**A78**	**GND**
B79	**+3.3V(I/O)**	**A79**	**AD48**
B80	**AD47**	**A80**	**AD46**
B81	**AD45**	**A81**	**GND**
B82	**GND**	**A82**	**AD44**
B83	**AD43**	**A83**	**AD42**
B84	**AD41**	**A84**	**+3.3V(I/O)**
B85	**GND**	**A85**	**AD40**
B86	**AD39**	**A86**	**AD38**
B87	**AD37**	**A87**	**GND**
B88	**+3.3V(I/O)**	**A88**	**AD36**
B89	**AD35**	**A89**	**AD34**
B90	**AD33**	**A90**	**GND**
B91	**GND**	**A91**	**AD32**
B92	**Reserved**	**A92**	**Reserved**
B93	**Reserved**	**A93**	**GND**
B94	**GND**	**A94**	**Reserved**

8 Board Dimension

Figures 8-1 shows the dimension for the evaluation board.

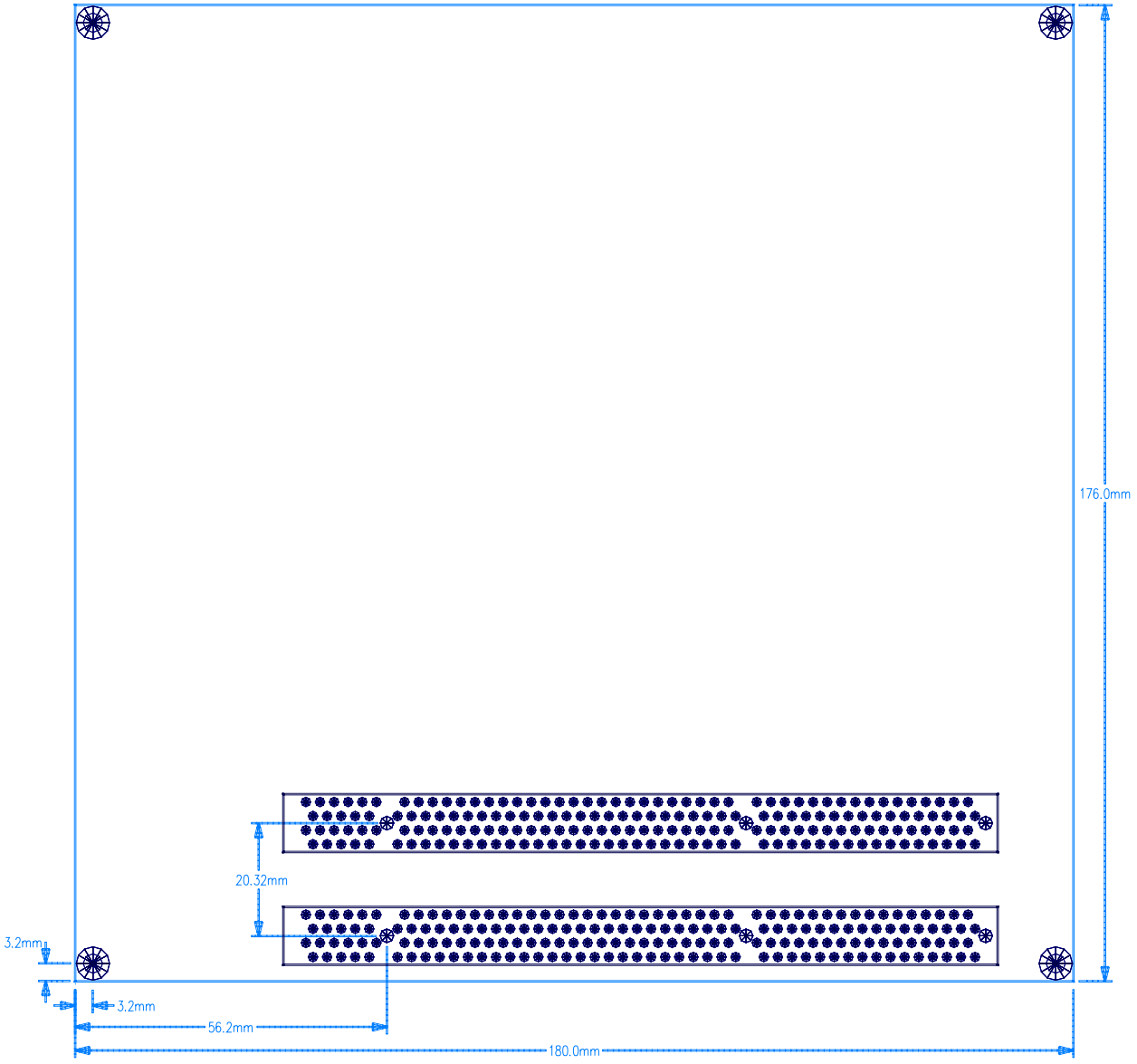


Figure 8-1. The evaluation board dimension

9 CPLD Programming

The following section contains CPLD code listing and the related registers refer to *section 1.10, "CPLD"*.

Figure 9-1. CPLD code listing

```
--*****************************************************************************--
--                    CPLD for the Taishan440GX Evaluation Board Ver10                    --
--*****************************************************************************--
--************ CPU R/W PORT, CPU STRAPPING, CONTROL SIGNALS **************--
--*****************************************************************************--

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY Taishan440GX_CPLD IS
PORT
    (
--  RESET SIGNALS
    POR_RESET           : IN STD_LOGIC;       -- POWER-ON RESET INPUT
    PER_RESET           : IN STD_LOGIC;       -- PERIPHERAL RESET
    SYS_RESET           : INOUT STD_LOGIC;    -- CPU RESET
    DEBUG_RESET         : IN STD_LOGIC;       -- TRACE RESET
    CPU_TRST            : OUT STD_LOGIC;      -- CPU JTAG RESET INPUT
    PHY_RESET           : OUT STD_LOGIC;      -- ETHERNET PHY RESET

--  CLOCK SIGNALS
    PER_CLK             : IN STD_LOGIC;       -- 83MHz
    CPLD_CLK            : IN STD_LOGIC;       -- 25MHz
--  TMR_CLK             : OUT STD_LOGIC;      -- 25MHz

--  CHIP SELECT, R/W, CLOCK, ADDRESS BUS, DATA BUS
    PER_CS1             : IN STD_LOGIC;
    PER_WE              : IN STD_LOGIC;
    PER_OE              : IN STD_LOGIC;

    PER_A               : IN STD_LOGIC_VECTOR(29 to 31);
    PER_D               : INOUT STD_LOGIC_VECTOR(4 to 7);

--  DIP SWITCH SIGNALS
    USER_DIP0           : IN STD_LOGIC;
    USER_DIP1           : IN STD_LOGIC;
```

```
    USER_DIP2           : IN STD_LOGIC;
    USER_DIP3           : IN STD_LOGIC;

--  16245 BIDIRECTIONAL TRANSCEIVER CONTROL SIGNALS
    PER_RW              : IN STD_LOGIC;
    EXTREQ              : IN STD_LOGIC;
    PER_CS2             : IN STD_LOGIC;
    PER_CS3             : IN STD_LOGIC;
    PER_CS4             : IN STD_LOGIC;
    PER_CS5             : IN STD_LOGIC;
    PER_CS6             : IN STD_LOGIC;
    PER_CS7             : IN STD_LOGIC;

    B245_OE             :OUT STD_LOGIC;
    B245_D_DIR          :OUT STD_LOGIC;
    B245_A_DIR          :OUT STD_LOGIC;

--  LCM CONTROL SIGNALS
    LCM_RW              :OUT STD_LOGIC;
    LCM_E               :OUT STD_LOGIC;
    LCM_CTL             :OUT STD_LOGIC;

--  SYSTEM ERROR INDICATOR
    SYSERR              :IN STD_LOGIC;
    SYSERR_N            :OUT STD_LOGIC;

--  PCIX CAPABILITY DETECTING AND CLOCKING CONFIGURATION
    PCI_CLK_GOOD        :IN STD_LOGIC;
    PCI_CLK_S1          :OUT STD_LOGIC;
    PCI_CLK_S0          :OUT STD_LOGIC;

    AUTO_DETECT_EN      :IN STD_LOGIC;
    PCI_CLK_S1_CFG      :IN STD_LOGIC;
    PCI_CLK_S0_CFG      :IN STD_LOGIC;

    PCI_PRSNT1          : IN STD_LOGIC;
    PCI_PRSNT2          : IN STD_LOGIC;
    PCIXCAP             : IN STD_LOGIC;
    PCI_M66EN           : IN STD_LOGIC;
    PCIXCAP_DETECT      : OUT STD_LOGIC;

--  CPU STRAPPING
    BOOT_CFG0           : IN STD_LOGIC;
    BOOT_CFG1           : IN STD_LOGIC;
```

```
        BOOT_CFG2           : IN STD_LOGIC;
        UART0_DCD           : OUT STD_LOGIC;    -- TRI-STATE OUTPUT
        UART0_DSR           : OUT STD_LOGIC;    -- TRI-STATE OUTPUT
        GMC1TXCTL_BOOT      : OUT STD_LOGIC;    -- TRI-STATE OUTPUT

--      UART1 SIGNALS MULTIPLEXING
        UART1_RTS_DTR       : IN STD_LOGIC;
        UART1_RTS           : OUT STD_LOGIC;
        UART1_DTR           : OUT STD_LOGIC;
        UART1_DSR           : IN STD_LOGIC;
        UART1_CTS           : IN STD_LOGIC;
        UART1_DSR_CTS       : OUT STD_LOGIC

        );
END Taishan440GX_CPLD;


ARCHITECTURE RTL OF Taishan440GX_CPLD IS

SIGNAL VER : STD_LOGIC_VECTOR(4 TO 7);
SIGNAL SWITCH : STD_LOGIC_VECTOR(4 TO 7);
SIGNAL CTL : STD_LOGIC_VECTOR(4 TO 7);
SIGNAL STS : STD_LOGIC_VECTOR(4 TO 7);

SIGNAL VCC,GND : STD_LOGIC;

SIGNAL BOARD_RESET : STD_LOGIC;

SIGNAL PCI_PRSNT : STD_LOGIC;
SIGNAL EN,ENN : STD_LOGIC;
SIGNAL SEL : STD_LOGIC_VECTOR(0 TO 1);

SIGNAL PCIXCAP_DETECT_TMP,PCIXCAP_DETECT_TMP_N : STD_LOGIC;

SIGNAL MUX_EN : STD_LOGIC;

SIGNAL PCI_CLK_S1_CFG_N : STD_LOGIC;
SIGNAL PCI_CLK_S0_CFG_N : STD_LOGIC;

SIGNAL PCI_CLK_S1_TMP : STD_LOGIC;
SIGNAL PCI_CLK_S0_TMP : STD_LOGIC;

SIGNAL DSR_DTR : STD_LOGIC;
SIGNAL UART1_DTR_TMP,UART1_RTS_TMP : STD_LOGIC;
```

```
SIGNAL UART1Flow_CTL : STD_LOGIC;

SIGNAL LCM_E_TMP1,LCM_E_TMP2,LCM_E_TMP3,LCM_E_TMP4 : STD_LOGIC;
SIGNAL PER_CS2_TMP1,PER_CS2_TMP2,PER_CS2_TMP3 : STD_LOGIC;

SIGNAL EXTREQ_TMP : STD_LOGIC;
SIGNAL EBC_EN : STD_LOGIC;



COMPONENT EN_GEN
PORT
    (
    CLK             : IN STD_LOGIC;
    EN        : OUT STD_LOGIC;
    ENN             : OUT STD_LOGIC
    );
END COMPONENT;


BEGIN

VCC <= '1';
GND <= '0';

--  Version: 1.0
VER <= "0100";

--  RESET
PROCESS (POR_RESET)
BEGIN

    IF POR_RESET = '0' THEN
        SYS_RESET <= POR_RESET;
    ELSE
        SYS_RESET <= 'Z';
    END IF;

END PROCESS;
BOARD_RESET <= POR_RESET AND SYS_RESET;
PHY_RESET <= BOARD_RESET;
CPU_TRST <= DEBUG_RESET AND BOARD_RESET;
--PER_RESET <= BOARD_RESET;
```

```
--    CLOCKING
--TMR_CLK <= CPLD_CLK;

--     16245 CONTROL
PROCESS (BOARD_RESET,PER_CLK)
BEGIN
      IF BOARD_RESET = '0' THEN
            PER_CS2_TMP1 <= '1';
            PER_CS2_TMP2 <= '1';
            PER_CS2_TMP3 <= '1';
      ELSIF PER_CLK'EVENT AND PER_CLK = '1' THEN
            PER_CS2_TMP1 <= PER_CS2;
            PER_CS2_TMP2 <= PER_CS2_TMP1;
            PER_CS2_TMP3 <= PER_CS2_TMP2;
      END IF;

END PROCESS;

B245_OE <= (PER_CS2 OR PER_CS2_TMP1 OR PER_CS2_TMP2 OR PER_CS2_TMP3) AND
PER_CS3 AND PER_CS4 AND PER_CS5 AND PER_CS6 AND PER_CS7;

EXTREQ_TMP <= '1' WHEN EBC_EN = '0' ELSE EXTREQ;
B245_A_DIR <= EXTREQ_TMP;
B245_D_DIR <= (EXTREQ_TMP AND (NOT PER_RW)) OR ((NOT EXTREQ_TMP) AND PER_RW) ;

--    LCM CONTROL
LCM_E_TMP1 <= NOT ((PER_CS2 OR PER_WE) AND (PER_CS2 OR PER_OE));
LCM_RW <= PER_RW;

PROCESS (BOARD_RESET,PER_CLK)
BEGIN

      IF BOARD_RESET = '0' THEN
            LCM_E_TMP2 <= '0';
            LCM_E_TMP3 <= '0';
      ELSIF PER_CLK'EVENT AND PER_CLK = '1' THEN
            LCM_E_TMP2 <= LCM_E_TMP1;
            LCM_E_TMP3 <= LCM_E_TMP2;
      END IF;

END PROCESS;

LCM_E_TMP4 <= LCM_E_TMP1 AND LCM_E_TMP2 AND LCM_E_TMP3;
```

```
PROCESS (BOARD_RESET,PER_CLK)
BEGIN

    IF BOARD_RESET = '0' THEN
        LCM_E <= '0';
    ELSIF PER_CLK'EVENT AND PER_CLK = '1' THEN
        LCM_E <= LCM_E_TMP4;
    END IF;

END PROCESS;

--    SYSERR_N, SYSTEM ERROR LED INDICATOR
SYSERR_N <= NOT SYSERR;

--   PCIX CAPABILITY DETECTING AND CLOCKING CONFIGURATION
U0: EN_GEN PORT MAP(CLK => CPLD_CLK,EN => EN,ENN => ENN);


PROCESS(CPLD_CLK)
BEGIN

    IF CPLD_CLK'EVENT AND CPLD_CLK = '1' THEN
        IF PCIXCAP = '0' AND EN = '1' THEN
            PCIXCAP_DETECT_TMP <= '1';
        ELSIF EN = '1' THEN
            PCIXCAP_DETECT_TMP <= GND;
        END IF;
    END IF;

END PROCESS;

PCIXCAP_DETECT_TMP_N <= NOT PCIXCAP_DETECT_TMP;

PCI_PRSNT <= PCI_PRSNT1 AND PCI_PRSNT2;

PROCESS(POR_RESET,PCIXCAP_DETECT_TMP_N)
BEGIN

    IF POR_RESET = '0' THEN
        PCIXCAP_DETECT <= PCIXCAP_DETECT_TMP_N;
    ELSE
        PCIXCAP_DETECT <= 'Z';
    END IF;
```

```
END PROCESS;

PROCESS(CPLD_CLK)
BEGIN

    IF CPLD_CLK'EVENT AND CPLD_CLK = '1' THEN
        IF EN = '1' THEN
            SEL(0) <= PCIXCAP;
        END IF;
    END IF;

END PROCESS;

PROCESS(CPLD_CLK)
BEGIN

    IF CPLD_CLK'EVENT AND CPLD_CLK = '1' THEN
        IF ENN = '1' THEN
            SEL(1) <= PCIXCAP;
        END IF;
    END IF;

END PROCESS;

PROCESS(CPLD_CLK)
BEGIN

    IF CPLD_CLK'EVENT AND CPLD_CLK = '1' THEN
        IF ENN = '1' THEN
            MUX_EN <= VCC;
        END IF;
    END IF;

END PROCESS;

PCI_CLK_S1_CFG_N <= NOT PCI_CLK_S1_CFG;
PCI_CLK_S0_CFG_N <= NOT PCI_CLK_S0_CFG;

PROCESS(CPLD_CLK)
BEGIN

    IF CPLD_CLK'EVENT AND CPLD_CLK = '1' THEN
        IF MUX_EN = '1' THEN
            CASE SEL IS
```

```
                    WHEN "00" => PCI_CLK_S1_TMP <= '0';
                                 PCI_CLK_S0_TMP <= PCI_M66EN;
                    WHEN "01" => PCI_CLK_S1_TMP <= '0';
                                 PCI_CLK_S0_TMP <= '1';
                    WHEN "10" => PCI_CLK_S1_TMP <= '0';
                                 PCI_CLK_S0_TMP <= '0';
                    WHEN "11" => PCI_CLK_S1_TMP <= PCI_CLK_S1_CFG_N;
                                 PCI_CLK_S0_TMP <= PCI_CLK_S0_CFG_N;
                    WHEN OTHERS => NULL;
                END CASE;
            END IF;
        END IF;

END PROCESS;

PCI_CLK_S1 <= PCI_CLK_S1_TMP WHEN AUTO_DETECT_EN = '1' ELSE PCI_CLK_S1_CFG;
PCI_CLK_S0 <= PCI_CLK_S0_TMP WHEN AUTO_DETECT_EN = '1' ELSE PCI_CLK_S0_CFG;



--    UART1 SIGNALS MULTIPLEXING
UART1_DTR_TMP <= UART1_RTS_DTR WHEN DSR_DTR = '0' ELSE VCC;
UART1_RTS_TMP <= VCC WHEN DSR_DTR = '0' ELSE UART1_RTS_DTR;

UART1_DTR <= '0' WHEN UART1Flow_CTL = '0' ELSE UART1_DTR_TMP;
UART1_RTS <= '0' WHEN UART1Flow_CTL = '0' ELSE UART1_RTS_TMP;

UART1_DSR_CTS <= UART1_DSR WHEN DSR_DTR = '0' ELSE UART1_CTS;



--   CPLD REGISTER:
--                        000: VER(4 TO 7)  R     _VERSION REGISTER
--                        001: SWITCH(4 TO 7)  R     _USER SWITCH STATUS REGISTER
--                        010: CTL(4 TO 7)  R/W _CONTROL REGISTER
--                        011: STS(4 TO 7)   R     _CPLD STATUS REGISTER

--    CPU WRITES CPLD REGISTER: CTL(4 TO 7)
PROCESS (BOARD_RESET,PER_CLK)
BEGIN

    IF BOARD_RESET = '0' THEN
        CTL(4 TO 7) <= "0000";          --    Uart1 Flow control & EBC MASTER & UART1
SIGNALS MULTIPLEXING & LCM BACKLIGHT CTL
    ELSIF PER_CLK'EVENT AND PER_CLK = '1' THEN
```

```
        IF PER_CS1 = '0' AND PER_WE = '0' AND PER_A(29 TO 31) = "010" THEN
            CTL(4) <= PER_D(4);
            CTL(5) <= PER_D(5);
            CTL(6) <= PER_D(6);
            CTL(7) <= PER_D(7);
        END IF;
    END IF;

END PROCESS;

UART1Flow_CTL <= CTL(4);            -- Uart1 Flow control
EBC_EN <= CTL(5);                   -- EBC MASTER ENABLE
LCM_CTL <= CTL(6);                  -- LCM BACKLIGHT CTL
DSR_DTR <= CTL(7);                  -- UART1 SIGNALS MULTIPLEXING


--    CPU READS CPLD REGISTER: VER(4 TO 7), SWITCH(4 TO 7), CTL(4 TO 7), STS(4 TO 7)
SWITCH <= USER_DIP0 & USER_DIP1 & USER_DIP2 & USER_DIP3;
STS <= "00" & PCI_PRSNT & PCI_CLK_GOOD;

PROCESS (PER_CS1,PER_OE,PER_A(29 TO 31),VER,SWITCH,CTL,STS)
BEGIN

    IF PER_CS1 = '0' AND PER_OE = '0' AND PER_A(29) = '0' THEN
        CASE PER_A(30 TO 31) IS
            WHEN "00" => PER_D <= VER;
            WHEN "01" => PER_D <= SWITCH;
            WHEN "10" => PER_D <= CTL;
            WHEN "11" => PER_D <= STS;
            WHEN OTHERS => NULL;
        END CASE;
    ELSE
        PER_D <= (OTHERS => 'Z');
    END IF;

END PROCESS;

--  CPU STRAPPING
PROCESS (BOARD_RESET,BOOT_CFG0,BOOT_CFG1,BOOT_CFG2)
BEGIN

    IF BOARD_RESET = '0' THEN
        UART0_DCD <= BOOT_CFG0;
        UART0_DSR <= BOOT_CFG1;
```

```
            GMC1TXCTL_BOOT <= BOOT_CFG2;
        ELSE
            UART0_DCD <= 'Z';
            UART0_DSR <= 'Z';
            GMC1TXCTL_BOOT <= 'Z';
        END IF;

END PROCESS;

END RTL;



--    COMPONENT
--    EN_GEN __PCIXCAP DETECT PULSE GENERATE

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE IEEE.std_logic_arith.all;
USE IEEE.std_logic_unsigned.all;

ENTITY EN_GEN IS
PORT
    (
    CLK             : IN STD_LOGIC;
    EN        : OUT STD_LOGIC;
    ENN             : OUT STD_LOGIC
    );
END EN_GEN;

ARCHITECTURE BEHAV OF EN_GEN IS

SIGNAL VCC : STD_LOGIC;

SIGNAL COUNT_OUT : STD_LOGIC_VECTOR(0 TO 7);

SIGNAL COUT : STD_LOGIC;

SIGNAL EN_TMP,ENN_TMP : STD_LOGIC;
SIGNAL SCLR : STD_LOGIC;

BEGIN

VCC <= '1';
```

```
PROCESS(CLK)
BEGIN

    IF CLK'EVENT AND CLK = '1' THEN
        IF SCLR = '1' THEN
            COUNT_OUT <= (OTHERS => '0');
        ELSE
            COUNT_OUT <= COUNT_OUT + 1;
        END IF;
    END IF;

END PROCESS;

COUT <= '1' WHEN COUNT_OUT = (0 TO 7 => '1') ELSE '0';

PROCESS(CLK)
BEGIN

    IF CLK'EVENT AND CLK = '1' THEN
        IF COUT = '1' THEN
            EN_TMP <= VCC;
        END IF;
    END IF;

END PROCESS;

EN <= NOT EN_TMP AND COUT;
ENN_TMP <= EN_TMP AND COUT;
ENN <= ENN_TMP;

PROCESS(CLK)
BEGIN

    IF CLK'EVENT AND CLK = '1' THEN
        IF ENN_TMP = '1' THEN
            SCLR <= VCC;
        END IF;
    END IF;

END PROCESS;

END BEHAV;
```

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