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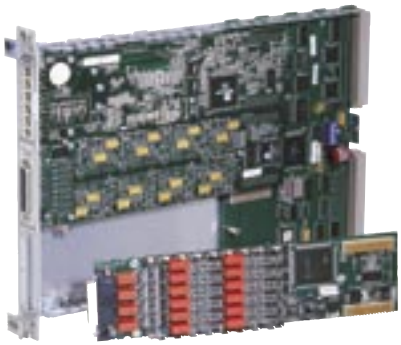
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VM4018



16-channel Precision Analog Comparator/Interrupter (VMIP™)

Features

- Up to 48 Differential Channels per Single VXIbus C-size Slot
- Message or Register-based Data Access
- Inputs can be Masked, Inverted, and Combined to Produce Interrupts
- Programmable Debounce Circuitry Prevents Erroneous Readings
- ±1.0 V, ±2.5 V, ±10.0 V, ±25.0 V, ±100.0 V, and ±250.0 V Input Ranges
- SCPI Compatible

Overview

The VM4018 is a high-performance analog comparator module with sixteen input channels per VMIP™ daughter module. Each input channel can be programmed for the following ranges: ±1 V, ±2.5 V, ±10 V, ±25 V, ±100 V, and ±250 V. Each input is compared against a reference voltage derived from an independent 12-bit DAC. The VM4018 is an ideal device in go/no-go testing where a device fails if the voltage outputs exceed a threshold or window, or even in control applications if a device or test needs to be shut down if a voltage level is exceeded. Using an analog comparator/interrupter in certain applications, as opposed to a traditional DMM/switch approach, considerably improves the overall throughput of the test, while substantially reducing cost.

Each input signal is digitally debounced for a programmed time ranging from approximately 12.8 µs to 0.42 s. This prevents input signal noise from causing undesired interrupts. After debounce, the signal may be inverted via serial word command to select the input transition edge of interest (rising or falling edge) and masked to prevent unused channels from causing interrupts.

The VM4018 is part of the VMIP™ family of instruments and can be combined with up to two other modules to form a high-density VXIbus instrument that fully utilizes the capabilities of the VMIP™. For example, when combined with the VM1602 Time Stamp, all analog interrupts can be time stamped.

Programming

All the masked inputs are OR'd together to produce a single interrupt signal. This interrupt signal is used to generate a VXIbus interrupt, a VXI TTL trigger bus event or to generate front panel interrupt outputs. Special logic will latch the first input to cross its threshold, into the first latched register. This records the originating input. The first latched register can be cleared by querying the latched register contents using the word serial command, or by querying the data via pseudo-register access.

The state of each channel's debounced input and the inverted and masked status may be read directly in the user-defined area of the VXIbus registers, as can the first latched register. This information may also be retrieved using the message-based word serial interface.

To further ease progamming, VXI*plug&play* drivers are provided.

16-channel Precision Analog Comparator/Interrupter (VMIP™)

Specifications

Input Ranges: ±1.0 V, ±2.5 V, ±10.0 V, ±25.0 V, ±100 V, ±250 V

Input Threshold: 0.05% of range within 5 °C range

Warm-Up Time: 30 minutes

Input Type: Differential, may be configured for single-ended by grounding the negative input

Input Impedance: >1 MΩ ≤10 V Ranges
1 MΩ ≥25 V Ranges

Input Polarity: Rising or falling edge

Debounce Time: 12.8 µs to 0.41943045 s, 6.4 µs resolution

IRQ and Latched IRQ Output: Open Collector Driver, 200 mA max. sink. Internally pulled up to +5 V with 10 k resistor

Accuracy: ±0.05% of Range + Gain/Offset Error

Gain/Offset Error: ±1 count of 12-bit DAC

VXI Interface: Message-based, word serial interface. Direct register access in the user-defined area of the VXIbus register map.

Logical Addressing: Static or dynamic configuration

Raw Data Register: Logical Address + 20 H

Masked Data Register: Logical Address + 28 H

First Latched Register: Logical Address + 30 H

User Connector: The user connector is a standard 44 pin female high-density D-Sub connector. A mating connector is provided with each unit

Ordering Information

VM4018

VM4018	16-channel Precision Analog Comparator/Interrupter (must be configured with VM9000 host module)

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