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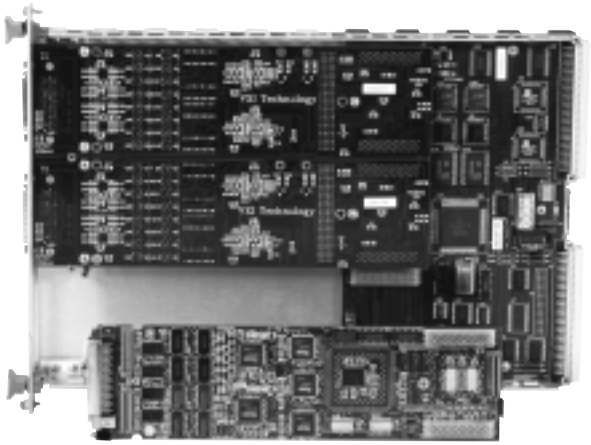
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VM6069

Custom Protocol Interface (VMIP™)

- Designed to Satisfy Virtually any Communication Protocol
- Up to 10Mb/s, Parallel or Serial Communications
- 2 Mbytes of On-board RAM
- Programmable Multi-mode Serial Transceivers
- Open-collector Transceivers, or Programmable Pin Drivers/Receivers
- Modify Protocols "On-the-Fly"
- Custom Protocol Development Services Available
- VXI*plug&play* Drivers



Overview

The VM6069 is a VMIP™ instrument designed to help solve the never-ending problem customers have when forced to develop custom solutions. Whenever a device under test has a communication protocol that cannot be satisfied by a standard interface module, such as the VM6068 for UART and HDLC protocols, or ARINC 1553 and 429 interface modules, customers have been driven to develop their own custom solutions.

The heart of the VM6069 is an SRAM FPGA, which can be modified over the VXIbus backplane. Logic patterns are created to make the VM6069 conform to the communication protocol and downloaded to flash memory on the VM6069. There is 512k of on-board Flash memory; 64K is used for the SRAM FPGA patterns and the remainder is available to the VM6069 for other user-defined patterns. The SRAM FPGA is also supported by up to 2 Mbytes of RAM for data reception and transmission. There are three types of electrical interfaces that can be manipulated by the SRAM FPGA:

- **Two programmable multi-mode serial transceivers (RS232, RS422, RS449, RS485, V35, EIA530). These two programmable interfaces can be used as two standard serial interface channels, or a total of 12 differential drivers and 8 differential receivers can be independently manipulated by the SRAM FPGA.**
- **Two 8-bit open-collector transceivers, controlled as either input or output on an 8-bit basis.**
- **Eight programmable pin drivers and 8 differential pin receivers can replace the open collector transceivers. The output levels of the pin drivers are software configurable, driven by on-board DACs.**

Typical Applications

Some typical applications of the VM6069 are:

Serial communication protocols such as RS485, RS422, RS449, etc., that have 10 or more data bits instead of the standard 7 or 8 data bits for UART protocols.

Framing protocols that do not follow standard HDLC frames.
Parallel communication busses

Telemetry signals

Pattern generators

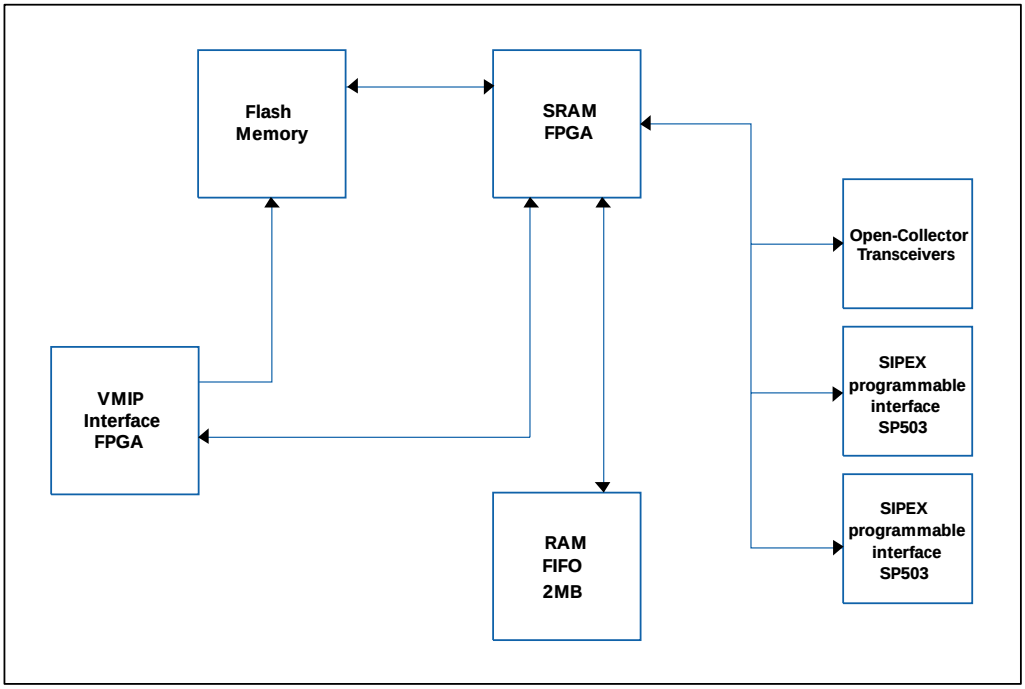
Video frame buffers

Simulation of devices

Real-time data reception, decision making and response with the device under test

VM6069
Custom Protocol Interface (VMIP™)

Block Diagram



Programming

The VM6069 is a register-based module that allows for fast data throughput along the VXI backplane. A VXI*plug&play* driver allows VHDL patterns to be downloaded seamlessly into the on-board flash. Examples in the manual show how to integrate customer-defined logic patterns with what is required to operate the VM6069. Services are also available through VXI Technology's custom engineering services to develop the VHDL code from protocol information.

The User FPGA (XILINX XC4013XL) is used for protocol execution. The configuration data forthis device is loaded from flash memory by the master parallel configuration mode. This allows changing the VHDL/VERILOG design code dynamically for different protocol FPGA designs by loading flash memory through the VXIbus. If the User FPGA has to transmit data, data would be written to SRAM through the VXIbus. The User FPGA then reads the data from SRAM and transmits it through the external interface. If the User FPGA has to receive data, the User FPGA will receive the data from the external interface and then writes the data into SRAM. Data can then be read from SRAM through theVXIbus.

The 2Mbytes of SRAM can be used as FIFO. The FIFO logic to interface the SRAM is emulated in the User FPGA. 6069 Programming

Specifications

SRAM FPGA:	13K gates. Xilinx XC4013X/L
RAM:	2Mbytes
Serial Drivers/ Receivers:	12 drivers, 8 receivers 2 channels. Sipex 503CF 5Mbs data rate Programmable RS232, RS422, RS449, RS485, V35, EIA530
Open-collector Transceivers:	16 channels, programmable on an 8-bit basis as TTL inputs or open-collector outputs. 10 MHz data rate

Ordering Information

VM6069	Custom Protocol Interface (must be configured with VM9000 host module)

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