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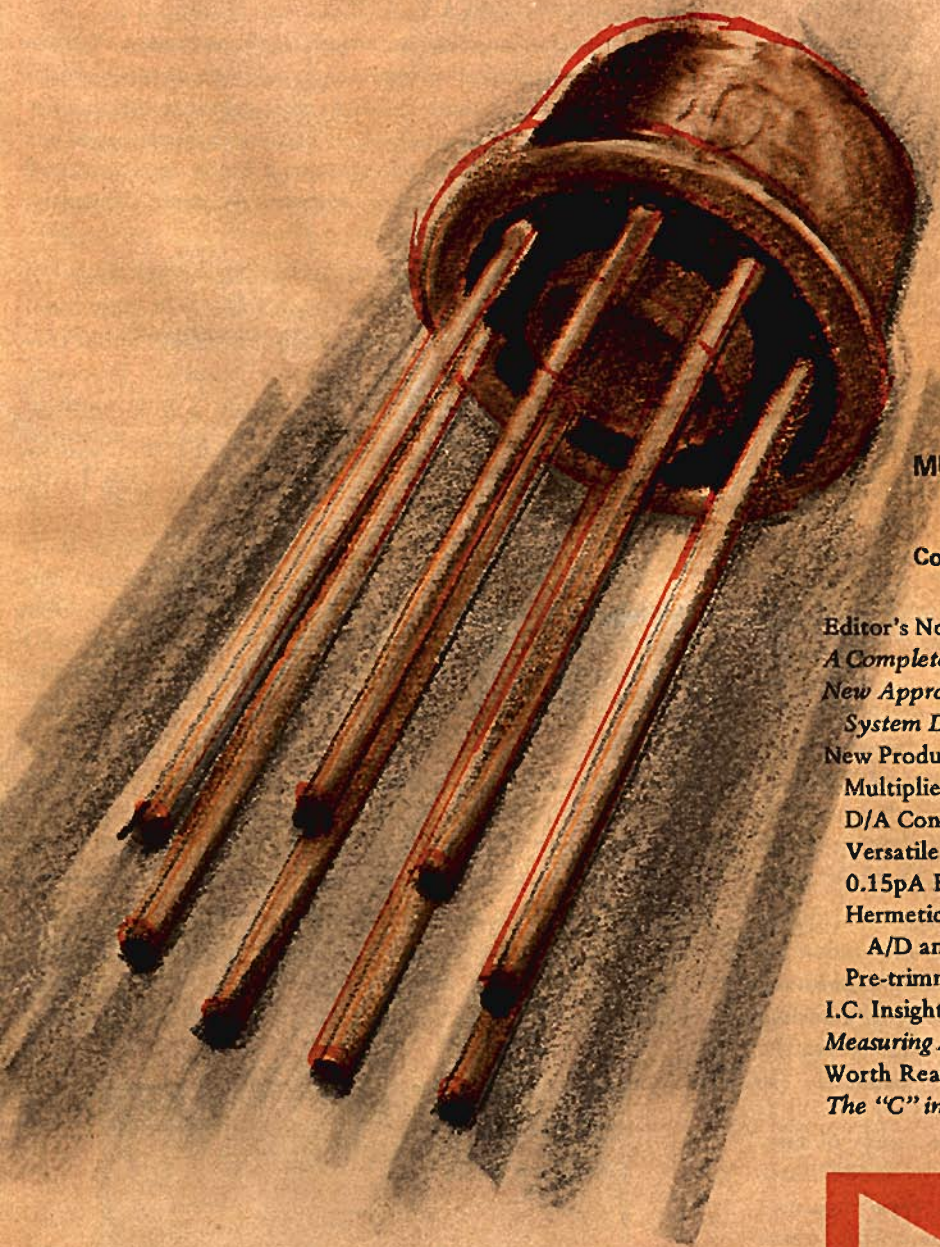
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ANALOG DIALOGUE

A forum for the exchange of circuit technology: Analog and Digital, Monolithic and Discrete



A COMPLETE MONOLITHIC MULTIPLIER/DIVIDER — see page 3

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Editor's Notes



Multiplier Memories and Meanderings
The AD530 IC Multiplier (/Divider) was an exciting development for one who has been looking at multipliers for more than 20 years with emotions running the gamut from hatred* to despair† to disappointment§ to envy‡. We recall our very first introduction to an analog multiplier, a black Dural box, about 17" X 7" X 6", weighing 10 pounds, costing about $1,500, requiring ±300V, and having a voltage signal range of ±25V. It also required 115V ac to derive power for the heaters of its ranks of 12AX7's, festively aglow and protectively surrounding a large octal tube with a red base: a 5687 (?) RCA "Red Tube", offered to the world as the utmost in thermionic reliability (at least, in 1949), but having the additional property (secretly discovered) of square-law plate current vs. plate voltage at a magic value of bias voltage. With it, one could build a quarter-square multiplier! (Unfortunately, the yield of good squarers was vanishingly small)

This was the first of many encounters in the search for a Natural Law that would engender effective, reproducible, cheap, compact, fast, accurate multiplication. We read about crossed fields, masks, servos, modulation, arbitrary functions of two variables, and even the elusive (at that time) Hall Effect. (The lament went, "The Hall Effect is a small effect.")

In 1954, we were playing with triangular-wave modulation multipliers. The late '50's brought the double-bridged six-legged "sex-iplier," with its 0.1% accuracy (only 7" by 19" by 13", and $1,265, including a hard-working fan), undoubtedly the apex of the vacuum-tube multiplier era, and reminiscent of the last days of the dinosaurs.

The transistor era brought with it better, smaller, cheaper (0.1%, 3½" X 4¼" X 13", $995) faster quarter-square multipliers, but nothing to excite the OEM designer with lots of ideas as to how to use multipliers ... or—if only they could be made smaller, cheaper, and faster, and free of the glitches inherent in the piecewise-linear approximations to the square law.

Finally, the widespread availability of near-ideal dual planar transistors at low cost (the same kinds of transistors used in the input stages of op amps), with their exponential/logarithmic characteristics and linear g_m with collector current, unlocked the Natural Law we had all been waiting for, and led to the Analog Devices 420 and its successors, and—ultimately (*so far*)—the complete multiplier-on-a-chip, the AD530!

Applications Galore. What you can do with arrays of fast, tiny, low-cost multipliers beggars the imagination: modulation, automatic gain-setting, power measurement, ratio measurement, for openers! Analog correlation, trigonometric transformations, adaptive controls, phase measurement, frequency multiplication, servos, roots and powers, two-dimensional display linearizing! And more ... power series function generation, rms measurements, watts and var measurement, variable-frequency filters, etc. ... etc. ... etc!

Paper Call. We'd be interested in hearing how *you* are using the AD530 and its larger brothers, e.g., 422, 424, 426. We'd like to publish interesting, useful, repeatable applications that promise to be popular. And you may be interested in the honoraria awarded when we print fresh (previously unpublished) application briefs submitted from outside the family.

DAN SHEINGOLD

* at the test bench
† ibid.
§ ibid.
‡ as an erstwhile competitor, at the time that Analog introduced the 420, the first commercially available transconductance multiplier in a small modular package

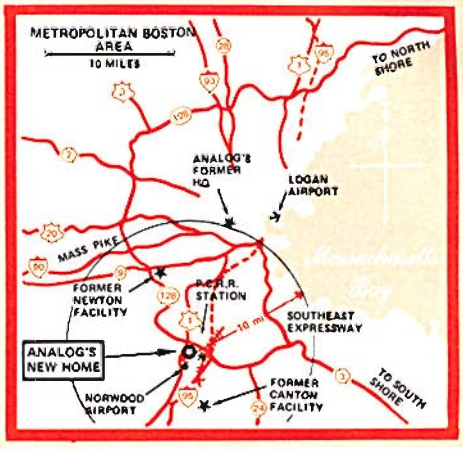
Company Note

ANALOG DEVICES IS ON THE MOVE! (GEOGRAPHICALLY, TOO)

After a 6-year sojourn in Cambridge, on the very edge of urban redevelopment, and after repeated expansions of our facilities until they included three buildings in Cambridge, one in Newton, and one in Canton, Mass., it became evident that it just might be possible to give our customers better service, as well as to operate our business more responsively, more efficiently, and more profitably, by "putting it all together."

And so, we have built a spanking-new plant with nearly 2½ acres of floor space to house our growing family. At just about the time you read these words, we will be moving to our consolidated facility on Route 1, at the Norwood-Westwood line, about 11 miles south of Boston and 1 mile south of Route 128. Although separated from Boston's urban amenities (and its urban traffic!) by about twenty minutes, we are closer to the rest of the world, by road (Route 128), by air (Norwood Airport, a short helicopter ride from Logan International), and by rail (P.C.R.R. Route 128 Station).

The map shows our new location in relation to major highways and other transportation facilities in the Boston area. If you happen to be in the vicinity, the light is in the window and the latchstring is out. Otherwise, write or phone us at our new address.



ANALOG DIALOGUE
A FORUM FOR THE EXCHANGE OF CIRCUIT TECHNOLOGY: ANALOG AND DIGITAL, MONOLITHIC AND DISCRETE
VOLUME 5 • NUMBER 1 • Published by Analog Devices, Inc. • Norwood • Massachusetts 02062 • January 1971

Publishable monthly by Analog Devices, Inc., and available at no charge to engineers and scientists who use or think about circuits. All correspondence should be addressed to Editor, ANALOG DIALOGUE, Post Office Box 280, Norwood, Massachusetts 02062 U.S.A.

A Complete Multiplier/Divider on a Single Chip

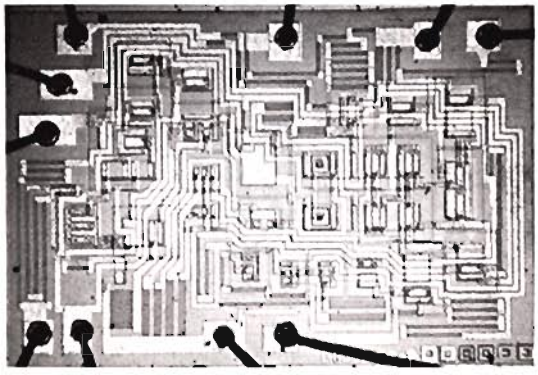
by Richard S. Burwen

The AD530 is the first completely monolithic Multiplier/Divider to appear on the market. It will multiply, divide, square, and square-root, with basic accuracy of the order of 1% and bandwidth of 1MHz. Transcending any monolithic multiplier yet offered, it contains an output operational amplifier, a regulator, and low-TC-thin-film gain-setting resistors on the same chip as the variable transconductance multiplier circuit, with the resulting improvement in simplicity, reliability, and general all-around usefulness. To further its reliability, it is housed in a hermetically-sealed TO-100 package. Because it is monolithic, one can expect its cost to decrease substantially with quantity and time. One can also expect it to appear in additional forms of packaging in the future. Finally, in times to come, one can expect to see additional IC function circuits of this type, resulting from the extensive "know-how" of Analog Devices in the design, development, application, and production of both discrete and integrated circuit multipliers and related function circuits.

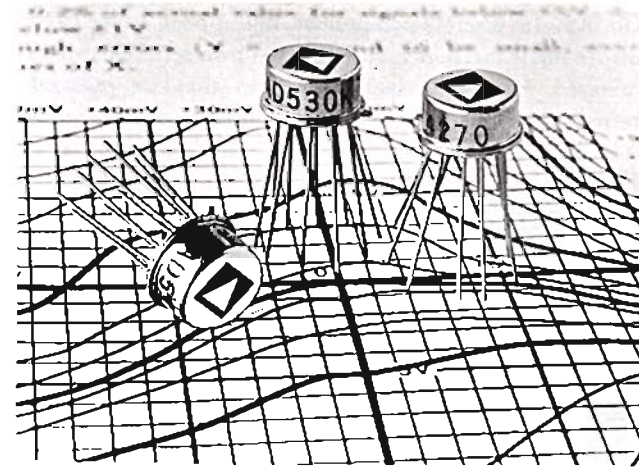
While there are a number of excellent discrete analog multiplier modules available today, only a portion of the circuit has been built in integrated circuit form. To produce an output XY/10 from the most popular present day IC "multiplier" requires the addition of an external differential-input operational amplifier, about fifteen resistors, four potentiometers, and closely placed power-supply by-pass capacitors. In such a device, multiplication accuracy cannot be guaranteed, because it depends upon the various external parts, and the bandwidth is likely to be limited by the external operational amplifier to substantially less than that of the multiplier itself.

The four-quadrant linear IC Multiplier/Divider described below (AD530*) incorporates the output operational amplifier and thin-film resistors as well as zener-diode-power-supply decoupling on the same IC chip that contains the basic variable-transconductance multiplier circuit (Figure 1).

Without any external elements, it will operate as a multiplier/divider with entirely adequate performance for many applications. Optionally, potentiometers may be connected externally to trim offsets associated with either input, the output, and/or



*For technical data on Type AD530, use the reply card. Circle A11



the overall scale factor (Figure 2). In any event, the adjustments correct basically *linear* errors; nonlinearity, which determines the ultimate limits of accuracy, is essentially unchanged, whether the unit is trimmed or not.

CHARACTERISTICS

As a multiplier, the AD530 has the transfer function XY/10 and, as a divider, +10Z/X. The X, Y, and Z input levels are ±10V for multiplication, and the output is ±10V @ 5mA. DC overall multiplication accuracies are graded in production to ±2% and ±1%, fully trimmed. As a divider, the device is somewhat more accurate, because operation is restricted to two quadrants (where X is negative), which facilitates optimal trim settings, and feedback is connected to the Y input, which is more linear than the X input. Divider error is typically 0.15% at full scale denominator input and increases gradually to 1.5% as X decreases to −1V. Multiplier nonlinearity over the range of variation of X is typically ±0.35%, and for the range of Y variation, it is typically ±0.15%.

Both the frequency amplitude response and the maximum undistorted output of the multiplier are down 3dB at 1MHz, and the circuit operates well with capacitive loads up to 0.001μF. When dividing, the bandwidth decreases with decreasing denominator voltage, as in other dividers, because there is less feedback around the internal operational amplifier. At X = −10V, the bandwidth is 700kHz, decreasing to 60kHz at X = −1V.

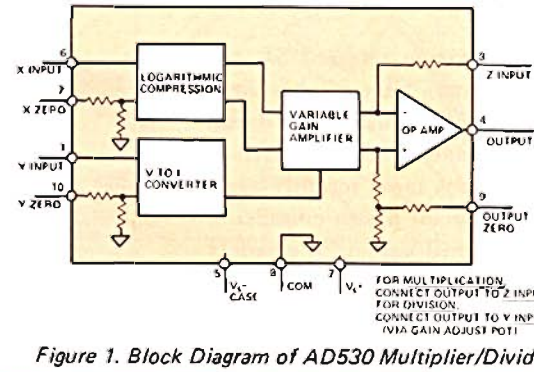


Figure 1. Block Diagram of AD530 Multiplier/Divider

Multiplier circuits, regardless of type, require trimming, either internally or externally, to achieve rated accuracy. There are four parameters to be trimmed: X zero, Y zero, output zero, and gain. Without trimming, the error of the AD530 is about 10%, made up almost entirely of linear components. See ERRORS. In discrete-component multipliers, some of these trims are made internally, and external trim terminals are often eliminated. However, since the errors that are reduced by external trims are linear, it is often possible to trim out their effects by adjusting gains or offsets elsewhere in the system, either ahead of the multiplier (gain trim and input zero trims) or following the multiplier (output offset trim or gain trim).

CIRCUIT

The complete circuit schematic is shown in Figure 3. Transistors Q1 through Q15, and Q28, constitute the multiplier section; and transistors Q16 through Q27 make up the output operational amplifier.

The multiplier section design is based on established principles, using emitter-current variation in a differential pair to vary the gain. Transistors Q7 and Q8 are one differential pair, whose emitter current and transconductance are controlled by the current source, Q9. A second differential pair, Q14 and Q15, and the current source Q10, develop an output across R8 and R16 opposite in phase to that produced by Q7 and Q8. When the Y input voltage is 0, their output signals cancel.

When Y is positive, the emitter current in Q7 and Q8 increases, the emitter current in Q14 and Q15 decreases, and an output is produced across R8 and R16 in proportion to the differential base signal. (Negative Y reverses polarities.)

This differential base voltage is developed across a pair of diode-connected transistors, Q1 and Q2, by currents, proportional to the X input voltage, produced by the current sources Q3 and Q4. These diodes compensate the nonlinearity

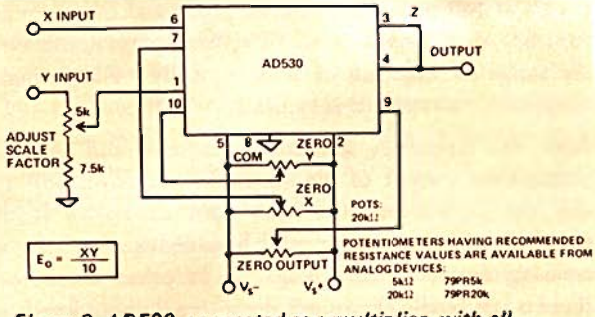


Figure 2. AD530, connected as a multiplier, with all trims connected. Unused zero trim terminals should be connected to common

THE AUTHOR



Richard S. Burwen received SB and AM degrees from Harvard, has since been involved in creative circuit design at Bell Labs and a large number of other companies, most recently as an independent circuit design consultant. His many original designs in a variety of fields have resulted in a number of patents and technical papers. One of the founders of ADI, he is now Director of Advanced Development.

of Q7 and Q8, Q14 and Q15, and thereby permit a larger X input signal which improves the dynamic range by about 14dB.

The output operational amplifier's input stage consists of a differential PNP pair, Q16 and Q17, having an active current-inverter load, Q19, Q20, R24, and R25. Q17 feeds an emitter-follower stage, Q21, having a current-source load, Q24, and a pair of output emitter followers, Q25 and Q27.

Transistor Q26 limits the short circuit current in the positive direction, and the decrease of current gain of Q27 at high currents limits the short-circuit current in the negative direction. The zener diode, Q18, helps to minimize output zero drift by making the quiescent collector voltages of Q16 and Q17 nearly equal.

The gain of the system is determined by resistor ratios, and by the emitter currents of Q1, Q2, Q7, Q8, Q14, and Q15. If these six transistors match one another perfectly, variations in their transconductance cancel out, and so does their variation with temperature. For example, if the currents from transistors Q3 and Q4 are increased in the same proportion as the currents in Q9 and Q10, there will be a decrease in signal voltage developed across Q1 and Q2, but the corresponding increase in transconductance (in Q7, Q8, Q14, and Q15) will cancel the effect on gain. Left over, however, is the effect of the fractional modulation of the emitter currents of Q1 and Q2 caused by the value of the X input signal. Thus, an increase in the negative supply voltage, which tends to increase the currents from the current sources Q5, Q6, Q11, and Q12, thereby decreases the fractional modulation and causes a decrease in scale factor. The zener diode Q28 regulates these current sources against supply variations, and transistor Q13 compensates against variations in scale factor with temperature.

In a transconductance multiplier of this type, a small mismatch in the base to emitter voltage of Q1 and Q2, Q7 and Q8, or Q14 and Q15, can cause a large error at the output. For the most part, output deviations are corrected for by the potentiometer adjustments. However, the offsets also produce a second-harmonic distortion component which is proportional to the offset in any one of the three transistor pairs. A small offset also affects the dc accuracy—that is, offsets as small as 0.5mV in each of the three pairs, adding up in the worst direction, can produce a 1% multiplication error. Careful layout and processing techniques have allowed consistently successful production of units having low offset combinations.

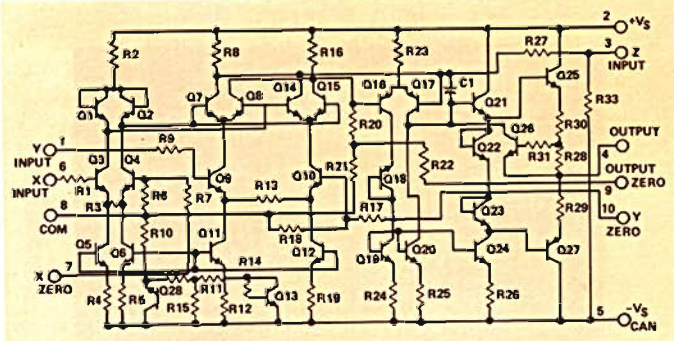


Figure 3. Schematic Diagram of AD530 Multiplier/Divider

Application Notes

CONNECTIONS

As a *Squarer* (Figure 4) Squaring is essentially multiplying the X input by itself. The output is connected to the Z input; gain is trimmed at the Y input.

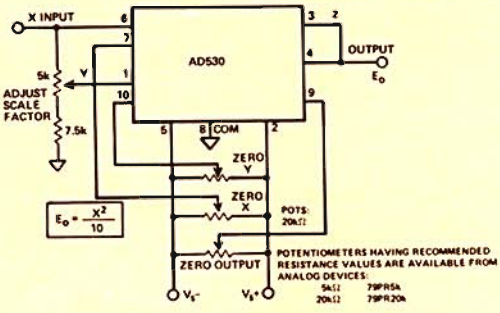


Figure 4. AD530, connected as a squarer.

As a *Divider* When using the AD530 Multiplier/Divider in the Divider mode (Figure 5), the numerator input signal is fed to the Z input, and the denominator to X. The output terminal is connected to the Y input, via the gain trimming potentiometer. Division by positive values of the X input signal is not possible, unless the X input is preceded by a sign inversion, because positive X inputs invert the polarity of the feedback loop, and the resulting positive feedback causes the output to "peg." This will not harm the AD530, but it won't divide until the X polarity is reversed.

As a *Square Rooter* (Figure 6) In rooting, the divider's input is divided by the output; thus the constraint enforced by the circuit is equality between the input and the square of the output, and the output is proportional to the square root of the input. Operation in this mode is restricted to positive Z inputs. Unrestricted sign reversal in any feedback square rooter will cause the output not only to peg, but to lock itself up at a positive limit, and it cannot be brought back without removing the power, opening the loop, or momentarily connecting the output to a negative voltage.

Fortunately, latchup is easily prevented in the AD530 by connecting a diode in series with the output terminal. The diode causes the loop to open when the AD530 output is positive, assuming the load is connected to or below ground potential. The diode is inside the feedback loop of a high-gain op amp, and its voltage drop will therefore introduce negligible error for operation at normal polarity.

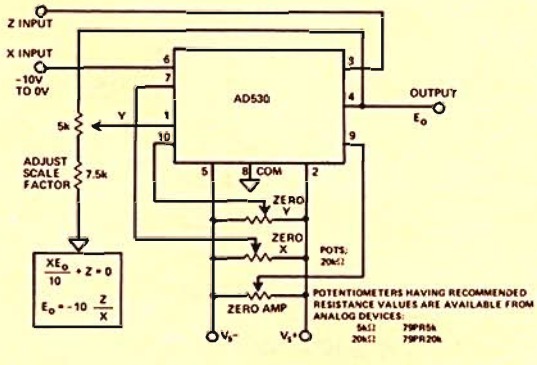


Figure 5. AD530, connected as divider.

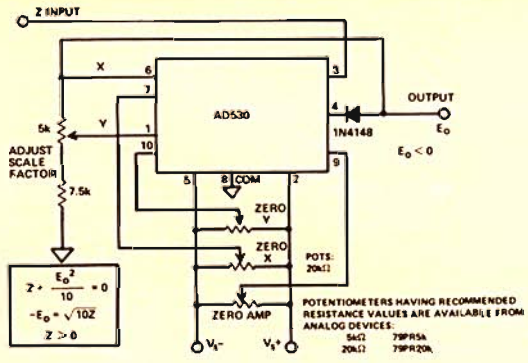


Figure 6. AD530 connected as square rooter. For best results, adjust trims in divider connection, then trim output near zero as square rooter.

SPECIFICATIONS, ERRORS, & ADJUSTMENTS

A complete set of specifications for the AD530 is listed in the table on page 15. There are at least three ways of looking at the dc errors of a multiplier-connected unit at room temperature (or over a temperature range):

1. Overall error. This is defined by the basic accuracy specification—when trimmed—(±1% of full scale output for AD530K, ±2% for AD530J). It includes error from all sources.

2. Error contributions. The error is subdivided into a number of components, the sum of which invariably is greater than the achievable overall accuracy. These components include: offset, gain error, X/Y feedthrough and nonlinearity (respectively, 0, 0.5%, 60/80mV, 0.2%/0.6%, for a well-adjusted AD530K).

3. The error may be measured at a number of points and a contour map drawn, showing the interpolated error at all points in the X–Y plane, for a given unit. Contours of equal error are called "Iso-Vers"[Iso: equal, Ver(ity): truth].

In a coming issue of *Analog Dialogue*, the sources and uses of multiplier error contributions will be discussed in some detail, as they apply to Analog's multiplier product line. On page 15 of this issue will be found some comments that are of *particular* relevance to AD530. *(continued on page 15)*

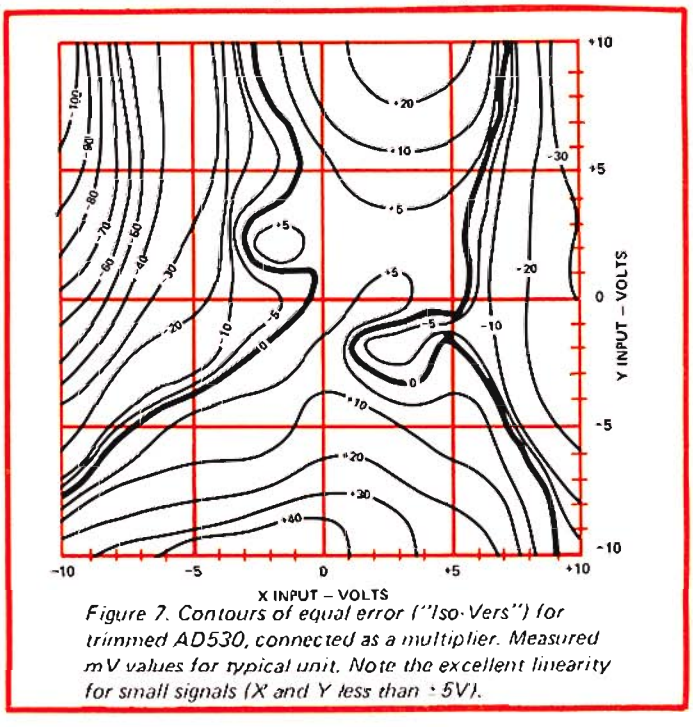


Figure 7. Contours of equal error ("Iso-Vers") for trimmed AD530, connected as a multiplier. Measured mV values for typical unit. Note the excellent linearity for small signals (X and Y less than ±5V).

New Approaches to Data-Acquisition System Design

by T. O. Anderson

Low cost conversion components (such as ADI's μDAC's) make feasible "decentralized" conversion systems—systems wherein each analog input is quantized independently, at the source. These systems exhibit higher overall reliability, higher speeds, and ready ability to compress data and thus increase transmitted intelligence.

With the coming of new components at progressively lower prices, data acquisition system designers should consider new system design approaches. Starting with analog sources, traditional sampled data systems consist of analog transmission lines, a centralized analog time-switching system (viz., multiplexer), a single analog-to-digital converter, and serial computer processing. However, there are many benefits to be obtained by considering a decentralized system design approach wherein each analog input is quantized, preprocessed and buffered *at the source*. The digital data from the source buffers can then be readily transmitted and multiplexed for final central processing. A buffer at each source further suggests self-adaptive multiplexing for efficient bandwidth allocation between sources.

In the paragraphs that follow, we shall first explain the difference between the traditional centralized design approach and the decentralized approach advocated here, then compare the two system-design approaches and finally discuss in some detail the technique of self-adaptive digital output multiplexing.

BASIS FOR COMPARISON

Figure 1 shows a block diagram of a traditional data-acquisition system, and Figure 2 shows such a system of the new design. The sources in both cases are of the same general type (e.g., preamplifier outputs), and the preprocessing, in its simplest form, could be thought of as being some sort of redundancy-reduction data compression.*

*An example of *redundancy-reduction data compression* would be to store in the buffer only those values that change by at least a predetermined amount from the previous value, and to cause the buffer to read out only after it had reached an appropriately full "level-of-content," i.e., number or magnitude of changes stored. Such a process would considerably increase the amount of intelligence transmittable via a data link of given capacity.

In comparing the advantages and disadvantages of the two system configurations, some parameters must be considered fixed and equal for both systems. For the purpose of this discussion, the following parameters are the same for both systems.

1. Cost
2. Number of channels
3. Sampling rate per channel
4. Throughput rate
5. Sample resolution
6. Sample accuracy
7. Channel buffer size

With everything else being equal, the number of channels that can be handled at comparable cost is typically of the order of 20 to 50 at the present time.

OVERALL SYSTEM CONSIDERATIONS

For a given level of cost, the most important advantage of the Figure 2 configuration is the lower probability of catastrophic system failure. In the case of a spacecraft system, this could mean the difference between success and failure; in industrial control, it could be equally important.

Another advantage of the configuration of Figure 2 is that it simplifies system interfaces between the experiments (or sources of data) and the communication system. In a practical system, the interface between the inputs and the communications system can be considered to be the buffer stage. In Figure 2, experiments and preprocessing systems are independent from one another and from the communication system. The signal statistics and processing algorithms of each channel determine the characteristics of the feedback loop between the buffer and the processor for that channel. For example, in a redundancy-reduction data compression scheme, the level-of-content of the buffer may control the significance criteria for the detector. The bandwidth allotment between channels may be

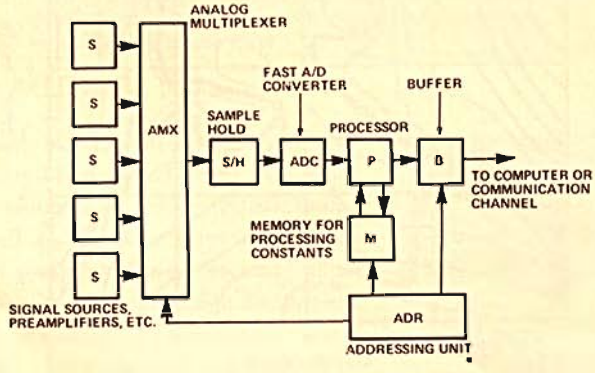


Figure 1. Conventional Centrally-Controlled Data Acquisition System

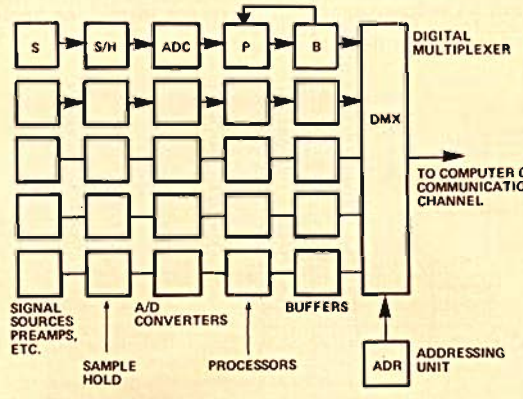


Figure 2. Block Diagram of Decentralized Data Acquisition System

made self-adaptive by making the output multiplexer sample the outputs of those buffers having a higher level of content more often. In an adaptive allotment scheme, prescribed allotments are then also controlled by varying the level-of-content at which a channel buffer is sampled.

On the other hand, the processor in the centralized scheme (Figure 1) could no doubt become quite complex. Not only is a rate buffer required to buffer data for continuous transmission at a fixed rate, but processing constants, which may vary from channel to channel, must also be stored, in a memory. Furthermore, it must be possible conveniently to recall the last accepted sample from a channel.

In the *basic* decentralized system, the implementation of these functions is easily achieved. And when the adaptive output is included, the benefits that are realized occur at only a slight increase of complexity.

In the decentralized scheme, the sampling rate for each channel can be conveniently and independently set, while in that of Figure 1, the sampling rate for each channel is tied to sampling rate of the multiplexer. To achieve variable sampling rates in the centralized system, for example, one must resort to super commutation (one channel connected to more than one multiplexer input) and/or subcommutation (multiple levels of multiplexing).

OTHER DESIGN CONSIDERATIONS

The decentralized scheme lends itself to simple and independent special-purpose preprocessing, at both analog and digital stages. It introduces the possibility of self-adaptive bandwidth allotment. It assures that the experiments do not interact and increases system reliability. A number of detailed technical problems which the designer must cope with in the centralized scheme simply do not exist in the decentralized scheme. For example, in the system of Figure 1, the speed of the converter must be greater than for that of Figure 2 by a factor equal to the number of channels, at least. In the centralized scheme, the sometimes low-level, high-impedance analog voltage must be communicated over long distances, making it susceptible to noise and perhaps requiring costly transmission links. In the decentralized scheme, the transmission of high-level, low-impedance, digital signals normally poses little or no problem. In many instances, they can be transmitted serially over a single wire.

In the scheme of Figure 1, the analog multiplexer can introduce such analog errors as offset voltages and switching noise; in addition, it is bandwidth-limited. The digital multiplexer cannot introduce analog errors and has no significant speed limitations.

MAINTENANCE CONSIDERATIONS

The principal reason the decentralized scheme is cost-competitive is its repetitiveness. A large number of essentially identical, large- or medium-scale, integrated circuits are used, rather than a large number of different circuits having diverse properties, which make up the centralized system. The multiplicity of identical circuits has favorable implications, not only for manufacturing cost, but also for maintenance of the system. Trouble shooting can often be reduced simply to substitution of units, and only a very few kinds of spare units are required.

BUFFER UTILIZATION

In a multi-channel data sample system which includes some form of processing and which then also includes a buffer, a basic decision concerning the buffer utilization is necessary: Should an accepted sample from one channel be allowed to enter the buffer based on the past history of activity of the individual channel, or should it be allowed to enter the buffer based on the past history of activity of all the channels collectively? The system of Figure 1 clearly reflects the "collective" arrangement while that of Figure 2 in its basic configuration clearly is the "individual." However, the addition of the self-adaptive bandwidth feature allows the system of Figure 2 to secure, in addition, the benefits of the collective system.

TIME AND ADDRESS

Considering the same buffer-storage capacity for both systems, and with the buffer organized as one large serial buffer in Figure 1, and as several smaller serial buffers in Figure 2, the time and address integrity is maintained as follows: In the centralized system with the large serial buffer, only the address need accompany a sample. The time* is deduced from its location in the frame.* In the basic form of the decentralized system, the address is deduced from its location in the frame, but time must accompany each sample through the channel buffer. In neither of the basic configurations must *both* time and address accompany the data.

ADAPTIVE BANDWIDTH ALLOCATION

In the system of Figure 2, the processor and its associated buffer are assumed to be equipped with feedback between the buffer level-of-content (see footnote on page 6) and the processor significance detector. This configuration makes it possible also for the *output* of the buffers to be *controlled* by the level-of-content. A simple arrangement may be devised by which nearly empty buffers are sampled less frequently than are buffers that are nearly full.†

The design of such an arrangement is depicted in the logic diagram, Figure 3. A sequencer, whose main purpose it is to control the data flow from a particular buffer onto the output data bus, is normally augmented (i.e., indexed, or advanced) by a word clock. By means of additional control gates, as shown in the diagram, the sequencer can also be augmented by a high speed service clock. This operation is controlled by the level-of-content control terms $b_1, b_2, b_3, \ldots b_n$ from the various buffers as follows: The sequencer will advance at high speed until it reaches the position of a buffer whose control term calls for unloading, and stop. The next advance pulse will be the word clock. If the following position is a buffer with a low level-of-content, the sequencer will again advance at high speed until it finds a buffer term indicating a high level-of-content.

When the self-adaptation bandwidth allocation feature is applied to the system, both time and address *must* accompany a sample. The channel address may be the actual address in

*Time: the instant at which the measurement was taken (e.g., the data was latched into the Sample-Hold). In the case of redundancy-reduction data compression, it is the time at which an item of data accepted into the buffer was obtained. "Location in the frame" means a specific interval in the multiplex cycle.

†Sometimes known as the "squeaky wheel" philosophy.

the frame (mechanized as shown in Figure 4), or in incremental address (number of channels bypassed, Figure 5), or a word that reflects the sampling pattern (Figure 6), transmitted at the end of each frame. In reference to buffer utilization, the addition of the self adaptive bandwidth feature will again allow an accepted sample to enter the buffer based on the past history of activity of all channels collectively rather than on that of an individual channel.

Non-adaptive or prescribed bandwidth allotment between channels is controlled by varying the level-of-content threshold above which the buffer is sampled.

HARDWARE IMPLEMENTATION

Recent advances in the state of the Digital-to-Analog art have made possible complete integrated-circuit Analog-to-Digital converters of physical size small enough to be utilized directly at the signal source. An example of such a device is the Analog Devices, Inc. μDAC, which can be cascaded in 4 bit segments to a maximum resolution of 16 bits. Switching time is 800ns to ±½LSB (10 bits) allowing conversion rates approaching 1MHz at the signal source. The device is monolithic, which enhances its reliability and ability to operate continuously in a deep-space environment. Utilizing the μDAC, and taking advantage of Medium-Scale Integration techniques to provide the logic, a complete 8 bit analog-to-digital converter should be possible in 6 to 8 TO-87 flatpacks.

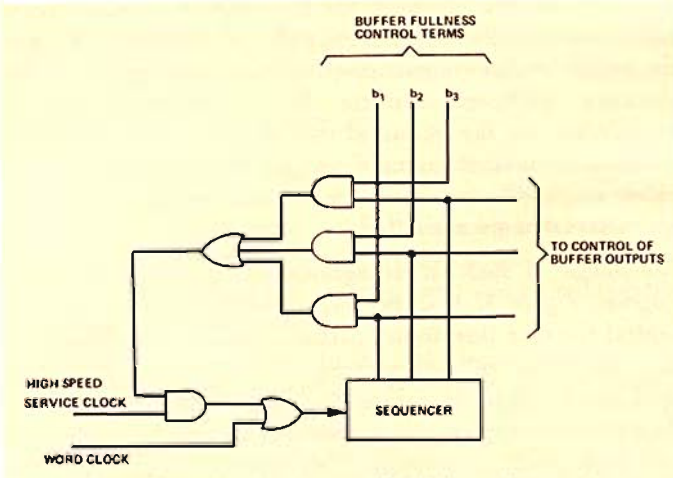


Figure 3. Adaptive Output Multiplexer Control

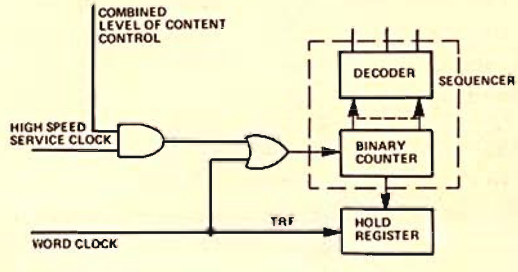


Figure 4. Actual Address Register Logic

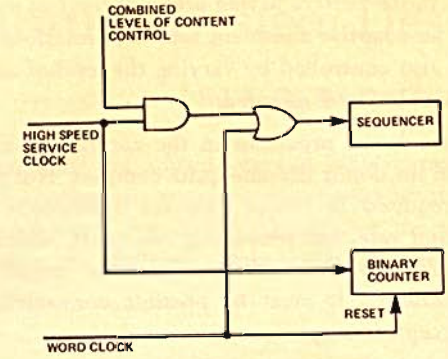


Figure 5. Incremental Address Logic (Counting Number of By-Passed Channels)

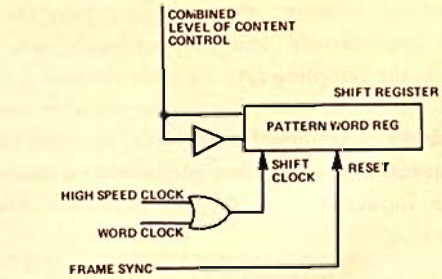


Figure 6. Sampling—Pattern—Word Logic

THE AUTHOR

Tage O. Anderson was born in Mellerud, Sweden, on August 7, 1926. He received a degree in electrical engineering at the Chalmers Institute of Technology, Gothenberg, Sweden, in 1947.

From 1948 to 1953 he was an Instrumentation Engineer in the Nuclear Chemistry Department, Chalmers Institute of Technology. From 1953 to 1958 he was engaged in design work on digital data processing equipment for a Swedish company, and from 1958 to 1963 he was with Consolidated Systems Corporation (now part of Xerox Data Systems), Pasadena, Calif., where he held a position as Principal Systems Engineer. In 1963 he joined the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, where he is now a member of the Technical Staff in the Telecommunications Division, active in the fields of synchronization, error-control coding, and data compression. He is the holder of several patents in those fields.

Mr. Anderson is a member of Sigma Xi.

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2. J. H. Chang, "Comparison of Synchronous and Asynchronous Time Division Multiplexing Techniques," 1970 International Conference on Communications, San Francisco, June 8, 9, 10, 1970.
3. "Low-cost A/D Converters May Revolutionize Data Acquisition," *EEE*, January 1970, pp. 32–34.

new products

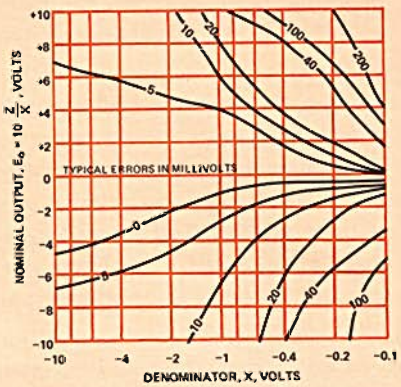
Accurate Multiplier/Divider

PRE-TRIMMED MULTIPLIER/DIVIDER WITH 0.2% ACCURACY, 100kHz BANDWIDTH

Based on the highly-successful Model 424, the 427K* is internally trimmed to specified accuracy and requires no external adjustments for multiplication. It uses pulse-width modulation to obtain accuracies to 0.2% (FS),† offset drifts as low as 200μV/°C, and nonlinearity of 0.04% maximum, for both inputs. Unlike most high-accuracy multipliers embodying the modulation principle, 427's high carrier frequency allows a bandwidth rating of 100kHz for −3dB response. Depending on how it is connected, the 427 can be used for multiplying, dividing, squaring, or square rooting.



The real test of the mettle of a Multiplier/Divider is its accuracy when connected as a divider, especially for small denominators. The plot indicates the contours of equal error as a function of X (log scale) and nominal output (10Z/X) for a typical unit. Because of its excellent small-signal linearity, the errors are very much smaller than one would predict by simply multiplying the specified full-scale error by 10/X. For example, when X = −0.2V, the error is less than 0.2V (2% of full scale) and even better for negative output values; compare this with the predicted 20mV X 10 / 200mV = 1.0V.



SPECIFICATIONS:	427J	427K
Overall Accuracy, % error	0.25% max	0.2% max
(with optional ext. trim)	0.15%	0.1% max
Error vs. Temp. max	0.02%/°C	0.02%/°C
Output Offset	±5mV	±5mV
Offset vs. Temp.	200μV/°C	200μV/°C max
Nonlinearity, max	0.08%	0.04%
Feedthrough, max p-p (10V X 0)	10mV	10mV
Bandwidth (small signal, −3dB)	100kHz	100kHz
Full Power Response	30kHz	30kHz
Price (1–9)	$159.	$210.

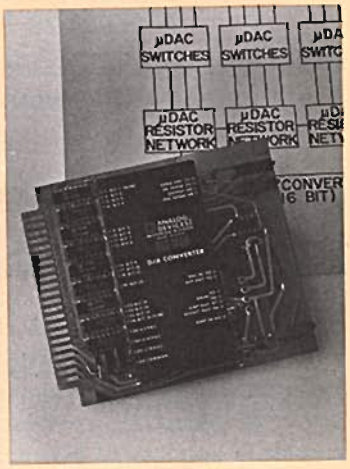
*For technical data on Model 427K, use the reply card. Circle A12

†If desired, 427K can be trimmed externally to 0.1% max

DAC's with 16-Bit Resolution

The Modular DAC-QM series* of D/A Converters now includes the 16-bit DAC-16QM and the 14-bit DAC-14QM. 16-bit resolution means that the least significant bit is 1/65,536 of full scale (about *16ppm*!). In order to obtain this degree of resolution, the nonlinearity is ±8ppm (±½LSB), and conversion is fully monotonic for all transitions. The high-resolution DAC-QM's are compatible with both TTL and DTL logic, and optional codes include both complementary binary and complementary BCD. Output options include digital-to-current conversion: 0 to −2mA into zero volts (op-amp summing point) and digital-to-voltage conversion at ±5V, ±10V, 0 to +10V, all at 1mA. Price is only $395 for 14-bit linearity, $745 for 16-bit linearity. How do we obtain high linearities at such low cost and in such small space (2" X 4" X 0.4")? The "secret ingredients" are Analog's own μDAC switch and resistor networks.





MANIFOLD BOARD PROVIDES OPTIONS, FLEXIBILITY

The modular DAC-QM series is intentionally provided in the most simple, basic and compact form so that the user can have the greatest degree of flexibility in packaging, input codes, and output circuitry. For the user who would like Analog to "put it all together," we make available the DAC-QG edge-connector manifold board, with its many circuit options, to accept any DAC-QM, from 8 to 16 bits. It will provide such services as a versatile input register, with 5 code combinations; a "deglitcher," for limiting switching transients to ±5mV; a choice among high-performance output amplifiers to match settling time, dc offset stability, or cost (using DAC-QM's internal output amplifier) to your needs; as well as offset and scale factor trim adjustments for DAC-QM's.

FEATURES:
DAC-16QM MODULAR D/A CONVERTER
16 Bit Resolution and Linearity
TTL/DTL Compatible
Nonlinearity ±8ppm of Full Scale
Monotonic for all Transitions
Codes: Complementary Binary or BCD
Dimensions: 2" X 4" X 0.4"
Output Short-Circuit Protected

Prices:	DAC-14QM	$395.
	DAC-16QM	$745.

*For technical data on the DAC-QM series, use the reply card. Circle A13

FEATURES (continued):
DAC-QG MANIFOLD BOARD
Options:
Storage Register with 5 Code Combinations
Deglitcher
Output Op Amp (13μs settling to 15ppm with Model 45, 0.5ppm/°C offset with Model 233K, for unipolar output
Circuit Card with Edge Connector, 4½" X 4¾"
Includes Gain and Zero Pots and receptacle pins
Prewired to Receive DAC-16QM and the following elements:

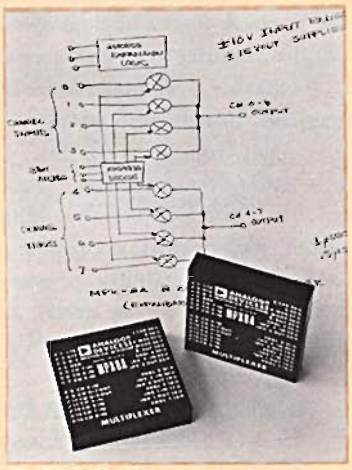
	Prices
Prewired Board	$ 75.
Input Register	120.
Low-drift op amp (233K)	55.
Fast-settling op amp (45K)	55.
Transient suppressor	150.

Versatile Multiplexer

8-CHANNEL MULTIPLEXER CAN BE USED DIFFERENTIALLY OR SINGLE-ENDED FOR 0.01% ACCURACY; HAS ALL NECESSARY LOGIC FOR USE IN 64-CHANNEL SYSTEMS

The MPX-8A* is a complete 8-channel high-speed MOSFET Multiplexer packaged in a small (2" X 2" X 0.4") encapsulated module. The TTL/DTL-compatible binary address selection logic is unusually complete, containing all the logic elements needed for expansion to 64 channels, either single-ended or differential. When the MOSFET switches "play into" high-performance buffer or instrumentation amplifiers in the conventional manner, the combined switch/amplifier subsystem is capable of accuracy of better than 0.01% and CMR of 120db and beyond. Data throughput rates will in most cases be limited by the associated circuitry and equipment, since the MPX-8A itself settles to within 0.01% in from 400ns to 2μs, depending on the direction in which the signal slews.

FEATURES:
8-Channel Single-Ended or 4-Channel Differential Operation
High-Impedance MOSFET Switches
DTL/TTL Compatible Control Logic
Binary Address Selection
±10V Signal Range with ±15V Power
No High Voltage Supplies are Necessary
Settling Time Less than 2μs to 0.01%
Crosstalk less than −80dB
Small Modular Package: 2" X 2" X 0.4"
Multiplex System can be Expanded to 64 Channels without adding External Logic Gates
Price (1–9): $175.



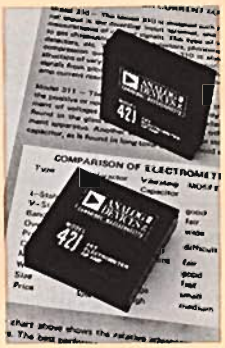
MANY APPLICATIONS

Accurate and easily addressable multiplexers, such as the MPX-8A, are the key to cost control in computer data acquisition systems. For it is the time-sharing characteristic of the system that results in cost sharing of the relatively expensive computer among many data channels and brings down the "per-channel" equipment cost to highly competitive levels. Typical examples of systems in which the MPX-8A might be employed are data acquisition systems, (prior to A/D conversion), data distribution systems (following D/A conversion), and simultaneous sample-hold and sequential readout in the analog portions of systems.

*For technical data on Model MPX-8A, use the reply card. Circle A14

0.15pA FET Op Amps

LOW-COST "ELECTROMETER TYPE" J-FET OP AMPS HAVE 0.15pA BIAS CURRENT AND LOW DRIFT, CHALLENGE PARAMPS AND MOSFETS



Low-cost FET op amps feature bias currents in the 25–100pA region and prices from around $10 (e.g., Analog's Model 40). Premium FET types bring bias current down to the 5pA neighborhood, but escalate price to $40 and up. Until now, FET-input op amps with bias currents below 1pA have been pretty rare, and their cost has been pretty high.

Thanks, however, to newly-developed FET transistor pairs (*Analog Dialogue*, Vol. 4, No. 2) we have been able to develop a new generation of FET op amps, whose 0.15pA bias current levels puts them virtually in the electrometer category, midway between 0.01pA varactor bridge amplifiers (such as 310 and 311) and the existing FET premium types. Price, on the other hand, has not risen with performance, but remains in the $36–$84 region for Models 42* and 41*. Furthermore, substantial discounts are available in quantity; for example, the 100-piece price of Model 42J is only $25, an economical alternative to in-house manufacture.

Besides approaching the varactor bridge amplifier's current sensitivity, the new FET units solve a major varactor bridge limitation (very modest bandwidth) in two ways: First, their input capacitance is only 3pF (vs. 30pF); second, their inherent bandwidth is greater: 1MHz small-signal (vs. 2kHz). Thus, the Models 41 and 42 FET amplifiers can be applied in fast-response circuits that the varactor-bridge types can't touch.

APPLICATIONS

In contrast to varactor types, the new FET-input versions can handle fast integrator, differentiator, and sample-hold circuits, where low bias current *and* rapid response are required simultaneously. Additional circuits combining the need for fast response and utmost current sensitivity include charge amplifiers, and—especially—wideband logarithmic amplifiers that must span many decades of input signal swing, the lowest decade at high impedance. Fast response (or low input capacitance) and extreme current sensitivity are also characteristic of amplifiers required to handle the output signals developed by automated blood analyzers, ion gages, gas chromatographs, mass spectrometers, pH meters, and other modern on-line and quality-control instrumentation. No other types meet these speed/sensitivity needs with adequately low noise and drift.

*For technical data on Models 41 & 42, use the reply card. Circle A15

TWO VERSIONS

Model 41 is designed as a differential amplifier and therefore handles both inverting and noninverting configurations (and, of course, differential circuits). Model 42, a less costly unit, is designed with a common-mode capability of ±1V and CMRR of 2,000. (This feature enables Model 42 to be used for applications that are only marginally in the noninverting category, such as in elimination of millivolts of ground loop error.) A brief summary of their specifications follows:

SPECIFICATIONS:	41J/K/L	42J/K/L
Bias Current (pA, max)	0.5/0.25/0.15	0.5/0.25/0.15
Voltage Drift (μV/°C, max)	25/10/25	75/25/75
Current Noise (0.1–10Hz)(pA)	0.005	0.005
Voltage Noise (5Hz–50kHz) (μV rms)	10	8
Unity–Gain Bandwidth (MHz)	1	0.5
Full Power Bandwidth (kHz, min)	50	4
Common Mode Rejection Ratio (±1V range)		2,000
(±5V range) (min, ±10V range, 41JV/KV/LV)	50,000 10,000	
Price (1–9) J/K/L	$66./$84./$84.	$36.†/$48./$48.
41JV/KV/LV	$71./$89./$89.	

12-Bit Resistor Networks

HERMETICALLY-SEALED IC THIN-FILM RESISTOR NETWORKS FOR D/A'S AND A/D'S TO 12-BITS*

Somewhat overshadowed by that dramatic duo of monolithic IC's for high-precision D/A and A/D conversion, the AD550 current switch quads and the AD555 voltage switch quads, are their more prosaic passive partners for precise conversion, the thin film resistor networks. Nichrome thin-film construction and small physical size combine to provide temperature tracking of ±1ppm/°C and excellent stability. Starting with a precision reference voltage or input current, the μDAC resistor network, paired with the appropriate μDAC switch, forms the heart of 4- to 12-bit D/A (and A/D) converters capable of 0.0125% accuracy.

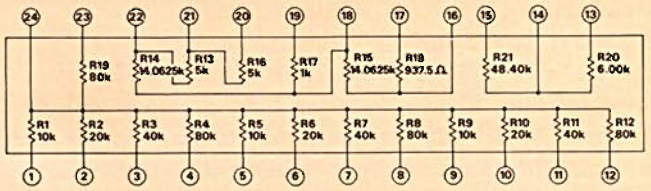
FEATURES:

- 12-Bit Resolution
- ±½LSB Accuracy
- ±1ppm/°C Tracking
- −55°C to +125°C Operation
- Long Term Stability
- Meets MIL-STD-883
- Hermetic Flat Pack or Dual In-Line Package

*For technical data on Thin Film Resistors, use the reply card. Circle A16
†Model 42J: $25 in 100's

AD850 12-BIT BINARY NETWORK FOR USE WITH AD550 CURRENT SWITCHES

This network, designed for use with AD550's, will work equally well in industrial or military applications. Its complement of tracking resistors on a single substrate furnishes all the precision resistors needed for accurate conversion. Included are: current weighting resistors, interquad current-dividing resistors, amplifier-feedback resistors for 5V or 10V output, and offset-reference resistors for bipolar output. *Soon to be announced:* AD851: networks for BCD conversion, in the same package.



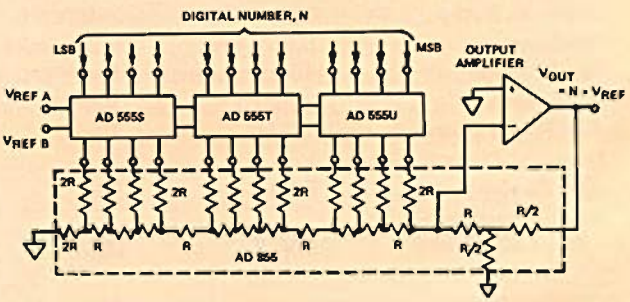
AD852 AND AD853 IN TO-87 FLAT PACKS OR TO-116 CERAMIC DUAL IN-LINE PACKAGES FOR MILITARY AND "HI-REL" APPLICATIONS WITH AD550 IN DIFFICULT ENVIRONMENTS

Electrically, these two 14-pin types combine to perform the same functions as the AD850. Where 8-bit accuracy is sufficient, the AD852 is designed to be capable of doing the whole job by itself. Both types are available with the following environmental conditioning in accord with MIL-STD-883, level B, 100% testing:

- Internal visual inspection, method 2010, Condition A,
- Temperature cycling, MIL-STD-883, method 1010, Condition C, −65°C to +150°C,
- Mechanical shock, MIL-STD-883, method 2002, Condition F, 20,000 g's on the Y_1 axis (on a sample basis),
- Fine leak, hermetic seal, MIL-STD-883, method 1014, condition A, 5×10^{-7} cc/sec.
- Gross leak, hermetic seal, method 1014, Condition C.

AD855, AN R–2R NETWORK IN 16-LEAD CERAMIC DUAL IN-LINE PACKAGES OR FLAT PACKS FOR USE WITH AD555 VOLTAGE SWITCHES

An unusual design, specifically conceived to mate with the AD555, the first 4 bits of this resistor ladder are slightly low in value to exactly compensate for the nominal series resistance of the monolithic switches. Conversion errors are due only to variations of resistance in the switches, a second-order error. AD855 networks are available in 8-, 10-, or 12-bit versions for both military and industrial temperature ranges.



new products

0.5% Multiplier/Divider



PRE-TRIMMED 0.5% TRANSCONDUCTANCE MULTIPLIER/DIVIDER IS "BEST BUY" AT $89 (1–9), AN EVEN BETTER BUY IN LARGER QUANTITY

Analog's new Model 428* analog multiplier/divider is internally adjusted during manufacture for 0.5% accuracy, and 0.02%/°C temperature coefficient, thereby enabling it to operate over a 50°C temperature range with less than 1% error increase. Besides featuring 0.5% accuracy without adjustment, Model 428 can actually be trimmed by the user to within 0.25% in special applications requiring utmost accuracy at lowest cost. (Note: most analog multipliers capable of 0.5% accuracy list for $125 or more, compared with $89 for Model 428A).

Specifications for the new multiplier, besides the 0.5% 'off-the-shelf' accuracy, or 0.25% with user trim adjustments, include 500μV/°C and 200μV/°C output offset drift (Models 428A and 428K, respectively), 5V/μs slewing rate, and ±11V, 11mA output. Not only will Model 428 perform as a multiplier or squarer—implementing such functions as modulator, demodulator, phase-locked loop, mean square computing, variable cutoff active filter—but it operates as a divider or square-rooter without requiring an external operational amplifier in the feedback loop.

The nonlinearity component of error is particularly low in this unit, resulting in excellent performance as a divider, for example: 50mV maximum error for a 10:1 dynamic range of denominator.

In addition to its excellent dc performance, it has 300kHz small signal bandwidth (−3dB) and full power output to beyond 70kHz, considerably exceeding the audio range. Model 428 is packaged in a 1.5" square by 0.62" high case.

Both Models 428A and 428K are available from stock, and list at $89 and $109 each (1–9).

Salient specifications are listed below.

SPECIFICATIONS:	428A	428K
Overall Error	0.5% max	0.5% max
Accuracy vs. Temp	0.02%/°C	0.02%/°C max
Output Offset	±10mV	±10mV
Offset vs. Temp	500μV/°C	200μV/°C
Nonlinearity	0.25% max	0.25% max
Feedthrough	40mV p-p max	40mV p-p max
Bandwidth	300kHz	300kHz
Full Power Response (Fp)	70kHz	70kHz
Division—Dynamic Range of Denominator	50:1	50:1
Square Rooting—Dynamic Range of Input	500:1	500:1

▶▶▶

*For technical data on Model 428, use the reply card. Circle A17

Analog Insight

A "741" with 2μV/°C Drift

HOW TO SAVE $ BY SELECTIVE PARAMETER OPTIMIZATION

by Dave Porta

The low cost of integrated circuits is a direct consequence of high-volume batch processing. In a batch of monolithic IC's are units meeting a wide variety of specifications. Variations result from both the circuit design and the limitations of practical process control. Small differences in such things as doping levels and silicon diffusion characteristics produce variations in electrical characteristics, both from unit to unit and from lot to lot.

Held to a practical minimum by careful processing, these variations are the key to both low user cost for large numbers of units (e.g., AD741C), and the availability of premium units at nominal extra cost (e.g., AD741K). Standard families developed in this way include the AD741, AD741K, AD741C, and the AD101A, AD201A, AD301A. Each parameter specification is established on the basis of yield and correlation with the yield of parameter values for a given family member. That is, yields of certain key parameter values will also include a large yield of related parameter values.

Knowledge of this is important to the OEM circuit designer who uses devices, because it can be the key to his obtaining units having the specs he needs at low cost through selection by the manufacturer (viz., Analog Devices) from among very large numbers of popular units having low basic prices, instead of designing with more expensive families (or combinations of devices into hybrid circuits), which can result in much higher cost, and perhaps more performance than is actually needed.

An example may serve to illustrate the case. An OEM user designs a circuit using a 741-type amplifier preceded by a μA727 constant-temperature differential pair to obtain drifts in the 1–2μV/°C region. He subsequently discovers that he can purchase, in the quantity he requires, as a selection from standard AD741 production, at a parts cost saving of some 70%, a *single device* having the following characteristics:

	25°C	Avg. Drift
Offset Voltage, max	0.5mV	2μV/°C
Bias Current, max	30nA	200pA/°C
Offset Current, max	2nA	20pA/°C

This type of selection is possible because of the high volume of product constantly flowing through Analog's automatic linear IC test system. Even though the yield to the specifications listed above is relatively low, the heavy flow of units allows selection of a sizeable number of such devices. The same technique may be used to select devices having better-than-standard parameters other than those listed above, for example: Gain, CMR, PSR, etc. By specifying a low-cost, specially selected unit, the user saves money, because the cost is increased only by the cost of testing and the factors affecting yield. Analog's excellent yields and testing expertise have made it feasible to make special selections from a number of popular families, including the AD101A, AD502A, AD741, and AD503.

To draw an analogy from another field, if you want to win a race, it may be done at lower cost with a souped-up Chevvy than with a Corvette. ▶▶▶

Application Brief

Measuring Air Flow Using a Self-Balancing Bridge

The design of a hot wire anemometer presents an interesting application for operational amplifiers.

The purpose of the instrument is to measure air speed by its cooling effect upon an electrically heated platinum filament that exhibits a high positive temperature coefficient of resistivity.

The filament characteristic is shown in Figure 1, for two values of air speed. Two classical ways of operating it would be at constant voltage or constant current.

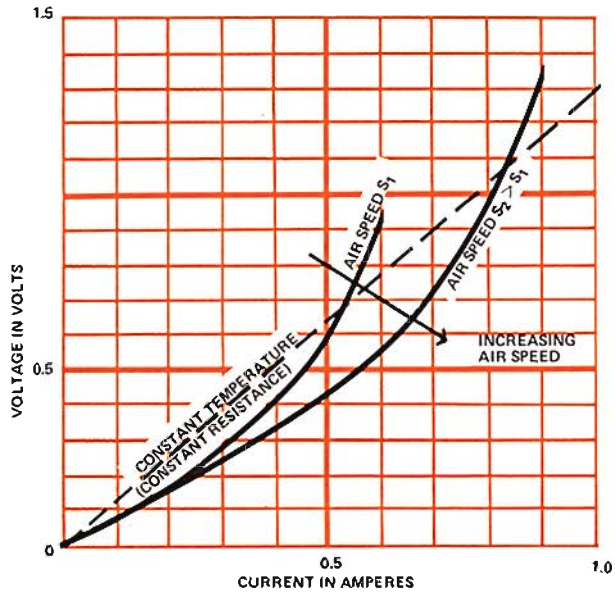


Figure 1. Volt-ampere characteristics of 7/16"L X 0.002"D straight filament of pure platinum in the presence of moving air, for two values of air speed.

With constant current applied (say, 0.6 amperes), the sensitivity is reasonably good—about 0.4V change for $\Delta s = s_2 - s_1$. However, there is every prospect that in still air the filament has the potential of burning itself up (resistance increases as temperature increases, due to lack of air flow, which causes the voltage to increase [constant current], increasing the dissipation, the temperature, and again the resistance, etc.).

With constant voltage applied, the increase of resistance with temperature causes operation to be quite safe, but also relatively insensitive, especially at low air speeds.

Another factor that makes both constant-current and constant-voltage operation unsatisfactory is the necessity for the temperature of the filament to change to detect a change in air speed; this necessarily causes delay. If the air speed indicator is part of a control loop, the measurement delay could cause slow response or instability of the control loop.

An approach that answers all of these objections satisfactorily is to operate the filament as though it had constant resistance (i.e., constant temperature).

THE AUTHOR

Ing. José Miyara is a partner in the firm TELEGUARD, in Rosario, Argentina. Their principal activities are in Industrial Electronics and Automatic Control.

If, for example, the resistance were maintained at 1.3Ω, as indicated by the dashed line, one could obtain a current change of 0.3A and a voltage change of 0.4V, with no danger of overheating in normal operation. Response would be quite speedy, since temperature changes are momentary and small.

The basic circuit for achieving constant temperature operation is the feedback circuit of Figure 2, consisting of a bridge, an op amp, and a power amplifier. The operational amplifier continuously adjusts the flow of current (through the power transistor) to maintain its two inputs equal. This can be done only by keeping the voltage across the filament equal to that across R2, and the filament current equal to the current through R1. However, since the current through R1 is proportional to the current through R0, (which has the same voltage drop as R1) and the current through R0 is determined by the voltage drop across R2, it can be seen that the resistance of the filament, R_F, must be equal to that of R2, multiplied by the ratio of R_1 to R_0.

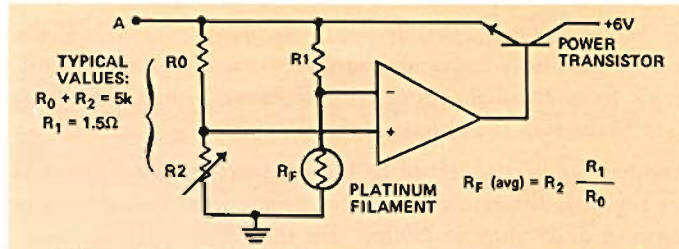


Figure 2. Basic circuit of the temperature-controlled bridge

Suppose now, that, starting from a given operating equilibrium point, the air flow increases. This will take heat away from R_F, causing its voltage to tend to drop. The amplifier's output voltage increases, which increases the current through the power transistor, and thus makes more power available for the filament to dissipate to maintain its temperature (and hence its resistance) constant.

The output voltage is measured at terminal "A", which provides an amplified version of the filament voltage, at an impedance level low enough to operate even the crudest of meter movements.

The zero-air-speed voltage is backed off by means of an auxiliary constant voltage, and the readings can be displayed with a moving coil meter. The scale is a nonlinear function of air speed, actually expanding toward the lowest values. Low air speeds can be read with high sensitivity; in fact, the device can virtually detect a whisper several feet away.

CIRCUIT NOTES

For practical realization, the following points must be considered:

1. A voltage offset must be deliberately introduced into the operational amplifier (or elsewhere) to insure that the output goes positive with zero differential input; otherwise, the circuit might remain dead when turned on.

2. The power transistor must have ample current-handling capacity; the filament requires several hundred mA.

3. Depending on the physical layout, especially when the filament is away at the end of a twisted pair, wild high frequency oscillations are possible. Though not visible with low

frequency readout devices (however, rectification can cause voltage offsets), they look nasty on an oscilloscope screen. A 0.1μF capacitor between the base and collector of the power transistor can often serve to stabilize these oscillations. A small resistor in series with the base may also be helpful.

4. The filament is a physical device with thermal lag. Although the circuit is fast enough to prevent loop oscillations when used in a larger control loop, it is itself a process control loop and may require the usual compensation techniques to maintain its own internal stability.

5. R0 and R2 form a trim potentiometer to set the operating temperature (e.g. resistance) of the filament. If R2 is a variable resistance, you start with $R_2 = 0$, and increase it until the filament just starts to glow, then back down a little. This will give optimal sensitivity.

APPLICATIONS

The device has been used in a commercially-produced apparatus to trip out equipment when the air speed in a forced draft duct falls below a preset value, but the approach is suggestive of a number of other applications in instrumentation.

In gas chromatographs, it could be used to monitor the minute gas flows required, and also to assure optimum sensitivity from thermal-conductivity filaments, while preventing their burnout in faulty operation.

Another application could be for constant-temperature ovens for crystals, differential pairs, etc., using copper or a thermally sensitive alloy such as "Balco" for the combined heater/temperature-sensor function. In such an arrangement, the controlled temperature could be slaved to another (arbitrarily) variable temperature (e.g., to insure a constant temperature difference) if R2 were a platinum temperature bulb with the circuit so dimensioned as to avoid causing it to introduce errors due to its own self-heating. ▶▶▶

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Multiplier Handbook



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Worth Reading

"Detection and Measurement of Three-Phase Power, Reactive Power, and Power Factor, with Minimum Time Delay," by I. R. Smith and L. A. Snider, University of Birmingham (England), *Proc. IEEE*, November, 1970, p. 1866

In this brief but significant communication, the authors show how to compute average power in a symmetrical 3-phase system with sinusoidal waveforms, without the time delay normally introduced by filtering. With three multipliers to compute the instantaneous power developed by the phase voltages and line currents in each phase, and summing the outputs with an op amp, the dc "average power" terms add, and the harmonic terms cancel algebraically, without the intervention of filters. By phase shifting either the voltages or the currents by 90°, reactive power can be computed in the same way. And the ratio of reactive to real power (using a divider) is tan ϕ, an often useful parameter in control systems. For small values of ϕ, it is, in fact, equal to phase angle.

"Selecting the Optimum Multi-Path Digital-to-Analog Configuration," by D. H. Sheingold, *Electronic Instrument Digest*, (A Kiver Publication), July, 1970

Virtually a complement to Mr. Anderson's paper (page 6 of this issue of *Dialogue*) for output systems, this article considers the question of whether to multiplex digitally and use many D/A converters, or to convert in one location, and route the analog output via sample-holds. The tradeoffs involved in selecting an output configuration that provides the desired performance at the lowest overall cost are identified and discussed. Copies of this six-page paper are available from Analog Devices. Use the reply card. *Circle* **A2**

NOTED BRIEFLY

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"FET Op Amps–Make or Buy" *Application Brief* by Stan Harris, **Circle A7.**

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IC FET-Input Op Amp in a TO-99 can, 15μV/°C drifts, 2pA bias, 6V/μs slew rate, AD503, **Circle A10.**

(Continued from Page 5)

ERRORS AND ADJUSTMENTS

The basic low frequency equation of AD530, connected as a multiplier, indicates the salient sources of error and provides an insight into the adjustment scheme

$$E_0 = Z = \pm Z_0 + (X \pm X_0)\,\frac{Y \pm Y_0}{10B} + f(X,Y)$$

Carrying out the multiplication, grouping and labeling errors,

$$E_0 = \underbrace{\frac{XY}{10B}}_{\text{PRODUCT (WITH GAIN ERROR)}} \pm \underbrace{\frac{X_0 Y}{10B}}_{\text{Y FEEDTHROUGH (X OFFSET)}} \pm \underbrace{\frac{XY_0}{10B}}_{\text{X FEEDTHROUGH (Y OFFSET)}} \pm \underbrace{\frac{X_0 Y_0}{10B} \pm Z_0}_{\text{OFFSET}} + \underbrace{f(X,Y)}_{\text{NON-LINEARITY}}$$

This grouping immediately suggests an adjustment procedure.

1. The offset is trimmed to zero (pin 9 – Z_0).
2. The "feedthroughs" are trimmed to minimum output excursion by applying a ±10V sweep at low frequency to one input, zero volts to the other, and trimming for minimum peak-to-peak output. [±10V to Y, 0 to X, adjust at pin 7 (X_0); ±10V to X, 0 to Y, adjust at pin 10 (Y_0)]
3. Since the X_0Y_0 term is now trimmed out, the offset should be re-zeroed.
4. The gain is trimmed to give ±10V full scale output for ±10V full scale input multiplied by ±10V dc. The simplest and quickest way to do this is to apply −10 volts to one input, a ±10 volt sweep to the other, and sum the output and sweep input passively via a pair of equal resistors (or actively in a summing amplifier). Adjust for zero end point or minimum peak-to-peak error. This will optimize accuracy in the negative half plane of the constant input. (For example, if the sweep is X and the constant Y = −10V, greatest accuracy will be obtained for Y negative.)

To obtain best adjustment for the positive half plane, the fixed input is +10V, and the output must be *subtracted* from the swept input instead of added to it. For best average accuracy in all four quadrants, it may be desirable to make a compromise adjustment at the "least worst" error.

For best accuracy over *limited* ranges of voltage (e.g. ±5V), gain and feedthrough adjustments should be optimized with inputs in the desired range. When so optimized, error will probably be greater over the *specified* range. However, linearity is considerably better over smaller ranges of input (see Figure 7).

DIVISION

For division, the above equation can be applied to the feedback configuration of Figure 5. The result is expressed as follows:

$$E_0 = Y = (10B)\,\frac{Z}{X}\left[\frac{1}{1 \pm \frac{X_0}{X}}\right] \pm Y_0 \pm (10B)\,\frac{Z_0}{X}\left[\frac{1}{1 \pm \frac{X_0}{X}}\right] \pm (10B)\,\frac{f(x,y)}{X \pm X_0}$$

CONSTANT SCALE FACTOR — X-SENSITIVE SCALE FACTOR — CONSTANT OFFSET — X-SENSITIVE OFFSET — X-SENSITIVE NONLINEARITY

The suggested trim procedure is (starting with centered adjustments):

1. With Z = 0, trim Z_0 to hold output constant, as X is varied from −10V toward −1.0V.
2. With Z = 0, trim Y_0 for zero at X = −10V.
3. With Z = X and/or Z = −X, trim X_0 for minimum worst-case variation as X is varied from −10V to −1.0V.
4. Repeat 1 and 2 if step 3 required large initial adjustment.
5. With Z = X and/or Z = −X, trim scale factor for closest average approach to ±10V output as X is varied from −10V to −3.0V.

SPECIFICATIONS: MODELS AD530J & AD530K

(Typical at +25°C and nominal supply voltages unless otherwise noted)

	AD530J	AD530K
Output Function (as Multiplier)	XY/10	XY/10
Max Error, External Trim	2%, 0.8% typ	1%, 0.5% typ
Accuracy vs. Temp	0.06%/°C	0.05%/°C
Accuracy vs. Supply	0.15%/%	0.15%/%
Warm up Time to Specifications	30 sec.	30 sec.
Divides and Square Roots	Yes	Yes
Output Offset		
Initial	Adj to 0	Adj to 0
Avg vs. Temp, 0°C to 70°C	2mV/°C	2mV/°C
Avg vs. Supply	10mV/%	10mV/%
Scale Factor		
Avg vs. Temp, 0°C to 70°C	0.04%/°C	0.04%/°C
Nonlinearity		
X input (X = 20V p-p, Y = ±10VDC) max	0.8%	0.5%
Y input (Y = 20V p-p, X = ±10VDC) max	0.3%	0.2%
Feedthrough		
X = 0, Y = 20V p-p 50Hz with external trim	30mV p-p	30mV p-p
Y = 0, X = 20V p-p 50Hz with external trim	30mV p-p	30mV p-p
Feedthrough vs. Temp, each input	2mV p-p/°C	2mV p-p/°C
Bandwidth		
−3dB small signal	1MHz	1MHz
Full Power Response	750kHz	750kHz
Slew Rate	45V/µs	45V/µs
Settling Time for ±10V Step	1µs to 2%	1µs to 2%
Overload Recovery	1µs to 2%	1µs to 2%
Output Noise		
5Hz to 10kHz	600µV rms	600µV rms
5Hz to 5MHz	3mV rms	3mV rms
Output Characteristics		
Voltage at rated load (min)	±10V	±10V
Current (min)	±5mA	±5mA
Load Capacitance range	0.001µF	0.001µF
Input Resistance		
X / Y / Z input	10MΩ/6MΩ/36kΩ	10MΩ/6MΩ/36kΩ
Input Bias Current		
X / Y / Z input	0.6/0.6/1.0µA	0.6/0.6/1.0µA
Maximum Input Voltage		
For rated accuracy	±10V	±10V
Safe level	$\pm V_S$	$\pm V_S$
Power Supply (V_S)		
Rated Performance	±15V	±15V
Operating	±14 to ±18V	±14 to ±18V
Quiescent Current	±3.5mA, 6mA max	±3.5mA, 6mA max
Temperature Range		
Rated Performance	0°C to +70°C	0°C to +70°C
Operating derated	−55°C to +125°C	−55°C to +125°C
Storage	−65°C to +150°C	−65°C to +150°C

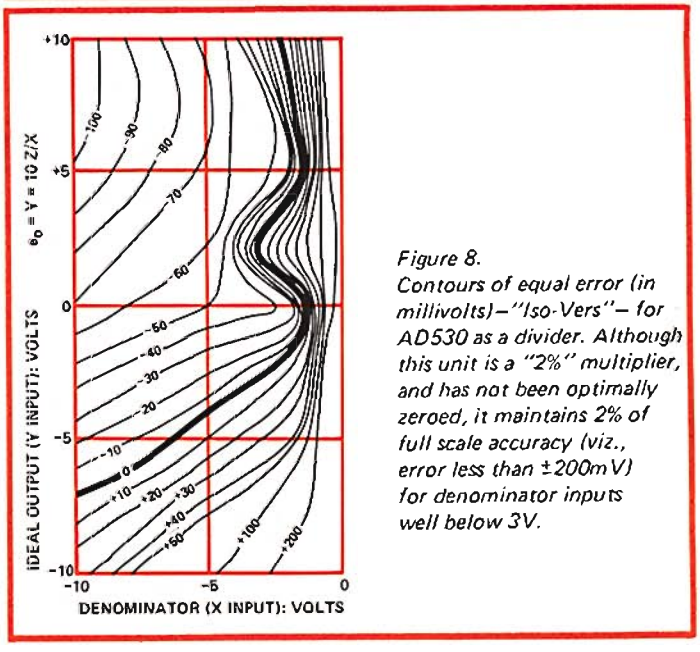
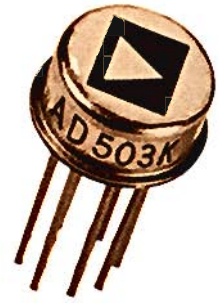


Figure 8. Contours of equal error (in millivolts)—"Iso-Vers"— for AD530 as a divider. Although this unit is a "2%" multiplier, and has not been optimally zeroed, it maintains 2% of full scale accuracy (viz., error less than ±200mV) for denominator inputs well below 3V.

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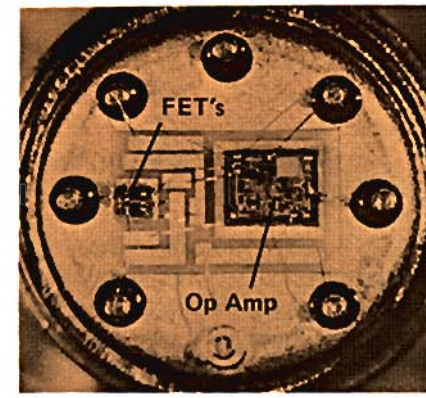
Here's how we do it: the AD503 is a dual-chip IC, combining a monolithic dual FET chip with a specially designed monolithic amplifier chip. This permits independent optimization of both chips, since they are processed independently, each with the most favorable starting materials and doping profiles for its function. Consequently, the yield is high, the cost is low, and the performance is superb. The AD503, in other words, is not limited by the processing constraints inherent in single-chip FET op-amp designs.

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Parameter	AD503J	μA 740C	AD503K	μA 740
Max V_{os} (mV)	50	no max spec*	20	20
Max I_b (pA)	25	2000	10	200
Max ΔV/ΔT (μV/°C)	75	no max spec*	25	no max spec*
Min Gain	20K	no min spec*	50K	50K
Min CMRR (dB)	70	no min spec*	70	64
Min Slew Rate (V/μsec)	4	no min spec*	4	no min spec*

*Manufacturer gives this parameter as typical value only. (Note that only the AD503 is completely min and max specified; the μA 740C is almost completely unspecified.)



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