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Evaluation Board for 4-Channel 500 MSPS DDS with 10-Bit DACs

AD9959/PCB

EVALUATION BOARD BLOCK DIAGRAM

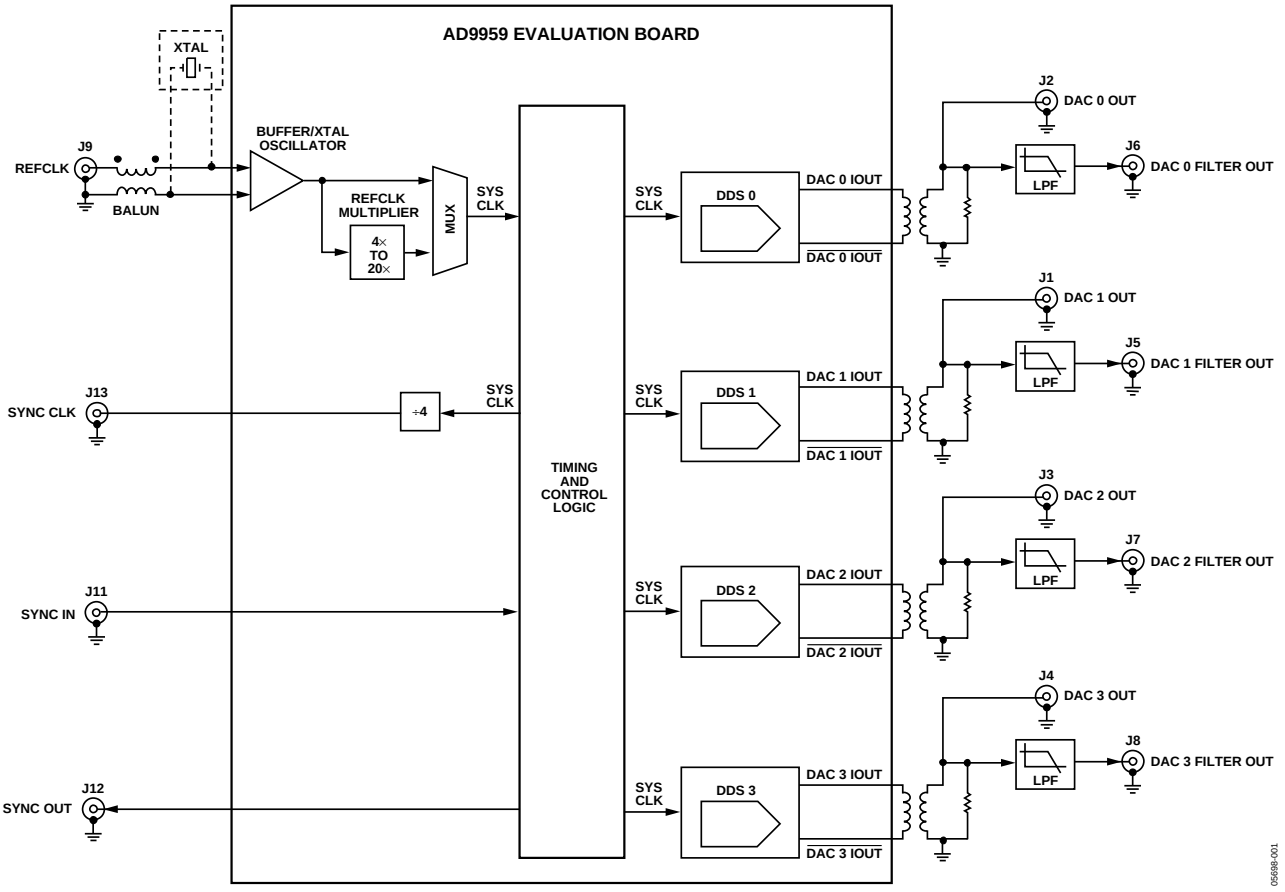


Figure 1.

FEATURES

Full-featured evaluation board for the AD9959

PC evaluation software for control and measurement of the AD9959

USB interface

Graphic user interface (GUI) software with frequency sweep capability for board control and data analysis

Factory tested and ready to use

APPLICATIONS

AD9959 performance evaluation

GUI control panel for learning AD9959 programming

GENERAL DESCRIPTION

This document serves as a guide to the setup and use of the AD9959 evaluation board. The AD9959 is a multichannel frequency synthesizer that incorporates four synchronous direct digital synthesis (DDS) cores with many user-programmable functions.

The evaluation board software provides a graphical user interface for easy communication with the device along with many user-friendly features such as the "mouse-over effect." Many elements of the software can be clarified by placing your mouse over the element. Figure 19 shows how this feature works when users place their mouse over the **Ref Clock** box.

This document is intended for use in conjunction with the AD9959 data sheet, which is available from Analog Devices at www.analog.com.

Rev. 0

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REVISION HISTORY

10/05—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

PACKAGE CONTENTS

The AD9959/PCB kit contains the following:

- AD9959 evaluation board
- AD9959/PCB installation software

REQUIREMENTS

In order to successfully use the evaluation board and run the software, the requirements listed in Table 1 must be met.

Table 1. AD9959/PCB Requirements

Item	Requirement
Operating System	Windows® 98/Me/2000/XP
Processor	Pentium® I or better
Memory	128 MB or better
Ports	One USB port
Clocking	Signal generator capable of generating sinusoidal waves of at least 3 dBm power, up to at least 10 MHz
Power Supplies	Capability to generate at least 2 independent dc voltages (1.8 V/3.3 V)
Measurement	Appropriate measurement device, such as a spectrum analyzer or a high bandwidth oscilloscope
Cables	USB 1.1/2.0 cable, and SMA-to-X cables (X = SMA or BNC, depending on the connector of the device interfacing with the board)

SETTING UP THE EVALUATION BOARD

Powering the Part

The AD9959 evaluation board has seven power supply connectors: TB1, J10, J16, J17, J18, J19, and J20. TB1 powers the DDS, the PC interface logic, and the USB circuitry. J10 powers the input clock circuitry. J18 provides the reference voltage needed for band gap functionality. J16, J17, J19, and J20 power the analog circuitry of individual DACs. It is important to keep in mind that the AD9959 evaluation board has been pre-configured so that these four AVDD connections (J16, J17, J19, and J20) are tied together. Supplying power to any one of the AVDD connections allows for the proper functionality of the analog circuitry of all four DACs. Table 2 shows the necessary connections and the appropriate biasing voltage.

Table 2. Connections and Biasing Voltage

Connector	Pin No.	Label	Voltage (V)
TB1	1	VCC_USB	3.3
TB1	2	DVDD_I/O	3.3
TB1	3	GND	0
TB1	4	DVDD	1.8
J10		CLK_VDD	1.8
J16		AVDD	1.8
J17		AVDD	1.8
J18		BG_VDD	1.8
J19		AVDD	1.8
J20		AVDD	1.8

Note that the AD9959/PCB is preconfigured so that the CLK_VDD, BG_VDD, and all other AVDD connections are tied together. Therefore, only one connection (J10, J16, J17, J18, J19, or J20) needs power for proper functionality of all four channels. These AVDD connections can be separated for better channel isolation. This is accomplished by removing the 0 Ω resistors (R21, R32–R51, R54–R64) that tie the planes together found on the back of the evaluation board. When doing this, be sure that CLK_VDD, BG_VDD, and the AVDD connection for all desired channel(s) are powered.

Clocking the Part

The AD9959 architecture provides the user with two options when providing an input signal to the part. Figure 1 shows that the user can clock the frequency synthesizer/DDS directly by connecting an external clocking signal to the REF CLK connector, J9, or by providing an external crystal. Place jumper W11 on REF CLK to use the external clocking option. To use an external crystal as the clocking source, place jumper W11 on CRYSTAL.

Please refer to the AD9959 data sheet for details on the maximum input speeds and input sensitivities of these two inputs.

Communicating with the Part

Two interface standards are available on the evaluation board:

1. USB 1.1/2.0 interface.
2. Header row (U2, U13), which places the part under the control of an external controller (such as a µP, FPGA, or DSP).

Analog Devices provides a GUI for the PC; it does not provide control software for external controllers.

Use the jumper settings listed in Table 3 to enable different modes of communication.

Table 3. Jumper Settings for Communication Modes

Mode	Settings
PC control, USB port	Set W7 to PC. Place a jumper on W1, W2, W3, W9, and W10.
External control	Set W7 to manual. Place a jumper on W9, and remove W1, W2, W3, and W10 (or leave it stored as a shunt).

EVALUATION BOARD LAYOUT

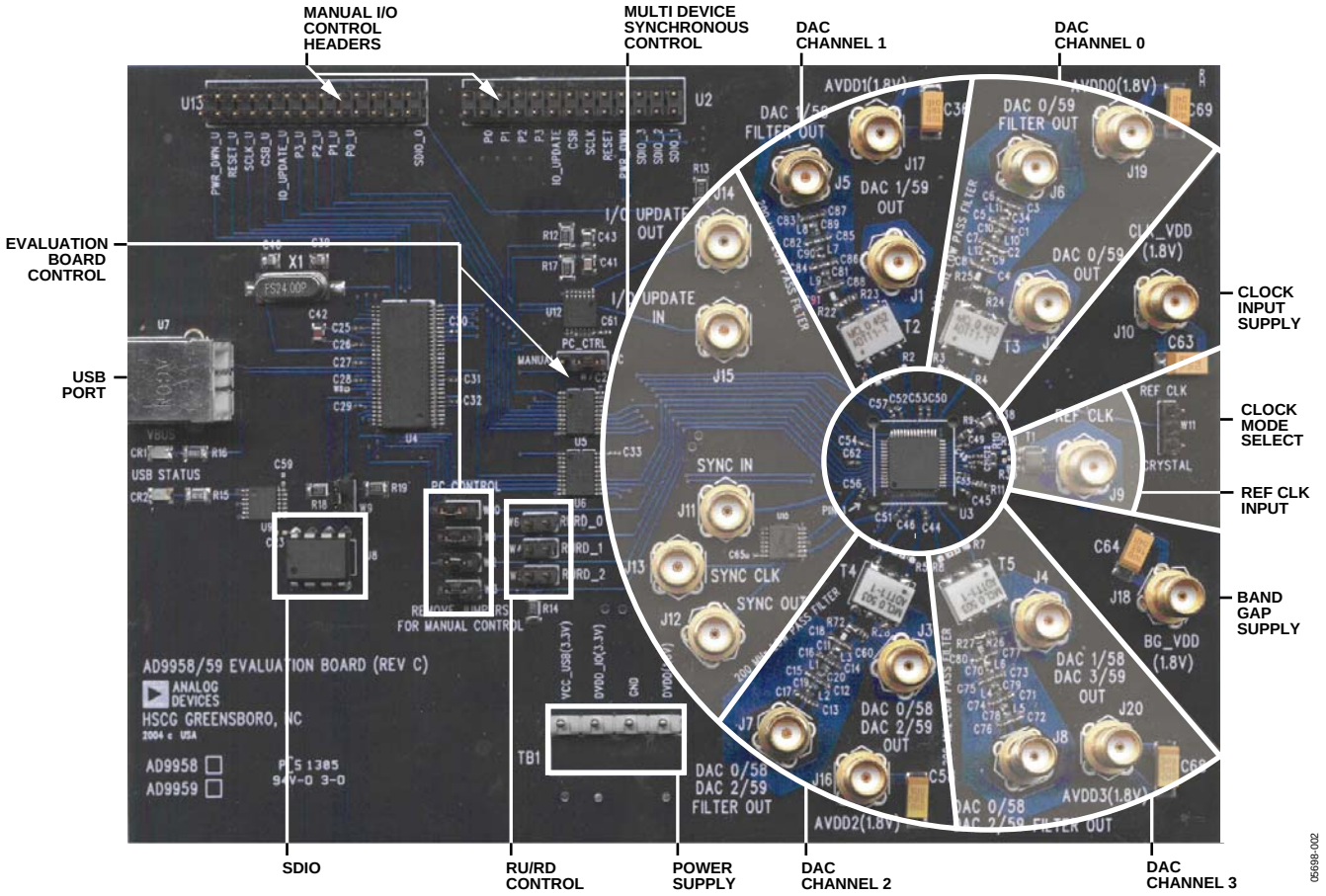


Figure 2.

Manual I/O Control Headers

Provides the interface for communication with the AD9959 when the part is under the control of an external controller (manual control). See Eval Board Control for correct jumper settings.

Multi Device Synchronous Control

These connections set up the AD9959 for multi device synchronous operation.

DAC Channels

These connections represent the DAC filtered/unfiltered output and AVDD power supply.

Clock Input Supply

Powers the AD9959's clock input circuitry.

Clock Mode Select

Controls whether the part is driven by a 20 MHz to 30 MHz crystal provided by the user, or by an external signal generator, such as Ref Clk.

Ref Clk Input

Input for the external Ref Clk signal.

Band Gap Supply

Provides the voltage needed for band gap functionality.

Power Supply

Powers the AD9959's USB circuitry, I/O circuitry, and the digital portion (DVDD) of the DACs. Note AVDD is not powered via this connector (TB1).

RU/RD Control, SDIO

Jumpers W6, W5, and W4 must be set to control the Ramp Up/Ramp Down feature using the SDIO pins.

USB Port

When the part is under PC control (default mode), the evaluation board communicates with the AD9959 via this port.

Eval Board Control

These jumpers set up the AD9959 for manual or PC control (control through the USB port). Figure 3 shows the correct jumper placements for PC control. For manual control remove jumpers W0, W1, W2, and W3; set W7 on the manual control pin (move jumper one position to the left).

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

Follow these steps to install the AD9959 evaluation software:

1. Log into your PC system with administrative privileges; this is an essential requirement in successfully installing the AD9959 evaluation software.
2. Uninstall any previous versions of the AD9959 evaluation software from your PC system.
3. Insert the AD9959 evaluation software CD into your CD-ROM drive. It is important not to connect the AD9959 evaluation board to the computer until the AD9959 evaluation software has been successfully installed. Refer to the **Readme.txt** file located in the **Software** folder before proceeding with the installation of the AD9959 evaluation software.
4. Run the **setup.exe** file located in the **Software** folder and follow the AD9959 evaluation software's on-screen installation instructions.

CONFIGURING THE EVALUATION BOARD

Once the software has been successfully installed onto your PC, the next step is to interface the AD9959 evaluation software to the AD9959 evaluation board via the USB Port (see Figure 2).

In order for the evaluation board and software to communicate properly, drivers must be loaded onto your PC system. The following instructions explain how to install these drivers on your PC system.

Windows 98/ME/2000 Users

1. Power up the AD9959 evaluation board (see Table 2).
2. Connect the evaluation board to the computer using a USB cable via the USB port; the VBUS LED (CR1 on AD9959 evaluation board) illuminates.
3. When the USB cable is connected, this window appears and then disappears (Figure 3).



Figure 3.

4. Then, this window (Figure 4) also appears and disappears.

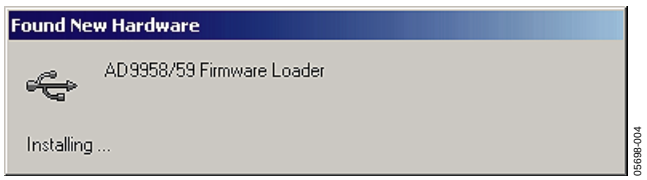


Figure 4.

5. If you are using Windows 2000, click **Finish** if you see this window (Figure 5).

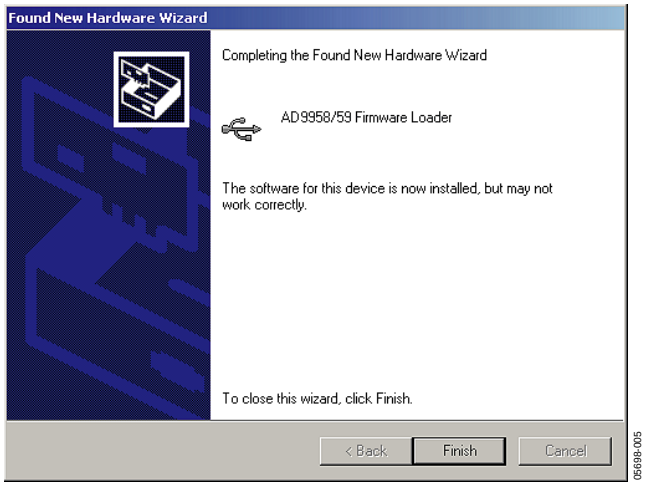


Figure 5.

6. Next, the window in Figure 6 appears.



Figure 6.

After the window has disappeared, the USB Status LED (CR2 on AD9959 evaluation board) flashes, which indicates that the evaluation board is connected properly.

Windows XP Users

1. Power up the AD9959 evaluation board (see Table 2).
2. Connect the evaluation board to the computer using a USB cable via the USB port. Then, the VBUS LED (CR1 on AD9959 evaluation board) illuminates.
3. When the USB cable is connected, the screen below appears (Figure 7). Click **Next** to continue.



Figure 7.

4. Click **Continue Anyway** when you see the window in Figure 8.

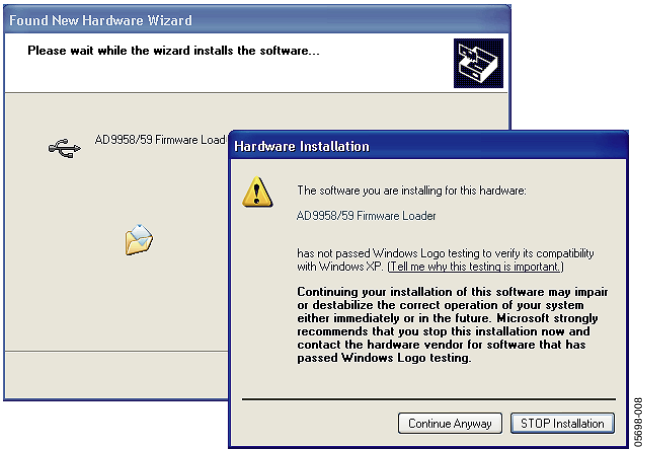


Figure 8.

5. Click **Finish** after this window (Figure 9) appears.

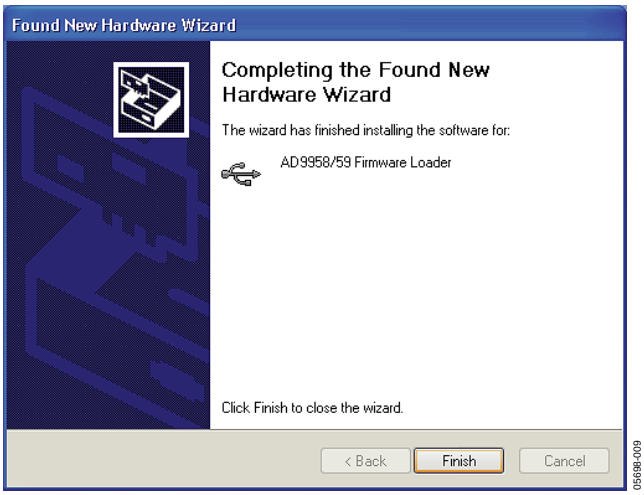


Figure 9.

6. Click **Next** after you see the window below (Figure 10).



Figure 10.

7. Click **Continue Anyway** when this window (Figure 11) appears.

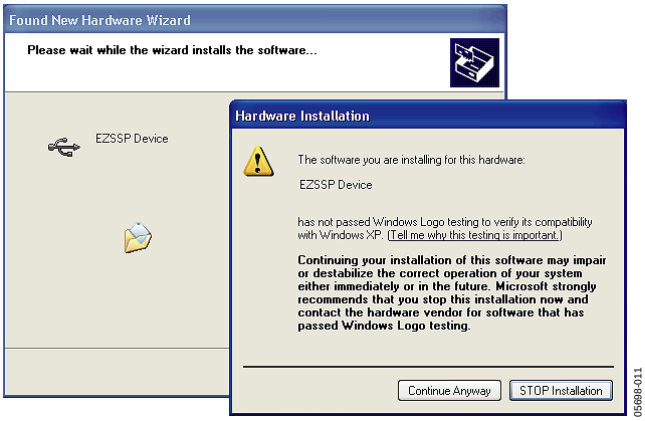


Figure 11.

8. After the window in Figure 12 appears, click **Finish** to exit.

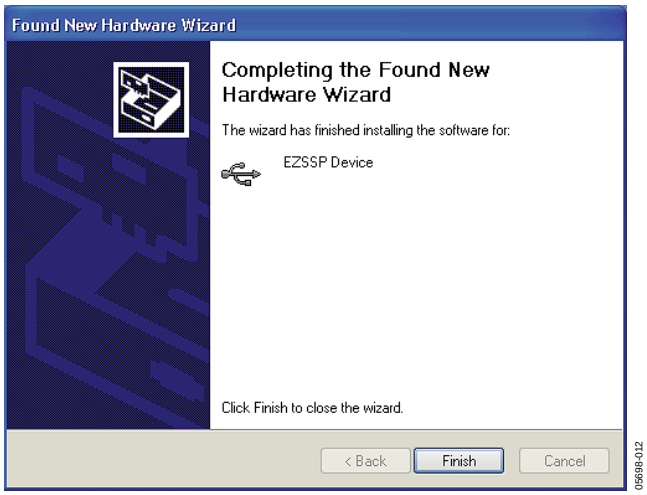


Figure 12.

Once this screen has disappeared, you should notice that the USB Status LED (CR2 on AD9959 evaluation board) is flashing, which indicates that the evaluation board is connected properly.

LOADING THE SOFTWARE

Follow these three steps to load the AD9959 evaluation software:

1. Before starting the software, make sure that the AD9959 evaluation board is powered up, connected to the computer, and that the USB Status LED is flashing.
2. Click on the **Start** button, located at the bottom left-hand corner of your desktop.
3. Select **Programs**, then the **AD9958_59 Eval Software folder**, and then **AD9958_59 Eval Software** to load the software (see Figure 13).



Figure 13.

After completing these steps, the AD9959 evaluation software loads onto your PC system. You are then presented with one of several status messages. These messages are discussed in further detail in the next section, Status Messages upon Loading Software.

Status Messages upon Loading Software

Once the AD9959 evaluation software has been loaded, a green splash screen appears as shown in Figure 14. The status box within the splash screen gives the status of the AD9959 evaluation software. A cursor is provided for easy navigation throughout this box. Green writing in the status box indicates that the software has successfully loaded.

A splash screen with red writing in the status box indicates that the software did not load successfully and that an error occurred (see Figure 15). Scrolling up through the status box with the cursor will indicate why the software did not load correctly.

Most status message errors can be resolved by checking jumper settings, making sure that the evaluation board is powered up correctly, and inspecting the USB port and cable connections.

When all power, USB port/cable connections, and jumper settings are correct, an error may still appear if the clock input is not properly configured. If this occurs, a pop-up window will appear in the center of the splash screen explaining that the software does not recognize the REF CLK input. Follow the directions given (see Figure 16).

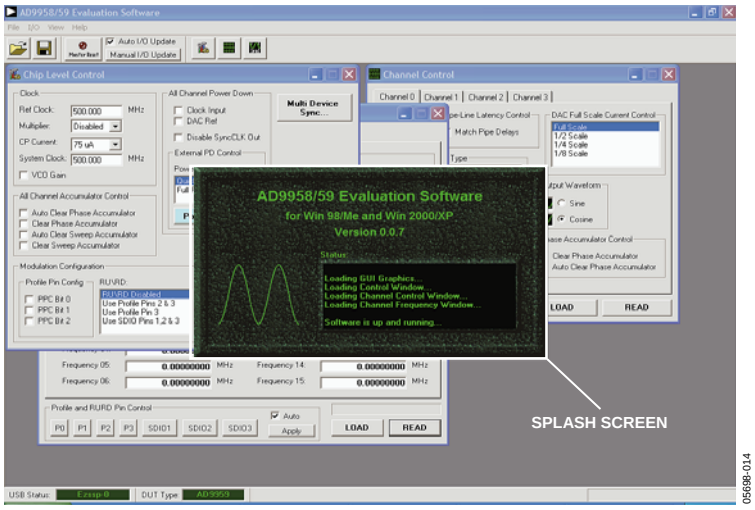


Figure 14. Successful Load

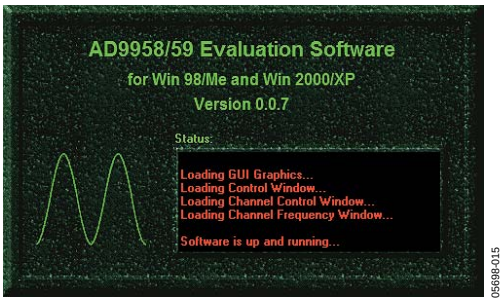


Figure 15. Error Message

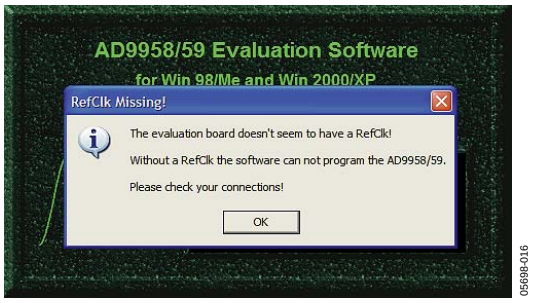


Figure 16. REF CLK Not Recognized.

FEATURE CONTROL WINDOWS

Chip Level Control

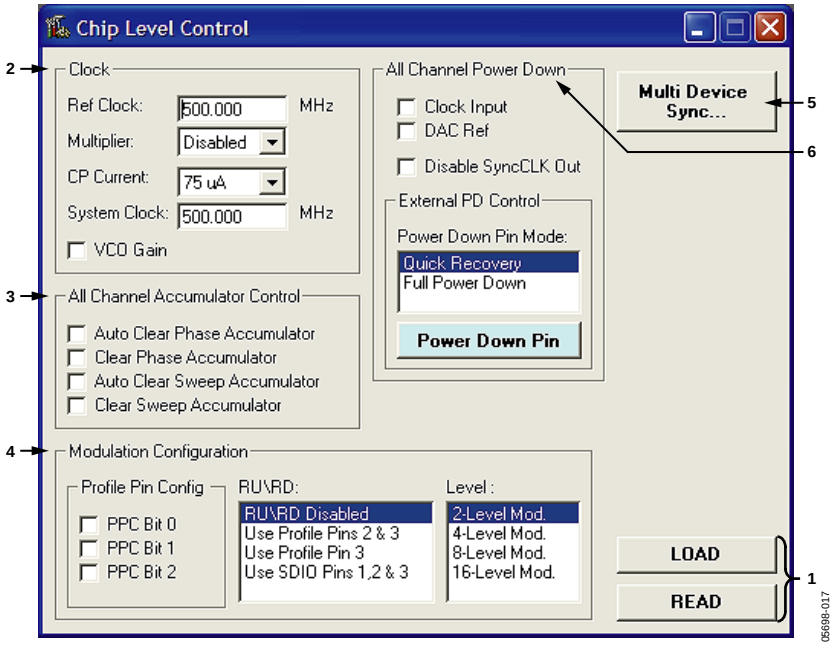


Figure 17. Chip Level Control Window

The **Chip Level Control** window provides control of the features that affect all channels of the AD9959; this window is not channel-specific. The following describes the sections of the chip level control window as they are numerically indexed in Figure 17.

1. LOAD and READ

The LOAD and READ buttons are used to send data and retrieve register settings. All LOAD and READ buttons found in the evaluation software have the same functionality.

When new data is detected, LOAD flashes orange, indicating that you need to click **LOAD** to send the updates to the serial I/O buffer where they are stored until an I/O update is issued. The I/O update sends the contents of the serial I/O buffer to active registers.

I/O updates can be sent manually (**Manual I/O Update**) or automatically (**Auto I/O Update**). By default, the AD9959 evaluation software is set to Auto I/O Update, so that when **LOAD** is clicked, an I/O update signal is automatically sent to the device. If synchronization across channels is desired, use the Manual I/O Update button. To do this, uncheck the **Auto I/O Update** box and press the **Manual I/O Update** button when you wish to send an I/O update (see Figure 18).

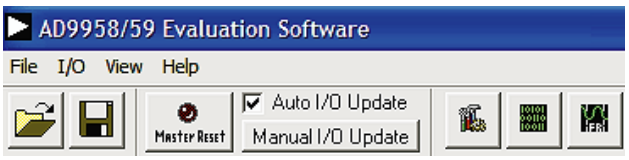


Figure 18.

Click **READ** to perform a readback of the current state of the settings and update the GUI with those settings.

2. Clock

The Clock section allows the user to configure the reference clock path in the AD9959.

Ref Clock inputs the operating frequency of the external reference clock or crystal. The maximum reference clock frequency of the AD9959 is 500 MHz, which is the default setting of this box. A red outline indicates that the value entered is out of range. (See Figure 19).

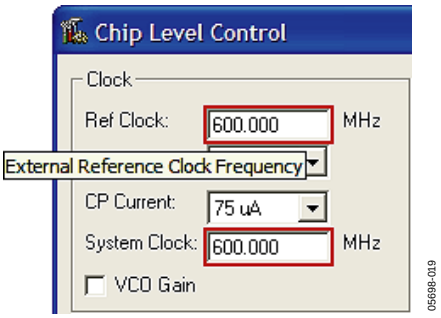


Figure 19.

Multiplier selects the PLL multiplication factor (4× to 20×) by which to scale the input frequency. The default setting of this box is **Disabled**, indicating that the Ref Clock Multiplier circuitry is bypassed and the Ref Clock/Crystal input is piped directly to the DDS core.

CP Current selects the charge pump current output of the PLL in the Ref Clock Multiplier circuitry. Selecting a higher current output will result in the loop locking faster, but there is a trade-off. Increasing this current output will also increase phase noise. The default setting of this box is 75 µA.

System Clock displays the operating frequency the DDS core (system). The value shown here is derived from the values entered in the Ref Clock and Multiplier boxes.

VCO Gain is automatically set when the Ref Clock Multiplier is being used to generate a system clock that is greater than 255 MHz. This is done to ensure stability of the Ref Clock Multiplier circuitry. A pop-up window will appear alerting you to this update (see Figure 20).

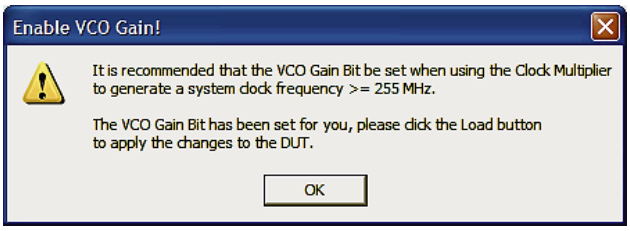


Figure 20.

Please refer to the Reference Clock Modes section of the AD9959 data sheet for more information regarding clock modes and operation.

3. All Channel Accumulator Control

The All Channel Accumulator Control provides control over the phase and sweep accumulators for all channels.

Check the **Auto Clear Phase Accumulator** or **Auto Clear Sweep Accumulator** boxes to clear and release the corresponding accumulator. The auto clear function sets the accumulator to 0 and then begins accumulating.

Select the **Clear Phase Accumulator** or **Clear Sweep Accumulator** to clear and hold the corresponding accumulator. The clear function clears and then holds the contents of the corresponding accumulator to 0 until the box is unchecked.

4. Modulation Configuration

The Modulation Configuration section configures the modulation operation of the AD9959.

Profile Pin Configuration provides access to the PPC Bits (**FR1<14:12>**). These bits are used to control the modulation scheme of the AD9959. **PPC Bit 0** is the LSB (**FR1<12>**), and **PPC Bit 2** is the MSB (**FR1<14>**).When a PPC bit is selected, it is set to Logic 1 from its default setting of 0. These bits are discussed in more detail in the Modulation Mode section of the data sheet.

RU/RD assigns which pins will control the scaling (Ramp Up/Ramp Down) of the output amplitude of the AD9959. This feature can be controlled via the profile or SDIO data pins.

Select **Use Profile Pins 2 & 3** if you would like to control the RU/RD feature with Profile Pin 2 and Profile Pin 3, or **Use Profile Pin 3** to control this feature using only Profile Pin 3. If you wish to use the SDIO data pins to control this feature, simply select **Use SDIO pins 1, 2, & 3**. Note that to use the SDIO pins to control the RU/RD feature, the **SDIO RU/RD Control** jumpers must be placed (see Figure 2). The default setting of this box is **RU/RD Disabled**. In this mode, you will not be able scale the output amplitude.

The AD9959 can be configured to perform many operations in various combinations. Please refer to the Channel Constraint Guidelines and the Modulation Mode sections of the AD9959 data sheet for more details regarding the use of the RU/RD function in combination with the different modes of operation (single-tone, modulation, linear sweep) of the AD9959. For more information regarding the theory of the RU/RD operation, note the Output Amplitude Control Mode section of the AD9959 data sheet.

Level selects the desired level of modulation of the AD9959. The AD9959 can perform 2-level, 4-level, 8-level, or 16-level modulation of frequency, phase, or amplitude (FSK, PSK, ASK). This modulation is controlled via the data pins; note the Channel Constraint Guidelines and the Modulation Mode sections of the AD9959 data sheet for more details.

5. Multi Device Sync

It is possible to synchronize multiple evaluation boards. Refer to the Synchronizing Multiple AD9959 Devices section in the AD9959 data sheet and the evaluation board schematic (located in the schematic folder of the AD9958_59 evaluation software CD) for more details on synchronizing multiple AD9959s.

6. All Channel Power Down

The All Channel Power Down section allows you to power down all channels collectively using software configurations or the external power down options found in the **External PD Control** subsection.

Select the **Clock Input**, **DAC Ref**, or **Disable SyncCLK Out** boxes to power down those circuit blocks respectively for each individual channel. Once the selection has been made, click the **LOAD** button to execute the power down.

When using the **External PD Control,** select from the **Power Down Pin Mode: Quick Recovery** (default setting) or **Full Power Down mode**. In quick recovery mode, only the digital logic is powered down whereas all functions are powered down in full power down mode. To execute the power down when using external PD control, you must click the **Power Down Pin**. When pressed, the power down pin is at Logic 1, indicating the powered down mode. When this pin is not pressed, it is at Logic 0, indicating the powered up mode.

Channel Control

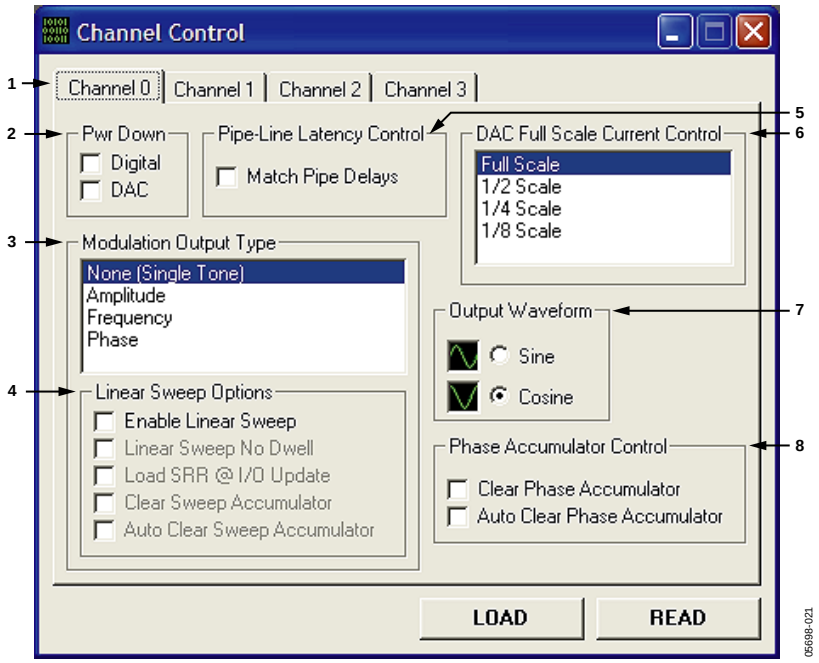


Figure 21. Channel Control Window

The **Channel Control** window provides control of the features that affect the AD9959 at a channel-specific level. The following describes the sections of the Channel Control window as they are numerically indexed in Figure 21.

1. Channel Select

Use the **Channel Select** tabs to select which specific channel options to configure. The AD9959 has four independent channels: Channel <0:3>. The default channel select tab setting is Channel 0.

2. Pwr Down

Use the **Pwr Down** section to power down the digital logic (check **Digital** box) or the DAC circuitry (check **DAC** box). Upon default, both of these boxes are unchecked, indicating that the digital logic and the DAC circuitry of that channel are enabled (powered up).

3. Modulation Output Type

The **Modulation Output Type** box controls what type of modulation is performed on the channel's output. Select **Phase**, **Frequency**, **Amplitude**, or **None (Single Tone)** depending upon which type of modulation you want. The level of modulation for the channel is set using the **Chip Level Control** window under the **Modulation Configuration** section in the **Level** box.

4. Linear Sweep Options

Use the **Linear Sweep Options** section to control the linear sweep features. Select **Enable Linear Sweep** to turn on the linear sweep function and the additional associated options (see Figure 22).

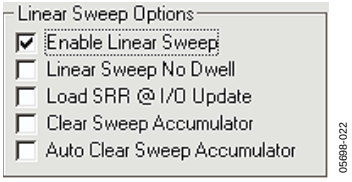


Figure 22.

Select **Linear Sweep No Dwell** to enable this feature, see the Linear Sweep No Dwell Mode section of the AD9959 data sheet for more information regarding the no dwell feature.

When you select **Load SRR @ I/O Update**, the contents of the sweep ramp rate register are loaded into the sweep ramp rate timer every time an I/O_UPDATE is sent to the device.

The **Clear Sweep Accumulator** and **Auto Clear Sweep Accumulator** have the same basic functionality as described in the All Channel Accumulator Control section of the Chip Level Control window. The difference is that here the function is channel-specific.

See the Linear Sweep (Shaped) Modulation Mode section of the AD9959 data sheet for a detailed explanation of this mode.

5. Pipe-Line Latency Control

When you check the **Match Pipe Delays** box in the **Pipe Latency Control** section, the pipeline delay for updates to frequency, amplitude, and phase will be equal, but only for the channels operating in single tone mode. The default setting of this box is unchecked, meaning the pipeline delay for updates to frequency, amplitude, and phase will not be equal.

See the DATA LATENCY (PIPELINE DELAY) section in the Specifications table of the AD9959 data sheet for the exact timing delays with and without this feature enabled. Also, refer to the Single Tone Mode-Matched Pipeline Delay section of the AD9959 data sheet.

6. DAC Full Scale Current Control

Use the **DAC Full Scale Current Control** section to scale the output current of the DAC. Select either **Full Scale** (default setting), **½ Scale**, **¼ Scale**, or **⅛ Scale** for the DAC output current. See the Scalable DAC Reference Current Control Mode section of the AD9959 data sheet.

7. Output Waveform

In the **Output Waveform** box, select either a **Cosine**(x) or a **Sine**(x) function for the angle-to-amplitude conversion. The default setting is Cosine(x).

8. Phase Accumulator Control

The **Clear Phase Accumulator** and **Auto Clear Phase Accumulator** have the same basic functionality as described in the All Channel Accumulator Control section of the Chip Level Control window. The difference is that here the function is channel-specific.

Channel Output Config

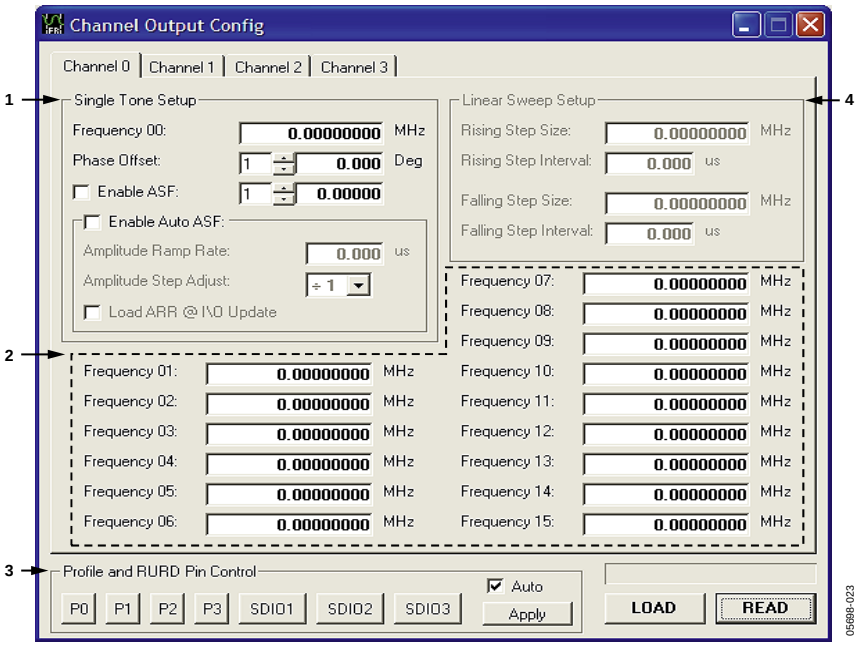


Figure 23. Channel Output Config Window

The **Channel Output Config** window configures various output characteristics of the channel(s). Use the **Channel Select** tabs to select which specific channel options to configure. The following describes the sections that are numerically indexed in Figure 23.

1. Single Tone Setup

Use the **Single Tone Setup** section to configure the channel output for the single tone mode of operation (default).

Enter the desired output frequency directly in the **Frequency 00** box or double-click the **Frequency 00** box to launch the **Edit Output Frequency** pop-up box to set the output frequency in the **Frequency** box. The output frequency can alternatively be set in decimal, hex, or binary format by editing the respective boxes in the **Tuning Word Values** section (see Figure 24).

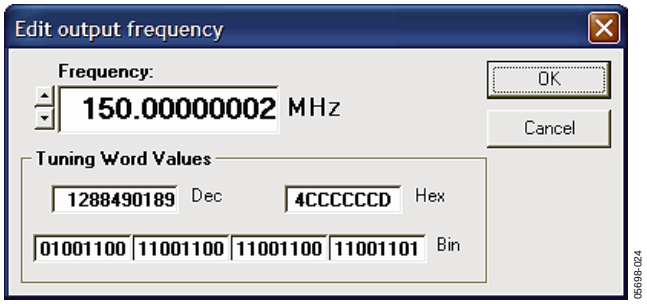


Figure 24.

Note that the **Phase Offset**, **Enable ASF**, **Amplitude Ramp Rate**, **Profile Registers**, **Rising Step Size**, **Rising Step Interval**, **Falling Step Size**, and **Falling Step Interval** boxes all offer the edit option shown in Figure 24 by double-clicking their respective boxes.

The Frequency 00 box also sets the starting point of the linear frequency sweep and the first level in frequency modulation (FSK).

Phase Offset consists of two boxes. In the first box, set the integer factor (1–999) to increment or decrement the phase offset by. The default setting of this box is 1, indicating that the phase offset is incremented/decremented by .022 degrees when pressing the up or down arrow keys. The value of .022 degrees is derived from this equation:

$$IntegerFactor \times \left(\frac{1}{2^{(14\ bits\ of\ phase\ resolution)-1}} \right) \times 360^\circ$$

Therefore, entering a factor of 3 in the first box will allow you to increment/decrement the phase offset by .066 degrees. In the second box, input the desired phase offset (from 0 degrees to 360 degrees) of the output signal.

The Phase Offset box also represents the starting point of the linear phase sweep and the first level in phase modulation (PSK).

In order to use the output amplitude scalar, the **Enable ASF** box must be checked. In the first box, set the integer factor (1–999) to increment or decrement the amplitude scale factor. The default setting of this box is 1, meaning the output amplitude will be scaled up/down by .00098 when pressing the up or down arrow keys. The value of .00098 is derived from this equation:

$$IntegerFactor \times \left(\frac{1}{2^{(10\ bits\ of\ output\ amplitude\ scalar\ resolution)-1}} \right)$$

In the second box, set the desired output amplitude scale factor (between 0 and 1) of the output signal, where 1 is equivalent to full scale.

The Enable ASF box also represents the starting point of the linear amplitude sweep and the first level in amplitude modulation (ASK). Note that when performing linear amplitude sweeps, the Enable ASF box must be left unchecked.

When using the RU/RD feature, the Enable Auto ASF box must be checked. Once the Enable Auto ASF box has been checked, the **Amplitude Ramp Rate**, **Amplitude Step Adjust**, and the **Load ARR @ I/O Update** options are available (see Figure 25).

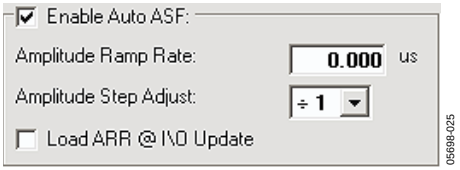


Figure 25.

Use the **Amplitude Ramp Rate** box to set the Amplitude Ramp Rate (ARR) time. This time (entered in µs) can range from a minimum value of:

$$\left(\frac{1}{SYNC\ CLK}\right)\times 1$$

to a maximum value of:

$$\left(\left(\frac{1}{SYNC\ CLK}\right)\times 2^{(8\ bits\ of\ output\ ramp\ rate\ resolution)-1}\right)$$

This implies that if the system clock is 500 MHz, the ARR value can range from 8 ns (minimum) to 2.040 µs (maximum). If the value entered exceeds the maximum time, then a pop-up window (Figure 26) alerts the user that the value entered will be changed to the appropriate maximum value.



Figure 26.

In the **Amplitude Step Adjust** box, select the amplitude scale factor step size. The default setting of this box is 1, indicating that step size will be 1 LSB. A selection of 8 means the step size will be 8 LSB.

Select **Load ARR @ I/O Update** to load the contents of the amplitude ramp rate register into the amplitude ramp rate timer every time an I/O_UPDATE is sent to the device.

2. Profile Registers

The AD9959 features up to 16 programmable registers per channel as shown in Figure 23. Due to certain channel constraints, however, there are limitations on how the Profile Registers can be used in some configurations as described in the Channel Constraint Guidelines section of the AD9959 data sheet.

Use the **Profile Registers** to enter the information needed for modulation (FSK, PSK, or ASK) and linear sweep modes of operation. Upon default, the Profile Registers are configured for frequency inputs, but these registers can be changed to intake phase or amplitude information by selecting the desired modulation type in the Modulation Output Type box in the Channel Control window. Figure 27 shows how the Profile Registers appear when phase modulation (PSK) is selected.

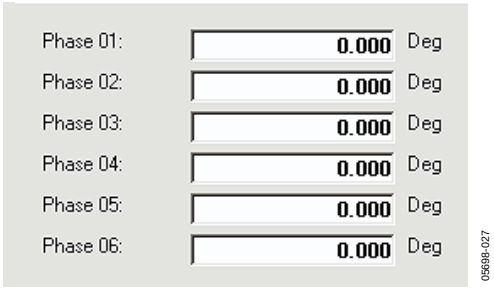


Figure 27.

When the channel is in the modulation or linear sweep mode of operation, input the starting frequency in the **Frequency 00** box, starting phase in the **Phase Offset** box, and the starting amplitude in the **Enable ASF** box. In modulation mode, use the **Profile Registers** to input frequency, phase, or amplitude information for the level of modulation selected. For instance, if 4-level frequency modulation is selected, input the starting frequency in the **Frequency 00** box, second frequency in the **Frequency 01** box, third frequency in the **Frequency 02** box, and fourth frequency in the **Frequency 03** box. An example of using the **Profile Registers** for 2-level frequency modulation is shown in Figure 28. In this configuration, the frequency starts at 10 MHz and ramps up to 50 MHz.

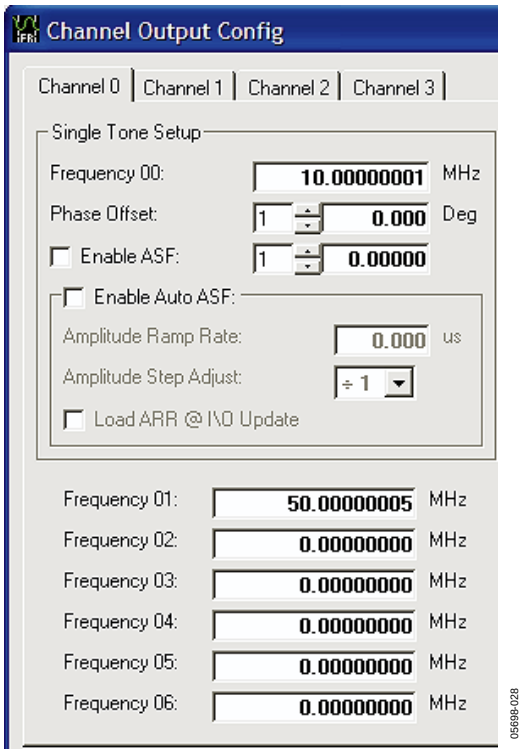


Figure 28.

In the linear sweep mode of operation, only the first **Profile Register** box (**Frequency 01**, **Phase 01**, or **Amplitude 01**) is used. It indicates the ending point of the sweep. In Figure 28, the frequency linear sweep begins at 10 MHz and ends at 50 MHz.

3. Profile and RURD Pin Control

The **Profile and RURD Pin Control** section covers the profile pins (**P0, P1, P2**, and **P3**) and SDIO data pins (**SDIO1, SDIO2,** and **SDIO3**). The profile pins can be configured to control modulation, linear sweep, or RU/RD operations, whereas the SDIO data pins can only control the RU/RD operation. To perform the desired modulation, linear sweep, or RU/RD operation, toggle the profile/SDIO data pin(s) associated with that operation. When these pins are pressed, they are set to Logic 1 (see Figure 29).

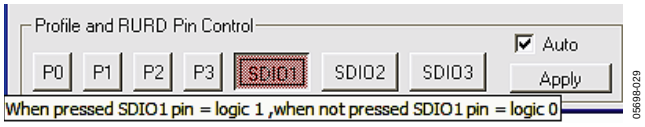


Figure 29.

Upon default, the **Auto** box is checked, meaning that once you click one of the pins (profile or SDIO), the action executes. If this box is unchecked, the Apply button must be clicked before the desired action is carried out. The Apply button mimics the LOAD button; it will flash orange when new data is detected, but all changes and updates occur simultaneously when Apply is clicked.

If we were performing 2-level frequency modulation-no RU/RD, and had the same configurations as shown in Figure 28, **P0** would be used to control the modulation on CH0 (see the AD9959 data sheet for more information). Therefore, the output of CH0 will stay at 10 MHz until the P0 button is clicked. Once the P0 button is selected, the frequency will change to 50 MHz. To return to 10 MHz, simply release (unclick) P0.

For more information regarding the use of the profile and SDIO data pins to control various modulation, linear sweep, and RU/RD schemes, refer to the Modes of Operation section of the AD9959 data sheet.

4. Linear Sweep Setup

Use the **Linear Sweep Setup** section to setup the slope of the linear sweep. In the **Rising Step Size** box, enter the desired value for the rising step size. Input the amount of time you wish to be spent at each step in the **Rising Step Interval** box.

Input the desired falling step size in the **Falling Step Size** box, and the time that should be spent at each step in the **Falling Step Interval** box. The Rising/Falling Step Size boxes are similar to the Profile Registers; upon default, they are set up for frequency inputs, but these boxes can be changed to intake phase or amplitude information by selecting the type of linear sweep desired in the Modulation Output Type box in the Channel Control window.

The number of steps in a ramp can be calculated by determining the difference between the starting and ending points of the sweep and dividing by the step size. The time required to sweep is then the number of steps times the amount of time spent at each step.

The range of the Rising/Falling Step Interval is computed similarly to the time range for the Amplitude Ramp Rate. Note that the Rising Step Interval and Falling Step Interval boxes also have the pop-up window feature exhibited in Figure 25 when the maximum rising/falling step interval value is exceeded.

For more information regarding the Linear Sweep Setup, refer to the Setting the Slope of the Linear Sweep section of the AD9959 data sheet.

Debug

The **Debug Window**, shown in Figure 30, lets you write directly to any of the AD9959's internal registers and subsequently read them back. Use **View Channel** to select which channel's internal registers you would like to view. The default setting of this box is Channel 0. To access the internal registers of the selected channel, use the **RegAddr** drop menu to select which register(s) you would like to read/write. You can also directly toggle the states of any external input pins such as the profile or SDIO data pins.

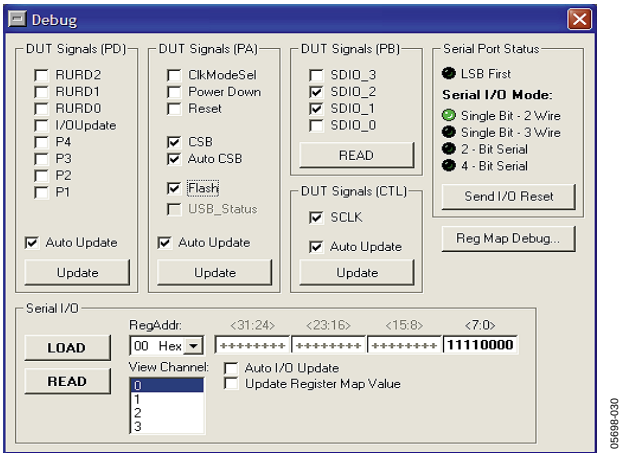


Figure 30.

To access the **Debug Window**, click **View** and select **Debug Window** (see Figure 31).

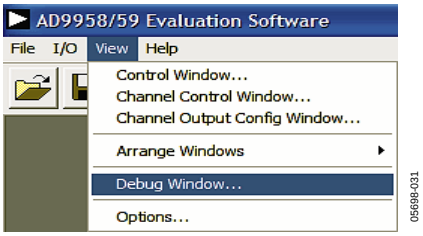


Figure 31.

DUT I/O Box

This dialog box (Figure 32) controls the I/O configuration for the device. Click **I/O Reset** to send an I/O reset to the corresponding serial port state machine. Select **LSB First** to change the data format to LSB first from the default setting of MSB first. Use the **Serial I/O Mode** drop menu to select the desired serial I/O mode of operation: **Single Bit-2 Wire** (default), S**ingle Bit-3 Wire**, **2-Bit Serial**, or **4-Bit Serial**. For more information, please refer to the Serial I/O Modes of Operation section of the AD9959 data sheet.

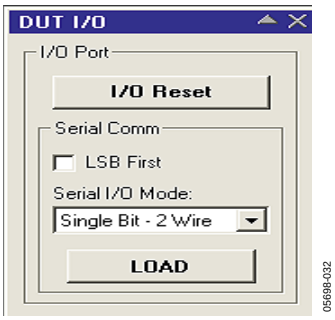


Figure 32.

To access the **DUT I/O** box, click I/O button (left of View–see Figure 31) and select **DUT I/O**.

SETUP FILES

Introduction

The AD9959 can be configured to perform many operations in various combinations. Preconfigured setup files have been included with the AD9959 evaluation software that show the device in all three modes of operation: single tone, modulation, and linear sweep. These example setup files serve as a reference and/or starting point when trying to configure the device for a desired setup for the first time.

To load these setup files click **File**, and select **Load Setup…** (Figure 33), or click the **open folder** (Figure 34) to access these files.

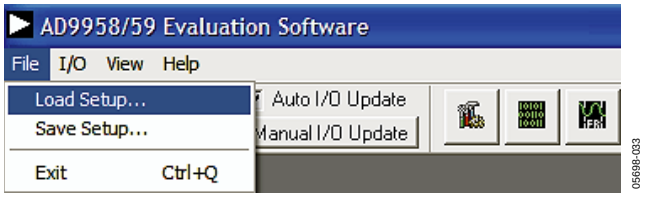


Figure 33.

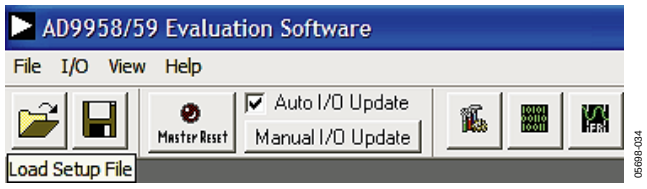


Figure 34.

Next, open the **AD9959 Configuration Files** folder (Figure 35).

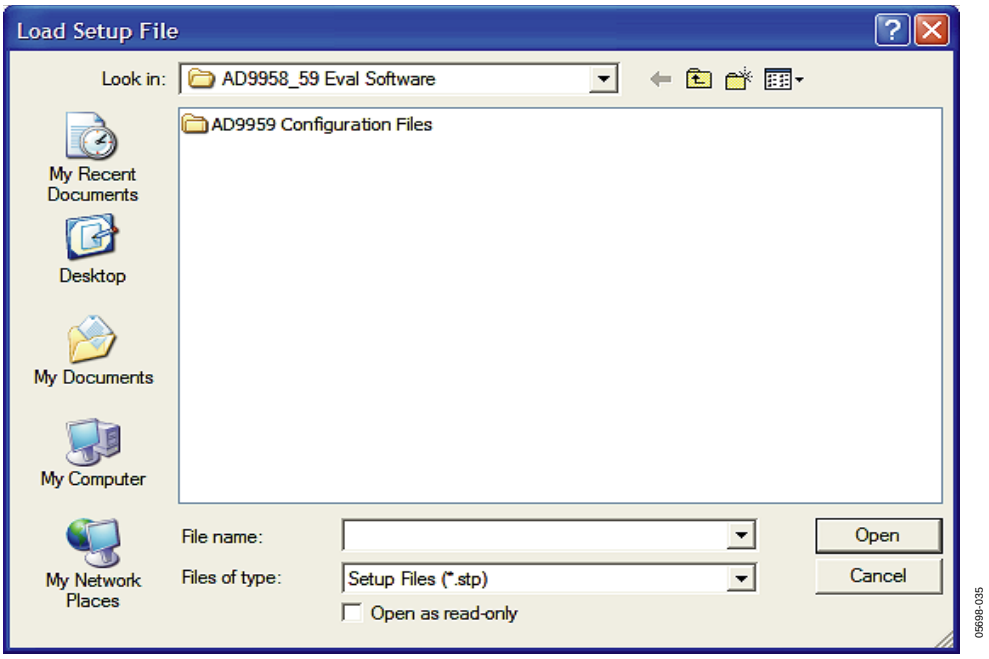


Figure 35.

Then select which mode of operation setup file(s) you would like to view (see Figure 36).
Select **Linear Sweep Mode**, **Modulation Mode**, or **Single Tone Mode.**

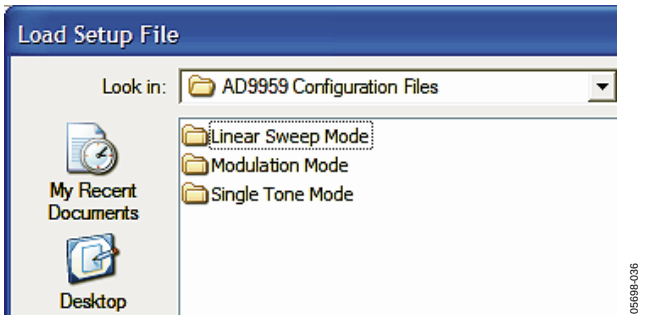


Figure 36.

Single Tone Mode

Open the **Single Tone Mode** folder to access the single tone mode of operation example setup files. This section discusses the **All Channels on @ 10_20_30_40MHz_RURD enabled.stp** file.

The **Chip Level Control** window (Figure 37) from this particular setup shows that a 500 MHz System Clock is running, with the RU/RD operation enabled. In the **RU/RD** box, **Use Profile Pins 2 & 3** has been selected to control the RU/RD feature.

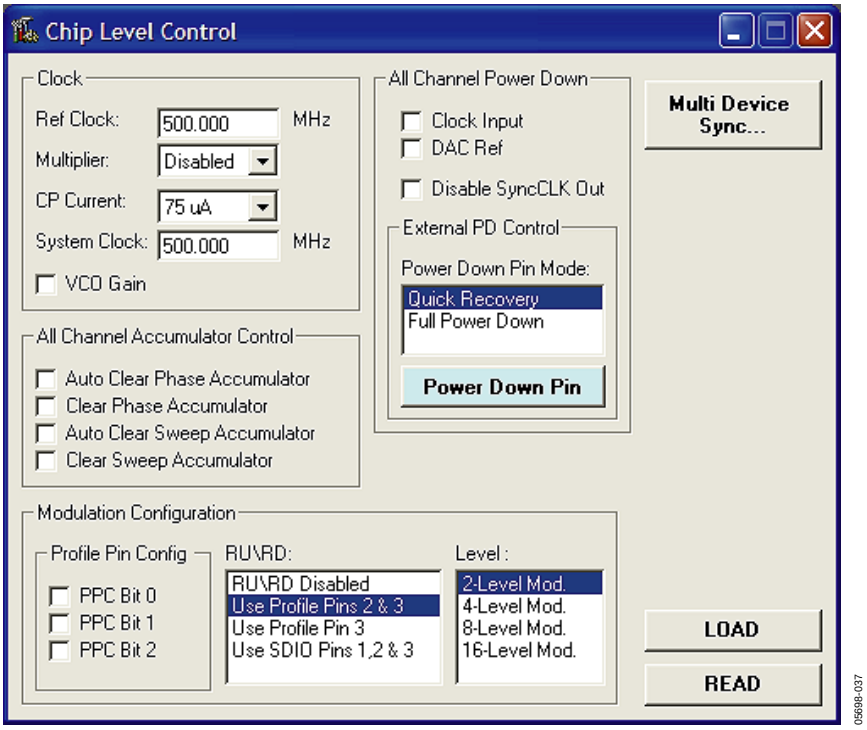


Figure 37.

In the **Channel Control** window (Figure 38), each channel has **None (Single Tone)** selected for their modulation output as shown in the **Modulation Output Type** box.

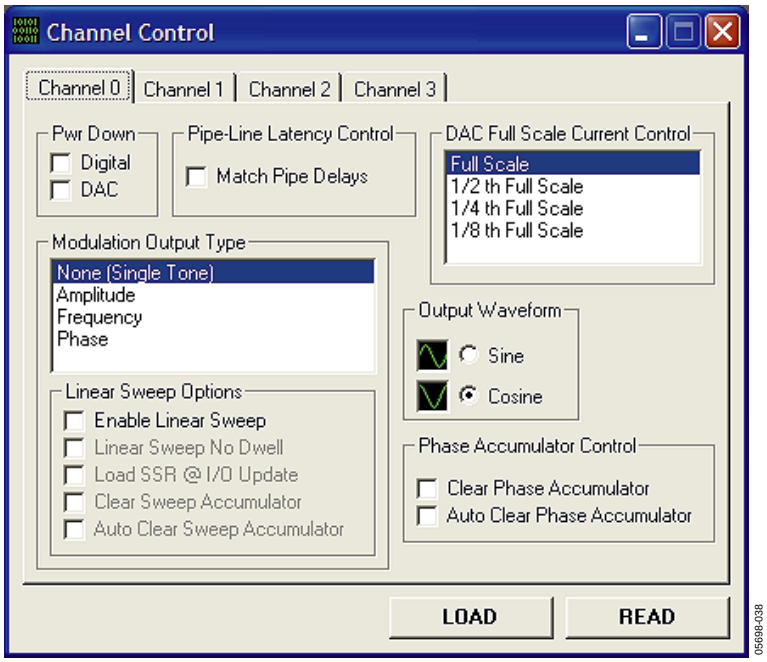


Figure 38.

In the **Channel Output Config** window (Figure 39), Channel 0 has a frequency output of 10 MHz (**Frequency 00** box), Channel 1 an output frequency of 20 MHz, Channel 2 an output frequency of 30 MHz, and Channel 3 has a frequency output of 40 MHz. Because the RU/RD operation is enabled, the **Enable ASF** and **Enable Auto ASF** boxes are checked. The amplitude scalar factor (**ASF**) is set to 1 (full scale). Therefore, the output signal will be 0 MHz until the correct profile pin is selected to ramp the frequency up to full scale. When this setup file is loaded, profile pins **P0**, **P1**, **P2**, and **P3** are pressed as shown in the **Profile and RURD Pin Control Section**. **P0** controls Channel 0, **P1** controls Channel 1, **P2** controls Channel 2, and **P3** controls Channel 3. If a profile pin is deselected, the associated channel's output will return to 0 MHz. To return to full scale, re-press the profile pin that triggers the RU/RD operation.

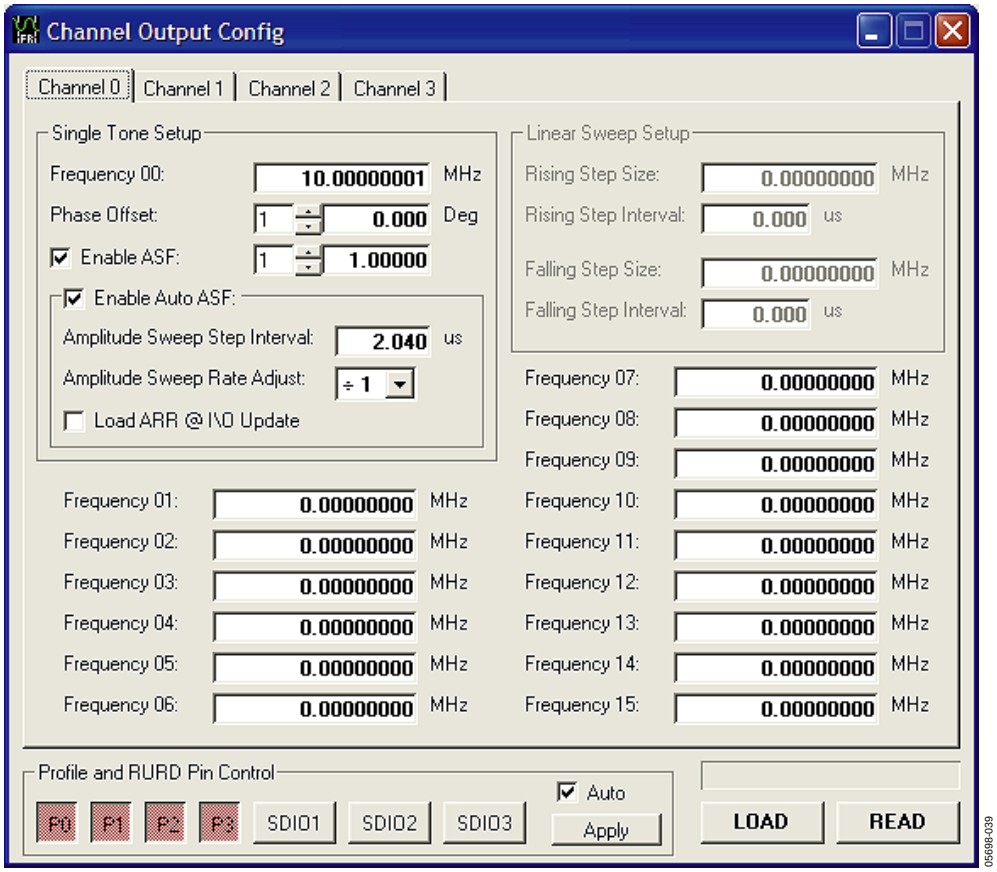


Figure 39.

Modulation Mode

Open the **Modulation Mode** folder to access the modulation mode of operation example setup files. Once this folder is opened you will be presented with the window shown in Figure 40.

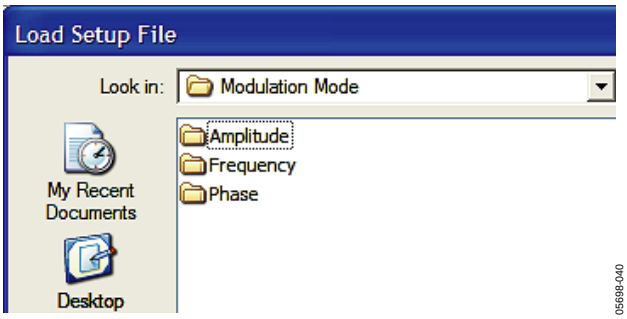


Figure 40.

For frequency modulation (FSK), open the **Frequency** folder; for phase modulation (PSK), open the **Phase** folder; and for amplitude modulation (ASK), open the **Amplitude** folder. In these folders, all setup files are indexed by their level (2, 4, 8, or 16-level). This section discusses the **CH2_@3 MHz increments.stp** file found in the **Frequency** folder under the **16-level** folder.

The **Chip Level Control** window (Figure 41) from this particular setup shows that a 500 MHz **System Clock** is running, and that a 16-level modulation-no RU/RD is being performed. Notice the **Level** box located in the **Modulation Configuration** section. The PPC Bit pattern in the **Profile Pin Config** subsection of the **Modulation Configuration** is <010>. Referring to the table in the **16-Level Modulation-No RU/RD** section of the AD9959 data sheet, we see that this bit pattern sets up 16-level modulation on Channel 2.

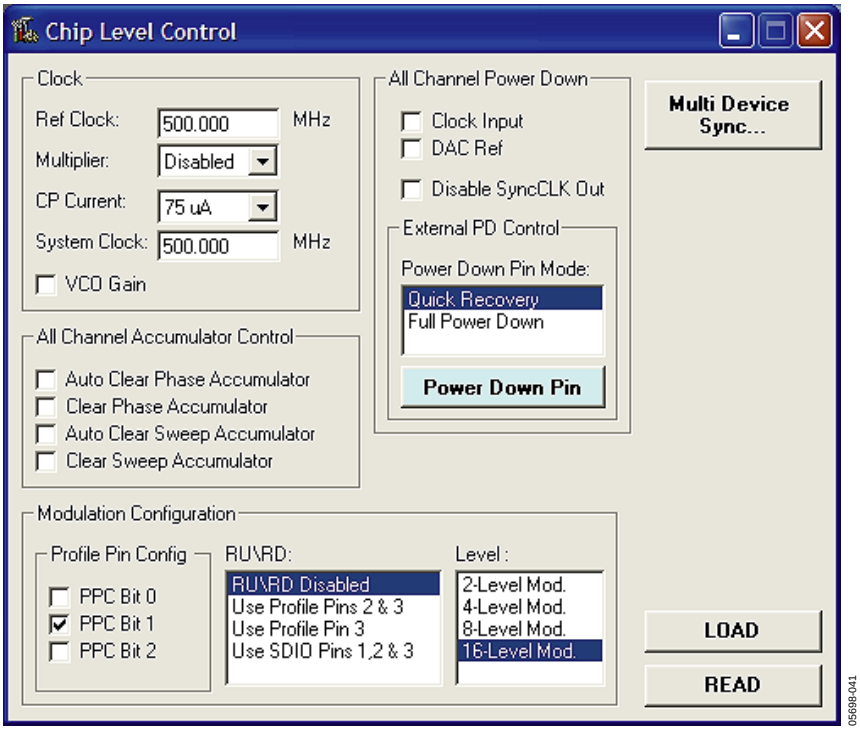


Figure 41.

In the **Channel Control** window (Figure 42), Channel 2 has **Frequency** selected as its modulation output as shown in the **Modulation Output Type** box. As discussed in the Channel Constraint Guidelines section of the AD9959 data sheet, when performing 16-level modulation on a selected channel, all other channels are available only for the single tone mode of operation.

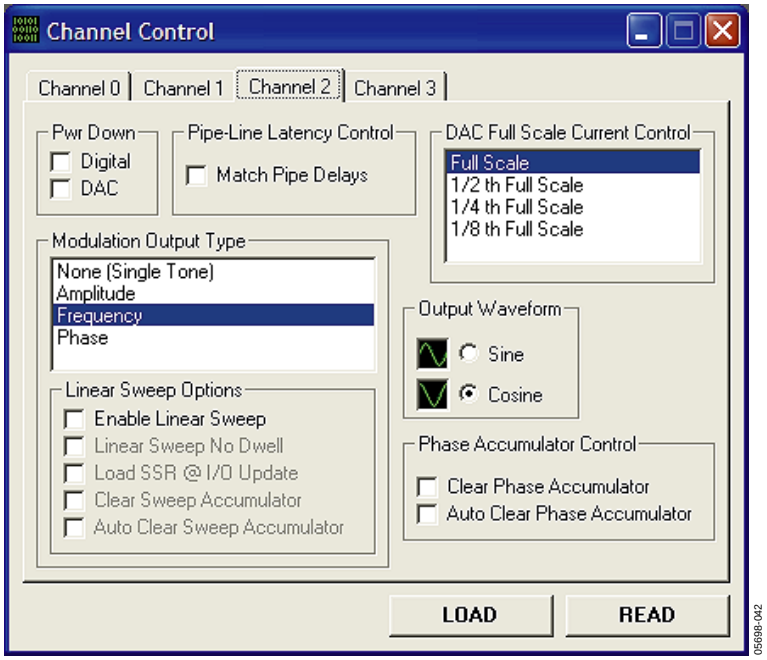


Figure 42.

In the Channel Output Config window (Figure 43), Channel 2 has a frequency output of 3 MHz (**Frequency 00** box). When this setup file is loaded, profile pins **P1** and **P3** are pressed as shown in the **Profile and RURD Pin Control Section**. In 16-level modulation, **P3** is the LSB and **P0** is the MSB. This explains why when this setup file is loaded, an output of 18 MHz is shown because 0101 binary = 5, and **Profile Register 05** contains 18 MHz as its output. If no profile pins are selected, then the output frequency is equivalent to the value entered in the Frequency 00 box (3 MHz in this setup). If all profile pins are pressed, the output frequency is equal to 48 MHz, the contents of **Profile Register 15** (1111 binary).

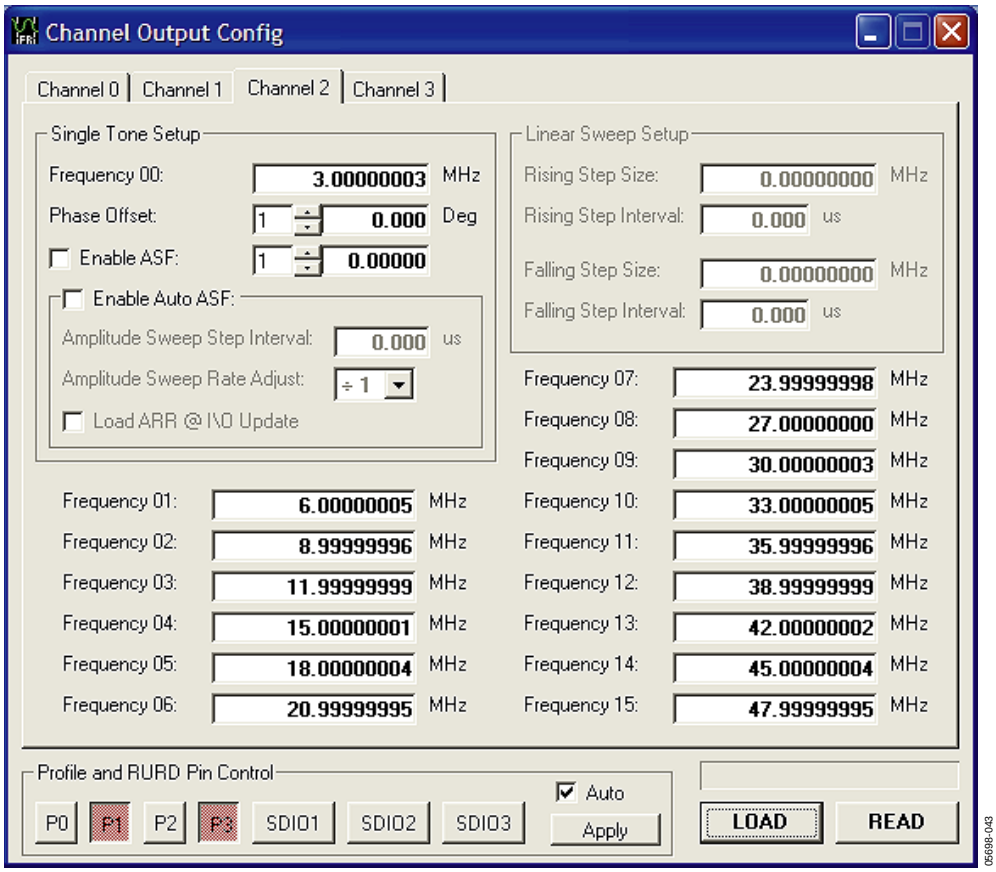


Figure 43.

Linear Sweep Mode

Open the **Linear Sweep Mode** folder to access the linear sweep mode of operation example setup files. Once this folder is opened you will be presented with the window shown in Figure 44.

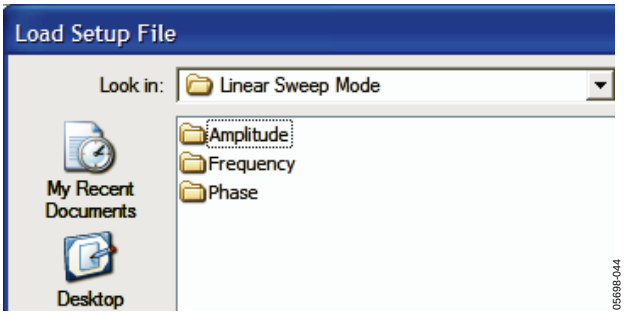


Figure 44.

For a frequency sweep, open the **Frequency** folder; for a phase sweep, open the **Phase** folder; and for an amplitude sweep, open the **Amplitude** folder. This section discusses the **All Channels@10 MHz_half to full scale.stp** file found in the **Amplitude** folder.

The **Chip Level Control** window (Figure 45) from this particular setup shows that a 500 MHz **System Clock** is running with RU/RD disabled. The **Auto Clear Phase Accumulator** and **Auto Clear Sweep Accumulator** boxes have been checked in the **All Channel Accumulator Control** section to ensure synchronization across channels and reinitialize the starting point once the linear sweep ends.

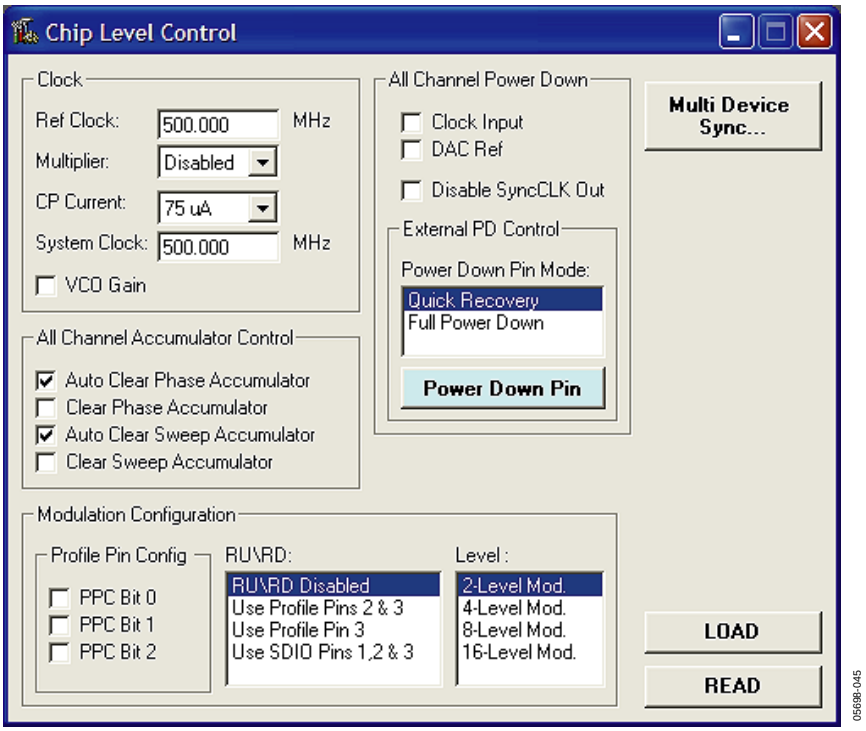


Figure 45.

In the **Channel Control** window (Figure 46), each channel has **Amplitude** selected for its modulation output as shown in the **Modulation Output Type** box. As discussed earlier in the Linear Sweep Options section, the **Enable Linear Sweep** box found in **Linear Sweep Options** section must be checked in order to configure the part for the linear sweep mode of operation.

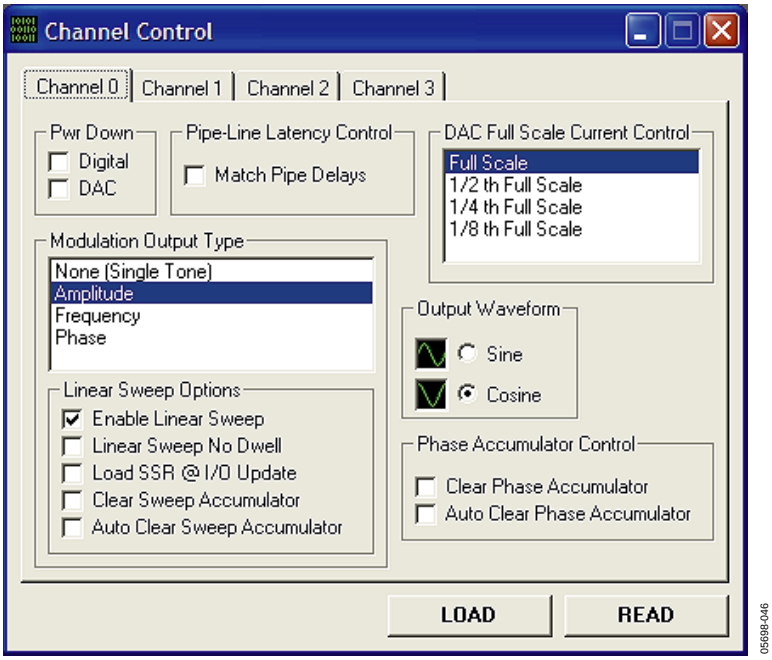


Figure 46.

In the **Channel Output Config** window (Figure 47), all channels (Channel 0 to Channel 3) have an output frequency of 10 MHz (**Frequency 00** box). The **Enable ASF** box is unchecked because a linear amplitude sweep is being performed. The amplitude scalar factor (**ASF**) is set to 0.5 (half scale), denoting that the sweep begins at half scale and sweeps up to full scale (**Amplitude 01**-ending point of sweep). In the **Linear Sweep Setup** section, the rising/falling step size and step intervals of the sweep are equal, indicating the sweep will rise and fall at the same rate. **P0** controls Channel 0, **P1** controls Channel 1, **P2** controls Channel 2, and **P3** controls Channel 3. To sweep up to full scale, press the profile pin associated with the channel's output. To return to half scale, unselect the profile pin.

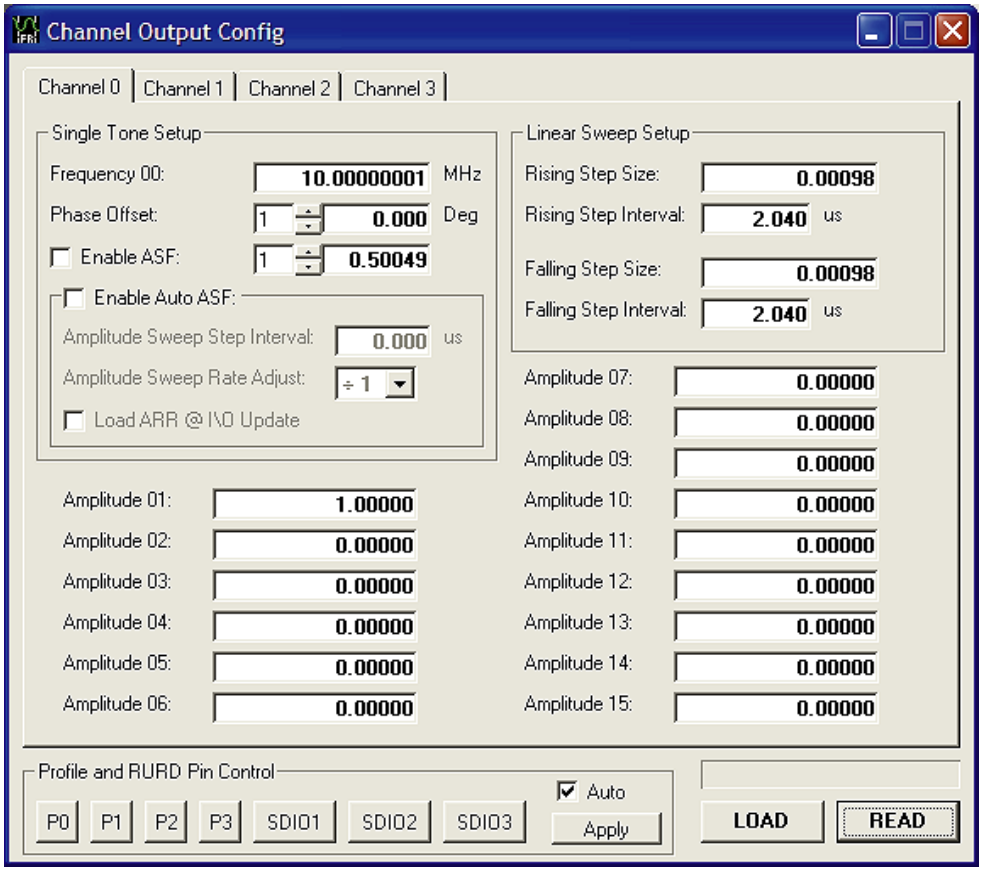


Figure 47.

SCHEMATIC

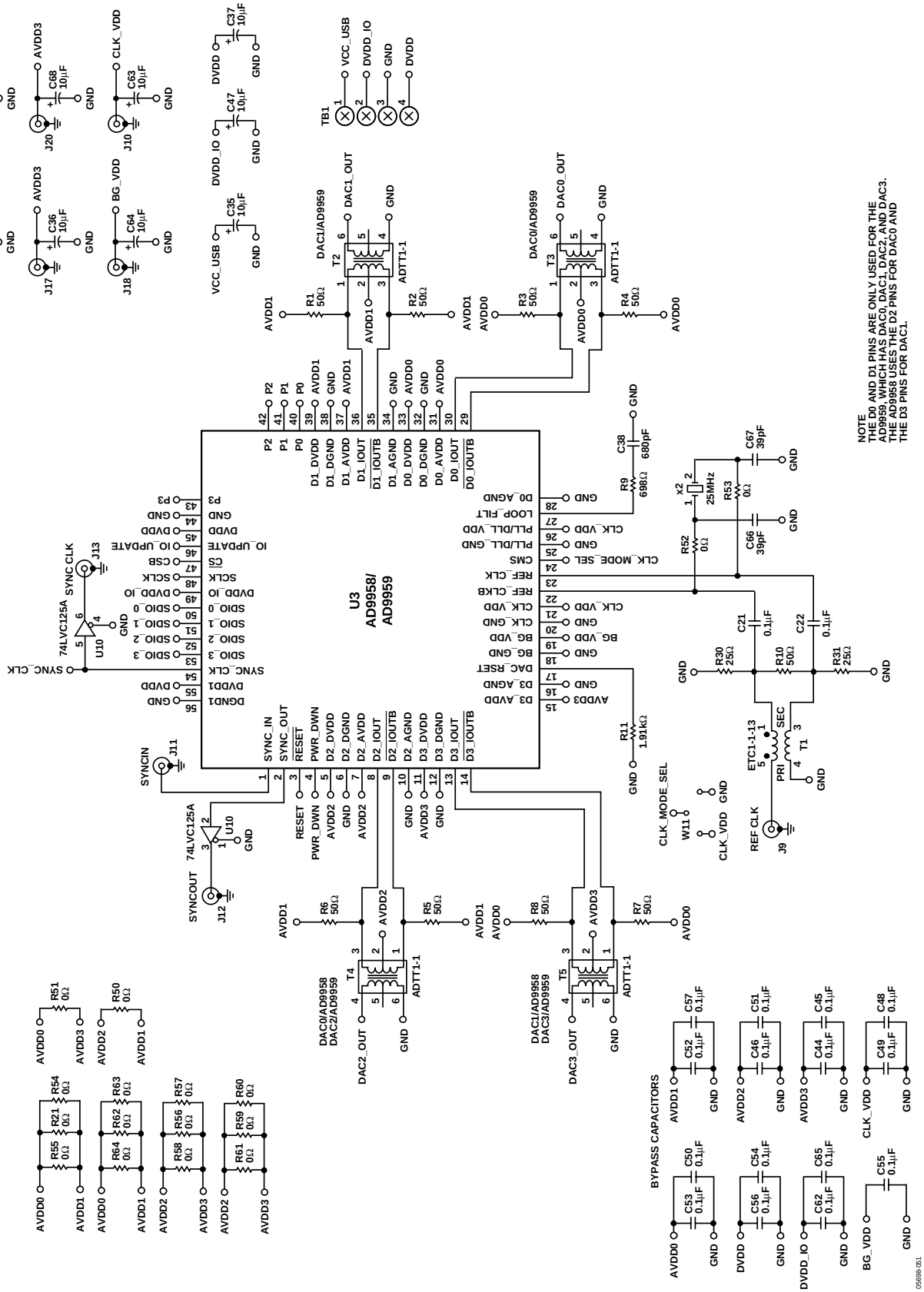


Figure 48. AD9959/PCB Schematic, Page 1

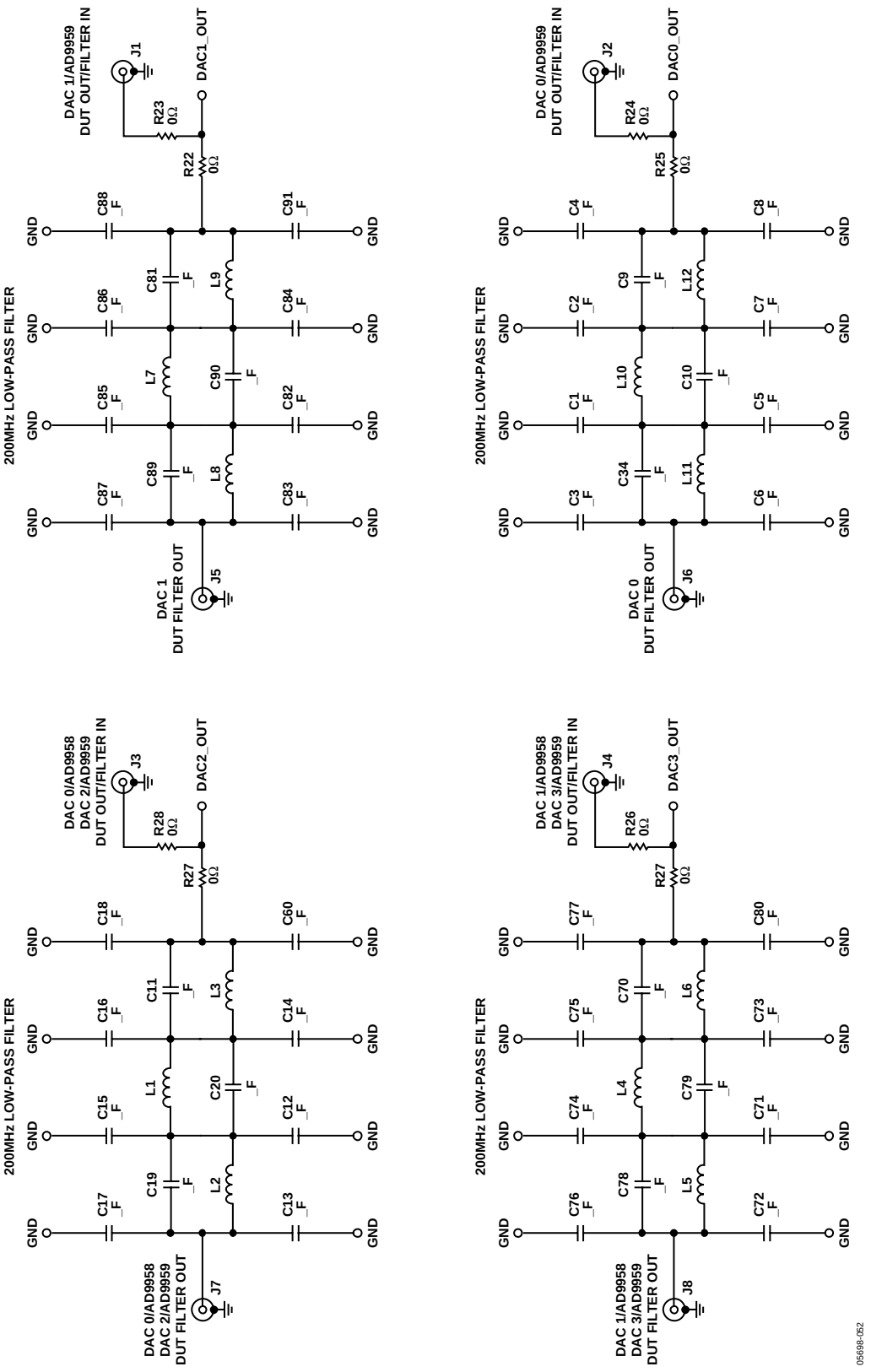


Figure 49. AD9959/PCB Schematic, Page 2

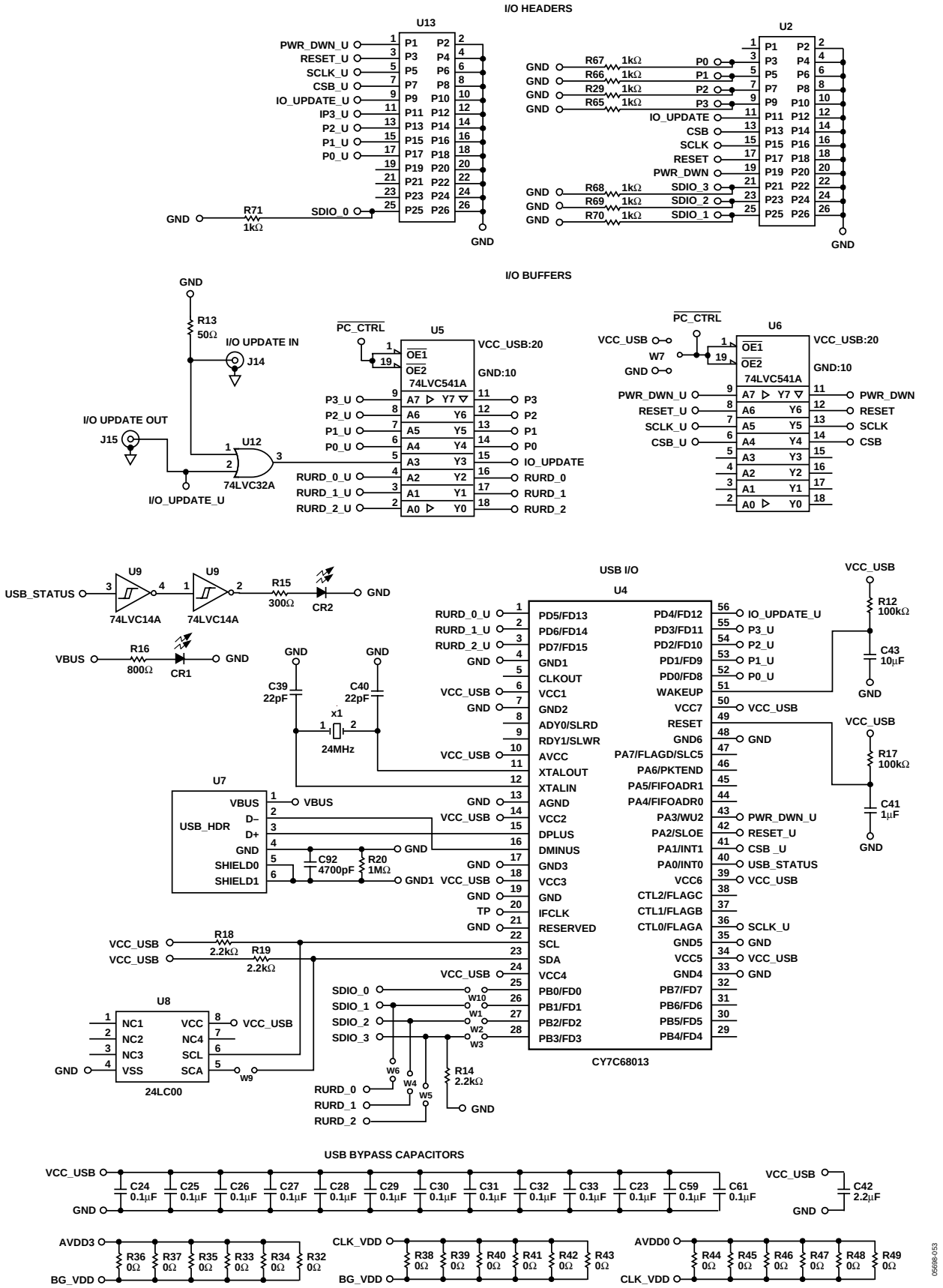


Figure 50. AD9959/PCB Schematic, Page 3

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
AD9959/PCB	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



NOTES

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EB05698-0-10/05(0)

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