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# Triaxial Inertial Sensor with Magnetometer

# ADIS16400/ADIS16405

## FEATURES

- Triaxial, digital gyroscope with digital range scaling
  - ±75°/sec, ±150°/sec, ±300°/sec settings
  - Tight orthogonal alignment, <0.05°
- Triaxial, digital accelerometer, ±18 *g*
- Triaxial, digital magnetometer, ±2.5 gauss
- Autonomous operation and data collection
  - No external configuration commands required
  - 220 ms start-up time
  - 4 ms sleep mode recovery time
- Factory-calibrated sensitivity, bias, and axial alignment
  - ADIS16400 calibration temperature: +25°C
  - ADIS16405 calibration temperature range: −40°C to +85°C
- SPI-compatible serial interface
- Embedded temperature sensor
- Programmable operation and control
  - Automatic and manual bias correction controls
  - Bartlett-window FIR length, number of taps
  - Digital I/O: data-ready, alarm indicator, general-purpose
  - Alarms for condition monitoring
  - Sleep mode for power management
  - DAC output voltage
  - Enable external sample clock input up to 1.2 kHz
  - Single-command self-test
- Single-supply operation: 4.75 V to 5.25 V
- 2000 *g* shock survivability
- Operating temperature range: −40°C to +105°C

## APPLICATIONS

- Unmanned aerial vehicles
- Platform control
- Digital compassing
- Navigation

## FUNCTIONAL BLOCK DIAGRAM

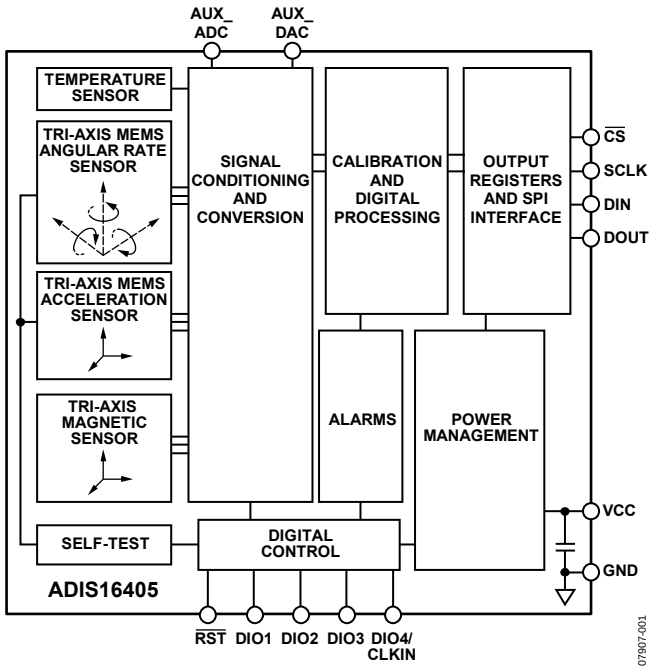



*Figure 1.*

## GENERAL DESCRIPTION

The ADIS16400/ADIS16405 *i*Sensor® products are complete inertial systems that include a triaxal gyroscope, a triaxial accelerometer, and a triaxial magnetometer. The ADIS16400/ADIS16405 combine industry-leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation for correction formulas that provide accurate sensor measurements over a temperature range of −40°C to +85°C. The magnetometers employ a self-correction function to provide accurate bias performance over temperature, as well.

The ADIS16400/ADIS16405 provide a simple, cost-effective method for integrating accurate, multi-axis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. An improved serial peripheral interface (SPI) and register structure provide faster data collection and configuration control. By using a compatible pinout and the same package as the ADIS1635x and ADIS1636x families, upgrading to the ADIS16400/ADIS16405 requires only firmware changes to accommodate additional sensors and register map updates.

These compact modules are approximately 23 mm × 23 mm × 23 mm and provide a flexible connector interface that enables multiple mounting orientation options.

**Rev. B**

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## REVISION HISTORY

**7/09—Rev. A to Rev. B**

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**4/09—Rev. 0 to Rev. A**

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**3/09—Revision 0: Initial Version**

# SPECIFICATIONS

$T_A$ = −40°C to +85°C, VCC = 5.0 V, angular rate = 0°/sec, dynamic range = ±300°/sec, ±1 *g*, unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GYROSCOPES | | | | | |
| Dynamic Range | | ±300 | ±350 | | °/sec |
| Initial Sensitivity | Dynamic range = ±300°/sec | 0.0495 | 0.05 | 0.0505 | °/sec/LSB |
| | Dynamic range = ±150°/sec | | 0.025 | | °/sec/LSB |
| | Dynamic range = ±75°/sec | | 0.0125 | | °/sec/LSB |
| Sensitivity Temperature Coefficient | ADIS16400: −40°C ≤ $T_A$ ≤ +85°C | | ±250 | | ppm/°C |
| | ADIS16405: −40°C ≤ $T_A$ ≤ +85°C | | ±40 | | ppm/°C |
| Misalignment | Axis-to-axis, Δ = 90° ideal | | ±0.05 | | Degrees |
| | Axis-to-frame (package) | | ±0.5 | | Degrees |
| Nonlinearity | Best fit straight line | | 0.1 | | % of FS |
| Initial Bias Error | 1 σ | | ±3 | | °/sec |
| In-Run Bias Stability | 1 σ, SMPL_PRD = 0x01 | | 0.007 | | °/sec |
| Angular Random Walk | 1 σ, SMPL_PRD = 0x01 | | 2.0 | | °/√hr |
| Bias Temperature Coefficient | ADIS16400: −40°C ≤ $T_A$ ≤ +85°C | | ±0.025 | | °/sec/°C |
| | ADIS16405: −40°C ≤ $T_A$ ≤ +85°C | | ±0.01 | | °/sec/°C |
| Linear Acceleration Effect on Bias | Any axis, 1 σ (MSC_CTRL, Bit 7 = 1) | | 0.05 | | °/sec/*g* |
| Bias Voltage Sensitivity | VCC = 4.75 V to 5.25 V | | 0.32 | | °/sec/V |
| Output Noise | ±300°/sec range, no filtering | | 0.9 | | °/sec rms |
| Rate Noise Density | f = 25 Hz, ±300°/sec, no filtering | | 0.05 | | °/sec/√Hz rms |
| 3 dB Bandwidth | | | 330 | | Hz |
| ACCELEROMETERS | | | | | |
| Dynamic Range | | ±18 | | | *g* |
| Initial Sensitivity | | 3.285 | 3.33 | 3.38 | m*g*/LSB |
| Sensitivity Temperature Coefficient | ADIS16400: −40°C ≤ $T_A$ ≤ +85°C | | ±120 | | ppm/°C |
| | ADIS16405: −40°C ≤ $T_A$ ≤ +85°C | | ±50 | | ppm/°C |
| Misalignment | Axis-to-axis, Δ = 90° ideal | | 0.2 | | Degrees |
| | Axis-to-frame (package) | | ±0.5 | | Degrees |
| Nonlinearity | Best fit straight line, ±17 *g* | | 0.1 | | % of FS |
| Initial Bias Error | 1 σ | | ±50 | | m*g* |
| In-Run Bias Stability | 1 σ | | 0.2 | | m*g* |
| Velocity Random Walk | 1 σ | | 0.2 | | m/sec/√hr |
| Bias Temperature Coefficient | ADIS16400: −40°C ≤ $T_A$ ≤ +85°C | | ±1.35 | | m*g*/°C |
| | ADIS16405: −40°C ≤ $T_A$ ≤ +85°C | | ±0.3 | | m*g*/°C |
| Bias Voltage Sensitivity | VCC = 4.75 V to 5.25 V | | 2.5 | | m*g*/V |
| Output Noise | No filtering | | 9 | | m*g* rms |
| Noise Density | No filtering | | 0.5 | | m*g*/√Hz rms |
| 3 dB Bandwidth | | | 330 | | Hz |
| MAGNETOMETER | | | | | |
| Dynamic Range | | ±2.5 | ±3.5 | | gauss |
| Initial Sensitivity | 25°C | 0.49 | 0.5 | 0.51 | mgauss/LSB |
| Sensitivity Temperature Coefficient | 25°C, 1 σ | | 600 | | ppm/°C |
| Axis Nonorthogonality | 25°C, axis-to-axis | | 0.25 | | Degrees |
| Axis Misalignment | 25°C, axis-to-base plate and guide pins | | 0.5 | | Degrees |
| Nonlinearity | Best fit straight line | | 0.5 | | % of FS |
| Initial Bias Error | 25°C, 0 gauss stimulus | | ±4 | | mgauss |
| Bias Temperature Coefficient | | | 0.5 | | mgauss/°C |
| Output Noise | 25°C, no filtering | | 1.25 | | mgauss rms |
| Noise Density | 25°C, no filtering, rms | | 0.066 | | mgauss/√Hz |
| 3 dB Bandwidth | | | 1540 | | Hz |

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TEMPERATURE SENSOR | | | | | |
| Scale Factor | 25°C, output = 0x0000 | | 0.14 | | °C/LSB |
| ADC INPUT | | | | | |
| Resolution | | | 12 | | Bits |
| Integral Nonlinearity | | | ±2 | | LSB |
| Differential Nonlinearity | | | ±1 | | LSB |
| Offset Error | | | ±4 | | LSB |
| Gain Error | | | ±2 | | LSB |
| Input Range | | 0 | | 3.3 | V |
| Input Capacitance | During acquisition | | 20 | | pF |
| DAC OUTPUT | | | | | |
| Resolution | | | 12 | | Bits |
| Relative Accuracy | Code 101 to Code 4095, 5 kΩ/100 pF to GND | | ±4 | | LSB |
| Differential Nonlinearity | | | ±1 | | LSB |
| Offset Error | | | ±5 | | mV |
| Gain Error | | | ±0.5 | | % |
| Output Range | | 0 | | 3.3 | V |
| Output Impedance | | | 2 | | Ω |
| Output Settling Time | 5 kΩ/100 pF to GND | | 10 | | µs |
| LOGIC INPUTS[1] | | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | | | V |
| Input Low Voltage, $V_{INL}$ | | | | 0.8 | V |
| | $\overline{CS}$ signal to wake up from sleep mode | | | 0.55 | V |
| $\overline{CS}$ Wake-Up Pulse Width | | 20 | | | µs |
| Logic 1 Input Current, $I_{INH}$ | $V_{IH}$ = 3.3 V | | ±0.2 | ±10 | µA |
| Logic 0 Input Current, $I_{INL}$ | $V_{IL}$ = 0 V | | | | |
| All Pins Except $\overline{RST}$ | | | −40 | −60 | µA |
| $\overline{RST}$ Pin | | | −1 | | mA |
| Input Capacitance, $C_{IN}$ | | | 10 | | pF |
| DIGITAL OUTPUTS[1] | | | | | |
| Output High Voltage, $V_{OH}$ | $I_{SOURCE}$ = 1.6 mA | 2.4 | | | V |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 1.6 mA | | | 0.4 | V |
| FLASH MEMORY | Endurance[2] | 10,000 | | | Cycles |
| Data Retention[3] | $T_J$ = 85°C | 20 | | | Years |
| FUNCTIONAL TIMES[4] | Time until data is available | | | | |
| Power-On Start-Up Time | Normal mode, SMPL_PRD ≤ 0x09 | | 220 | | ms |
| | Low power mode, SMPL_PRD ≥ 0x0A | | 290 | | ms |
| Reset Recovery Time | Normal mode, SMPL_PRD ≤ 0x09 | | 100 | | ms |
| | Low power mode, SMPL_PRD ≥ 0x0A | | 170 | | ms |
| Sleep Mode Recovery Time | Normal mode, SMPL_PRD ≤ 0x09 | | 4 | | ms |
| | Low power mode, SMPL_PRD ≥ 0x0A | | 15 | | |
| Flash Memory Test Time | Normal mode, SMPL_PRD ≤ 0x09 | | 17 | | ms |
| | Low power mode, SMPL_PRD ≥ 0x0A | | 90 | | ms |
| Automatic Self-Test Time | SMPL_PRD = 0x01 | | 12 | | ms |
| CONVERSION RATE | SMPL_PRD = 0x01 to 0xFF | 0.413 | | 819.2 | SPS |
| Clock Accuracy | | | | ±3 | % |
| Sync Input Clock | | | | 1.2 | kHz |

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Operating Voltage Range, VCC | | 4.75 | 5.0 | 5.25 | V |
| Power Supply Current | Low power mode at 25°C | | 45 | | mA |
| | Normal mode at 25°C | | 70 | | mA |
| | Sleep mode at 25°C | | 600 | | µA |

[1] The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.
[2] Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.
[3] The data retention lifetime equivalent is at a junction temperature ($T_J$) of 85°C as per JEDEC Standard 22, Method A117. Data retention lifetime decreases with junction temperature.
[4] These times do not include thermal settling and internal filter response times (330 Hz bandwidth), which may affect overall accuracy.

## TIMING SPECIFICATIONS

$T_A$ = 25°C, VCC = 5 V, unless otherwise noted.

**Table 2.**

| | | Normal Mode (SMPL_PRD ≤ 0x09) | | | Low Power Mode (SMPL_PRD ≥ 0x0A) | | | Burst Mode | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min[1]** | **Typ** | **Max** | **Min[1]** | **Typ** | **Max** | **Min[1]** | **Typ** | **Max** | **Unit** |
| $f_{SCLK}$ | Serial clock frequency | 0.01 | | 2.0 | 0.01 | | 0.3 | 0.01 | | 1.0 | MHz |
| $t_{STALL}$ | Stall period between data | 9 | | | 75 | | | $1/f_{SCLK}$ | | | µs |
| $t_{READRATE}$ | Read rate | 40 | | | 150 | | | | | | µs |
| $t_{CS}$ | Chip select to clock edge | 48.8 | | | 48.8 | | | 48.8 | | | ns |
| $t_{DAV}$ | DOUT valid after SCLK edge | | | 100 | | | 100 | | | 100 | ns |
| $t_{DSU}$ | DIN setup time before SCLK rising edge | 24.4 | | | 24.4 | | | 24.4 | | | ns |
| $t_{DHD}$ | DIN hold time after SCLK rising edge | 48.8 | | | 48.8 | | | 48.8 | | | ns |
| $t_{SCLKR}$, $t_{SCLKF}$ | SCLK rise/fall times | | 5 | 12.5 | | 5 | 12.5 | | 5 | 12.5 | ns |
| $t_{DF}$, $t_{DR}$ | DOUT rise/fall times | | 5 | 12.5 | | 5 | 12.5 | | 5 | 12.5 | ns |
| $t_{SFS}$ | $\overline{CS}$ high after SCLK edge | 5 | | | 5 | | | 5 | | | ns |
| $t_1$ | Input sync pulse width | | 5 | | | | | | 5 | | µs |
| $t_2$ | Input sync to data ready output | | 600 | | | | | | 600 | | µs |
| $t_3$ | Input sync period | 833 | | | | | | 833 | | | µs |

[1]Guaranteed by design and characterization but not tested in production.

## TIMING DIAGRAMS

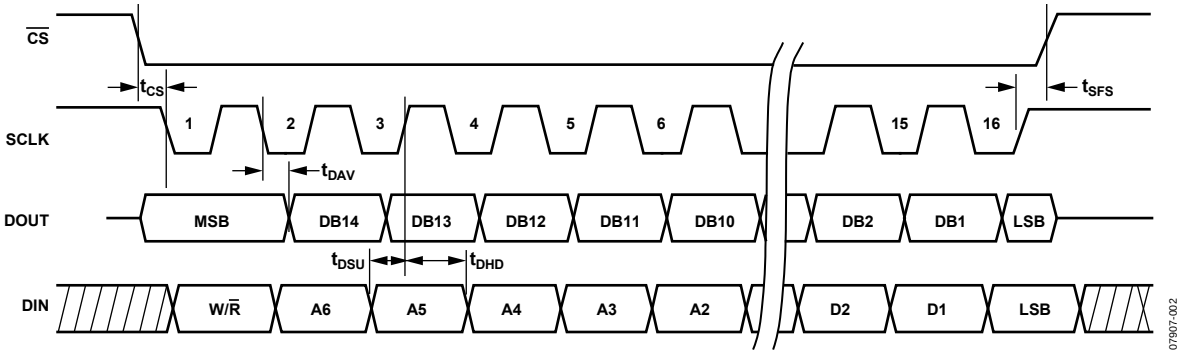



*Figure 2. SPI Timing and Sequence*

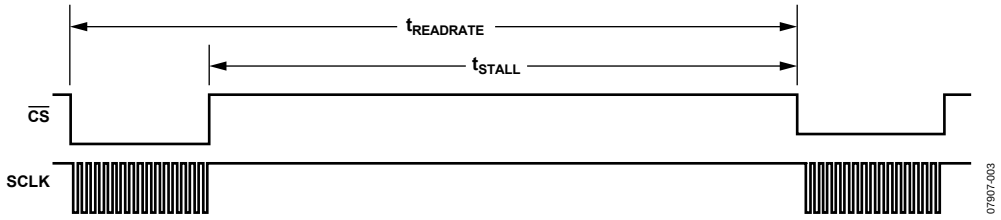



*Figure 3. Stall Time and Data Rate*

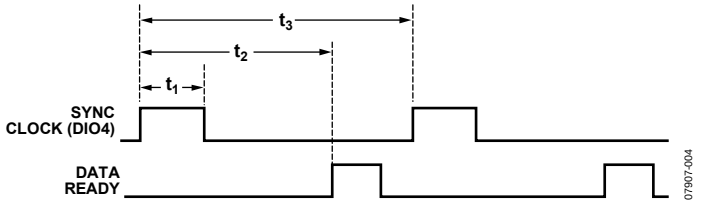



*Figure 4. Input Clock Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Acceleration | |
| Any Axis, Unpowered | 2000 *g* |
| Any Axis, Powered | 2000 *g* |
| VCC to GND | −0.3 V to +6.0 V |
| Digital Input Voltage to GND | −0.3 V to +5.3 V |
| Digital Output Voltage to GND | −0.3 V to VCC + 0.3 V |
| Analog Input to GND | −0.3 V to +3.6 V |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +125°C[1, 2] |

[1] Extended exposure to temperatures outside the specified temperature range of −40°C to +105°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +105°C.
[2] Although the device is capable of withstanding short-term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Package Characteristics**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Device Weight |
|---|---|---|---|
| 24-Lead Module | 39.8°C/W | 14.2°C/W | 16 grams |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

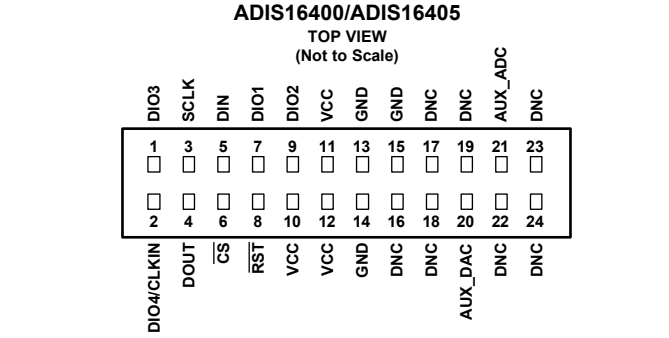



*Figure 5. Pin Configuration*

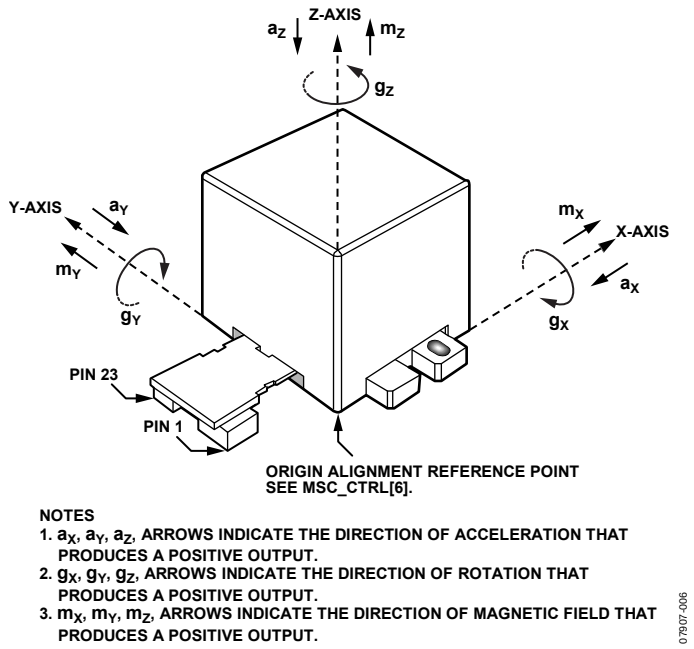



*Figure 6. Axial Orientation*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1 | DIO3 | I/O | Configurable Digital Input/Output. |
| 2 | DIO4/CLKIN | I/O | Configurable Digital Input/Output or Sync Clock Input. |
| 16, 17, 18, 19, 22, 23, 24 | DNC | N/A | Do Not Connect. |
| 3 | SCLK | I | SPI Serial Clock. |
| 4 | DOUT | O | SPI Data Output. Clocks output on SCLK falling edge. |
| 5 | DIN | I | SPI Data Input. Clocks input on SCLK rising edge. |
| 6 | $\overline{CS}$ | I | SPI Chip Select. |
| 7 | DIO1 | I/O | Configurable Digital Input/Output. |
| 8 | $\overline{RST}$ | I | Reset. |
| 9 | DIO2 | I/O | Configurable Digital Input/Output. |
| 10, 11, 12 | VCC | S | Power Supply. |
| 13, 14, 15 | GND | S | Power Ground. |
| 20 | AUX_DAC | O | Auxiliary, 12-Bit DAC Output. |
| 21 | AUX_ADC | I | Auxiliary, 12-Bit ADC Input. |

[1] S is supply, O is output, I is input, N/A is not applicable.

# TYPICAL PERFORMANCE CHARACTERISTICS

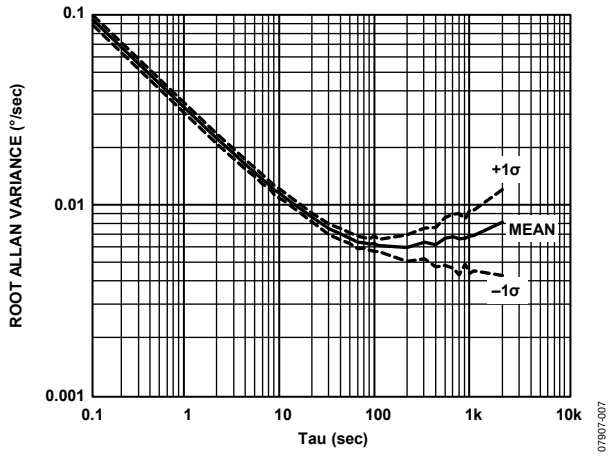



*Figure 7. Gyroscope Root Allan Variance*

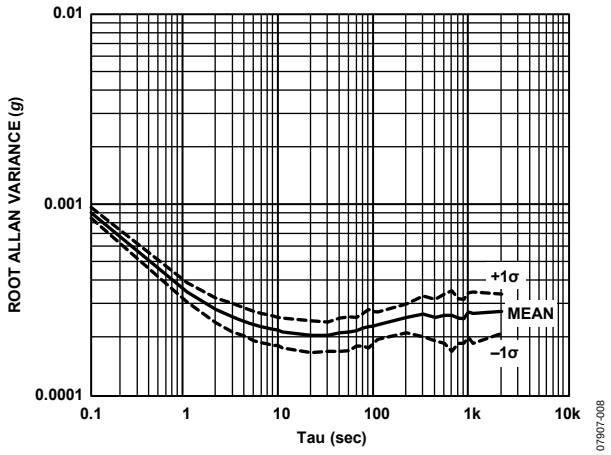



*Figure 8. Accelerometer Root Allan Variance*

# THEORY OF OPERATION

## BASIC OPERATION

The ADIS16400/ADIS16405 are autonomous sensor systems that start up after a valid power supply voltage is applied and then begin producing inertial measurement data at the factory-default sample rate of 819.2 SPS. After each sample cycle, the sensor data loads into the output registers and DIO1 pulses, providing a new data ready control signal for driving system-level interrupt service routines. In a typical system, a master processor accesses the output data registers through the SPI interface, using the hook-up shown in Figure 9. Table 6 provides a generic functional description for each pin on the master processor. Table 7 describes the typical master processor settings normally found in a configuration register and used for communicating with the ADIS16400/ADIS16405.

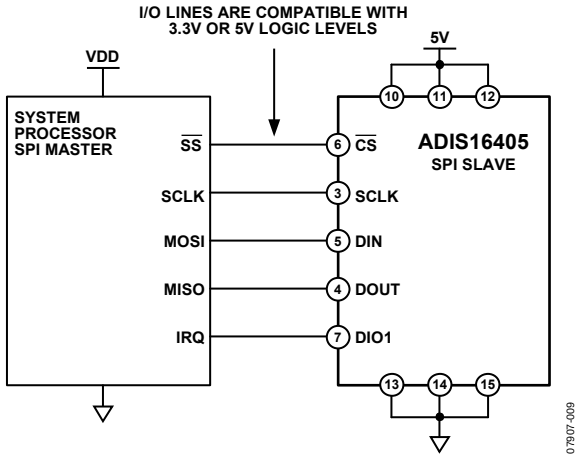



*Figure 9. Electrical Hook-Up Diagram*

**Table 6. Generic Master Processor Pin Names and Functions**

| Pin Name | Function |
|---|---|
| $\overline{SS}$ | Slave select |
| IRQ | Interrupt request |
| MOSI | Master output, slave input |
| MISO | Master input, slave output |
| SCLK | Serial clock |

**Table 7. Generic Master Processor SPI Settings**

| Processor Setting | Description |
|---|---|
| Master | The ADIS16400/ADIS16405 operate as a slave. |
| SCLK Rate ≤ 2 MHz[1] | Normal mode, SMPL_PRD[7:0] ≤ 0x08. |
| CPOL = 1 | Clock polarity. |
| CPHA = 1 | Clock phase. |
| MSB-First | Bit sequence. |
| 16-Bit | Shift register/data length. |

[1] For burst mode, SCLK rate ≤ 1 MHz. For low power mode, SCLK rate ≤ 300 kHz.

The user registers provide addressing for all input/output operations on the SPI interface. Each 16-bit register has two 7-bit addresses: one for its upper byte and one for its lower byte. Table 8 lists the lower byte address for each register, and Figure 10 shows the generic bit assignments.

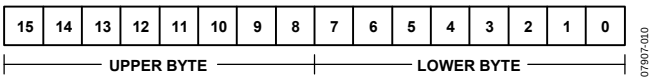



*Figure 10. Output Register Bit Assignments*

## READING SENSOR DATA

Although the ADIS16400/ADIS16405 produce data independently, these operate as SPI slave devices that communicate with system (master) processors using the 16-bit segments displayed in Figure 11. Individual register reads require two such 16-bit sequences. The first 16-bit sequence provides the read command bit ($\overline{R}/W = 0$) and the target register address (A6 to A0). The second sequence transmits the register contents (D15 to D0) on the DOUT line. For example, if DIN = 0x0A00, the content of XACCL_OUT shifts out on the DOUT line during the next 16-bit sequence.

The SPI operates in full duplex mode, which means that the master processor can read the output data from DOUT while using the same SCLK pulses to transmit the next target address on DIN.

## DEVICE CONFIGURATION

The user register memory map (Table 8) identifies configuration registers with either a W (write only) or R/W (read/write). Configuration commands also use the bit sequence displayed in Figure 11. If the MSB is equal to 1, the last eight bits (DC7 to DC0) in the DIN sequence load into the memory address associated with the address bits (A5 to A0). For example, if DIN = 0xA11F, then 0x1F loads into Address Location 0x21 (XACCL_OFF, upper byte) at the conclusion of the data frame.

Most of the registers have a backup location in nonvolatile flash memory. The master processor must manage the backup function. Set GLOB_CMD[3] = 1 (DIN = 0xBE04) to execute a manual flash update (backup) operation, which copies the user registers into their respective flash memory locations. This operation takes 50 ms and requires the power supply voltage to be within the specified limit to complete properly. The FLASH_CNT register provides a running count of these events for managing the long-term reliability of the flash memory.

## BURST MODE DATA COLLECTION

Burst mode data collection offers a more efficient method for collecting data from the ADIS16400/ADIS16405. In sequential data cycles (each separated by one SCLK period), all output registers clock out on DOUT. This sequence starts when the DIN sequence is 0011 1110 0000 0000 (0x3E00). Next, the contents of each output register are output from DOUT, starting with SUPPLY_OUT and ending with AUX_ADC (see Figure 12). The addressing sequence shown in Table 8 determines the order of the outputs in burst mode.

## MEMORY MAP

**Table 8. User Register Memory Map**

| Name | R/W | Flash Backup | Address[1] | Default | Function | Bit Assignments |
|---|---|---|---|---|---|---|
| FLASH_CNT | R | Yes | 0x00 | N/A | Flash memory write count | N/A |
| SUPPLY_OUT | R | No | 0x02 | N/A | Power supply measurement | See Table 9 |
| XGYRO_OUT | R | No | 0x04 | N/A | X-axis gyroscope output | See Table 9 |
| YGYRO_OUT | R | No | 0x06 | N/A | Y-axis gyroscope output | See Table 9 |
| ZGYRO_OUT | R | No | 0x08 | N/A | Z-axis gyroscope output | See Table 9 |
| XACCL_OUT | R | No | 0x0A | N/A | X-axis accelerometer output | See Table 9 |
| YACCL_OUT | R | No | 0x0C | N/A | Y-axis accelerometer output | See Table 9 |
| ZACCL_OUT | R | No | 0x0E | N/A | Z-axis accelerometer output | See Table 9 |
| XMAGN_OUT | R | No | 0x10 | N/A | X-axis magnetometer measurement | See Table 9 |
| YMAGN_OUT | R | No | 0x12 | N/A | Y-axis magnetometer measurement | See Table 9 |
| ZMAGN_OUT | R | No | 0x14 | N/A | Z-axis magnetometer measurement | See Table 9 |
| TEMP_OUT | R | No | 0x16 | N/A | Temperature output | See Table 9 |
| AUX_ADC | R | No | 0x18 | N/A | Auxiliary ADC measurement | See Table 9 |
| XGYRO_OFF | R/W | Yes | 0x1A | 0x0000 | X-axis gyroscope bias offset factor | See Table 10 |
| YGYRO_OFF | R/W | Yes | 0x1C | 0x0000 | Y-axis gyroscope bias offset factor | See Table 10 |
| ZGYRO_OFF | R/W | Yes | 0x1E | 0x0000 | Z-axis gyroscope bias offset factor | See Table 10 |
| XACCL_OFF | R/W | Yes | 0x20 | 0x0000 | X-axis acceleration bias offset factor | See Table 11 |
| YACCL_OFF | R/W | Yes | 0x22 | 0x0000 | Y-axis acceleration bias offset factor | See Table 11 |
| ZACCL_OFF | R/W | Yes | 0x24 | 0x0000 | Z-axis acceleration bias offset factor | See Table 11 |
| XMAGN_HIF | R/W | Yes | 0x26 | 0x0000 | X-axis magnetometer, hard-iron factor | See Table 12 |
| YMAGN_HIF | R/W | Yes | 0x28 | 0x0000 | Y-axis magnetometer, hard-iron factor | See Table 12 |
| ZMAGN_HIF | R/W | Yes | 0x2A | 0x0000 | Z-axis magnetometer, hard-iron factor | See Table 12 |
| XMAGN_SIF | R/W | Yes | 0x2C | 0x0800 | X-axis magnetometer, soft-iron factor | See Table 13 |
| YMAGN_SIF | R/W | Yes | 0x2E | 0x0800 | Y-axis magnetometer, soft-iron factor | See Table 13 |
| ZMAGN_SIF | R/W | Yes | 0x30 | 0x0800 | Z-axis magnetometer, soft-iron factor | See Table 13 |
| GPIO_CTRL | R/W | No | 0x32 | 0x0000 | Auxiliary digital input/output control | See Table 18 |
| MSC_CTRL | R/W | Yes | 0x34 | 0x0006 | Miscellaneous control | See Table 19 |
| SMPL_PRD | R/W | Yes | 0x36 | 0x0001 | Internal sample period (rate) control | See Table 15 |
| SENS_AVG | R/W | Yes | 0x38 | 0x0402 | Dynamic range and digital filter control | See Table 17 |
| SLP_CNT | W | No | 0x3A | 0x0000 | Sleep mode control | See Table 16 |
| DIAG_STAT | R | No | 0x3C | 0x0000 | System status | See Table 23 |
| GLOB_CMD | W | N/A | 0x3E | 0x0000 | System command | See Table 14 |
| ALM_MAG1 | R/W | Yes | 0x40 | 0x0000 | Alarm 1 amplitude threshold | See Table 25 |
| ALM_MAG2 | R/W | Yes | 0x42 | 0x0000 | Alarm 2 amplitude threshold | See Table 25 |
| ALM_SMPL1 | R/W | Yes | 0x44 | 0x0000 | Alarm 1 sample size | See Table 26 |
| ALM_SMPL2 | R/W | Yes | 0x46 | 0x0000 | Alarm 2 sample size | See Table 26 |
| ALM_CTRL | R/W | Yes | 0x48 | 0x0000 | Alarm control | See Table 24 |
| AUX_DAC | R/W | No | 0x4A | 0x0000 | Auxiliary DAC data | See Table 20 |
| | | | 0x4C to 0x55 | | Reserved | |
| PRODUCT_ID | | | 0x56 | 0x4105 | Product identifier | |

[1] Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte plus 1.

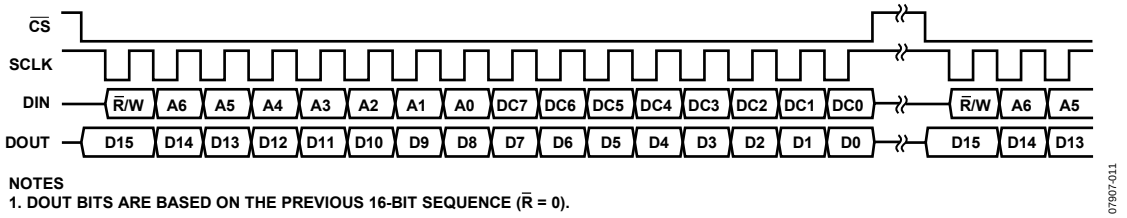



*Figure 11. Output Register Bit Assignments*

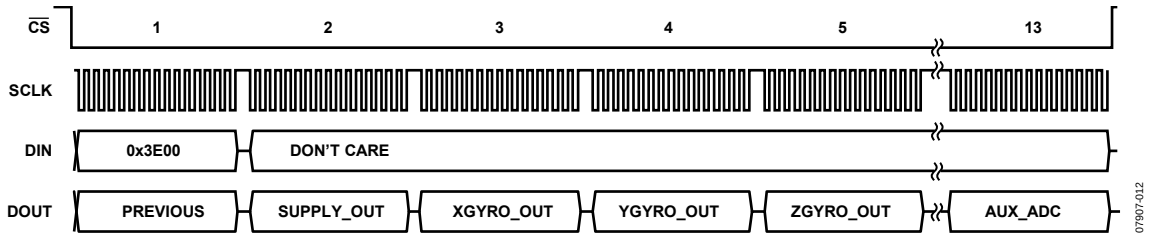



*Figure 12. Burst Mode Read Sequence*

## OUTPUT DATA REGISTERS

Figure 6 provides the positive measurement direction for each gyroscope, accelerometer, and magnetometer. Table 9 provides the configuration and scale factor for each output data register in the ADIS16400/ADIS16405. All inertial sensor outputs are in 14-bit, twos complement format, which means that 0x0000 is equal to 0 LSB, 0x0001 is equal to +1 LSB, and 0x3FFF is equal to −1 LSB. The following is an example of how to calculate the sensor measurement from the XGYRO_OUT:

*XGYRO_OUT* = 0x3B4A

0x000 − 0x3B4A = −0x04B6 = (4 × 256 + 11 × 16 + 6) − 0x04B6 = −1206 LSB

*Rate* = 0.05°/sec × (−1206) = −60.3°/sec

Therefore, an XGYRO_OUT output of 0x3B4A corresponds to a clockwise rotation about the z-axis (see Figure 6) of 60.3°/sec when looking at the top of the package.

**Table 9. Output Data Register Formats**

| Register | Bits | Format | Scale |
|---|---|---|---|
| SUPPLY_OUT | 14 | Binary, 5 V = 0x0814 | 2.418 mV |
| XGYRO_OUT[1] | 14 | Twos complement | 0.05°/sec |
| YGYRO_OUT[1] | 14 | Twos complement | 0.05°/sec |
| ZGYRO_OUT[1] | 14 | Twos complement | 0.05°/sec |
| XACCL_OUT | 14 | Twos complement | 3.33 m*g* |
| YACCL_OUT | 14 | Twos complement | 3.33 m*g* |
| ZACCL_OUT | 14 | Twos complement | 3.33 m*g* |
| XMAGN_OUT | 14 | Twos complement | 0.5 mgauss |
| YMAGN_OUT | 14 | Twos complement | 0.5 mgauss |
| ZMAGN_OUT | 14 | Twos complement | 0.5 mgauss |
| TEMP_OUT[2] | 12 | Twos complement | 0.14°C |
| AUX_ADC | 12 | Binary, 1 V = 0x04D9 | 806 µV |

[1] Assumes that the scaling is set to ±300°/sec. This factor scales with the range.
[2] The typical output for this register at 25°C is 0x0000.

Each output data register uses the bit assignments shown in Figure 13. The ND flag indicates that unread data resides in the output data registers. This flag clears and returns to 0 during an output register read sequence. It returns to 1 after the next internal sample updates the registers with new data. The EA flag indicates that one of the error flags in the DIAG_STAT register (see Table 23) is active (true). The remaining 14 bits are for data.

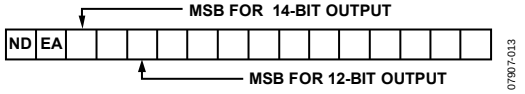



*Figure 13. Output Register Bit Assignments*

### *Auxiliary ADC*

The AUX_ADC register provides access to the auxiliary ADC input channel. The ADC is a 12-bit successive approximation converter that has an equivalent input circuit to the one shown in Figure 14. The maximum input is 3.3 V. The ESD protection diodes can handle 10 mA without causing irreversible damage. The on resistance (R1) of the switch has a typical value of 100 Ω. The sampling capacitor, C2, has a typical value of 16 pF.

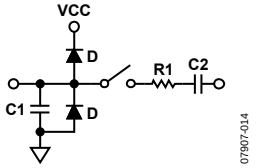



*Figure 14. Equivalent Analog Input Circuit*
*(Conversion Phase: Switch Open, Track Phase: Switch Closed)*

## CALIBRATION

### *Manual Bias Calibration*

The bias offset registers in Table 10, Table 11, and Table 12 (hard-iron correction for magnetometer) provide a manual adjustment function for the output of each sensor. For example, if XGYRO_OFF equals 0x1FF6, the XGYRO_OUT offset shifts by −10 LSB, or −0.125°/sec. The DIN command for the upper byte is DIN = 0x9B1F; for the lower byte, DIN = 0x9AF6.

**Table 10. XGYRO_OFF, YGYRO_OFF, ZGYRO_OFF**

| Bits | Description | Default = 0x0000 |
|---|---|---|
| [15:13] | Not used. | |
| [12:0] | Data bits. Twos complement, 0.0125°/sec per LSB. Typical adjustment range = ±50°/sec. | |

**Table 11. XACCL_OFF, YACCL_OFF, ZACCL_OFF**

| Bits | Description | Default = 0x0000 |
|---|---|---|
| [15:12] | Not used. | |
| [11:0] | Data bits. Twos complement, 3.3 m*g*/LSB. Typical adjustment range = ±6.75 *g*. | |

**Table 12. XMAGN_HIF, YMAGN_HIF, ZMAGN_HIF**

| Bits | Description | Default = 0x0000 |
|---|---|---|
| [15:14] | Not used. | |
| [13:0] | Data bits. Twos complement, 0.5 mgauss/LSB. Typical adjustment range = ±4 gauss. | |

### *Magnetometer Soft-Iron Correction (Scale Factor)*

The soft-iron correction factor for the magnetometer provides the opportunity to change the scale factor for each individual axis.

**Table 13. XMAGN_SIF, YMAGN_SIF, ZMAGN_SIF**

| Bits | Description | Default = 0x0800 |
|---|---|---|
| [15:12] | Not used. | |
| [11:0] | Data bits. Binary, linear scale adjustment factor between 0x0000 (0x) and 0x3FFF (2x). | |

### *Gyroscope Automatic Bias Null Calibration*

Set GLOB_CMD[0] = 1 (DIN = 0xBE01) to execute this function, which measures the gyroscope outputs and then loads the gyroscope offset registers with the opposite values to provide a quick bias calibration. Then, all sensor data resets to 0, and the flash memory updates automatically within 50 ms (see Table 14).

### *Gyroscope Precision Automatic Bias Null Calibration*

Set GLOB_CMD[4] = 1 (DIN = 0xBE10) to execute this function, which takes the sensor offline for 30 sec while it collects a set of gyroscope data and calculates a more accurate bias correction factor for each gyroscope. Once calculated, the correction factor loads into the three gyroscope offset registers, all sensor data resets to 0, and the flash memory updates automatically within 50 ms (see Table 14).

### *Restoring Factory Calibration*

Set GLOB_CMD[1] = 1 (DIN = 0xBE02) to execute this function, which resets each user calibration register (see Table 10, Table 11, and Figure 12) to 0x0000, resets all sensor data to 0, and automatically updates the flash memory within 50 ms (see Table 14).

### *Linear Acceleration Bias Compensation (Gyroscope)*

Set MSC_CTRL[7] = 1 (DIN = 0xB486) to enable correction for low frequency acceleration influences on gyroscope bias. Note that the DIN sequence also preserves the factory default condition for the data ready function (see Table 19).

## OPERATIONAL CONTROL

### *Global Commands*

The GLOB_CMD register provides trigger bits for several useful functions. Setting the assigned bit to 1 starts each operation, which returns to the bit to 0 after completion. For example, set GLOB_CMD[7] = 1 (DIN = 0xBE80) to execute a software reset, which stops the sensor operation and runs the device through its start-up sequence. This includes loading the control registers with their respective flash memory locations prior to producing new data. Reading the GLOB_CMD registers (DIN = 0x3E00) starts the burst mode read sequence.

**Table 14. GLOB_CMD**

| Bits | Description |
|---|---|
| [15:8] | Not used |
| [7] | Software reset command |
| [6:5] | Not used |
| [4] | Precision autonull command |
| [3] | Flash update command |
| [2] | Auxiliary DAC data latch |
| [1] | Factory calibration restore command |
| [0] | Autonull command |

### *Internal Sample Rate*

The SMPL_PRD register provides discrete sample rate settings, using the bit assignments in Table 15 and the following equation:

$$t_S = t_B \times (N_S + 1),$$

When SMPL_PRD[7:0] = 0x0A, the sample rate = 149 SPS.

**Table 15. SMPL_PRD**

| Bits | Description | Default = 0x0001 |
|---|---|---|
| [15:8] | Not used | |
| [7] | Time base ($t_B$)<br>0 = 0.61035 ms, 1 = 18.921 ms | |
| [6:0] | Increment setting ($N_S$)<br>Internal sample period = $t_S = t_B \times (N_S + 1)$ | |

The default sample rate setting of 819.2 SPS preserves the sensor bandwidth and provides optimal performance. For systems that value slower sample rates, simply read the device at a slower rate and keep the internal sample rate at 819.2 SPS. Use the programmable filter (SENS_AVG) to reduce the bandwidth along with the reduced read rates. The data-ready function (MSC_CTRL) can drive an interrupt routine that uses a counter to help assure data coherence at the reduced update rates.

### *Power Management*

Setting SMPL_PRD ≥ 0x0A also sets the sensor in low power mode. For systems that require the lower power dissipation, in-system characterization helps users to quantify the associated performance trade-offs. In addition to sensor performance, this mode affects SPI data rates (see Table 2). Set SLP_CNT[8] = 1 (DIN = 0xBB01) to start the indefinite sleep mode, which requires a $\overline{CS}$ assertion (high to low), reset, or power cycle to wake up. Use SLP_CNT[7:0] to put the device in sleep mode for a given period of time. For example, SLP_CNT[7:0] = 0x64 (DIN = 0xBA64) puts the device to sleep for 50 seconds.

**Table 16. SLP_CNT**

| Bits | Description |
|---|---|
| [15:9] | Not used |
| [8] | Indefinite sleep mode, set to 1 |
| [7:0] | Programmable sleep time bits, 0.5 sec/LSB |

### Digital Filtering

A programmable low-pass filter provides additional opportunity for noise reduction on the inertial sensor outputs. This filter contains two cascaded averaging filters that provide a Bartlett window, FIR filter response (see Figure 15). For example, SENS_AVG[2:0] = 100 (DIN = B804) sets each stage tap to 16. When used with the default sample rate of 819.2 SPS, this reduces the sensor bandwidth to approximately 16 Hz.

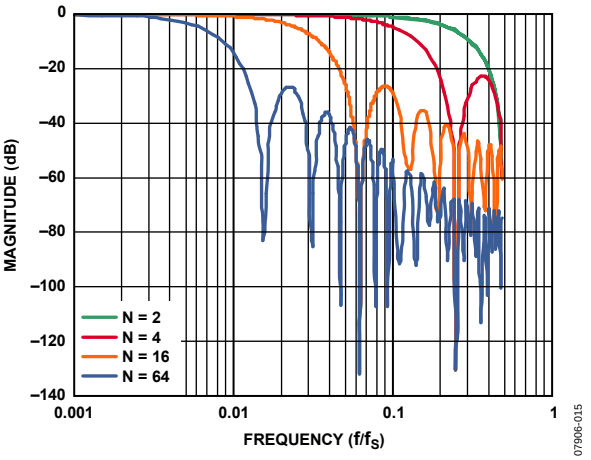



*Figure 15. Bartlett Window FIR Frequency Response (Taps = 2N + 1, Phase = N Samples)*

### Dynamic Range

There are three dynamic range settings for the gyroscope. The lower dynamic range settings (±75°/sec and ±150°/sec) limit the minimum filter tap sizes to maintain resolution. For example, set SENS_AVG[10:8] = 010 (DIN = 0xB902) for a measurement range of ±150°/sec. Because this setting can influence the filter settings, program SENS_AVG[10:8], then SENS_AVG[2:0] if more filtering is required.

**Table 17. SENS_AVG**

| Bits | Settings | Description | Default = 0x0402 |
|---|---|---|---|
| [15:11] | | Not used | |
| [10:8] | | Measurement range (sensitivity) selection | |
| | 100 | ±300°/sec (default condition) | |
| | 010 | ±150°/sec, filter taps ≥ 4 (Bits[2:0] ≥ 0x02) | |
| | 001 | ±75°/sec, filter taps ≥ 16 (Bits[2:0] ≥ 0x04) | |
| [7:3] | | Not used | |
| [2:0] | | Number of taps in each stage N = $2^M$ | |

## INPUT/OUTPUT FUNCTIONS

### General-Purpose I/O

DIO1, DIO2, DIO3, and DIO4 are configurable, general-purpose I/O lines that serve multiple purposes according to the following control register priority: MSC_CTRL, ALM_CTRL, and GPIO_CTRL. For example, set GPIO_CTRL = 0x080C (DIN = 0xB308, and then 0xB20C) to set DIO1 and DIO2 as inputs and DIO3 and DIO4 as outputs, with DIO3 set low and DIO4 set high.

**Table 18. GPIO_CTRL**

| Bits | Description | Default = 0x0000 |
|---|---|---|
| [15:12] | Not used | |
| [11] | General-Purpose I/O Line 4 (DIO4) data level | |
| [10] | General-Purpose I/O Line 3 (DIO3) data level | |
| [9] | General-Purpose I/O Line 2 (DIO2) data level | |
| [8] | General-Purpose I/O Line 1 (DIO1) data level | |
| [7:4] | Not used | |
| [3] | General-Purpose I/O Line 4 (DIO4), direction control<br>1 = output, 0 = input | |
| [2] | General-Purpose I/O Line 3 (DIO3), direction control<br>1 = output, 0 = input | |
| [1] | General-Purpose I/O Line 2 (DIO2), direction control<br>1 = output, 0 = input | |
| [0] | General-Purpose I/O Line 1 (DIO1), direction control<br>1 = output, 0 = input | |

### Input Clock Configuration

The input clock allows for external control over sampling in the ADIS16400/ADIS16405. Set GPIO_CTRL[3] = 0 (DIN = 0x0B200) and SMPL_PRD[7:0] = 0x00 (DIN = 0xB600) to enable this function. See Table 2 and Figure 4 for timing information.

### Data Ready I/O Indicator

The factory default sets DIO1 as a positive data ready indicator signal. The MSC_CTRL[2:0] register provides configuration options for changing this. For example, set MSC_CTRL[2:0] = 100 (DIN = 0xB404) to change the polarity of the data ready signal for interrupt inputs that require negative logic inputs for activation. The resulting pulse width is be between 100 µs and 200 µs over all conditions.

**Table 19. MSC_CTRL**

| Bits | Description | Default = 0x0006 |
|---|---|---|
| [15:12] | Not used | |
| [11] | Memory test (clears on completion)<br>1 = enabled, 0 = disabled | |
| [10] | Internal self-test enable (clears on completion)<br>1 = enabled, 0 = disabled | |
| [9] | Manual self-test, negative stimulus<br>1 = enabled, 0 = disabled | |
| [8] | Manual self-test, positive stimulus<br>1 = enabled, 0 = disabled | |
| [7] | Linear acceleration bias compensation for gyroscopes<br>1 = enabled, 0 = disabled | |
| [6] | Linear accelerometer origin alignment<br>1 = enabled, 0 = disabled | |
| [5:3] | Not used | |
| [2] | Data ready enable<br>1 = enabled, 0 = disabled | |
| [1] | Data ready polarity<br>1 = active high, 0 = active low | |
| [0] | Data ready line select<br>1 = DIO2, 0 = DIO1 | |

### *Auxiliary DAC*

The 12-bit AUX_DAC line can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches 0 V, the linearity begins to degrade (~100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC latch command moves the values of the AUX_DAC register into the DAC input register, enabling both bytes to take effect at the same time.

**Table 20. AUX_DAC**

| Bits | Description | Default = 0x0000 |
|---|---|---|
| [15:12] | Not used. | |
| [11:0] | Data bits. Scale factor = 0.8059 mV/code, offset binary format, 0 V = 0 codes. | |

**Table 21. Setting AUX_DAC = 1 V**

| DIN | Description |
|---|---|
| 0xB0D9 | AUX_DAC[7:0] = 0xD9 (217 LSB). |
| 0xB104 | AUX_DAC[15:8] = 0x04 (1024 LSB). |
| 0xBE04 | GLOB_CMD[2] = 1.<br>Move values into the DAC input register, resulting in a 1 V output level. |

## DIAGNOSTICS

### *Self-Test*

The self-test function offers the opportunity to verify the mechanical integrity of each MEMS sensor. It applies an electrostatic force to each sensor element, which results in mechanical displacement that simulates a response to actual motion. Table 1 lists the expected response for each sensor, which provides pass/fail criteria. Set MSC_CTRL[10] = 1 (DIN = 0xB504) to run the internal self-test routine, which exercises all inertial sensors, measures each response, makes pass/fail decisions, and reports them to error flags in the DIAG_STAT register. MSC_CTRL[10] resets itself to 0 after completing the routine. MSC_CTRL[9:8] (DIN = 0xB502 or 0xB501) provide manual control over the self-test function. Table 22 shows an example test flow for using this option to check the x-axis gyroscope. Zero motion provides results that are more reliable. The settings in Table 22 are flexible and provide opportunity for optimization around speed and noise influence. For example, using fewer filtering taps decreases delay times but increases the opportunity for noise influence.

### *Memory Test*

Setting MSC_CTRL[11] = 1 (DIN = 0xB508) performs a checksum verification of the flash memory locations. The pass/fail result loads into the DIAG_STAT[6] register.

### *Status*

The error flags provide indicator functions for common system-level issues. All of the flags clear (set to 0) after each DIAG_STAT register read cycle. If an error condition remains, the error flag returns to 1 during the next sample cycle. DIAG_STAT[1:0] does not require a read of this register to return to 0.

**Table 22. Manual Self-Test Example Sequence**

| DIN | Description |
|---|---|
| 0xB601 | SMPL_PRD[7:0] = 0x01, sample rate = 819.2 SPS. |
| 0xB904 | SENS_AVG[15:8] = 0x04, gyroscope range = ±300°/sec. |
| 0xB802 | SENS_AVG[7:0] = 0x02, four-tap averaging filter. |
| | Delay = 50 ms. |
| 0x0400 | Read XGYRO_OUT. |
| 0xB502 | MSC_CTRL[9] = 1, gyroscope negative self-test. |
| | Delay = 50 ms. |
| 0x0400 | Read XGYRO_OUT. |
| | Calculate the positive change from the first reading to the second reading of XGYRO_OUT, and check to make sure the change is within the positive self-test response range specified in Table 1. |
| 0xB501 | MSC_CTRL[9:8] = 01, gyroscope/accelerometer positive self-test. |
| | Delay = 50 ms. |
| 0x0400 | Read XGYRO_OUT. |
| | Calculate the negative change from the first reading to the third reading of XGYRO_OUT, and check to make sure the change is within the positive self-test response range specified in Table 1. |
| 0xB500 | MSC_CTRL[15:8] = 0x00. |

**Table 23. DIAG_STAT Bit Descriptions**

| Bit | Description |
|---|---|
| [15] | Z-axis accelerometer self-test failure (1 = fail, 0 = pass) |
| [14] | Y-axis accelerometer self-test failure (1 = fail, 0 = pass) |
| [13] | X-axis accelerometer self-test failure (1 = fail, 0 = pass) |
| [12] | Z-axis gyroscope self-test failure (1 = fail, 0 = pass) |
| [11] | Y-axis gyroscope self-test failure (1 = fail, 0 = pass) |
| [10] | X-axis gyroscope self-test failure (1 = fail, 0 = pass) |
| [9] | Alarm 2 status (1 = active, 0 = inactive) |
| [8] | Alarm 1 status (1 = active, 0 = inactive) |
| [7] | Not used |
| [6] | Flash test, checksum flag (1 = fail, 0 = pass) |
| [5] | Self-test diagnostic error flag (1 = fail, 0 = pass) |
| [4] | Sensor overrange (1 = fail, 0 = pass) |
| [3] | SPI communication failure (1 = fail, 0 = pass) |
| [2] | Flash update failure (1 = fail, 0 = pass) |
| [1] | Power supply above 5.25 V<br>(1 = power supply ≥ 5.25 V, 0 = power supply ≤ 5.25 V) |
| [0] | Power supply below 4.75 V<br>(1 = power supply ≤ 4.75 V, 0 = power supply ≥ 4.75 V) |

### *Alarm Registers*

The alarm function provides monitoring for two independent conditions. The ALM_CTRL register provides control inputs for data source, data filtering (prior to comparison), static comparison, dynamic rate-of-change comparison, and output indicator configurations. The ALM_MAGx registers establish the trigger threshold and polarity configurations.

Table 27 gives an example of how to configure a static alarm. The ALM_SMPLx registers provide the number of samples to use in the dynamic rate-of-change configuration. The period equals the number in the ALM_SMPLx register multiplied by the sample period time, which is established by the SMPL_PRD register. See Table 28 for an example of how to configure the sensor for this type of function.

**Table 24. ALM_CTRL Bit Designations**

| Bits | Settings | Description | Default = 0x0000 |
|---|---|---|---|
| [15:12] | | Alarm 2 source selection | |
| | 0000 | Disable | |
| | 0001 | Power supply output | |
| | 0010 | X-axis gyroscope output | |
| | 0011 | Y-axis gyroscope output | |
| | 0100 | Z-axis gyroscope output | |
| | 0101 | X-axis accelerometer output | |
| | 0110 | Y-axis accelerometer output | |
| | 0111 | Z-axis accelerometer output | |
| | 1000 | X-axis magnetometer output | |
| | 1001 | Y-axis magnetometer output | |
| | 1010 | Z-axis magnetometer output | |
| | 1011 | Gyroscope temperature output | |
| | 1100 | Auxiliary ADC input | |
| [11:8] | | Alarm 1 source selection (same as Alarm 2) | |
| [7] | | Rate-of-change (ROC) enable for Alarm 2<br>1 = rate of change, 0 = static level | |
| [6] | | Rate-of-change (ROC) enable for Alarm 1<br>1 = rate of change, 0 = static level | |
| [5] | | Not used | |
| [4] | | Comparison data filter setting<br>1 = filtered data, 0 = unfiltered data | |
| [3] | | Not used | |
| [2] | | Alarm output enable<br>1 = enabled, 0 = disabled | |
| [1] | | Alarm output polarity<br>1 = active high, 0 = active low | |
| [0] | | Alarm output line select<br>1 = DIO2, 0 = DIO1 | |

**Table 25. ALM_MAG1, ALM_MAG2**

| Bits | Description | Default = 0x0000 |
|---|---|---|
| [15] | Comparison polarity<br>1 = greater than, 0 = less than | |
| [14] | Not used | |
| [13:0] | Data bits that match the format of the trigger source selection | |

**Table 26. ALM_SMPL1, ALM_SMPL2**

| Bits | Description | Default = 0x0000 |
|---|---|---|
| [15:8] | Not used | |
| [7:0] | Data bits: number of samples<br>(both 0x00 and 0x01 = 1) | |

**Table 27. Alarm Configuration Example 1**

| DIN | Description |
|---|---|
| 0xAF55,<br>0xAE17 | ALM_CTRL = 0x5517.<br>Alarm 1 input = XACCL_OUT.<br>Alarm 2 input = XACCL_OUT.<br>Static level comparison, filtered data.<br>DIO2 output indicator, positive polarity. |
| 0xA783,<br>0xA641 | ALM_MAG1 = 0x8341.<br>Alarm 1 is true if XACCL_OUT > +0.5 *g*. |
| 0xA93C,<br>0xA8BF | ALM_MAG2= 0x3CBF.<br>Alarm 2 is true if XACCL_OUT < −0.5 *g*. |

**Table 28. Alarm Configuration Example 2**

| DIN | Description |
|---|---|
| 0xAF76,<br>0xAE87 | ALM_CTRL = 0x7687.<br>Alarm 1 input = ZACCL_OUT.<br>Alarm 2 input = YACCL_OUT.<br>Rate of change comparison, unfiltered data.<br>DIO2 output indicator, positive polarity. |
| 0xB601 | SMPL_PRD = 0x0001.<br>Sample rate = 819.2 SPS. |
| 0xAB08 | ALM_SMPL1 = 0x0008.<br>Alarm 1 rate of change period = 9.77 ms. |
| 0xAC50 | ALM_SMPL2= 0x0050.<br>Alarm 2 rate of change period = 97.7 ms. |
| 0xA783,<br>0xA641 | ALM_MAG1 = 0x8341.<br>Alarm 1 is true if XACCL_OUT > +0.5 *g*. |
| 0xA93C,<br>0xA8BE | ALM_MAG2= 0x3CBE.<br>Alarm 2 is true if XACCL_OUT < −0.5 *g*. |

# OUTLINE DIMENSIONS

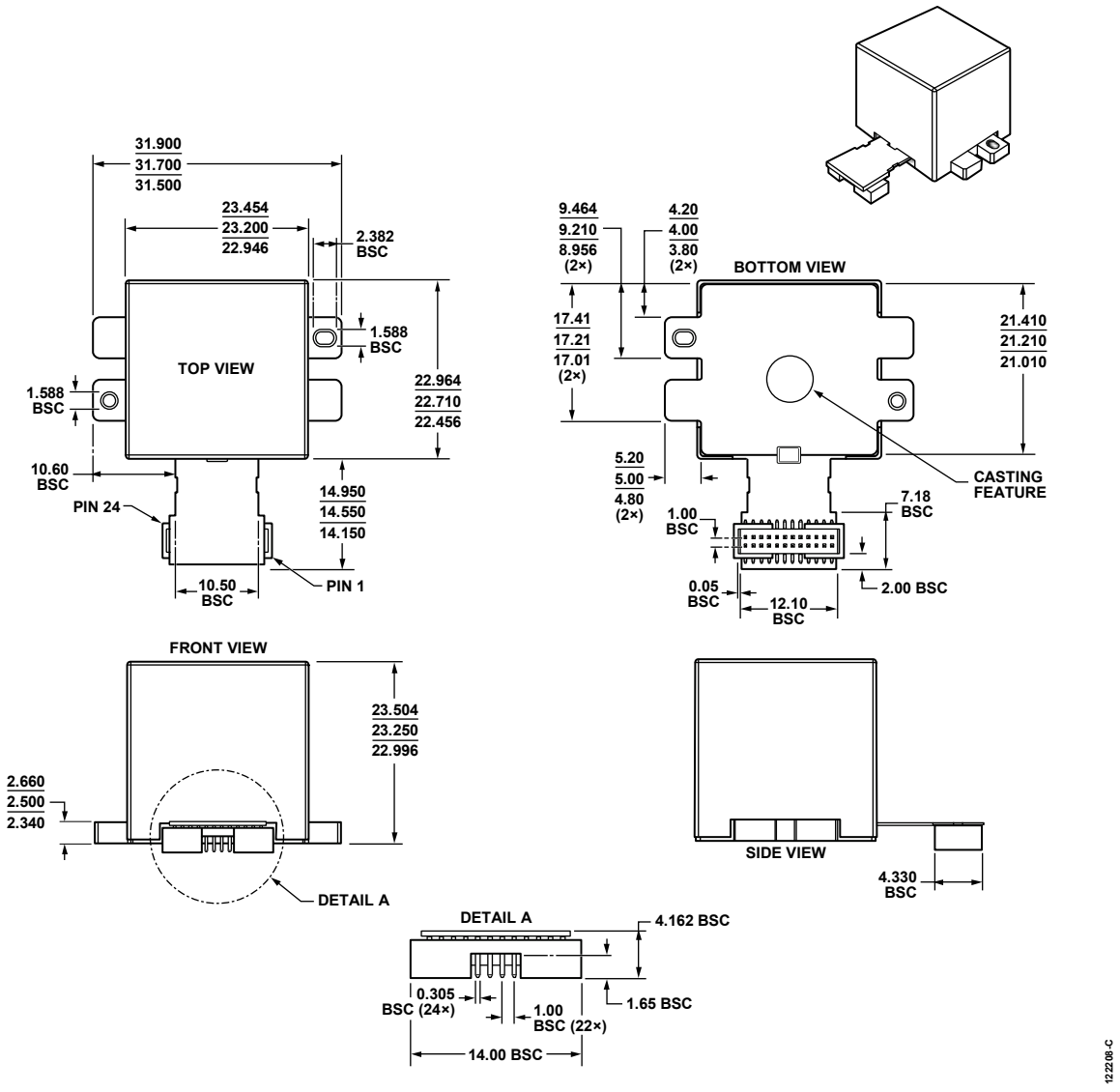



*Figure 16. 24-Lead Module with Connector Interface*
*(ML-24-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADIS16400BMLZ[1] | −40°C to +105°C | 24-Lead Module with Connector Interface | ML-24-2 |
| ADIS16400/PCBZ[1, 2] | | Interface Board | |
| ADIS16405BMLZ[1] | −40°C to +105°C | 24-Lead Module with Connector Interface | ML-24-2 |
| ADIS16405/PCBZ[1, 3] | | Interface Board | |

[1] Z = RoHS Compliant Part.
[2] This includes one ADIS16400BMLZ and an interface PCB.
[3] This includes one ADIS16405BMLZ and an interface PCB.

## NOTES

## NOTES

## NOTES

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