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Hardware User's Manual

# DBS 8700/8701

## VME/VXI Data Acquisition System

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Eight shielded, differential input ports are provided with both voltage and current protection. The DAS is directly expandable to 256 channels using the DVX family of multiplexer boards. The input port signals are multiplexed via an instrumentation amplifier (IA) and a programmable gain amplifier (PGA) with four software selectable gains (1, 2, 4 and 8) and then fed into a 400 kHz, 16-bit sampling A/D converter. The order of channels in the scan, the selected gain for each channel, the selected channel for data-dependent triggering as well as the sampling rate are user programmable.

The converted data is temporarily stored in a 1024 word deep FIFO. When the FIFO is half full, it signals the powerful dual-channel on-board DMA controller to acquire mastership of the bus. Then the DMA controller executes fast transfers over the VME bus sending data directly from the FIFO into the bus resident system memory until the FIFO is empty. The DMA controller automatically reads the necessary information regarding data set size and memory buffer areas from the bus resident memory relieving the controlling micro-processor of monitoring DMA operations.

Three flexible conversion trigger sources are available:

- An internal trigger derived from a precision clock with acquisition started by either the VMEbus resident host processor or the user supplied External Start command.
- A user supplied external trigger with acquisition started by either the VMEbus resident host processor or the user supplied External Start command.
- An internally- or externally-derived trigger with the acquisition started by the occurrence of a prespecified data dependent event on a selected channel.

An external precision clock can be fed into the board via the Front Panel EXT TRIG BNC connector or TTLTRG line 0, 1, 2 or 3. The TTLTRG line is program selectable using the Rate Register (See Section 5).

An external trigger can be fed to the DAS via the Front Panel EXT START BNC connector or TTLTRG line 4, 5, 6 or 7. The TTLTRG line is program selectable using the Rate Register (See Section 5).



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Upon contacting the Customer Service Office, the Service Coordinator will provide you with the following:

- ❑ Customer service order number (CSO)
- ❑ Warranty status of the units being returned
- ❑ Repair charge, if any

The CSO number is your authorization number. Please write this number on your purchase order and shipping label.

Send all authorized returns to:

Analogic Corporation
8 Centennial Drive
Peabody, MA 01960
Attn: Receiving Dock B.
CSO# _____

After the material has been returned, you will receive an acknowledgement copy of the CSO which will be marked with the scheduled return date.



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# Section 1
# Introduction

## 1.1 SCOPE OF MANUAL

This manual contains installation and operation information for the DBS 8700/8701 Data Acquisition System (DAS). The information is organized into the following sections:

Section 1, *Introduction,* describes the scope of this manual, the product, and how to obtain technical support if necessary.

Section 2, *Hardware Installation*, describes how to modify the jumper selectable features.

Section 3, *Software Installation*, details the installation of the driver on a Sun Microsystems workstation.

Section 4, *Programming*, contains the definitions of all the driver calls used to initiate the acquisition of data.

Section 5, *Functional Description*, is a detailed functional description of the cards and contains the necessary depth of information should a user choose to write his own driver.

Section 6, *Specifications*, contains a detailed list of performance specifications.

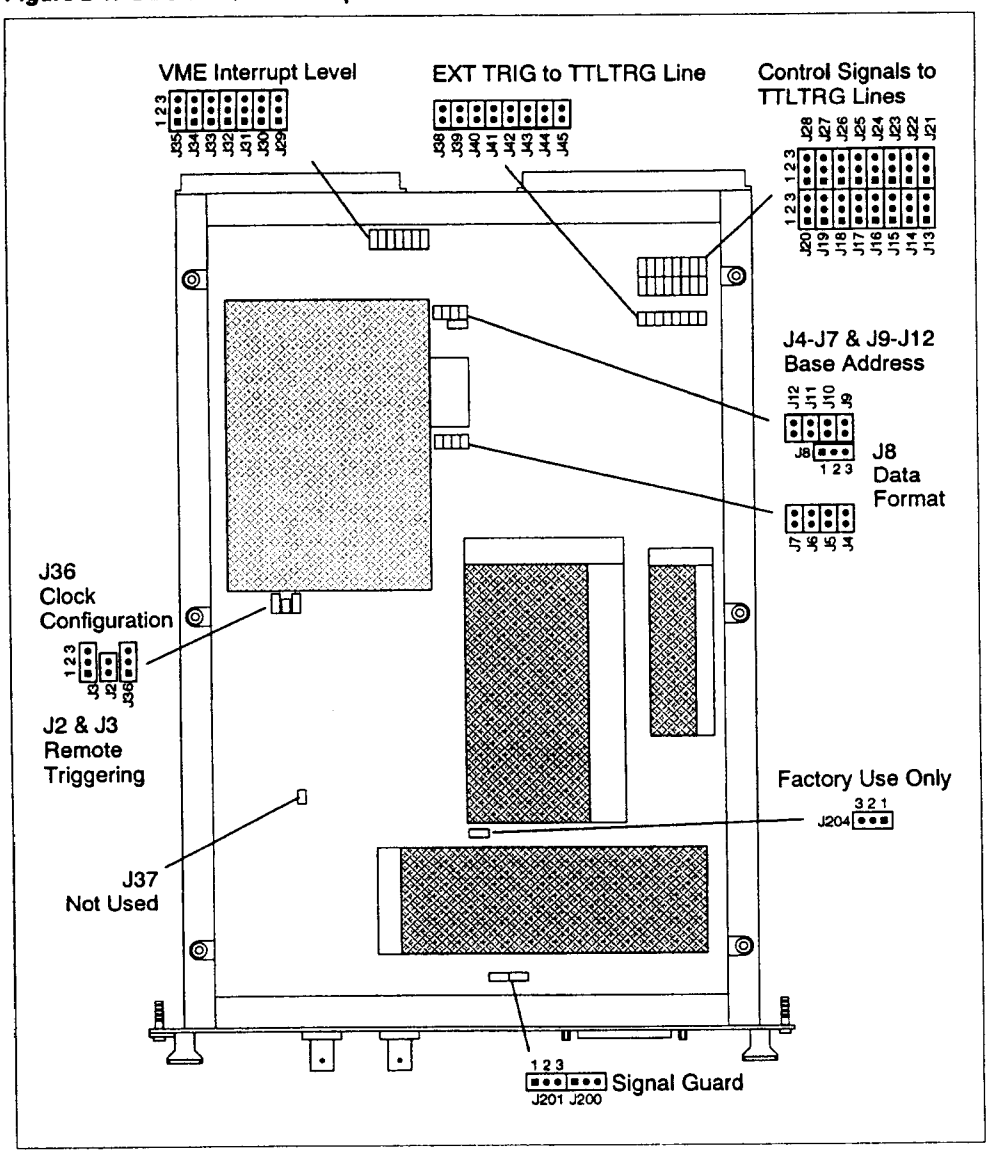
## 1.2 PRODUCT DESCRIPTION

The DBS 8700/8701 DAS is a 400 kHz, high resolution, multichannel data acquisition system combining precision measurement and high throughput in a VXI 'C' size format. Fully compatible with the VME specification Rev. C1 and the VXI specifications Rev. 1.4, the DAS occupies a single slot in a VME chassis and provides an unparalleled price-performance ratio when used either alone or in combination with other VME/VXI based boards (multiplexers, filters, digital-to-analog converters or array processors) in the DBS family of cards.



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**Figure 2-1. DBS 8700/8701 Jumper Selections**






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For ease of integration, a fully compatible UNIX (Berkeley 4.2)* software driver provides a set of high level routines for controlling the data acquisition.

## 1.3 TECHNICAL SUPPORT

If this product fails to operate upon arrival, contact your Analogic dealer or the Measurement and Control Division (MCD) at the Analogic factory in Peabody, MA 01960 to arrange for an exchange. Upon contacting MCD Order Entry, you will be given a Return Material Authorization (RMA) number.

To arrange for an exchange, contact MCD Order Entry:

Tel: (508) 977-3000, Ext. 3840 or 3844

FAX: (508) 977-6818

For technical assistance, contact MCD Applications Engineers:

Tel: (508) 977-3000
Domestic calls: Ext. 3876
International calls: Ext. 3011 or 3844

FAX: (508) 977-6814

To arrange for service, contact the Customer Service Office:

Tel: (508) 977-3000
Repairs: Ext. 3612
Parts: Ext. 3614

Before contacting the Customer Service Office, have the following information ready:

- ❑ Model number
- ❑ Serial number
- ❑ Purchase order number
- ❑ Quantity being returned
- ❑ A detailed description of the malfunction
- ❑ Your "Bill To" and "Ship To" addresses



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The external trigger signal is connected to the EXT START connector on the front panel. To use an external trigger input from the Front Panel or TTLTRG lines 4,5,6 or 7 (software-controlled selection), install J3-2 to J3-3.

Also, an external trigger from the Front Panel may be sent out on one of the TTLTRG lines using jumpers J38-J45. Refer to Section 2.2.6.

### 2.2.4 DAS Data Output Format

The output data format can be configured for Binary, Offset Binary or Two's Complement. The difference between Offset Binary (Table 2-2) and Two's Complement (Table 2-3) is that the MSB in Offset Binary is the complement of the MSB in 2's Complement.

To use Binary or Offset Binary, install J8-2 to J8-3. To use Two's Complement, install J8-1 to J8-2

**Table 2-2. Offset Binary Format**

| MSB | | | LSB | Value |
|---|---|---|---|---|
| 1111 | 1111 | 1111 | 1111 | + Full Scale |
| 1000 | 0000 | 0000 | 0001 | + 1 |
| 1000 | 0000 | 0000 | 0000 | Zero |
| 0111 | 1111 | 1111 | 1111 | – 1 |
| 0000 | 0000 | 0000 | 0000 | – Full Scale |

**Table 2-3. Two's Complement Format**

| MSB | | | LSB | Value |
|---|---|---|---|---|
| 0111 | 1111 | 1111 | 1111 | + Full Scale |
| 0000 | 0000 | 0000 | 0001 | + 1 |
| 0000 | 0000 | 0000 | 0000 | Zero |
| 1111 | 1111 | 1111 | 1111 | – 1 |
| 1000 | 0000 | 0000 | 0000 | – Full Scale |

### 2.2.5 VME Interrupt

Since the DAS requires a minimum of attention from the VME host processor after the necessary DMA transfer commands have been issued by the user's application program, there is little need to closely monitor the acquisition operation. Therefore, the DAS is shipped with interrupt level 1 selected, meaning that the only interrupt jumper



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# Section 2
# Hardware Installation

## 2.1 UNPACKING

Remove the DBS 8700/8701 Data Acquisition System (DAS) card from the carton and the anti-static bag, and visually inspect the assembly for any shipping damage. Retain the carton and packing. Should the DAS fail to function properly, contact Analogic Customer service (see Section 1.3) for return authorization. Any damage should be reported to the shipping company.

## 2.2 HARDWARE CONFIGURATION

The locations of the hardware jumpers that control the functional configuration of the board are shown in Figure 2-1. The board is shipped from the factory in the following configuration.

Base Address = C000 .....J4-J7 and J9-J12 installed
Internal Precision Clock .....J36 installed from 2-3
External Trigger Input.....J3 installed from 2-3
Two's Complement Data .....J8 installed from 1-2
Interrupt Level 1 .....J32 installed
Analog Ground Signal Guards .....J200 installed 2-3
ESTB on TTLTRG7 .....J21 installed 1-2
EXTSHL on TTLTRG4 .....J16 installed 2-3
EXTSH on TTLTRG5 .....J15 installed 1-2

The VXI specification requires a lock-out key on the front panel of a card that uses the A & C rows of pins on connector P2. This key prevents installing the DAS card adjacent to an incompatible VXI card that could cause electrical damage to the DAS. Since this DAS uses rows A & C on P2, it could be damaged if the backplane provides conflicting connections to other cards from these pins.

***CAUTION:*** ***Improper connection of signals on the P2 connector could cause damage to the DAS card.***



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### 2.2.7 *Remote Triggering*

In those installations where there are two to four DAS cards in the same chassis, you may wish to assign one card as "master" to trigger all the other DAS cards. In this case, the backplane of the applicable system must conform to the VXIbus specifications for interconnecting wiring between card slots.

***CAUTION:*** ***Failure to comply with the VXIbus electrical specifications may result in damage to, or unreliable operation of, the DAS (and the companion cards).***

In this case, the "master" trigger card should be configured to generate the Remote Trigger (REMTRG) pulse while the "slave" card(s) should be configured to receive it. The REMTRG signal must then be jumpered to one of the TTLTRG lines on the P2 connector (see Table 2-5). Jumpers selections on the Master and Slave card(s) are defined in Table 2-6.

**Table 2-6. Master/Slave Jumper Selections**

| Jumper | Master | Slave(s) |
|---|---|---|
| J2 | 1-2 | – |
| J3 | 1-2 | 1-2 |
| J21 - J28 | 2-3 | 2-3 |

### 2.2.8 *Analog Signal Guard*

The analog signal guards (shields) for all channels are connected together to jumpers J200 & J201. Refer to Table 2-7 and Figure 2-1 for jumper selections.

**Table 2-7. Analog Signal Guard Jumper Selections**

| Jumper Selection | Shield Connection |
|---|---|
| J201-1 to J201 - 2 | Digital ground from VME backplane |
| J200-1 to J200-2 | Chassis ground via front panel card cage screws |
| J200-2 to J200 - 3 | Analog ground |



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### 2.2.1 VME Slave Address

The Base Address of the board is determined by the installation of jumpers J4-J7 and J9-J12. The examples given in Table 2-1 illustrate the base address range. Any 64 byte block of addresses from FFC0 thru C000 can be configured.

**Table 2-1. Base Address Jumper Selection Examples**

| Address | J9 | J10 | J12 | J11 | J7 | J6 | J5 | J4 |
|---|---|---|---|---|---|---|---|---|
| FFC0 | OUT | OUT | OUT | OUT | OUT | OUT | OUT | OUT |
| FF80 | OUT | OUT | OUT | OUT | OUT | OUT | OUT | IN |
| FF00 | OUT | OUT | OUT | OUT | OUT | OUT | IN | IN |
| FE00 | OUT | OUT | OUT | OUT | OUT | IN | IN | IN |
| FC00 | OUT | OUT | OUT | OUT | IN | IN | IN | IN |
| F800 | OUT | OUT | OUT | IN | IN | IN | IN | IN |
| F000 | OUT | OUT | IN | IN | IN | IN | IN | IN |
| E000 | OUT | IN | IN | IN | IN | IN | IN | IN |
| C000 | IN | IN | IN | IN | IN | IN | IN | IN |

### 2.2.2 Internal/External Clock

The DAS provides a precision 3.6864 MHz clock (±0.001%) for use as the sampling clock. However, you may wish to use an external precision clock and divide it down to the desired sample rate. The external clock signal is connected to the EXT TRIG connector on the front panel. See Section 2.3.2.

To use an external precision clock from the Front Panel EXT TRIG input, install J36-1 to J36-2

To use the on-board precision clock or a precision clock input from TTLTRG lines 0, 1, 2 or 3 (software-controlled selection), install J36-2 to J36-3

### 2.2.3 Internal/External Trigger

The user may wish to trigger the conversion from an external source rather than use either of the options above. The external trigger initiates the actual sampling of the input analog signal(s) but the internal precision clock is required to run the internal A/D controls.

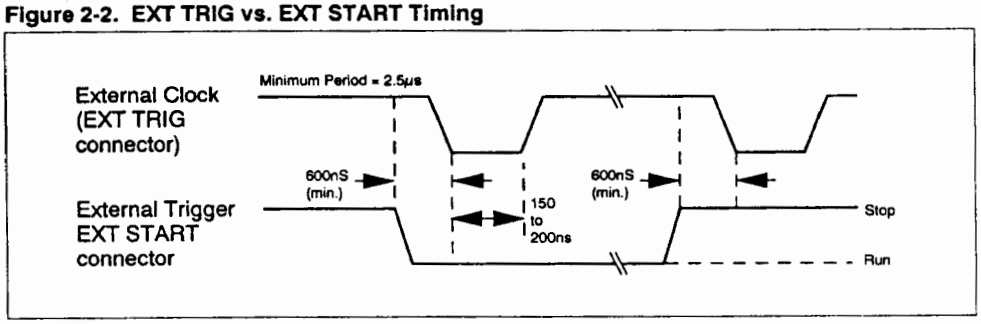


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The External Trigger, when enabled by its Control Register enable bit, starts or stops the ADC sampling. When the internal precision clock is used, the External Trigger is synchronized with the precision clock. If the External Trigger is used to trigger the ADC, it is up to the user to synchronize the External Trigger with the External Clock.

These two signals are independent of one another such that the trigger can be used either with the internal precision clock (internally synchronized) or the external clock (user synchronized). Figure 2-2 depicts the necessary user synchronization of the Ext.Start and the Ext. Trigger, when both are provided by the user.

**Figure 2-2. EXT TRIG vs. EXT START Timing**




## 2.4 VMEBUS BACKPLANE CONNECTIONS

### 2.4.1 BUS Grant In/Out Backplane Jumpers

The DAS uses only bus request BR3* for requesting VMEbus ownership. Therefore, the BG3IN-BG30UT bypass jumper (or switch) located in the backplane for the slot that the DAS occupies must be removed (open).

The bus grants BG0IN, BG1IN, BG2IN, are shorted through to the BG0OUT, BG10UT, BG20UT pins on the P1 connector.

### 2.4.2 IACKIN/IACKOUT Backplane Jumper

The DAS requires that the IACKIN-IACKOUT jumper (or switch) located in the backplane of the slot that the DAS occupies must be removed (open).



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installed is J32. To assign the DAS to another interrupt level, the BREQ_INT PAL (Z-14) must be reprogrammed for the desired level and the interrupt jumper (J32) must be moved to the new level. A copy of the BREQ_INT PAL equations is included with the Operating System Driver. Jumper selections are listed in Table 2-4.

**Table 2-4. Interrupt Level Selections**

| Interrupt level | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| Jumper Installed | J32 | J31 | J30 | J29 | J33 | J34 | J35 |

### 2.2.6 *TTLTRG Jumpers*

When other cards in the DBS family are used in conjunction with the DAS, the backplane of the applicable system must conform to the VXIbus specifications for interconnecting wiring between card slots.

***CAUTION:*** ***The DAS uses rows A & C on the P2 connector. Improper connection of signals on the P2 connector could cause damage to the DAS card. Failure to comply with the VXIbus electrical specifications may result in damage to, or unreliable operation of, the DAS (and companion cards).***

If a companion card is used with the DAS, TTLTRG jumpers are required to pass high speed control signals to the other cards. An extensive jumper field has been provided in conformance to the VXI bus specification. The signals that can be connected to the TTLTRG lines are listed in Table 2-5.

**Table 2-5. TTLTRG Jumpers for Control Signals**

| | TTLTRG– Jumper Connection | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Control Signal | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REMTRG Remote Trigger | J21 2-3 | J22 2-3 | J23 2-3 | J24 2-3 | J25 2-3 | J26 2-3 | J27 2-3 | J28 2-3 |
| ESTB External Strobe | J21 1-2 | J22 1-2 | J23 1-2 | J24 1-2 | J25 1-2 | J26 1-2 | J27 1-2 | J28 1-2 |
| EXTSHL External S/H (LO) | J13 2-3 | J14 2-3 | J15 2-3 | J16 2-3 | J17 2-3 | J18 2-3 | J19 2-3 | J20 2-3 |
| EXTSH External S/H (HI) | J13 1-2 | J14 1-2 | J15 1-2 | J16 1-2 | J17 1-2 | J18 1-2 | J19 1-2 | J20 1-2 |
| EXTRG External Trigger | J45 1-2 | J44 1-2 | J43 1-2 | J42 1-2 | J41 1-2 | J40 1-2 | J39 1-2 | J38 1-2 |



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## 3.2 INSTALLATION PROCEDURE

**Step 1** Copy the contents of the DVX/UNX release tape to the directory'/usr/sys/sundev' using the following command:

```
tar -xfr/dev/rs0<cr>
```

**Step 2** Insert the following section near the top of the file:

```
'/usr/sys/sun/conf.c'
```

```
#include "DVX/dvx.h"
#if NDVX > 0
int dvxopen ( ), dvxclose( ), dvxstrategy( ),
dvxread( ), dvxwrite( );
int dvxioctl( );
#else
#define     dvxopen         nodev
#define     dvxclose        nodev
#define     dvxstrategy     nodev
#define     dvxread         nodev
#define     dvxwrite        nodev
#define     dvioctl         nodev
#endif
```

Insert the following section in the Character Device switch table in any free device number location:

```
{
dvxopen, dvxclose, dvxread, dvxwrite, /*nn*/
dvxioctl, nodev, seltrue, 0,
0,
}
```

Make note of the number "nn" in the right hand column for you will need it later.



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## 2.3 EXTERNAL SIGNAL INPUT

### 2.3.1 Analog Signals

Analog signals should be brought to the DAS via twisted shielded pairs. The signal conductors and the shield drain wires should be connected according to Table 2-8. It is recommended that a metal-back shell be used with the standard D type 25 pin male connector. Suggested components are as follows:

- ITT Cannon DB-25P or TRW-Cinch DB25P 25 pin D type connector
- AMP #745833-1 metallic backshell
- Belden #8761 twin conductor shielded cable

**Table 2-8. Analog Signal Input Connections**

| | Connector Pin No. | | |
|---|---|---|---|
| Port | + IN | - IN | Guard |
| 0 | 8 | 7 | 9 |
| 1 | 19 | 18 | 17 |
| 2 | 11 | 10 | 12 |
| 3 | 16 | 15 | 14 |
| 4 | 24 | 25 | 23 |
| 5 | 1 | 2 | 3 |
| 6 | 22 | 21 | 20 |
| 7 | 4 | 5 | 6 |

### 2.3.2 Digital Signals

The DAS accepts either an external clock input (EXT TRIG) or an external trigger input (EXT START) via the front panel BNC connectors. Both inputs are terminated in 50 ohms.

The External Clock, when enabled by the enable bit in the Control Register, directly triggers the ADC. By means of a hardware jumper, the External Clock input can be substituted for the internal precision clock. For those sampling frequencies not available from the on-board precision clock and frequency divider, the external clock may be used. In such cases, the clock must have a 50% duty cycle.



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**Step 5** Run the 'config' utility to generate the necessary configuration data for the new kernel. For instance 'config DVX' builds the required configuration and places them in the file,

```
/usr/sys/sun3/DVX
```

**Step 6** Change directory to "/usr/sys/sun3/DVX" and type 'make' to build your new kernel. When 'make' has finished, change directory to the root and make a backup copy of the original "vmunix"; copy the new kernel into the root directory and reboot the system.

Observe the system messages,

```
'dvxm0 at vme24d16 xxxx'
```

and

```
'dvx0 at mve16d16 xxxx vec xxxx'
```

These indicate that the system has identified the DAS hardware. The driver will turn the PASS/FAIL light on the DAS to green if the startup diagnostics have passed.

If the driver does NOT detect the DAS card, then the only message displayed will be 'dvxm0 at vme24d16xxxx'.

**Step 7** Before using the driver, a device file must be created in the '/dev' directory for the DAS using the 'mknod' utility. For instance the command 'mknod /dev/dvx0 c nn 0' will create the device file 'dvx0' with a major device number of [nn]. Note that the device number used must correspond with the entry "nn" used in the character device table in 'conf.c' (Step 2). User applications access the device via an 'open' call to the appropriate device file.



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# Section 3
# Software Installation

## 3.1 INTRODUCTION

The DAS software is a UNIX device driver (based upon the Berkley Version 4.2) supplied in source file format. Installation of the software requires the reconfiguration of the UNIX kernel as described in the following paragraphs.

Figure 3-1 shows a typical directory configuration and shows at which level in the structure each step in the following paragaphs takes place. It also shows where certain files referred to in the test are located.

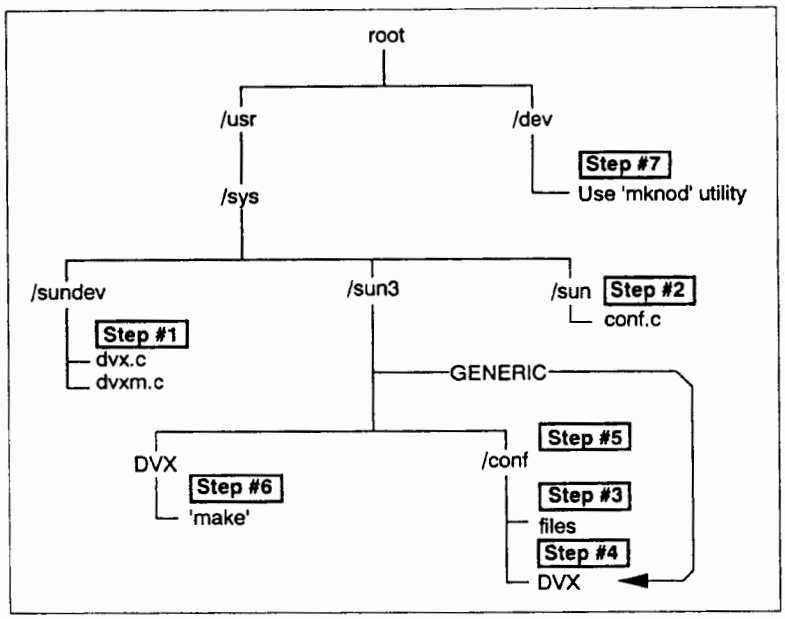



**Figure 3-1. Typical Directory Tree**



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In keeping with Unix driver conventions, all control and setup functions map to subfunctions of the Unix 'IOCTL' system call with the exception of the loading of the Sequence RAM which maps to the 'WRITE' function. The actual acquisition of data from the device is accomplished by the 'READ' Unix system call.

To program the DAS for data acquisition, follow these simple steps:

(1) Use 'OPEN' to establish communication with the device.

(2) Use 'WRITE' to specify a channel/gain sampling sequence.

(3) Use a series of 'IOCTL' calls to specify the setup configuration.

(4) Use 'READ' to acquire the data into a user buffer.

Any setup specified in steps 1, 2, and 3 will remain valid until the device is released or explicitly changed by the application.

## 4.2 DEFAULT DEVICE CONFIGURATION

When the DAS is 'opened' by the host application, the DAS default configuration is as follows:

Sampling Rate Divisor ..... 3 (1024 kHz sampling rate)

Start Mode ..... Internal

Trigger Mode ..... Internal

Trigger Threshold ..... 0

Trigger Polarity ..... Negative

Timeout for Data Acquisition ..... Infinite

Internal Threshold Triggering ..... Disabled

Ch./Gain Sequence RAM Contents ..... Non-initialize (User must specify a channel/gain sequence to the driver.)

Pre-Trigger Buffer size ..... 0

## 4.3 DRIVER FUNCTION DESCRIPTIONS

The paragraphs below describe each DAS driver call in detail. The calling convention, parameters, and returned status conform to the standard Unix protocol but are listed for completeness.



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**Step 3** Add the following lines to "/usr/sys/sun3/conf/" files:

```
/usr/sys/sundev/dvx.c        optional dvx
                             device-driver

/usr/sys/sundev/dvxm.c       optional dvxm
                             device-driver
```

The file'dvx.c' is the actual driver source code, while the file 'dvxm.c' is a dummy driver used only to allocate memory in VME A24D16 space.

**Step 4** Change directory to "/usr/sys/sun3/conf" and copy the file "GENERIC" to the file you wish to use for the DAS configuration data base. Add in the following lines to this file:

```
device dvxm0 at vme24d16? csr 0x800000

device dvx0 at vme16d16 ? csr 0xc000 flags
0x800000 priority 1\vector dvxintr 0xc8
```

These lines define the particular device hardware configuration to the system by specifying the base address of the board in the appropriate VME address space, the interrupt priority, and the interrupt vector.

The line for 'dvxm0' allocates system memory in VME A24D16 address space for the Scan Sequence RAM; note that the 'flags' parameter in the line for "dvx0' must match the address specified for 'dvxm0'.

The line for device 'dvx0' specified a DAS base address of 0xffc000, an interrupt priority of one, and an interrupt vector of 0xc8; refer to the Hardware Installation Manual if the default settings are not desirable.

Ensure that the addresses and interrupt vectors specified for the DAS do not conflict with those of other devices. Before moving on, check that the CSR address (0xc000), the interrupt vector (0xc8), and the physical location of the Sequence RAM memory (0x800000) are NOT used by any other device listed in this file.



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Each channel to be specified will have one entry in the 'SeqRam' array. The 'Channel' field specifies the channel number to be sampled, the 'Gain' field specifies the gain (1,2,4,8) for that channel, and the 'Trigger' field enables or disables internal threshold triggering on the channel. A one in the 'Trigger' field enables threshold triggering on that specific channel, while a zero disables threshold triggering. Note that only one channel in a sampling sequence may be selected for triggering.

The 'count' parameter indicates to the driver the number of channels specified in the 'SeqRam' array.

The 'WRITE' function returns a zero value if successful and a negative value if loading the sequence RAM failed. Causes for failure include specifying threshold triggering on more than one channel, or exhausting the physical capacity of the sequence RAM.

### 4.3.4 READ (FID, BUFFER, COUNT)

The "READ" call starts the acquisition process with previously loaded setup values.

The "fid" field is the "file id" returned from a prior call to the "open" routine.

The "buffer" field is a pointer to an array which receives the data from the DAS. NOTE THAT THE USER BUFFER MUST BE AT LEAST 64 BYTES LONG. Failure to assure this condition is met, may lead to fatal system failures.

The "count" field specifies the total number of bytes to acquire which is two times the number of 16-bit data words desired.

The "READ" driver routine returns a zero value if successful or a negative value if an error was encountered. Common causes for an acquisition failure include FIFO overflow, or the timeout limit for data acquisition expired before all the data was acquired.

### 4.3.5 IOCTL (FID, CMD, DATA, FLAG)

The 'IOCTL' driver routine supports a variety of control and diagnostic functions which are discussed separately below. As with the



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# Section 4
# Programming

## 4.1 PROGRAMMING OVERVIEW

The Unix device driver enables the host application to configure the hardware and acquire data directly into user process buffers using the DAS on-board DMA controller. Additionally, upon request from the main program, the driver can perform a diagnostic check of the hardware and report the status. All DAS control, acquisition, and diagnostic functions are accessed by the application through standard Unix system calls: 'READ', 'WRITE', and 'IOCTL'.

Table 4-1 lists the DAS Unix driver calls and functions.

**Table 4-1. DAS UNIX Drivers**

| Driver | Hardware Function |
|---|---|
| OPEN | Allocate the device and establish communication |
| CLOSE | Release the device |
| WRITE | Initialize the DAS Channel/Gain Sequence RAM |
| READ | Acquire data from the DAS using DMA |
| IOCTL | Perform Diagnostic Self Test<br>DAS Hardware Reset<br>Set Sampling Rate Divisor<br>Read Sequence RAM<br>Set Start Mode (internal/external)<br>Set Trigger Threshold<br>Set Trigger Source (external/internal)<br>Set Trigger Polarity<br>Set Data Acquisition Timeout<br>Return Last DAS Specific Error Code<br>Set Trigger Mode ( Normal, Post-, Pre-/Post-)<br>Set Input Signal Type<br>Read A DAS Hardware Register<br>Write A DAS Hardware Register<br>Return Diagnostic Status<br>Set Pre-Trigger Buffer Size |



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#### 4.3.5.6 GET_DIAG_ERROR

The IOCTL GET__DIAG__ERROR returns the last diagnostic status code in the data parameter.

#### 4.3.5.7 THRESHOLD

The THRESHOLD command loads the DAS threshold register with the trigger threshold value contained in the data parameter. An error is returned if the threshold value is greater than six bits.

#### 4.3.5.8 TRIGGER_POLARITY

The IOCTL TRIGGER__POLARITY command sets/clears the polarity bit in the DAS threshold register. A non-zero value sets the bit while a zero value clears the bit. A one specifies positive edge triggering while a zero specifies negative edge triggering.

#### 4.3.5.9 READ_SRAM

The IOCTL READ__SRAM command returns up to 64 bytes of sequence RAM data to the user and is primarily used for diagnostics. The flag parameter specifies which block of 64 bytes of sequence RAM is returned(0 - 31). The base address of the sequence RAM to be read is calculated as 'flag * 64 .' An error is returned if the specified flag value is greater than 31.

#### 4.3.5.10 TIMEOUT

The IOCTL TIMEOUT command sets the timeout limit for data acquisitions in seconds. The value is passed in the data parameter.

#### 4.3.5.11 GET_ERROR

The IOCTL GET__ERROR command returns a device specific error number which can be interpreted from the error codes supplied in the include file 'dvx2502io.h'. The user should make this call after a negative value is returned from an open, write, read, or ioctl call to obtain the specific cause of the error.

#### 4.3.5.12 PRE_POST_TRIGGER

The IOCTL PRE__POST__TRIGGER command sets the data collection mode for internal threshold triggering. A zero for the



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### 4.3.1 OPEN (DEV, FLAG)

The 'OPEN' entry point verifies that the device is physically present in the system; if the device is present the driver attempts to allocate the device to the user and initialize the hardware. If the device is not in the system or another user is currently using the device a [-1] will be returned. Note that the device must first be 'opened' by the user before any subsequent communication can take place.

The 'dev' parameter is a character string which specifies the device file name in the /dev subdirectory of the root. Ask the system manager for the assigned device name or refer to the DAS Unix Driver Installation in Section 3.0 for more detail.

The 'flag' parameter specifies the attributes with which the device should be opened; for the DAS the flag parameter should indicate read/write attributes (the O__RDWR flag defined in the system include files).

If the call to the open routine was successful the driver will return an integer greater than zero which will be used as the 'file id' parameter in subsequent calls to the driver.

### 4.3.2 CLOSE (FID)

CLOSE deallocates a previously opened DAS device. The 'fid' parameter is the 'file id' returned from a prior open statement.

### 4.3.3 WRITE (FID, BUFFER, COUNT)

The 'WRITE' procedure will load the scan sequence RAM with a user supplied channel/gain sequence. The user must specify a channel/gain sequence to the driver prior to initiating an acquisition.

The 'fid' parameter is an integer 'file id' obtained by a previous call to the 'OPEN' routine. The 'buffer' parameter is a pointer to an array of structure of type 'SeqRam'.The structure, defined in the included module 'dvx2502io.h', is as follows:

```
struct SeqRam{short Channel;  /*channel number (0–255)*/
       short Gain;            /*gain (1, 2, 4, 8)*/
       short Trigger;         /*trigger control (1=trigger)*/
       }
```



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## 4.4 ERROR HANDLING

Driver error conditions will be flagged by returning a negative number from any of the system calls. The following errors are logically defined in the include file 'dvx2502io.h":

a.) Device not present
b.) Other user owns device
c.) Attempt to write more than 2048 bytes to sequence RAM
d.) Unexpected interrupt
e.) FIFO overflow
f.) Power-on test failure
g.) Invalid channel number
h.) Invalid gain (only one gain per acquisition
i.) Invalid rate divisor
j.) Device timeout
k.) Invalid device model number
l.) Cannot access sequence RAM
m.) Invalid threshold value
n.) Attempt to assign trigger to multiple channels
o.) See dvx2502io.h for the complete list of error codes.

## 4.5 DATA ACQUISITION EXAMPLES

### 4.5.1 Simple Acquisition

This example shows the ease of setting up a simple acquisition and averaging the data set. The user is prompted to enter the number of channels and the number of samples per channel and to select the type of input signal. This information plus the control parameters are downloaded into the DAS. Acquisition is then started and the acquired data is scaled and the average is computed.



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other driver routines the 'fid' parameter is an integer containing the file identifier for the device. The 'cmd' indicates to the driver the particular IOCTL' function being requested by the user; the include file 'dvx2502io.h' contains the valid subfunction codes for the DAS driver. The 'data' and 'flag' parameters are interpreted differently for each driver subfunction.

#### 4.3.5.1 RESET

The IOCTL RESET command sets the RESET bit in the control/ status register and waits 2 seconds for the bit to clear. If the bit is not clear after 2 seconds or if the power-on test bit is 0, an error is returned. The data parameter is ignored for this function.

#### 4.3.5.2 RATE_DIVISOR

The IOCTL RATE__DIVISOR command loads the DAS rate divisor register with a user specified divisor. The data parameter contains the desired rate. If the specified rate divisor is greater than the allowable 10-bit value, an error is returned in the user structure.

#### 4.3.5.3 CLOCK_SOURCE

The IOCTL CLOCK__SOURCE command sets/clears the external clock select bit in the DAS CSR according to the value passed in the data parameter. A non-zero value sets the bit while a zero value clears the bit. A one in this word specifies an external clock source.

#### 4.3.5.4 START_MODE

The IOCTL START__MODE command sets/clears the external start bit in the DAS CSR according to the value passed in the data parameter. A non-zero value sets the external start bit to a one while a zero value clears the bit. A one in this word selects an external start signal.

#### 4.3.5.5 RUN_AD_DIAGS

The IOCTL RUN__AD__DIAGS command initiates a diagnostic self test of the DAS hardware. If the tests pass, a zero is returned in the 'data' parameter, otherwise a non-zero diagnostic error code is returned. Diagnostic error codes are defined in the include file 'dvx2502io.h'.



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```
{
      printf("\nERROR: sample size too big");
      exit(0);
}

      /*SPECIFY SIGNAL INPUT TYPE*/
printf("\n\ t1 = Normal Input");
printf("\n\ t2 = Grounded Input");
printf("\n\ t3 = Positive Reference");
printf("\n\ t4 = Negative Reference");
printf("\n\ tEnter Signal Type:");
scanf("%d",&sigtype);

/*
* SETUP SAMPLING SEQUENCE STRUCTURE FOR THE WRITE TO SRAM
*/

for(i = 0;i < NCHAN;i + + )
{
      SeqRam[i].Channel=i;
      SeqRam[i].Gain=1;      /*only one gain per acquisition*/
      SeqRam[i].Trigger=0;
}

/*
*OPEN THE DEVICE
*/
fid = open("/dev/av0", O__RDWR);
if (fid = = -1 ) {
      printf("ERROR %4d, cannot open the device \ n",errno);
      /*get device specific error*/
      exit(0);
}
/*
* WRITE THE SRAM SAMPLING SEQUENCE AND GAINS
*/
if (write(fid,(char*)SeqRam, sizeof(struct SeqRam)*NCHAN)= = -1)
```



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'data' parameter specifies post trigger data collection only, while a non-zero value specifies both pre- and post-data collection. No error codes are returned.

#### 4.3.5.13 THRESHOLD_TRIG

The IOCTL THRESHOLD__TRIG command enables or disables internal threshold triggering. A zero in the 'data' parameter disables triggering, while a non-zero value enables triggering. No error codes are returned.

#### 4.3.5.14 PRE_TRIG_BUF_SZ

The IOCTL PRE__TRIG__BUF__SZ command sets the PreTrigger buffer size for threshold triggered acquisitions. Buffer size, expressed in 16-bit words, is user-supplied in the 'data' parameter.

#### 4.3.5.15 SET_SIGNAL_TYPE

The IOCTL SET__SIGNAL__TYPE command allows the user to ground the input to the input buffer, apply a positive or negative voltage reference to the input buffer, or allow the signal at the input connector to pass through the input multiplexer to the input buffer. The 'data' parameter specifies the input type; the include file 'dvx2502io.h' defines values for valid input signal types. An error is returned if the signal type specification is not defined.

#### 4.3.5.16 READ_REG

The IOCTL READ__REG command allows the user to read any DAS register. The 'flag' parameter specifies the register to be read and the 'data' parameter is a pointer to a user variable which receives the data. The include file 'dvx2502io.h' logically defines the valid register assignments. An error is returned if the register to be read is not defined.

#### 4.3.5.17 WRITE_REG

The IOCTL WRITE__REG command allows the user to write data to any DAS register. As with the READ__REG command, the 'flag' parameter specifies the register to be read. An error is returned if the register to be written is not defined.



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```
      /* CONVERT LEVELS TO VOLTAGE AND AVERAGE */
for (i = 0;i < NCHAN;i + + )
{
      avgvolts[i] = 0.;
      for(j = 0;j < samp;j + + ) avgvolts[i] + =
(float)dvxdata[i +j*NCHAN];
      avgvolts[i] /= (float)samp;
      avgvolts[i]* = SCALE;
}

for(i = 0;i < NCHAN;i + + )
      printf(" \ nAverage Voltage Channel %3d = %7.6f
",i,avgvolts[i]);

close(fid);
}
```

### 4.5.2 Pre/Post Data Acquisition

In this example, the user is prompted for the number of samples to acquire. Channels #2 and #3, each with a gain of 1, will be scanned continuously and the results stored in the Pre-trigger buffer. Data from channel #2 will be monitored, and when the converted value crosses the threshold of +3/16 of full scale in the positive direction, the DMAC will store all subsequent data points in the Post-trigger buffer. The Pre-trigger data buffer will be half of the total number of samples. The scan sequence will be downloaded along with the sampling rate and the threshold value, and the acquisition will be started. When the voltage on channel #2 increases across the threshold and the Post-trigger buffer is filled, the data will be scaled, the pretrigger data concatenated with the post-trigger data and the values displayed.

```
/* PRE/POST DATA ACQUISITION PROGRAM USING THE DAS A/D */
#include <sys/file.h>
#include "dvx2502io.h"
#define SCALE (20./65536.) /*converter level to voltage scale
                            factor*/
#define MAX __ SAMPLES 16384
```



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```
/*•
*SIMPLE DATA ACQUISITION PROGRAM USING THE *DVX2503/DBS8701 A/D
*/
#include <sys/file.h>
   #include "dvx2502io.h"        /*DAS I/O definitions */
   #define MAX__SAMPLES 16384
   #define SCALE (20./65536.)    /*converter level to voltage
                                 scale fact or */

main( )
{
int i,j,k;
int fid;
int sigtype,NCHAN;
extern int errno;
int averr;
int rate;
int thres;
struct SeqRam SeqRam[8];
short dvxdata[MAX __ SAMPLES];
int tsamp,samp;
float avgvolts[8];

      /* NUMBER OF CHANNELS TO SAMPLE */
printf("\n\ tEnter Number of Channels:");
scanf("%d",&NCHAN);
if (NCHAN >8) {
   printf("\nMax. number of channels is 8");
exit(0);
   }
      /* NUMBER OF SAMPLES PER CHANNEL */
printf("\n\ tEnter Number of Samples per Channel:");
scanf("%d",&samp);

tsamp = samp*NCHAN;     /* total number of samples */

if (tsamp > MAX__SAMPLES)
```



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```
/* OPEN THE DEVICE */
fid = open("/dev/avO", O__RDWR);
if(fid == -1){
      printf("ERROR %4d, cannot open the device \ n",errno);
/* get device specific error */
exit(0);
}

/* WRITE THE SRAM */
printf(" \ nSetting up SRAM");
if ( write(fid,(char *)SeqRam, sizeof(struct SeqRam)*2) = = - 1)
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVlCE ERROR %3d \ n",averr); exit(0);
}

/* SET THE RATE REGISTER */
rate = 1000;/* divide by 1000 */
printf("\nSetting up rate divisor");
if (ioctl(fid,RATE __ DlVlSOR,&rate,0) = = - 1)
{
      ioctl(fid,GET __ ERROR,&averr,0);
      printf("DEVlCE ERROR %3d \ n",averr); exit(0);
}

/* SELECT TRIGGER POLARITY AS POSITIVE */
i=1;
printf(" \ nSetting up trigger polarity");
if (ioctl(fid,TRlGGER __ POLARlTY,&i,0) = = - 1)
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVlCE ERROR %3d \ n",averr);
exit(0);
}
/* ENABLE THRESHOLD TRIGGERING */
printf(" \ nEnabling threshold triggering");
if (ioctl(fid,THRESHOLD __ TRlG,&i,0) = = - 1)
```



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```
{
      ioctl(fid,GET__ERROR,&averr,0);
      printf("DEVlCE ERROR %3d\n",averr);
      exit(0);
}


/*
*SET THE RATE REGISTER
*/
rate = 3;   /* divide by 3 */
if (ioctl(fid,RATE__DIVISOR,&rate,0) = = -1)
{
      ioctl(fid,GET_ ERROR,&averr,0);
      printf("DEVlCE ERROR %3d\n",averr);
      exit(0);
}
/*
* SELECT INPUT SIGNAL TYPE
*/
if (ioctl(fid,SET_SIGNAL_TYPE,&sigtype,0) = = - 1)
{
      ioctl(fid,GET_ERROR,&averr,0);
      printf("DEVlCE ERROR %3d\n",averr);
      exit(0);
}
/*
* GET SOME DATA
*/
if (read(fid,(char *)dvxdata,tsamp< <1) = = - 1)
{
      ioctl(fid,GET_ERROR,&averr,0);
      printf("DEVlCE ERROR %3d \ n",averr);
      exit(0);
}
```



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```
/* PRETRIGGER DATA */
for(i=0;i<(tsamp>>1);i+ =2)
printf("\n PreTrigger Data Chan[%1d] %4.3f Chan[%1d] %4. 3f",
CHAN1,volts[i],CHAN2,volts[i + 1]);

/* POSTTRIGGER DATA */
for(i = (tsamp> >1);i <tsamp;i + = 2)
printf("\n PostTrigger Data Chan[%1d] %4.3f Chan[%1d] %4 .3f",
CHAN1,volts[i + 1],CHAN2,volts[i]);
close(fid);
}
```



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```
#define CHAN1 2   /* define channels to use */
#define CHAN2 3   /*    ......*/
main( )
{
int i,j,k;
int fid;
extern int errno;
int averr;
int rate;
int thres;
struct SeqRam SeqRam[8];
short dvxdata[MAX __ SAMPLES];
int tsamp,samp;
int offset;
float volts[MAX __ SAMPLES];

/* NUMBER OF SAMPLES PER CHANNEL */
printf("\n\ tEnter Number of Samples per Channel:");
scanf("%d",&samp);

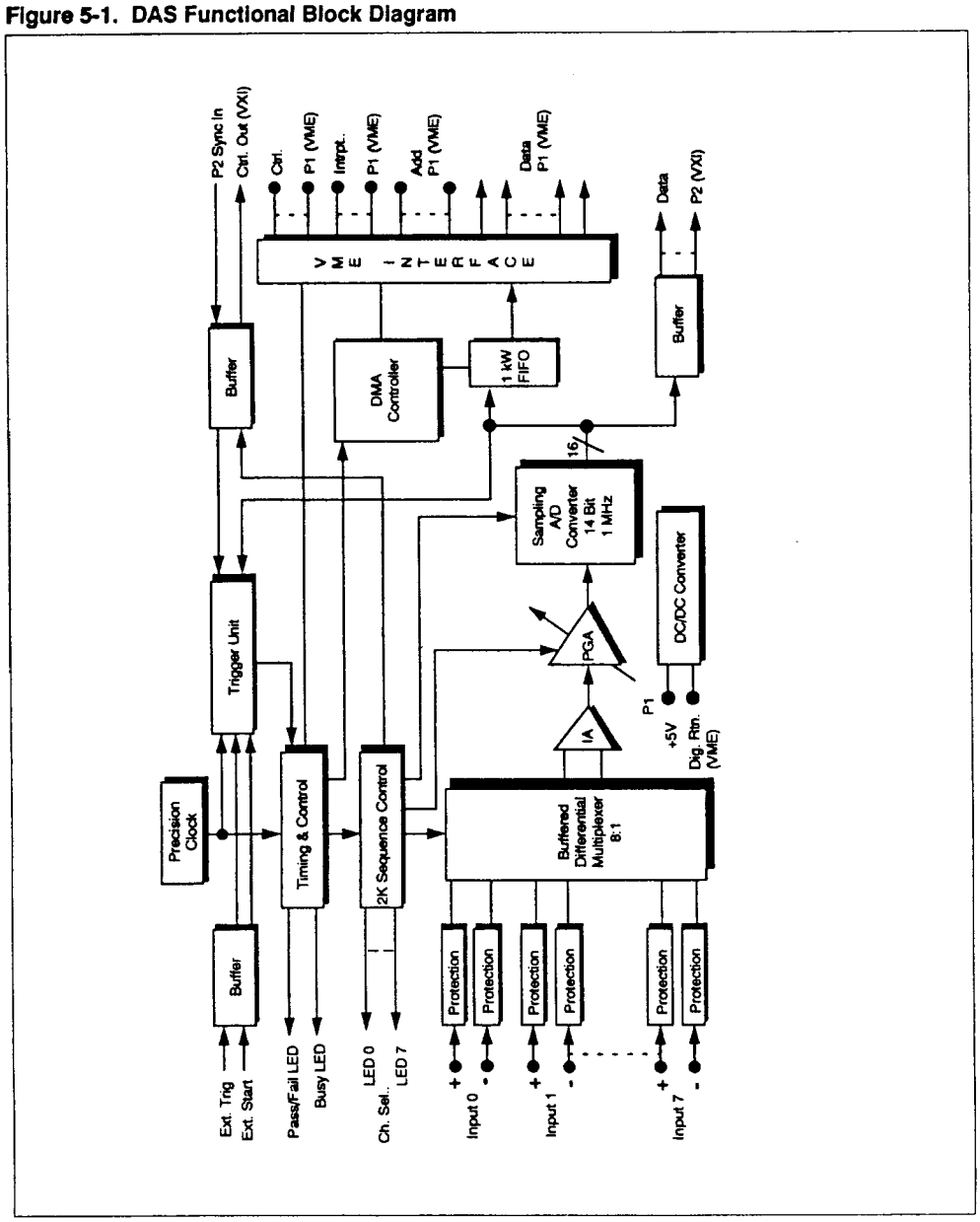

/* total number of samples (we use 2 channels)*/


/* SETUP SAMPLING SEQUENCE STRUCTURE FOR THE
* WRITE TO SRAM
*Two channels are used with triggering enabled on the
* 1st channel
*/
SeqRam[0].Channel = CHAN1;
SeqRam[0].Gain = 1;     /*only one gain per acquisition*/
SeqRam[0].Trigger = 1;  /* enable trigger */
SeqRam[1].Channel = CHAN2;
SeqRam[1].Gain = 1;
SeqRam[1].Trigger = 0;
```



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**Figure 5-1. DAS Functional Block Diagram**






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```
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVlCE ERROR %3d \ n",averr);
exit(0);
}
/* SET THE TRIGGER THRESHOLD */
i = 3d; /* 2's complement of +3/16 F.S. */
printf(" \ nSetting trigger threshold");
if (ioctl(fid,THRESHOLD __ TRlG,&i,0) = = - 1)
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVlCE ERROR %3d \ n",averr);
exit(0);
}
/* SET THE PRETRIGGER BUFFER SIZE TO 1/2 TOTAL No. OF SAMPLES */
i = tsamp>>1;
printf(" \ nSetting PreTrigger buffer size");
if (ioctl(fid,PRE __ TRIG __ BUF __ SZ,&i,0) = = - 1)
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVlCE ERROR %3d \ n",averr);
exit(0);
}

/* GET SOME DATA */
printf(" \ nWAlTlNG for TRIGGER");
if ( read(fid,(char *)dvxdata,tsamp< <1) = = - 1 )
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVlCE ERROR %3d \ n",averr);
exit(0);
}

/* CONVERT SAMPLES TO VOLTAGE */
for(i = 0;i < tsamp;i + + ) volts[i] = (float)dvxdata[i] *
SCALE;
```



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### 5.1.3 Control Sequencer

Before starting an acquisition sequence, prepare a gain/channel sequence file which contains the gain, port, and channel number of each channel to be scanned in the sequence; and the trigger flag (if required) marking the channel to be monitored for data-dependent triggering.

Then download the file into the Scan Sequence RAM. The Control Sequencer reads the Sequence RAM and synchronizes the DAS card as well as the associated multiplexer cards that can extend the total number of input channels to 256 (32 channels to each of 8 ports).

The sampling trigger and the start acquisition commands can be derived internally or from user-supplied signals via the two BNC connectors on the front panel. Internally, the sampling trigger is derived from a precision crystal controlled oscillator (3.6864 MHz + 0.001%) and the Start is issued under control of your program. Select the sampling rate, one of the downloadable parameters, prior to the initiation of the acquisition. Externally, you can supply both the sampling trigger and the start command by connecting the signals to the BNCs and downloading the necessary selection commands into the Command register.

In the data dependent triggering mode, the Control Sequencer continually scans through the channels. Each time the channel flagged for monitoring is sampled, the converted value is compared with the threshold level that you loaded into the Threshold register.

In the Post-trigger mode, when the threshold is crossed in the user-defined direction, the triggering event and all subsequent values are stored in the FIFO. Channel #2 of the DMA controller transfers all data to the VMEbus memory. In demultiplexing post-trigger data, the channel data point AFTER the triggering channel is the FIRST data point in the data set (NOT necessarily the first channel in the scan sequence).

In the Pre/Post triggering mode, all conversions are stored in the FIFO from the beginning of the scan. When the threshold is crossed in the user-defined direction, the value of the trigger event and all subsequent values are tagged as they are loaded into the FIFO. All



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# Section 5
# Functional Description

## 5.1 OVERVIEW

The DBS 8700/8701 Data Acquisition System (DAS) occupies a single slot in a standard double height VME chassis or 'C' size VXI chassis. Connectors for 8 differential analog input signals and two digital sampling control signals are available on the front panel. Ten LEDs indicate the 8-bit binary channel code (1 of 256), the Pass/Fail condition of the board and the BUSY condition while acquisition is in progress. On the rear of the card, the P1 connector is fully compatible with the VMEbus specifications and the P2 connector complies with the VXIbus specification. Refer to Figure 5-1 for the following functional description.



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diagnostics, in addition to testing all registers and the scan sequence memory, also select an on-board reference voltage to test the operation of the IA, PGA, ADC, FIFO and the DMA controller. It is also a means of measuring the offset voltage of the entire analog front end (from IA through the ADC). Successful completion of the tests sets the Pass/Fail lamp on the front panel from red to green.

### 5.1.6 DC/DC Converter

The DAS is equipped with an ultra-low noise DC/DC converter designed to meet the stringent power demands of the ADC4342 A/D converter. It draws only +5V power from the VME backplane and converts it to filtered +15V, -15V and +5V required by the ADC and the analog front end.

## 5.2 HARDWARE DEVICE REGISTERS

The purpose of this section is to familiarize you with the operations of the card and to define some of the driver calls. Most likely, you will never need to directly examine the contents of any register.

The DAS has 9 control and status registers that can be located on any 64 byte boundary above C000 (hexadecimal) in the VME A24 address space. The Base Address of the card is C000. The 8-bit on-board jumpers, which select the particular 64 byte group of addresses reserved for the DAS, complete the Base address. The registers are accessed as 16-bit words only. See Section 2.2.1 for full range of possible addresses.

### 5.2.1 Device Identification Register (Base address + 0000H)

The ID Register register (read-only) contains a unique VXI manufacturers code of CFF5 assigned by the VXIbus consortium.

### 5.2.2 Device Type Register (Base address + 0002H)

This read only register contains hexidecimal codes that identify memory size, product model and software revision. The memory size code complies with the VXI Specification. The contents of the Device Type Register for A16/24 devices is defined in Figure 5-2.



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### 5.1.1 Analog Front End

Eight differential analog signals can be connected to the card. To minimize the noise pick-up, these signals should be connected with twisted shielded conductor pairs, wired to a 25 pin D type male connector according to the table in Section 2.3.1. The connector should be covered with a metallic backshell.Unused inputs should be connected to ground to prevent them from floating and introducing spurious noise.

The analog inputs are both over-voltage and over-current protected. Any analog signal exceeding ±12 volts is clamped to an internal supply rail and the current is limited to 50 mA.

The 8 analog inputs (Ports) are differentially multiplexed into a low noise FET input Instrumentation Amplifier (IA) providing a Common Mode Rejection Ratio exceeding 100 dB at 60 Hz. The single-ended output of the IA is amplified by a software controlled Programmable Gain Amplifier (PGA) with gains of 1, 2, 4, or 8.

The gain can be changed under sequencer control every conversion cycle allowing the user to dynamically check for maximum signal amplitude. The sequence RAM can be reloaded with new gain settings so that the signal level of each channel will be optimally amplified to take full advantage of the dynamic range of the A/D converter.

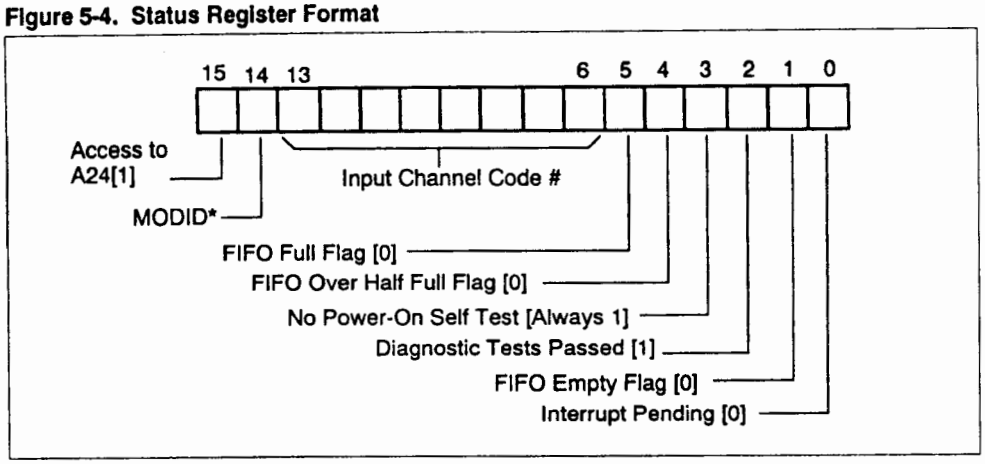
### 5.1.2 A/D Converter

A 400 kHz, 16-bit resolution sampling analog-to-digital converter digitizes the signals amplified by the PGA. The sampling rate of the converter is selectable in 1000 steps from 409.6 kHz to 3.600 kHz. The built in sample-and-hold has been optimized for acquisition time, hold mode settling time, noise, and aperture errors up to the maximum sampling rate. Upon completion of the conversion, the digitized results are transferred to a 1024 word FIFO for transfer over the VMEbus, or buffered for transfer to the adjacent card slot via the VXIbus.



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**Figure 5-4. Status Register Format**

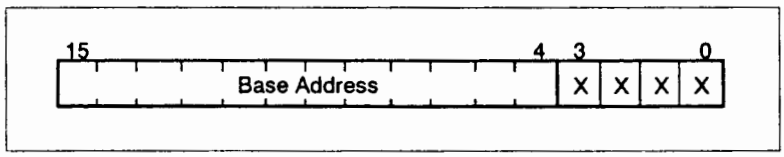



### *5.2.4 Sequence RAM Offset Register (Base address + 0006H)*

This 16-bit register (Figure 5-5) contains the offset address of the on-board memory that is mapped into an unassigned memory block of the A24 address space of the VME bus. Each offset address points to a single 256 byte block of memory. Since there are 16 such blocks on the DAS card, only the most significant 12 bits of the Offset register are required. For example, if the Sequence Ram were to be mapped into the A24 space at location 401000H, the Offset register would be loaded with 4010.

The access to the Sequence RAM is controlled by the A24 Enable bit in the Control/Status register (CSR15). When the bit is zero, access to the Sequence RAM is disabled and the SRAM will not respond to VMEbus accesses. After the Offset Register is loaded with the desired offset and the CSR15 (A24 Enable) is set, the SRAM will respond to the desired address.

**Figure 5-5. Sequence RAM Offset Register Format**






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pre-trigger data PLUS the trigger event data point, are transferred to the VMEbus memory pre-trigger buffer by channel #1 of the DMA controller and all post-trigger event data are transferred to the post trigger buffer in the VMEbus memory by channel #2.

In de-multiplexing pre/post triggered data, it is important to note that the pre-trigger data is stored in a circular buffer and that the trigger event aborted the DMA operation on channel #1. The trigger event data point is the LAST point written into the pre-trigger buffer before the operation was aborted. The data point following the trigger event data point is the FIRST point in the post-trigger data buffer. You must determine from DMA channel #1, which was the last location in the pre-trigger buffer to be written by reading the registers in the AM9516, and "unroll" the data before concatenating it with the post-trigger data, and then locate the beginning of a scan sequence in the pre-trigger data set.

### 5.1.4 VME/VXI Interface

To comply with both the VMEbus and VXIbus Specifications, the DAS has the following series of registers and jumper fields:

a. VMEbus slave data transfer
b. VMEbus master data transfer
c. VMEbus interrupt operations
d. VMEbus master bus arbitration
e. VXIbus software protocol requirements
f. VXIbus local bus connections
g. VXIbus TTLTRG bus connections

This facilitates the transfer of data from the DAS to both VMEbus resident memories and host processors as well as cards in the adjacent card slots. The detailed description of the various registers and jumpers appears below in Section 5.2.

### 5.1.5 Power-Up Diagnostic Stimuli

The DAS software driver includes diagnostics that are automatically run whenever the system is initialized. In addition, the user can execute them by issuing the RUN__AD__DIAG command. These

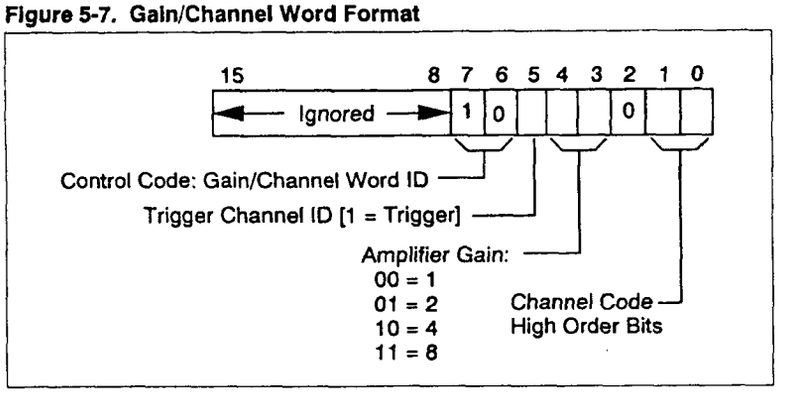


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### 5.2.4.2 Gain/Channel Word

The Gain/Channel word (Figure 5-7) contains the programmable gain amplifier setting, the high order two bits of the Channel code, the trigger ID bit identifying the channel as the trigger channel for data dependent triggering, and the control bits.

**Figure 5-7. Gain/Channel Word Format**




### 5.2.4.3 Channel/Port Word

The Channel/Port word (Figure 5-8) contains the 3-bit Port address, the 3 least significant bits of the channel code for the channel to be sampled, and the control code bits.

The scan sequence is loaded into the sequence RAM starting at the first location (VMEbus offset address + 0). When the sequencer encounters the loop back code in the Channel/Port word of the last channel in the scan sequence, the address of the SRAM is returned to zero. This last word of the scan table MUST be repeated in the following location of the sequence RAM.

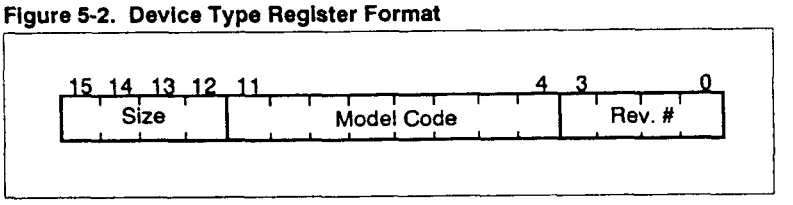
When a Multiplexer card is connected to a Port, it compares the 3-bit port code with the setting of its Port Selection switches and loads the 5-bit channel code into the Channel register when the port code matches the Port Selection code. The code stored in the Channel register selects which analog input signal is connected to the output of the multiplexer card.



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For this DAS, the memory size code is 'B' for 4096 bytes of on-board memory that can be accessed in the A24 address space (Only even-numbered bytes contain valid data.) The model code is 15 and the software revision code is 1 (Subject to change if future revisions are required). Therefore, the total content of this register is B151.

**Figure 5-2. Device Type Register Format**

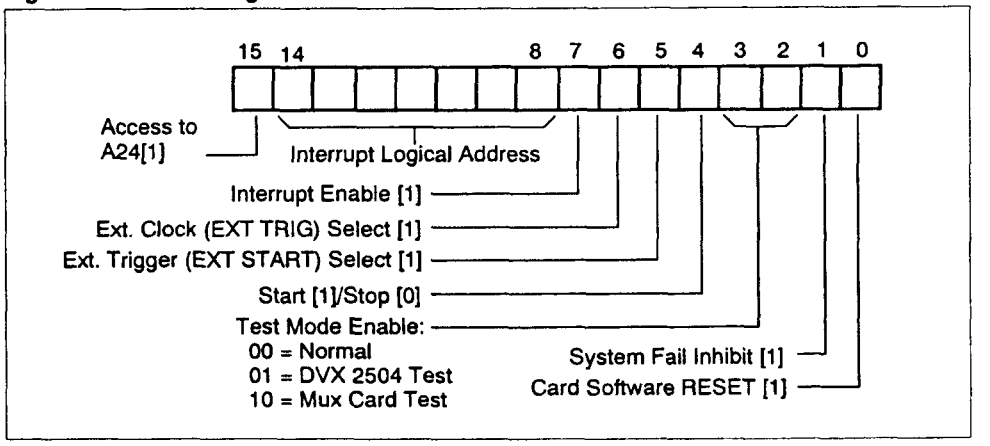



### 5.2.3 *Control/Status Register (Base address + 0004H)*

The CSR is a Read/Write register that is used for controlling the operational modes of the DAS (Write only) and for providing the current board status (Read only). The bit assignments for the Control Register (Write) are defined in Figure 5-3. The bit assignments for the Status register (Read) are defined in Figure 5-4.

At power-on, all bits in the Control Register are set to Zero and the Pass/Fail lamp is in the Pass condition. When Software RESET is asserted, the control logic on the card and the contents of the FIFO are cleared.

**Figure 5-3. Control Register Format**






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#### 5.2.4.5 SRAM Format for the DVX Family of Multiplexer Cards

When multiplexer cards are connected to one or more of the eight DAS input ports, the method of loading the SRAM in the DAS must be modified to account for the preselection (pipelining or overlapping) of the next channel to be scanned on the multiplexer cards. The Channel register on a multiplexer card must be loaded with the channel code before the sampling process begins. This register (pipeline register) can also be used to provide additional time for the amplifiers and multiplexers to settle before the selected channel's voltage is converted. For aggregate sampling rates below 200 kHz, the single stage of delay caused by the channel register is all that is required for optimum settling time. When aggregate sampling rates are between 200 kHz and 400 kHz, an additional stage of delay is necessary and when the aggregate sampling rate is between 400 kHz and 500 kHz, then 3 stages of delay are necessary.

Before a scan can begin, the channel register on each multiplexer card connected to the DAS must be loaded with the code of the first channel on that multiplexer card to be scanned. This is accomplished by the construction of a Pre-scan table that is loaded into the SRAM, starting an acquisition for a minimum of one complete scan of the pre-scan sequence, and the halting of the acquisition. The FIFO is then cleared, and the SRAM loaded with the complete scan sequence.

#### 5.2.4.6 Order of Scan Restrictions

There are no "order of scan" restrictions on scanning the multiplexer channels when only a single stage of delay is required. However, when two stages are required, the port to which the multiplexer is connected CANNOT be scanned twice in succession. That is, two or more ports must be scanned alternately. This allows an additional sample period of delay for settling. Similarly, when three stages are required, then at least three or more ports must be scanned alternately.

At this point some examples using a DBS 8720 multiplexer will help in understanding how ordering the scan increases the amount of time for settling. With the same port/channel pairs, let us configure three scan sequences, one each for 1, 2 & 3 stages of delay.



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### 5.2.4.1 *Loading the Scan Sequence RAM*

The Scan Sequence RAM on the DAS is a 2048 word memory in which ONLY the low byte is implemented. Two words (Figure 5-6) are required for each channel to be scanned. These words contain the following:

a. Channel code (channel number) of a Multiplexer input

b. Port number to which the multiplexer is connected

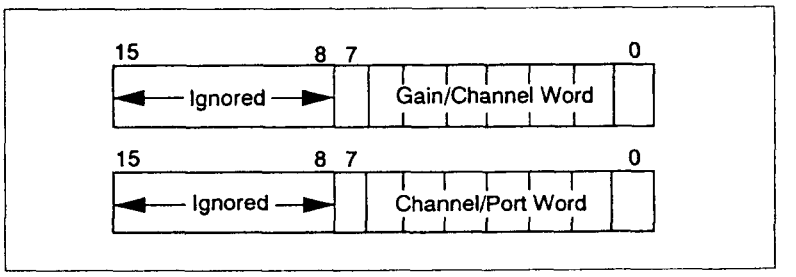
c. Gain setting for the Programmable Gain Amplifier when the channel is sampled

d. Trigger ID, used when channel data is being monitored for triggering

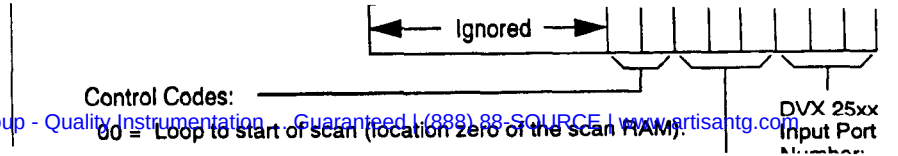
e. Control Code used by the sequencer

If a multiplexer is not connected to a port, then the port is a single channel port. The Channel number is split between the Gain/Channel word and the Channel/Port Word. The most significant two bits of the channel code are in the Gain/Channel word and the least significant three are in the Channel/Port word. This word-pair is written into the Scan RAM for each port or channel on that port in the desired order of scanning.

**Figure 5-6. Scan Sequence RAM Word-Pair Format**






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The sequence RAM is loaded with the Pre-scan table and an acquisition sequence is initiated and terminated after a minimum of one pass through the pre-scan table. This preloads the channel code registers on the three multiplexer cards. The acquired data is discarded.

The channel codes, as reordered above in the Single Delay SRAM Load acquisition table, are then combined with the gain, trigger, and control code bits (see Section 5.2.4.4). The resulting composite scan sequence is loaded into the sequence RAM for acquiring the data.

When the acquisition begins, the first channel converted will be Channel 1 on Port 0 (since that code had been pre-loaded), and channel code 2 will be loaded into the channel code register in the multiplexer on Port 0. The process is repeated as channels 2,3, and 4 are converted. When channel 5 is converted, the channel code register is loaded with the channel code 1, leaving the multiplexer set up for reading Channel 1 on Port 0 when the scan sequence is repeated. The same process is repeated for the other two ports.

#### *5.2.4.8 Example of two Stage Delay*

Now using the same set of channels and ports, let us construct a table with 2 delay stages (Figure 5-10). Here, note that the total number of channels scanned *must* be an integer multiple of 2, or else a "dummy" channel must be added. Also, the channels per port must be balanced so that in no case will a port be scanned twice in succession.

Notice that the same port code does not appear twice in succession but the order of the ports is the same as the desired order and, as before, the first channel on a port has slipped to the last position for that port. The pre-scan table must be loaded with the first channel on each port.

#### *5.2.4.9 Example of three Stage Delay*

With a three-stage version of channel/port codes (Figure 5-11), however, we cannot use the same channel/port order as in Figure 5-10 because of the requirement to separate each port by at least 2 other port codes. Therefore channel 1 on Port 0 is moved to Port 2 (relocating the signal from Multiplexer #0 to Multiplexer #2).



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**Figure 5-10. Two Stage Delay Example**

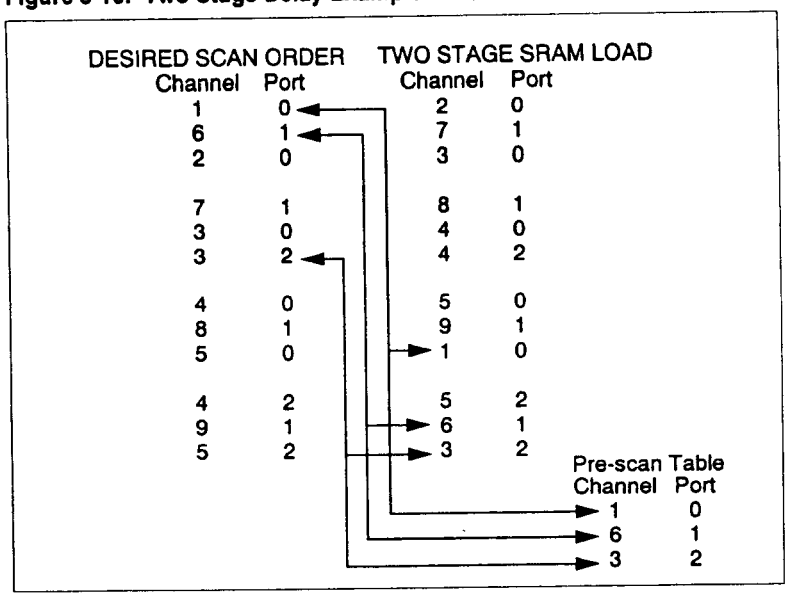
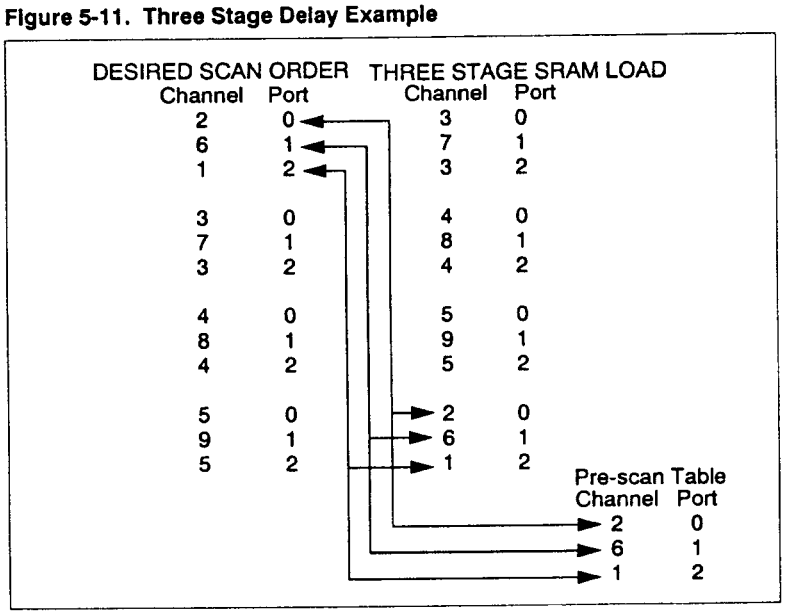



**Figure 5-11. Three Stage Delay Example**






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Notice that the same port code appears no more frequently than every third sample. As before, the first channel on a port has slipped to the last position for that port. The pre-scan table must be loaded with the first channel on each port.

#### *5.2.4.10 Example of a Single Stage Delay with Sample/Hold Multiplexer*

When a multiplexer card with simultaneous sample/hold amplifiers is connected to the DAS, the External S/H signal must be driven to place the S/H amplifiers into the 'track' mode to acquire the input signal voltage and then switched into the 'hold' mode for the scan cycle. This is accomplished by setting the control code bits in the Channel/Port word to "01" for asserting the Ext. S/H signal for a period of time and then setting the control code bits to "11" to negate the Ext. S/H signal and start the scan of the channels. The assertion of the Ext. S/H is done at the very beginning of the scan by inserting at the beginning of the SRAM load table the replication of the first entry with the control code for the assertion of the Ext. S/H for as many sample periods as required to reduce the effects of dielectric absorption. See Appendix B for notes on dielectric absorption.

Then the two words for the first channel to be sampled follow but with the control code bits of the second pair set to 11. This switches the external Sample/Hold circuits to the "hold" mode. The first converted value stored in the FIFO is the conversion for this entry in the scan table.

Note that when a Sample/Hold DVX multiplexer card is used, at least one sample cycle per S/H entry per scan loop is lost for the sample period. Therefore loop time = (the number of channels + the number of S/H entries) multiplied by the sample period (Tsamp). In the example below, assuming 5 μs for the sample period,

Loop Time = (12 channels + 5 S/H) × Sample period

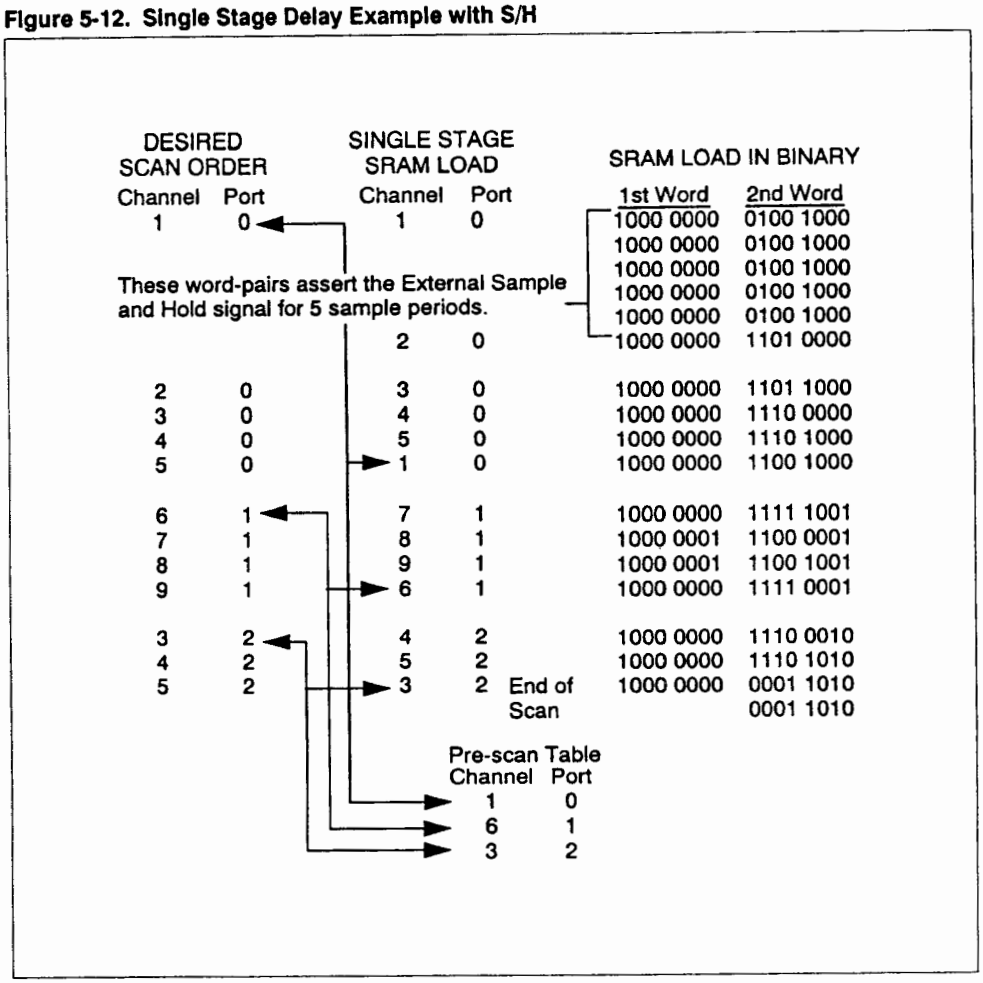
Loop Time = 17 periods × 5 μs = 85 μs

Sampling Frequency/ Channel = 1/Loop time = 1/85 μs = 11.765 kHz



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**Figure 5-12. Single Stage Delay Example with S/H**



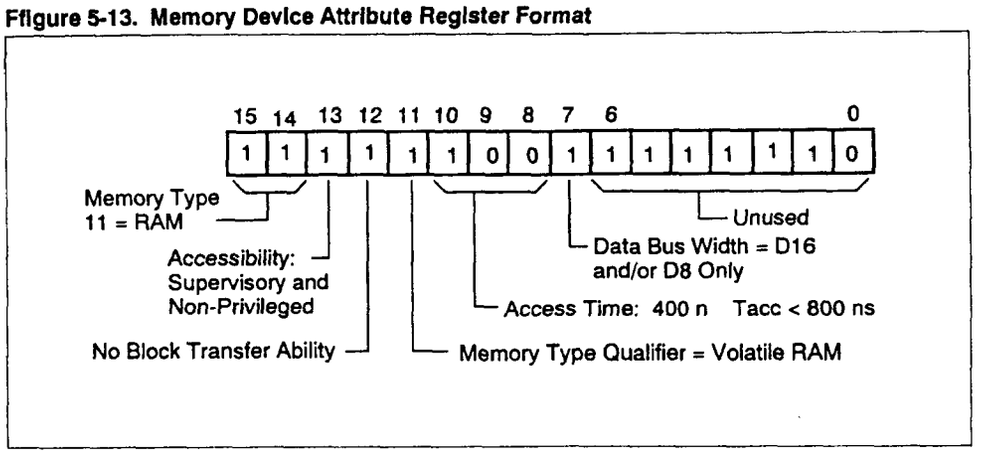



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### 5.2.5 Memory Device Attribute Register (Base address + 0008H)

The attribute register (Read Only) lists the important characteristics of the memory on the card.

**Figure 5-13. Memory Device Attribute Register Format**




### 5.2.6 Sampling Rate Select Register (Base address + 000AH)

The Sampling Rate Register (Figure 5-14) controls the external trigger and external clock inputs and determines the internal sampling clock frequency. The bit fields that control the trigger and clock inputs are described in the figure. To select one of the possible 1000 sampling rates, write the two's complement of the divisor of the 3.6864 MHz precision clock into this register.

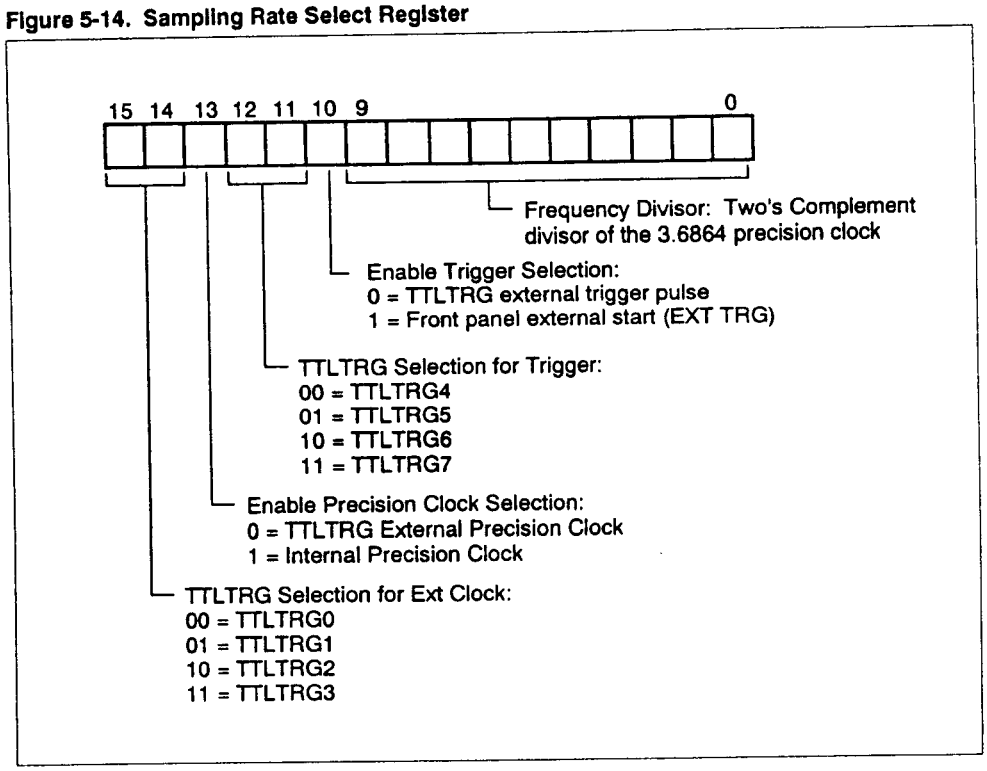
Typical sampling rates and divisors are:

| Divisor | Sampling Fequency |
|---|---|
| 9 | 409.6000 kHz |
| 10 | 368.64001 |
| 11 | 335.12726 |
| 12 | 307.20001 |
| 15 | 245.75999 |
| 18 | 204.80000 |
| 19 | 194.02106 |



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**Figure 5-14. Sampling Rate Select Register**





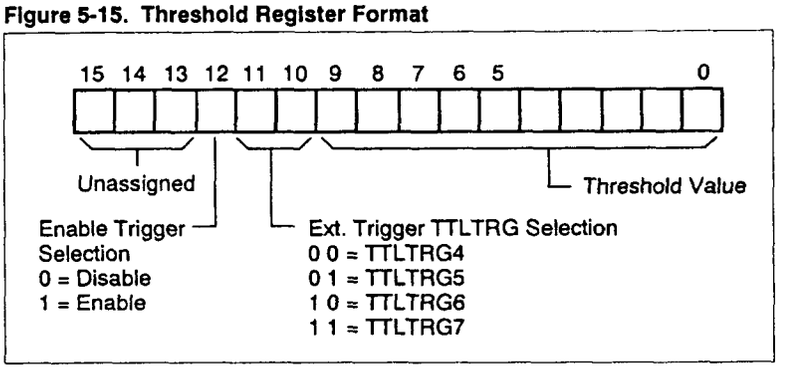

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### 5.2.7 *Threshold Register (Base address + 0010H)*

The Threshold Register (Figure -15) controls data-dependent triggering of a data acquisition. A special signal is generated on the board when the ten most significant bits of the digitized value from the selected channel crosses the value written to the threshold field (bits 9-0). This signal is used to tag the digitized data as it is written into the FIFO. This signal is also used to generate a 60-ns, active-low pulse that is routed to a TTLTRG line (4, 5, 6 or 7) selected by bits 11 and 10. The signal will be asserted only when data-dependent triggering is invoked, the TTLTRG is enabled and the triggering event has occurred. This applies to both Pre/post and Post Trigger acquisitions.

The "threshold value" is a Binary value, whereas the digital output of the ADC to which it will be compared is Offset Binary, regardless of the output data format that has been jumper-selected.

**Figure 5-15. Threshold Register Format**




### 5.2.8 *FIFO Register (Base address + 0012H)*

This Read-Only register allows the direct access to the contents of the FIFO by the host processor without the use of the DMA controller.



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### 5.2.9 AM9516 DMA Controller (DMAC) Pointer Register (Base address + 000CH)

The address of the DMAC's internal register to be accessed must be loaded into the Pointer register. The Pointer register is a Read/Write register. Table 5-2 lists the DMAC registers used for this card.

**Table 5-2. DMAC Registers**

| Register Name | Access Type<br>R = Host Read<br>W = Host Write<br>C = Chain Loadable | Address (Hex)<br>Ch 1/Ch 2 |
|---|---|---|
| Master Mode | R/W | 38 |
| Command Mode | W | 2E/2C |
| Chain Control | C | |
| Current Address A:<br>Upper Addr./Tag Field<br>Lower Address Field | R/W, C | <br>1A/18<br>0A/08 |
| Current Address B:<br>Upper Addr./Tag Field<br>Lower Address Field | R/W, C | <br>12/10<br>02/00 |
| Base Address A:<br>Upper Addr./Tag Field<br>Lower Address Field | R/W, C | <br>1E/1C<br>0E/0C |
| Base Address B:<br>Upper Addr./Tag Field<br>Lower Address Field | R/W, C | <br>16/14<br>06/04 |
| Current Operation Count | R/W, C | 32/30 |
| Base Operation Count | R/W, C | 36/34 |
| Status Register | R | 2E/2C |
| Interrupt Save | R | 2A/28 |
| Interrupt Vector | R/W, C | 5A/58 |
| Channel Mode | R/W, C | 52/50 |
| Chain Address:<br>Upper Addr./Tag Field<br>Lower Address Field | R/W, C | <br>26/24<br>22/20 |

### 5.2.10 AM9516 DMA Controller (DMAC) Data Register (Base address + 000EH)

Read/write operations to the DMAC Data Register access the register pointed to by the code in the DMAC Pointer Register.



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## 5.3 DMA OPERATIONS

The following is a brief discussion of the AM9516A Universal DMA Controller. Details of the operation of the chip may be found in one of the following publications.

a) Advanced Micro Devices Am9516/AmZ8016
Direct Memory Access Controller Manual, 1984
Document #CD-MU-10M-10/84, Order #04910A

b) Advanced Micro Devices MOS Microprocessors and Peripherals 1987-1988 Data Book, 1987, pg 2-66 to 2-118; order #09067A

### 5.3.1 DMA Modes of Operation

The AM9516 DMAC has two independent DMA channels for transferring data and instructions. Each channel has its own set of registers as shown in the table above. On the DAS, the AM9516 operates in the "flyby" word mode, writing data from the FIFO into the host memory. It operates in the "chaining" mode to load/initialize its registers and to automatically reload/reinitialize at the end of an acquisition cycle.

The DMAC can acquire data in three different ways: (1) Normal data acquisition, (2) Post trigger acquisition, and (3) Pre/Post trigger acquisition

In the normal mode, DMAC channel #2 is loaded via chaining prior to the start of the A/D. When the FIFO is more than half full, the DMAC #2 acquires the VME bus and transfers data until the FIFO is emptied. It then becomes idle until the FIFO again fills past half full.

In the Post trigger mode, the DMAC channel #2 is loaded as above, but the storing of data into the FIFO after the A/D is started is suspended until the threshold is crossed. The DMAC channel #2 transfers the data as before.

In the Pre/Post trigger mode, the DMAC channel #1 as well as DMAC channel #2 are used. When the A/D is started, all data acquired are written into the FIFO. DMAC channel #1 will transfer the data into one memory (circular) buffer area. When the threshold is



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crossed, all the data written into the FIFO are tagged. When the first tagged datum point is read out of the FIFO, it is written to the one memory (circular) buffer area, the DMAC channel #1 operation is terminated and DMAC channel #2 operation is started with the remaining tagged data being written into a second memory buffer area. This allows the continuous capture of an arbitrary amount of data before and after the triggering event.

### 5.3.2 DMA Address Modifiers

When the DAS becomes bus master, it accesses the A24 (standard) address space differently for the chaining operations and data transfer operations. For chaining commands, the DAS executes a Standard Supervisory Data access by generating the address modifier "3D". For data transfers, however, the DAS executes a Non-privileged Data Access by generating the address modifier "39".

Most VMEbus compatible memories respond to:

a) Supervisory Program Access Addr. Mod = 3E
b) Supervisory Data Access Addr. Mod = 3D
c) Non-privileged Program Access Addr. Mod = 3A
d) Non-privileged Data Access Addr. Mod = 39

## 5.4 INTERRUPT OPERATIONS

The DAS can generate an interrupt to the host CPU on the VME bus for several different conditions. The least significant 7 bits of the interrupt vector to be generated when the DAS acknowledge interrupt servicing are defined by a field within the DAS CSR; the most significant bit of the vector is not programmable and will always be a 1.

The interrupt enable bit in the CSR enables the DAS to interrupt when the FIFO becomes half-full and again when it becomes full. A half-full interrupt is dismissed upon acknowledgement from the host CPU; a full interrupt will not be dismissed until the FIFO goes non-full or the DAS is reset.

Interrupts can also be generated when a DMA operation has been completed or when a trigger condition has been met. The DMA interrupts are enabled by the appropriate register fields in the



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AM9516 internal register set. The DMA interrupt is dismissed when the CPU writes a Clear Interrupt command to the AM9516.

All interrupts generate the same interrupt vector. Normally, the user will enable only the FIFO interrupts OR the DMA interrupts. It is up to the user to keep a flag on which interrupt is enabled, and to read either the DAS Status Register or the AM9516 Status Register to determine the source of the interrupt.

## 5.5 AM9516A PROGRAMMING OVERVIEW

The following is an explanation of the programming of the AM9516 DMAC chip as it is used in the DAS. Therefore, only the registers that are meaningful in the DMA operations of the DAS are discussed.

### 5.5.1 Registers

#### 5.5.1.1 Chip-Level Registers

Three global registers configure the chip functions and control the chip's operation:

- Master Mode Register
- Command Register
- Chan Control Register

#### 5.5.1.2 Channel-Level Registers

Each DMA channel has 13 local registers that control its operation but only the following registers are of concern in the DAS:

Channel Mode Register
Current Address RegisterA
Base Address RegisterA
Current Address RegisterB
Base Address RegisterB
Current Operation Count
Base Operation Count
Status Register
Interrupt Save Register
Chain Address Register



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### 5.5.2 Commands

The host CPU can write any of 19 commands into the DMA device's Command Register. These commands initiate specific types of DMA operations, including chaining, mask setting and clearing, and the setting of specific bits to indicate transfer direction.

### 5.5.3 Chaining

Chaining allows a channel to load its own control parameters from a Chain Control Table in memory, thereby minimizing the need for CPU intervention.

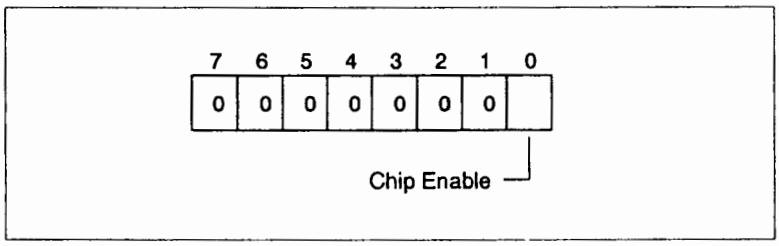
### 5.5.4 Register Description

Table 5-2 lists the registers used, their accessibility, and their addresses. The following is a detailed description of the bit assignments and usage.

#### 5.5.4.1 Master Mode Register

This 8-bit register (Figure 5-16), which controls the chip level interface, can be read or written at any time except during chaining. System RESET clears it to all zeroes. When the Chip Enable bit is a 1, the DMAC can gain access to the system bus to begin DMA operations. The other bits are assigned as shown for proper operation of the DAS.

**Figure 5-16. Master Mode Register Format**






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#### 5.5.4.2 Command Register

This register contains the command that the host CPU issues to the DMAC. Table 5-3 lists the commands used in the DAS.

**Table 5-3. DAS Commands**

| Command | OP Code<br>E = 1 to Set/Clear CIE, 0 for no effect<br>P = 1 to Set/Clear IP, 0 for no effect |
|---|---|
| Reset | 0000 0000 |
| Start Chan #1 | 1010 0000 |
| Start Chan #2 | 1010 0001 |
| Set Software Request Chan #1 | 0100 0010 |
| Set Software Request Chan #2 | 0100 0011 |
| Clear Software Request Chan #1 | 0100 0000 |
| Clear Software Request Chan #2 | 0100 0001 |
| Set Hardware Mask Chan #1 | 1000 0010 |
| Set Hardware Mask Chan #2 | 1000 0011 |
| Clear Hardware Mask Chan #1 | 1000 0000 |
| Clear Hardware Mask Chan #2 | 1000 0001 |
| Set CIE/IP Chan #1 | 001R 0P10 |
| Set CIE/IP Chan #2 | 001R 0P11 |
| Clear CIE/IP Chan #1 | 001R 0P00 |
| Clear CIE/IP Chan #2 | 001R 0P01 |
| Set Flip Bit Chan #1 | 0110 0010 |
| Set Flip Bit Chan #2 | 0110 0011 |
| Clear Flip Bit Chan #1 | 0110 0000 |
| Clear Flip Bit Chan #2 | 0110 0001 |

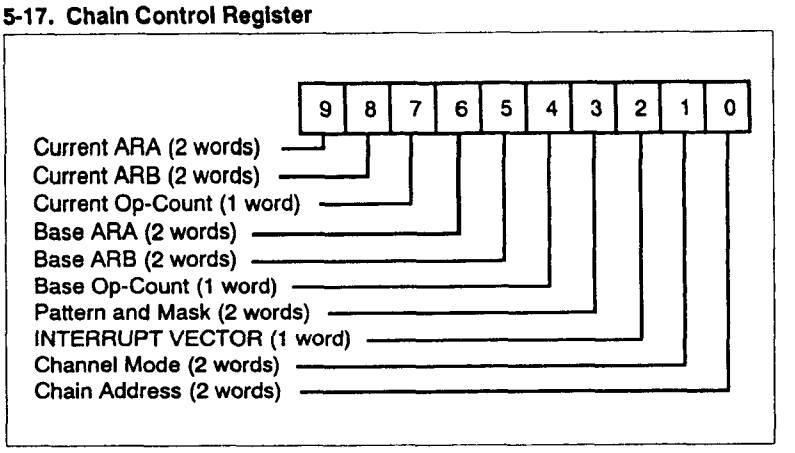
#### 5.5.4.3 Chain Control Register

When a channel begins a chaining operation, the Chain Control Register (Figure 5-17) is loaded with the Reload word from the memory location indicated by the address in the Chain Address register. The bits in this register identify all of the registers that must be loaded from the table in memory that follows the Reload word.



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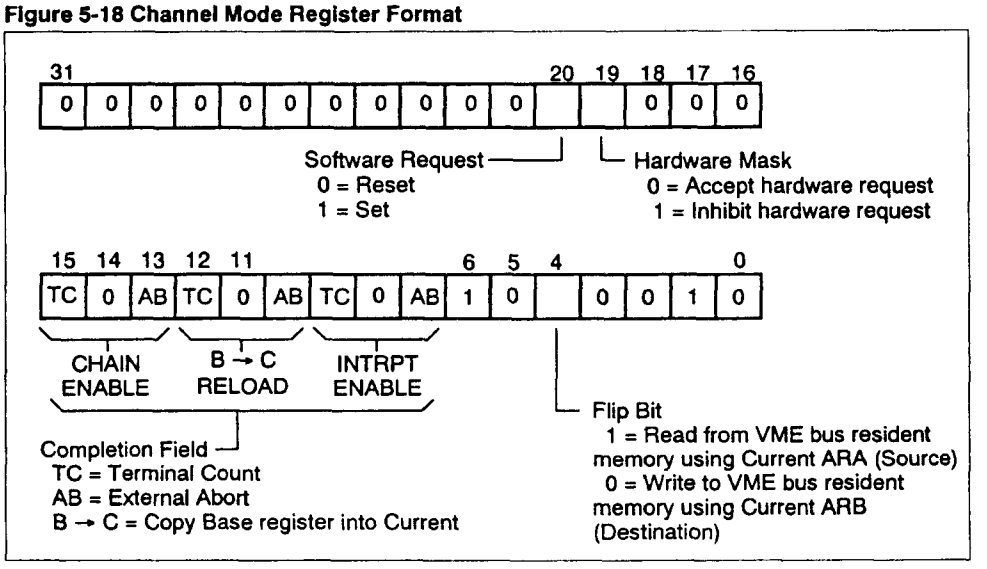
5-17. Chain Control Register




### *5.5.4.4 Channel Mode Register*

The Channel Mode Register (Figure 5-18) for each channel selects the type of DMA operation to be performed, the manner of execution, and the action to be taken upon the completion or the abnormal termination of the operation.

**Figure 5-18 Channel Mode Register Format**






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The Software Request bit is set when DMA operations are initiated to chain in the commands, address, etc. for data transfers and to chain in subsequent commands, addresses, etc. after the first data operation is complete. Although it can be loaded by writing to the Command Register, it is best done via chaining.

The Hardware Mask bit is to be set ONLY by chaining. Although it can be loaded by writing to the Command Register, it is best done via chaining.

The Completion Field specifies the enabling of the three named actions based upon the manner of termination of the current operation. For example, if the Chain Enable TC bit is set, when the current operation count reaches terminal count, the channel will switch to the chain mode and chain in the new Reload word. If the AB (abort) bit in the INTERRUPT field is set, when the operation is aborted due to abnormal conditions, the channel will generate an interrupt to the host processor. A bit set in the B→C RELOAD field causes the Base Address and Base Operations Count registers to be copied into the current Address and Current Operation Count registers when the terminal condition occurs. This allows the continued writing to a single (or circular) buffer.

#### *5.5.4.5 Current Address Registers, A & B*

For the purposes of this discussion, these registers contain the address of VMEbus resident memory accessed by the data DMA operations. These registers can be loaded with the contents of the Base Address Registers A & B for the auto-loading of repetitive operations without the overhead of chaining in the address.

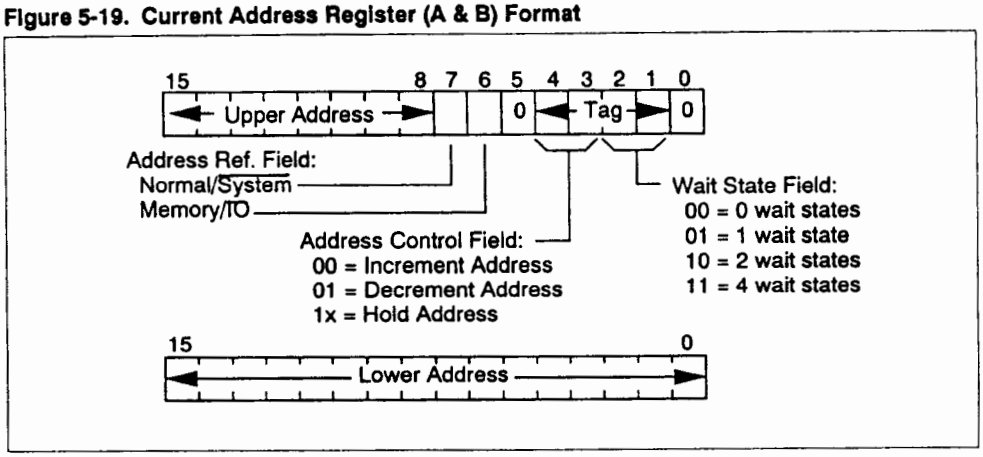
These registers consist of two 16-bit words, an Upper Address/Tag field and the Lower Address field as shown below.

The Upper address is the most significant byte of the 24-bit memory address and the Lower address is the remaining portion of the 24-bit address.



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**Figure 5-19. Current Address Register (A & B) Format**




#### 5.5.4.6 Base Address Registers, A & B

The Base Address Registers A & B are identical to the Current Address Registers A & B with regard to the content. Operationally, however, they are storage registers whose contents can be read, written, or copied into the Current Address Registers A & B.

#### 5.5.4.7 Current Operation Count Registers

This 16-bit register contains the number of words to be transferred during a DMA operation. With each transfer, the contents are incremented or decremented as specified in the Tag field of the Current Address Register.

When the contents have been decremented to 0000, the TC bit in the Status Register is set to 1 indicating a successful completion of the operation. The maximum number of words, 65535, can be transferred by loading the Current Count register with FFFF.

#### 5.5.4.8 Base Operation Count

This 16-bit register is a holding register which can be read, written, or copied into the Current Operation Count Register.

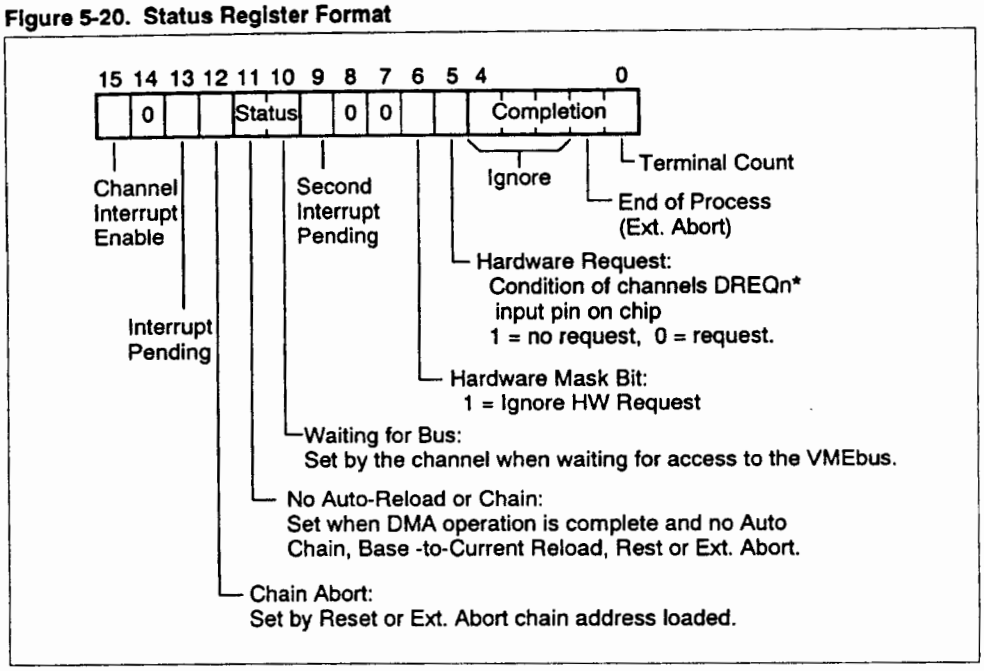


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#### 5.5.4.9 Status Register

The 16-bit Status Register reports the fields of information show in Figure 5-20.

**Figure 5-20. Status Register Format**



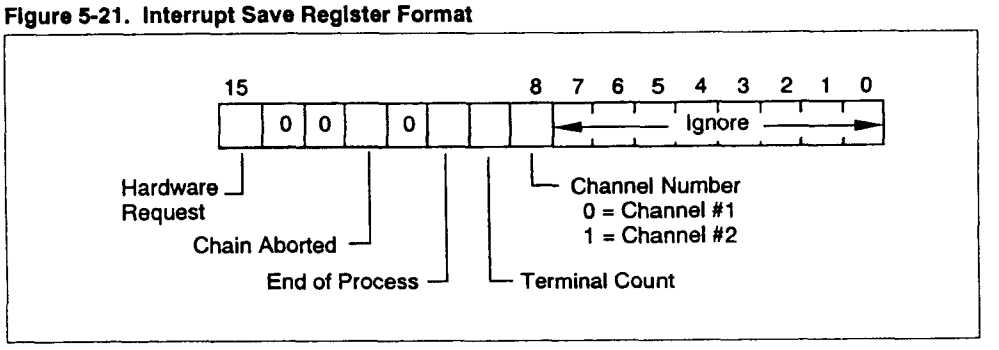

#### 5.5.4.10 Interrupt Save Register

The DMA controller has a two-deep interrupt queue. When two interrupts are queued in the channel, the Second Interrupt Pending (SIP) bit in the status register is set. Once set, all further activity on the channel is prohibited until the Interrupt Acknowledge clears it. This ensures that the DMA never gets more than two operations ahead of the host processor. The content of the Interrupt Save register is shown below.



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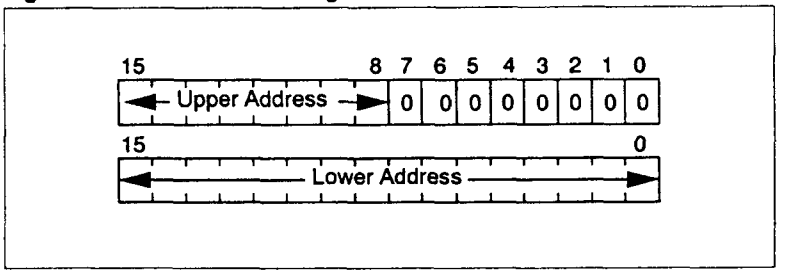
**Figure 5-21. Interrupt Save Register Format**




### 5.5.4.11 *Chain Address Register*

The contents of the Chain Address Register point to the Chain Control Table in the VMEbus resident memory where the data to be loaded into the channel's other registers during chaining are located. The contents are shown below.

**Figure 5-22 Chain Address Register Format**




### 5.5.4.12 *Chain Control Register*

The first step in a chaining operation is to read the Reload word from the VMEbus memory location pointed to by the Chain Address Register and store it in the Chain Control Register. The channel then retains control of the VMEbus until all of the registers defined in the Reload word have been reloaded.



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### 5.5.5 *Simple Example of the DMA Operations*

The following example written in "C" demonstrates the set-up for the Pre-Post triggering operation of the DMA controller.

```
      /* A simple example for setting up DMA operations
      for Pre/Post-triggering acquisition. */

#define DMAPointerReg = 0x000c
#define DMACommandReg = 0x000e
#define CSR = 0x0004
#define THRSH = 0x0010
#define OFFSET = 0x0006
#define DevAdr = 0xffc040
#define WordCount = 0x0fff

int DataTablAdrL, DataTablAdrH;
long DataTableAddr, ChainAddr1, ChainAddr2;
int WordCount, IntrVect;
int ChanModeH, ChanModeL;

/* RESET THE 9516A CONTROLLER */
 {
      /*set the software reset bit */
      WriteReg(DevAdr + CSR,0x0003)
      /* clear the software reset bit and enable the SRAM.*/
      WriteReg(DevAdr + CSR,0x8002)
      /* Load the SRAM A24 Offset Register */
      WriteReg(DevAdr + OFFSET,0x4000)


/* LOAD THE MASTER MODE REGISTER */
      /*Load the address of the Master Mode*/
WriteReg(DevAdr + DMAPointerReg,0x0038)
      /* Load the Mode Command */
WriteReg(DevAdr + DMACommandReg,0x000d)
```



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```
/* SET UP THE CHAIN TABLE FOR CHANNEL 2 IN MEMORY */
      /* write the Reload word at the top of the Chain Table.
      The Reload word calls for loading the following registers:
      Current Address Reg. B (2 words)
      Current Operation Count (1 word)
      Channel Mode (2 words) */

WriteMem (ChainAddr2,0x182)
DataTablAdrH = (((DataTableAddr + WordCount) > > 8)
      &&0xff00||0x000000c0)
DataTablAdrL = (DataTableAddr + WordCount)
      &&0x0000ffff

      /* write post trigger starting address into chain table */
WriteMem(ChainAddr2 + 1,DataTablAdrH)
WriteMem(ChainAddr2 + 2,DataTablAdrL)

      /* write word count */

WriteMem(ChainAddr2 + 3,WordCount)

      /* write channel mode words */
ChanModeH = 0x0004;     /* interrupt on Terminal Count after
                  reading the chaining table */
ChanModeL = 0x0252;
WriteMem(ChainAddr2 + 4,ChanModeH)
WriteMem(ChainAddr2 + 5,ChanModeL)

/*  SET UP THE CHAIN TABLE FOR CHANNEL 1 IN MEMORY */
      /* write the Reload word at the top of the Chain Table.
      The Reload word calls for loading the following registers:
      Current Address Reg. B (2 words)
      Current Operation Count (1 word)
      Base Address Reg. B (2 words)
      Base Operation Count (1 word)
      Channel Mode (2 words) */
```



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```
WriteMem(ChainAddr1 ,0x1d2)
DataTablAdrH = ((DataTableAddr > > 8)
      &&0xff00||0x00c0)
DataTablAdrL = DataTableAddr&&0x0000ffff

      /* write pre-trigger starting address into chain table */
WriteMem(ChainAddr1 + 1,DataTablAdrH)
WriteMem(ChainAddr1 + 2,DataTablAdrL)

      /* write word count */
WriteMem(ChainAddr1 + 3,WordCount)

      /* write the base address into chain table */
WriteMem(ChainAddr1 + 4,DataTablAdrH)
WriteMem(ChainAddr1 + 5,DataTablAdrL)

      /* write base word count */
WriteMem(ChainAddr1 + 6,WordCount)

      /* write channel mode words */
ChanModeH = 0x0004;

      /* interrupt on terminal count after reading
      the chaining table */
 ChanModeL = 0x9052
WriteMem(ChainAddr1 + 7,ChanModeH)
WriteMem(ChainAddr1 + 8,ChanModeL)

/* SETUP THE THRESHOLD */

      /* set the trigger enable, positive transition */
WriteReg(DevAdr + THRSH,0x01e0)

/* START THE 9516 CHAIN LOAD ON CHANNEL 1  */

      /* Load the address of the Channel #1 Command Register*/
WriteReg(DevAdr+ DMAPointerReg,0x002e)
```



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```
      /* Start Ch. #1 Chaining */
WriteReg(DevAdr + DMACommandReg,0x00a0)

/* START THE 9516 CHAIN LOAD ON CHANNEL */
      /* Load the address of the Channel #2 Command Register*/
WriteReg(DevAdr+ DMAPointerReg,0x002c)
      /* Start Ch. #2 Chaining */
WriteReg(DevAdr+ DMACommandReg,0x00a1)

/* START ACQUISITION */
      /*Start the ADC sampling */
WriteReg(DevAdr + CSR,0x8012)
}
```

### 5.5.6 Driver Excerpt for DMA Operations

The following is an excerpt from the DAS driver that sets up the DMA controller.

```
      /* #define DEBUG */
#include <dvx.h>
#include <sys/types.h>
#include < sys/errno.h >
#include <sys/param.h>
#include < sys/buf.h >
#include <sys/ulser.h>
#include < sys/uio.h >
#include < machine/psl.h >
#include <sundev/mbvar.h>
#include < sundev/dvx2502io.h >
#include <sundev/dvx2502.h>

      /* maximum DMA block size for this device*/
#define     AV__MAX__BLK__SIZE    0x10000
#define     CLOCK__TICK  15

      /* allocate buffers */
struct buf dvxbuf[NDVX];
```



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```
      /* system structure definitions */
struct AV25deviceAV25device[NDVX];
int dvxattach( ),dvxintr( ),dvxprobe( );
struct mb__device*dvxinfo[NDVX];
struct mb__driver dvxdriver = {
      dvxprobe,0,dvxattach,0,0,dvxintr,
      sizeof(struct AV__regs),"dvx",dvxinfo,0,0,0};

      /* The following program sets up the AM9516A for straight
      DMA, Pre- and Post-trigger data acquisition. */

      /* dvxstrategy:  DMA strategy routine */
dvxstrategy(bp)
register struct buf*bp;
{
register struct mb__device*md;
register struct AV25device*av;
register struct AV__regs*regs;
register struct ChainBlk*cbp;
register struct ChainBlk*cb; }
int unit;
int s,i,j,k;
short *addr,*addrl;
long CHANNEL__MODE;

#ifdef DEBUG
short *caddr;
printF("/nDVXstrategy:");
#endif

      /*get unit number from buf structure */
unit = minor(bp→b__dev);
md = dvxinfo[unit];av
= &AV25device[unit];

      /*register base address*/
regs = (struct AV__regs*)md→md__addr:
```



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```
      /*chain reload block*/
      /*Post-trigger*/
cb = (struct ChainBlk *)&AV25device[unit].ChainBlk[0];
      /*Pre-trigger*/
cbp = (struct ChainBlk *)&AV25device[unit].ChainBlk[1];

      /*raise priority level*/
s = splx(pritospl(md->md__intpri));

      /* sleep while resources in use */
while(av->busy)
sleep((caddr__t)av,AVPRI);

      /* ready to start DMA */
      av->busy = 1;
      av->bp = bp;

      /* clear out the FIFO with a reset */
      i = regs->offset;        /* save offset reg. */
      j = regs->ratediv;       /* save rate reg */
      k = regs->thresh;        /* save threshold reg. */
      regs->csr = AV__RESET;   /* apply the RESET */
      regs->cst = avcontrol__reg;
      regs->offset = i;        /* restore the offset reg. */
      regs->ratediv = j;
      regs->thresh = k;

      /* grab bus resources */
      av->mbinfo = mbsetup(md->md-hd,bp,0);

      addr1 = addr = (short *)MBI__ADDR(av->mbinfo);

#ifdef DEBUG
caddr = (short *)(int)addr + 0xff00000);
print("/nDVXstrategy: Unit = %x, DMA Virt. Addr =
%x",unit,addr);
#endif
```



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```
        /* check pre trigger buffer size */
        if (regs→thresh & AV__TRIG__SEL)
        if ( ((bp→b__bcount>>1)< = avPreTrigBufSz)
        ||(av→PreTrigBufSz==0))
{
        av→error = EINVALIDPREBUFSZ;
        dvxbuf[unit].b__flags  = B__ERROR;
        mbrelse(md→md__hd,&avmbinfo);
        av→busy = 0;
        (void) splx(s);
        iodone(&dvxbuf[unit]);
        return;
}

        /*check for 24 bit address */
if( (int)addr & 0xff000000 )
{
        /*ERROR if physical address is > than 24 bits */
        av→error = EINVALIDDMAADDRESS;
        dvxbuf[unit].b__flags |= B__ERROR;
        mbrelse(md→md__hd, &av→mbinfo);
        av→busy = 0;
        (void) splx(s);
        iodone(&dvxbuf[unit]);
        return;
}
        /* set up chain reload block in device structure for pre
trigger chan.*/
        if(regs→thresh & AV__TRIG__SEL)
        {

#ifdef DEBUG
print("/nDVXstrategy: Setting up Pre-Trigger DMA channel");
#endif
        /* chain reload word */
        cpb→LoadCtl = CHAIN__RELOAD;
```



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```
        /* DMA word count */
        cpb→BCount = cpb→Count = av→PreTrigBufSz;

        /* current and base addresses */
        cpb→AddrL = cbp→BAddrL=(short)((int)addr & 0xffff);
        cbp→AddrH = cbp→BAddrH=(short)(((int)addr>> 8)&0xff00)
        | ADDRESS__REF|(WAIT__STATES<<1);

        /* channel mode register */
cbp→ModeH = (short)( (CHANNEL__MODE>>16)&0xffff);
cbp→ModeL = (short)( CHANNEL__MODE & 0xffff );
cbp→ModeL | = BC__TC; /* base to current reload on term. cnt

        /*load 9516 chain address register */
        regs→am9516ptr = AM__CAR__LOW+2;
        i = (int)addr + sizeof(struct ChainBlk);
        regs→am9516dat = (short)(i & 0xffff );

        regs→am9516ptr = AM__CAR__UP+2;
        regs→am9516dat =
        (short)((((int)i>>8)&0xff00)|(WAIT__STATES<<1));

        addr = (short *)((unsigned int)addr+av→PreTrigBufSz<<1);
        }
        /* set up chain reload block in device structure for
        post channel */
        /* chain reload word */
        cb→LoadCtl = CHAIN__RELOAD;

        /* DMA word count */
        cb→BCount = cb→Count = (bpb__bcount>>1);

        /* current and base addresses */
        cb→AddrL = cb→BAddrL = (short)((int)addr & 0xffff);
        cb→AddrH = cb→BAddrH = (short)(((int)addr>>8)&0xff00)
              |ADDRESS__REF|(WAIT__STATES<<1);
```



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```
        /* channel mode register */
        cb→ModeH = (short)( (CHANNEL__MODE>>16) & 0xffff);
        cb→ModeL = (short)(CHANNEL__MODE & 0xffff);
        cb→ModeL | = INT__TC;/* interrupt on terminal count */

        /*load 9516 chain address register */
        regs→am9516ptr = AM__CAR__LOW;
        regs→am9516dat = (short)((int)addr1 & 0xffff);

#ifdef DEBUG
printf("/nDVXstrategy: Chain Addr Lo Addr = %x
Dat = %x",AM__CAR__LOW,regs→am9516 dat);
#endif
        regs→am9516ptr = AM__CAR__UP; regs→am9516dat = (short)
        ((((int)addr>>8)&0xff00)
        |(WAIT__STATES<<1) );

#ifdef DEBUG
print("/nDVXstrategy: Chain Addr Hi Addr = %x
Dat = %x",AM__CAR__UP,regs→am9516dat);
#endif

        /* move the 9516 parameters into the top of the user's
        buffer /*
        uiomove((caddr__t)cb,(sizeof(struct ChainBlk)<<1),
                                UIO__READ,av→uio);
```



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```
#ifdef DEBUG
print("/nDVXstrategy:Phys Addr = %x, Data = %x",caddr,caddr[0]);
print("/nDVXstrategy:Phys Addr = %x, Data = %x",caddr,caddr[1]);
#endif

      /* bootstrap the 9516 to begin DMA */
      /* point to command register */
      regs→am9516ptr = AM__CMDR;
      if ( regs→thresh & AV__TRIG__SEL)
      /* start channel 1 chaining */
      regs→am9516dat = ST__CHAIN__1;
      /* start channel 2 chaining */
      regs→am9516dat = ST__CHAIN__2;
      /* start up the converter if the external start mode is
      NOT selected */
      if ( (av→control__reg & AV__XSTART__STOP) = = 0)
            av→control__reg | = AV__START__STOP;
            regs→csr = avcontrol__reg;
      }
(void)splx(s);    /* restore CPU priority */
}
```



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# Section 6
# Specifications

*Unless otherwise noted all specifications apply at +25°C.*

## Analog Inputs

| | |
|---|---|
| Input voltage ranges | ±10V (Model B10), ± 5V (Model B05 ), or 0 to + 10V (Model U10) |
| Input Bias current | 5 nA max. |
| Input Resistance | 100 MOhms typ. |
| Input Capacitance | 70 pF max. |
| Common Mode voltage | ± 10V max. |
| Input Overvoltage Protection | ± 25V max. |
| Input Current Protection | 50 mA max. |
| Connector Type | D type 25 pin (mates with ITT Cannon DB 25P or TRW-Cinch DB25P) |

## Amplifier Characteristics

| | |
|---|---|
| Gain | 1,2,4,8 |
| Gain accuracy | ±0.02% |
| Offset | 10 mV max. |
| Slew rate | 12 V/µs min. (8700); 80 V/µs min. (8701) |
| CMRR | 100 dB @ 60 Hz Typ. |
| Settling time | 1.5 µs typ., to 0.001% of 10V step @ Gain = 1 |
| Full Power Bandwidth | 400 kHz |

## Dynamic Characteristics

| | |
|---|---|
| Aggregate Conversion rate | 204.8 Ksamp/s max. (8700); 409.6 Ksamp/s max. (8701) |
| Noise | (0.5 LSB + 50 µV) rms, Referred to input over 700 kHz equiv. noise bandwidth. |
| Differential crosstalk | -100dB @ 1 kHz (8700); -90 dB @ 1 kHz (8701) |
| S/H Aperture Delay | 25 ns typ. |
| S/H Aperture Jitter | 400 ps rms max. (8700); 100 ps rms max. (8701) |
| S/H Feedthrough | -90 dB typ. @ 1 khz |
| S/H Acquisition Time | 2.0 µs max. typ. (8700); 800 ns max. typ. (8701) |
| Peak Distortion | -91 dB typ. @ 10 kHz (±10V differential input signal) |

*Peak Distortion represents the ratio between the highest spurious frequency component below the Nyquist rate and the signal.*

Total Harmonic Distortion ..... -90 dB typ. @ 10 kHz (±10V differential input signal)

*Total Harmonic Distortion represents the ratio between the rms sum of all harmonics up to the 20th harmonic and the rms value of the signal.*



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## Transfer Characteristics

| | |
|---|---|
| Resolution | 16 bits |
| Integral Non-Linearity | ±.002% of FSR ±0.5 LSB |
| Quantization Error | ±0.5 LSB max. |
| Integral Non-Linearity | ±0.003% FSR max. |
| No Missing Codes | Guaranteed<br>0°C to +50°C |
| Monotonicity | Guaranteed |
| Gain Error | 0.01% of FSR |
| Offset Error | 0.01% of FSR |

## Stability (0° C to + 50° C)

| | |
|---|---|
| Recommended warm-up time | 15 Minutes |
| Offset Tempco | 50 µV/°C max. |
| Gain Tempco | 20 ppm FSR/°C max. |
| Differential Non-Linearity Tempco | ±1 ppm FSR/°C max. |
| Precision Clock | 3.6864 MHz + 0.001% |

## Trigger Modes

| | |
|---|---|
| Internal | Derived from an on-board precision clock or received from a Master Trigger module within the system. |
| External | Supplied by the User. |
| Data Dependent | Generated at the occurrence of a predefined value on a monitored channel. |

## Data Transfer

| | |
|---|---|
| Output coding | Two's complement, Offset Binary, Binary. |
| Via VMEbus | 16-bit word transfer by means of an on-board DMA controller using a 1024 word FIFO buffer. |
| Interrupts | 7-level, jumper configurable. |
| Via VXIbus | 2 successive byte transfers to the adjacent slot on the left (towards slot 0). |

## Sequence Controller

| | |
|---|---|
| Number of steps | 2048 |
| Gain change capability | Every cycle |
| Max no. of addressable channels | 256 |
| Sampling rate | 3.6 kHz to 409.6 kHz in 1000 steps. |

## Power Requirements

| | |
|---|---|
| Input Voltage | 5.0V ±5% |
| Power Dissipation | 20W max. |



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## Environmental

| | |
|---|---|
| Operating Temperature Range | 0° to +50°C |
| Storage Temperature | -25 °to +75 °C |
| Relative Humidity | 0 to 85% non-condensing, up to +40 °C |
| Recommended Forced Air Cooling | 10 CFM |

## Digital Inputs/Outputs

| | |
|---|---|
| Logic Levels | TTL/CMOS compatible<br>Logic 0: 0.8V max.<br>Logic 1: 2.0V min. |
| External Trigger | TTL Active low, 150 ns min., 200 ns max., 50 Ohms |
| External Start | TTL Active Low, 50 Ohms |
| Multiple-channel S & H command | TTL (on P2) Active High |
| S & H Complement | TTL (on P2) Active Low |
| Remote Trigger | TTL (on P2) Active High |
| External Strobe | TTL (on P2) Active High |

## VME Data Transfer Rates

Actual data transfer rates for the DMA operations are highly dependent upon system configuration and system operation. The latency of the VME bus resident memory boards, the relative position of the DAS on the bus request daisy chain, the length of time other bus masters retain control of the bus, and other factors degrade the maximum data rates achievable on the VME bus. The DAS can sustain an average data rate of 1.2 million words per second when there is no contention for the VME bus mastership. The user can approximate the expected transfer rate by calculating the minimum transfer time per word as 600 ns plus the maximum write cycle time of the target bus memory.



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# Appendix A

## A.1 VMEIVXI COMPLIANCE

The DAS conforms to the VMEbus Specification Rev. C.1 and has the following compliance code.

MA24, MD16, SAD016, SAD024, SD16, 11-7 (ROAK & RORA)

The DAS conforms to the VXIbus Specification Rev. 1.4 for register based cards. It is a class 1 (TTL) user of the P2 connector based local buses A and C.

## A.2 CONNECTOR PIN ASSIGNMENTS

### A.2.1 Analog Input Connector (J1)

| Pin # | Signal | Pin # | Signal |
|---|---|---|---|
| 1 | Input 5 + | 14 | Input 3 Guard |
| 2 | Input 5 – | 15 | Input 3 – |
| 3 | Input 5 Guard | 16 | Input 3 + |
| 4 | Input 7 + | 17 | Input 1 Guard |
| 5 | Input 7 – | 18 | Input 1 – |
| 6 | Input 7 Guard | 19 | Input 1 + |
| 7 | Input 0 + | 20 | Input 6 Guard |
| 8 | Input 0 – | 21 | Input 6 – |
| 9 | Input 0 Guard | 22 | Input 6 + |
| 10 | Input 2 + | 23 | Input 4 Guard |
| 11 | Input 2 – | 24 | Input 4 – |
| 12 | Input 2 Guard | 25 | Input 4 + |
| 13 | Not Used | | |



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### A.2.2 VME Bus Connector (P1)

| Pin | Signal Mnemonics | | |
|---|---|---|---|
| | Row a | Row b | Row c |
| 1 | D00 | BBSY* | D08 |
| 2 | D01 | BCLR* | D09 |
| 3 | D02 | ACFAIL* | D10 |
| 4 | D03 | BG0IN* | D11 |
| 5 | D04 | BG0OUT* | D12 |
| 6 | D05 | BG1IN* | D13 |
| 7 | D06 | BG1OUT* | D14 |
| 8 | D07 | BG2IN* | D15 |
| 9 | GND | BG2OUT* | GND |
| 10 | SYSCLK | BG3IN* | SYSFAIL* |
| 11 | GND | BG3OUT* | BERR* |
| 12 | DS1* | Not Used | SYSRESET* |
| 13 | DS0* | Not Used | LWORD* |
| 14 | WRITE | Not Used | AM5 |
| 15 | GND | BR3* | A23 |
| 16 | DTACK* | AM0 | A22 |
| 17 | GND | AM1 | A21 |
| 18 | AS* | AM2 | A20 |
| 19 | GND | AM3 | A19 |
| 20 | IACK* | GND | A18 |
| 21 | IACKIN* | Not Used | A17 |
| 22 | IACKOUT* | Not Used | A16 |
| 23 | AM4 | GND | A15 |
| 24 | A07 | IRQ7* | A14 |
| 25 | A06 | IRQ6* | A13 |
| 26 | A05 | IRQ5* | A12 |
| 27 | A04 | IRQ4* | A11 |
| 28 | A03 | IRQ3* | A10 |
| 29 | A02 | IRQ2* | A09 |
| 30 | A01 | IRQ1* | A08 |
| 31 | Not Used | Not Used | Not Used |
| 32 | + 5V | + 5V | + 5V |

***NOTE:*** ***"Not Used" means that the VME/VXI signal is not connected on the card.***



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### A.2.3 VMEIVXI Bus Connector (P2)

| | Signal Mnemonics | | |
|---|---|---|---|
| Pin | Row a | Row b | Row c |
| 1 | Not Used | + 5V | Not Used |
| 2 | Not Used | GND | Not Used |
| 3 | Not Used | Not Used | GND |
| 4 | Not Used | Not Used | Not Used |
| 5 | LBUSA00 | Not Used | LBUSC00 |
| 6 | LBUSA01 | Not Used | LBUSC01 |
| 7 | Not Used | Not Used | GND |
| 8 | LBUSA02 | Not Used | LBUSC00 |
| 9 | LBUSA03 | Not Used | LBUSC01 |
| 10 | GND | Not Used | GND |
| 11 | LBUSA04 | Not Used | LBUSC00 |
| 12 | LBUSA05 | GND | LBUSC01 |
| 13 | Not Used | + 5V | Not Used |
| 14 | LBUSA06 | Not Used | LBUSC00 |
| 15 | LBUSA07 | Not Used | LBUSC01 |
| 16 | GND | Not Used | GND |
| 17 | LBUSA08 | Not Used | LBUSC00 |
| 18 | LBUSA09 | Not Used | LBUSC01 |
| 19 | Not Used | Not Used | Not Used |
| 20 | Not Used | Not Used | LBUSC00 |
| 21 | Not Used | Not Used | LBUSC01 |
| 22 | GND | GND | GND |
| 23 | TTLTRG0* | Not Used | TTLTRG1* |
| 24 | TTLTRG2* | Not Used | TTLTRG3* |
| 25 | Not Used | Not Used | GND |
| 26 | TTLTRG4* | Not Used | TTLTRG5* |
| 27 | TTLTRG6* | Not Used | TTLTRG7* |
| 28 | GND | Not Used | GND |
| 29 | Not Used | Not Used | Not Used |
| 30 | MODID | Not Used | GND |
| 31 | Not Used | Not Used | Not Used |
| 32 | Not Used | + 5V | Not Used |

***NOTE:*** ***"Not Used" means that the VME/VXI signal is not connected on the card.***



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# Appendix B

## NOTES ON DIELECTRIC ABSORPTION

The charging and discharging of capacitors is always associated with the phenomenon known as dielectric absorption. Charged and then discharged capacitors will exhibit residual charge for extended periods of time. The extent of effect is dependent upon the dielectric material used in the construction of the capacitor and the charge-discharge time relationship.

The charge on the Hold Capacitor in a Sample and Hold circuit is influenced by this phenomenon and the user MUST be aware of the consequences in the acquisition of data, for the stored residual charge will alter the subsequent signal voltage stored on the Hold capacitor.

The amount of alteration depends upon:

a) the amount of time that the Hold capacitor was tracking (sampling) the signal voltage

b) the amount of time the Hold capacitor was holding the voltage before the instant of conversion

c) the physical properties of the dielectric and the mechanical construction of the Hold capacitor

The error voltage caused by dielectric absorption can be calculated from the following expression:

$$Err = \Delta Vin \bullet K \bullet \log_{10}[\, 1 + (Th/Ts)\,]$$

where,

$\Delta Vin$ = the voltage difference between the previous and the current samples

K = 0.0001, the dielectric absorption factor for the hold capacitor in the S/H circuits used in the S/H MUX

Ts = the period that the sample/hold circuit is in the 'sample' or 'track' mode

Th = the period between the end of the sample period and the instant of conversion.



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Observe that if the input signal to a channel is a fixed level, or if Ts >> Th, then Err ≈ 0.

The sample period Ts is controlled by the user via the DAS card and the hold time Th is determined by position of the channel in the scan sequence. The first channel will have the minimum error while the last channel in the scan will have the maximum error. Therefore, it is recommended that those channels with the greatest signal swing from sample to sample or requiring most precision be located in the beginning of the scan sequence.

For example, calculate the error for the 1st, 16th, and 32nd channels in a sequence where the sample time Ts = 500.0 μs and the hold time for the channel, at 200 kHz sampling rate is Th, = 5N μs where N = the Nth channel in the scan. Assume that the voltage change on any given channel will be the full scale voltage of 20 volts.

For the 1st channel,

$$Err = Vin \cdot K \cdot Log_{10} [\, 1 + (Th/Ts) \,]$$
$$Err = 20 \cdot 0.0001 \cdot Log_{10} [\, 1 + (5.0/500.0) \,]$$
$$Err = 8.64\ \mu V, \text{ or } 0.028\ LSB$$

For the 16th channel,

$$Err = 20 \cdot 0.0001 \cdot Log_{10} [\, 1 + 16(5.0)/500.0 \,]$$
$$Err = 128.9\ \mu V, \text{ or } 0.43\ LSBs$$

For the 32nd channel,

$$Err = 20 \cdot 0.0001 \cdot Log_{10} [\, 1 + 32(5.0)/500.0 \,]$$
$$Err = 241.1\ \mu V, \text{ or } 0.804\ LSBs$$

On the other hand, if Ts = 5.0 μs, then for the 1st channel,

$$Err = 20 \cdot 0.0001 \cdot Log_{10} [\, 1 + 5.0/5.0 \,]$$
$$Err = 602\ \mu V, \text{ or } 2.0\ LSB$$

and for the 16th channel,

$$Err = 20 \cdot 0.0001 \cdot Log_{10} [\, 1 + 16(5.0)/5.0 \,]$$
$$Err = 2461\ \mu V, \text{ or } 8.2\ LSBs$$



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P/N 82–5097
Revision 0
March 1993

***NOTE:*** ***This manual applies to revision 4 and following DBS 8700 and DBS 8701 VXI Data Acquisition Systems.***

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