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High Precision Digitizers 16-Bit at 200 kHz or 400 kHz

in a "C" Size VXI Module

Introduction

The DBS 8700/8701 features the first 200 kHz/400 kHz, high resolution, multi-channel Digitizing Systems that combine the superior precision of 16-bit measurement with high throughput in a "C" size VXI module. Fully compatible with VXI specification Rev. 1.3, a DBS 8700/8701 occupies a single slot in a "C" size VXI chassis and provides an unparalleled price/performance ratio when used alone or in combination with other VXI modules (multiplexers, or digital-to-analog converters) within the Analogic DBS 8700/8701 series. Reflecting the many years of Analogic experience in precision instrumentation, a DBS 8700/8701 is designed to meet the stringent demands of fast and accurate measurements associated with multichannel applications such as vibration analysis, the testing of rotating machinery, and automotive and jet engine testing, as well as the analysis of large mechanical structures and other complex mechanisms.

Eight shielded, differential inputs are provided with both voltage and current protection. The unit is directly expandable to 256 channels with the Analogic family of DBS multiplexer modules. Input signals are multiplexed via an instrumentation amplifier and a programmable gain amplifier, with four software selectable gains, into an ultrafast, high resolution, sampling analog-to-digital converter. The acquisition time, hold-mode settling time and droop rate ensure 16-bit system performance up to the maximum sampling rate.

The DBS 8700/8701 provides a powerful 2-channel, on-board DMA controller as a standard feature. The DMA controller executes fast transfers over the VMEbus (P1) sending data directly into the system's memory, significantly enhancing total system performance by dramatically reducing the I/O overhead of the bus.

Three flexible trigger sources are available: a user-supplied outside trigger, an internal trigger derived from a precision clock residing on the module, and a data dependent trigger produced by the occurrence of a specified event on a selected channel. Before beginning the data acquisition, trigger information, as well as channel selection inside a scan, and gain setting are downloaded into the timing and control unit resident on the DBS 8700/8701 module. For ease of integration, a selection of available software drivers is offered for use with the card. No coding is required by the user; all necessary commands are included in the driver.

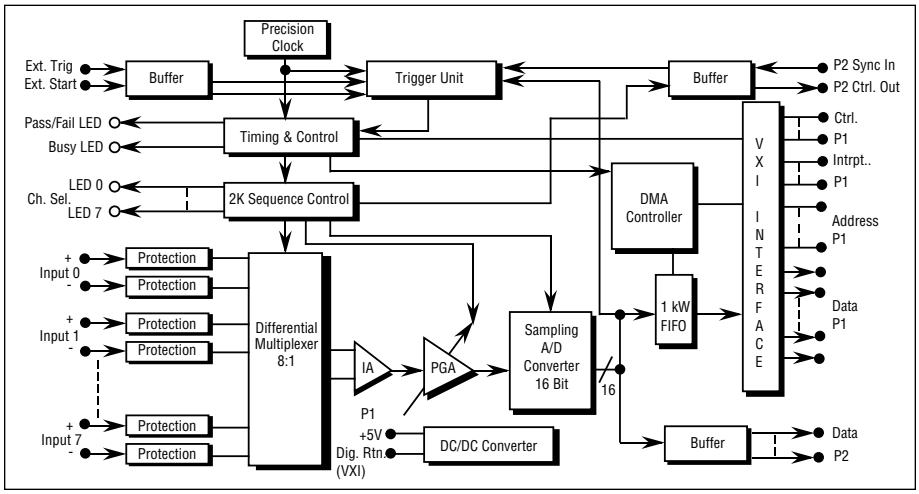
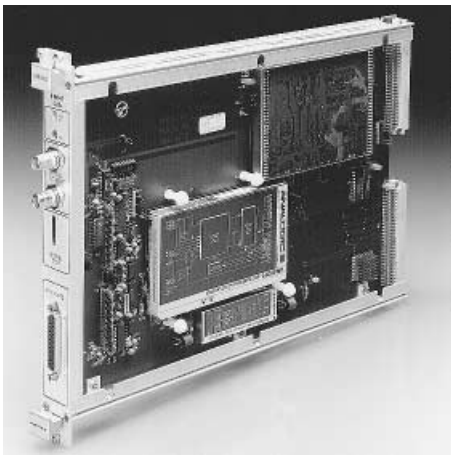


Figure 1. The DBS 8700/8701 Block Diagram.



Features

- 16-Bit Resolution & Accuracy
- 200 kHz or 400 kHz Throughput Rate
- On-Board Sequencer
- 8 Differential Inputs
- Expandability up to 256 Channels
- Simultaneous Sampling via Companion Multiplexer Module DBS 8710
- Dynamically Set Gain per Channel
- Peak Distortion –96 dB (DBS 8700) –91 dB (DBS 8701)
- Variable Sampling Rate
- Multiple Sample Clock Sources
- Versatile Trigger Unit
- Software Drivers Available

Applications

- Real Time Data Acquisition
- Precision Instrumentation
- Automatic Test Equipment
- Monitoring and Control

VXI bus

CE

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DBS 8700/8701

Specifications[1]

ANALOG INPUTS	DBS 8700			DBS 8701		
Number of Channels	8 differential, expandable to 256			8 differential, expandable to 256		
Input Ranges	**DBS 8700-B05**	**DBS 8700-B10**	**DBS 8700-U10**	**DBS 8701-B05**	**DBS 8701-B10**	**DBS 8701-U10**
Gain 1	±5V,	±10V,	0 to +10V	±5V,	±10V,	0 to +10V
Gain 2	±2.5V,	±5V,	0 to +5V	±2.5V,	±5V,	0 to +5V
Gain 4	±1.25V,	±2.5V,	0 to +2.5V	±1.25V,	±2.5V,	0 to +2.5V
Gain 8	±0.625V,	±1.25V,	0 to +1.25V	±0.625V,	±1.25V,	0 to +1.25V
Input Bias Current	5 nA Max.			5 nA Max.		
Input Resistance	100 MΩ Typ.			100 MΩ Typ.		
Input Capacitance	70 pF Max.			70 pF Max.		
Common Mode Voltage	±10V Max.			±10V Max.		
Input Overvoltage Protection	±25V Max.			±25V Max.		
Input Current Protection	50 mA Max.			50 mA Max.		
CLOCK/TRIGGER INPUTS						
Logic Levels, LSTTL/CMOS Compatible						
Logic "0"	0.8V Max.			0.8V Max.		
Logic "1"	2.0V Min.			2.0V Min.		
Termination	50Ω			50Ω		
AMPLIFIER CHARACTERISTICS						
Gain	1, 2, 4, 8 (±0.02% Max.)			1, 2, 4, 8 (±0.02% Max.)		
Offset Voltage	±10 mV Max.			±10 mV Max.		
Slew Rate	12 V/µs Min.			80 V/µs Min.		
CMRR	100 dB @ 60 Hz Typ.			100 dB @ 60 Hz Typ.		
Full Power Bandwidth	200 kHz			400 kHz		
Settling Time To ±0.001% (10V Step, Gain = 1)	1.5 µs Typ.			1.5 µs Typ.		
DYNAMIC CHARACTERISTICS						
Maximum Sampling Rate	204.8 kHz			409.6 kHz		
Noise	(0.5 LSB + 30 µV) RMS			(0.5 LSB + 50 µV) RMS		
(Referred to input and measured over 700 kHz equivalent noise bandwidth)						
Differential Crosstalk	–96 dB (@ 1 kHz) Typ.			–90 dB (@ 1 kHz) Typ.		
S/H Aperture Delay	25 ns Typ.			25 ns Typ.		
S/H Aperture Jitter	±400 ps RMS Max.			±100 ps RMS Max.		
S/H Feedthrough	–90 dB (@ 1 kHz) Typ.			–90 dB (@ 1 kHz) Typ.		
Peak Distortion[2,4]	–96 dB Typ. (@ 10 kHz)			–91 dB Typ. (@ 10 kHz)		
Total Harmonic Distortion[3,4]	–91 dB Typ. (@ 10 kHz)			–90 dB Typ. (@ 10 kHz)		
TRANSFER CHARACTERISTICS (A/D CONVERTER)						
Resolution	16 Bits			16 Bits		
Quantization Error	±0.5 LSB Max.			±0.5 LSB Max.		
Integral Non-Linearity	±0.003% FSR Max.			±0.003% FSR Max.		
No Missing Codes	Guaranteed from 0°C to +50°C			Guaranteed from 0°C to +50°C		
Full Scale Range (Gain Accuracy)	±0.01%			±0.01%		
Monotonicity	Guaranteed			Guaranteed		
STABILITY (0°C TO +50°C)						
Required Warm-up Time (for ultimate specifications)	15 minutes			15 minutes		
Offset Tempco	50 µV/°C Max.			50 µV/°C Max.		
Gain Tempco	20 ppm FSR/°C Max.			20 ppm FSR/°C Max.		
Differential Non-Linearity Tempco	±1 ppm FSR/°C Max.			±1 ppm FSR/°C Max.		
Precision Clock	±10 ppm, 0-50°C			±10 ppm, 0-50°C		
Recommended Recalibration Interval	6 months			6 months		
TRIGGER (START/STOP) MODES						
Internal	Software write to register. Automatically synchronized with on-board precision clock.			Software write to register Automatically synchronized with on-board precision clock.		
External (TTL Active Low)	Via front panel BNC or TTLTRG Line			Via front panel BNC or TTLTRG Line		
Data Dependent	Generated at the occurrence of a predefined value and slope, at a specified channel			Generated at the occurrence of a predefined value and slope, at a specified channel		

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SAMPLE CLOCK	DBS 8700	DBS 8701
	Internal via programmable, 10 bit divider and 3.6864 MHz ±0.001% Clock. Produces 3.6k samples/sec to 204.8k samples/sec in 1006 steps.	Internal via programmable, 10 bit divider and 3.6864 MHz ±0.001% Clock. Produces 3.6k samples/sec to 409.6k samples/sec in 1015 steps. .
	External, 2.5 MHz to 4.0 MHz, TTL, 50% duty cycle clock via front panel BNC connector & Internal, programmable 10-bit divider. Min. sample rate = 2.5 MHz ÷ 1023 = 2.4k samples/sec.	External, 2.5 MHz to 4.0 MHz, TTL, 50% duty cycle clock via front panel BNC connector & Internal, programmable 10-bit divider. Min. sample rate = 2.5 MHz ÷ 1023 = 2.4k samples/sec.
	External, 0 to 204.8 kHz sample clock via front panel BNC connector or P2 TTLTRG line per VXI spec. Clock signal is TTL active low, edge triggered with low period = 150-200 ns.	External, 0 to 409.6 kHz sample clock via front panel BNC connector or P2 TTLTRG line per VXI spec Clock signal is TTL active low, edge triggered with low period = 150-200 ns.
	Master/slave(s) for sychronizing multiple modules via P2 TTLTRG line per VXI spec.	Master/slave(s) for sychronizing multiple modules via P2 TTLTRG line per VXI spec. .
DATA TRANSFER		
Output Coding	Binary, Offset Binary, Two's Complement	Binary, Offset Binary, Two's Complement
Via VMEbus	16-bit word transfer via on-card DMA into VXI A24 Memory using a 1k word FIFO buffer	16-bit word transfer via on-card DMA into VXI A24 Memory using a 1k word FIFO buffer
Data Buffers	Single buffer = 65K words Max. Multiple buffers limited only by available system A24 memory. Continuous Acquisition via multiple swinging buffers.	Single buffer = 65K words Max. Multiple buffers limited only by available system A24 memory Continuous Acquisition via multiple swinging buffers.
Interrupts	FIFO status or DMA memory buffer filled	FIFO status or DMA memory buffer filled
Via VXI Local Bus	2 successive bytes transfer to adjacent slot	2 successive bytes transfer to adjacent slot
VXI/VME COMPLIANCE		
VXI	Register Based, Local Bus User	Register Based, Local Bus User
VME	A24/16, D16, I1, Slave A24, D16 Master (DMA)	A24/16, D16, I1, Slave A24, D16 Master (DMA)
SCAN SEQUENCE CONTROLLER		
Number of Steps	1024	1024
Gain Change Capability	Every scan list entry. Rated performance maintained.	Every scan list entry. Rated performance maintained.
Maximum Number of Multiplexed Channels	256 when using companion multiplexer modules.	256 256 when using companion multiplexer modules.
FRONT PANEL INDICATORS		
Pass/Fail LED	Green/Red	Green/Red
Busy LED	Red	Red
Channel Selection	Green	Green
POWER REQUIRED		
+5V Supply	+4.75V Min., +5.25V Max.	+4.75V Min., +5.25V Max.
Power Consumption	20W Max.	20W Max.
ENVIRONMENTAL AND MECHANICAL		
Temperature Range Rated Performance	0°C to +50°C	0°C to +50°C
Storage	–25°C to +75°C	–25°C to +75°C
Relative Humidity	0 to 85% non-condensing up to +40°C	0 to 85% non-condensing up to +40°C
Cooling	1.2 litre/sec. airflow for 10°C rise at 0.29 mm H_2O back pressure	1.2 litre/sec. airflow for 10°C rise at 0.29 mm H_2O back pressure
Dimensions	VXI "C" Size	VXI "C" Size
Front Panel Potential	Chassis Ground	Chassis Ground
Weight	3 Lb, 6oz/1.53 Kg	3 Lb, 6oz/1.53 Kg

NOTES:

1. Unless otherwise noted all specifications apply at +25°C.
2. Peak Distortion represents the ratio between the highest spurious frequency component below the Nyquist rate and the signal.
3. Total Harmonic Distortion represents the ratio between the RMS sum of all harmonics up to the 20th harmonic and the RMS value of the signal.
4. ±10V input signal.
5. Single gain setting per scan.

Specifications subject to change without notice.

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Ordering Guide

DBS 8700
16-Bit, 200 kHz DAS/Digitizer
DBS 8700 – B05 – Bipolar, ±5V
DBS 8700 – B10 – Bipolar, ±10V
DBS 8700 – U10 – Unipolar, 0 to ±10V

DBS 8701
16-Bit, 400 kHz DAS/Digitizer
DBS 8701 – B05 – Bipolar, ±5V
DBS 8701 – B10 – Bipolar, ±10V
DBS 8701 – U10 – Unipolar, 0 to ±10V

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