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User's Manual



DBS 8751A
DBS 8752A

16-bit, 200 kHz, 4-Channel, Register-Based, D/A Waveform Generator

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Revision 1

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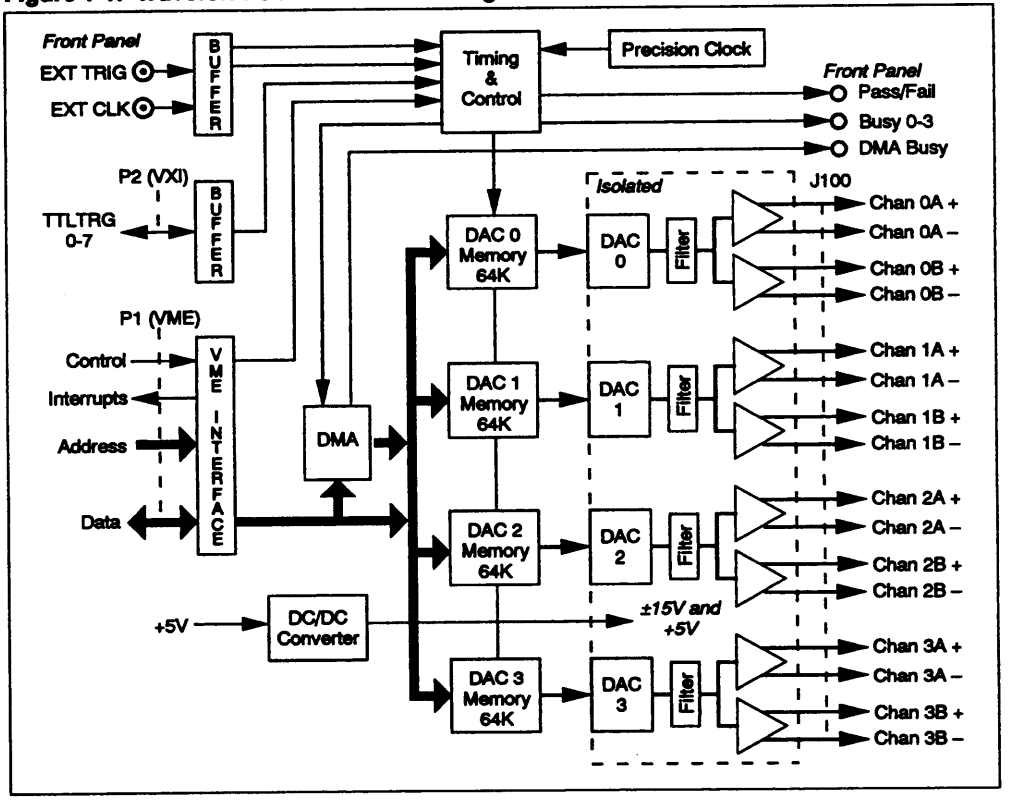
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Section 1
Introduction

1.1 PRODUCT DESCRIPTION

The DBS 8751A or DBS 8752A is a high-speed, 16-bit, four-channel Waveform Generator (Figure 1-1). It is a VXIbus register-based instrument packaged in a C-size module. Both models operate identically except for the full-scale output voltage range. The output range for the DBS 8751A is ±6-volts single-ended or ±3-volts differential, and for the DBS8752A is ±10-volts single-ended or ±5-volts differential.

Figure 1-1. Waveform Generator Block Diagram



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Each of the four independent analog output channels consists of a 64K-word block of memory, a high-speed Digital-to-Analog Converter (DAC), a by-passable 6-pole Butterworth filter, and output amplifier. The DAC memory outputs and control signals are transformer-coupled to the isolated analog output circuit of each channel. The output of each DAC passes through an internal inverting deglitching amplifier before being fed to a six-pole reconstruction filter. By means of a hardware jumper, the filter can be bypassed, connecting the deglitching amplifier output of the DAC directly to the input of the output amplifier. Two differential output amplifiers are connected to each DAC port. Using hardware jumpers, the output amplifiers can be configured as differential or single-ended outputs. All supply voltages for the isolated analog section are generated by a low-noise, DC-to-DC converter.

The data representing the waveform to be generated by each DAC is stored in a 64-Kword data table memory in two's complement format. Only one waveform can be stored in memory at a time. Data is transferred to DAC memory via programmed I/O or DMA cycle.

Each DAC channel can operate independently in the Loop, One-Shot or Hold mode, allowing the generation of four completely independent signals. In the Hold Mode, the DAC outputs a single value. In the Loop Mode, each successive location of the data table is read and loaded into the DAC. When triggered in the One-Shot mode, the waveform is generated only once. When all words in the data table have been read, the DAC memory controller loops back to the beginning (location zero) of the data table. When triggered internally, a One-Shot port generates the waveform only once, after which a command is given to stop and re-arm the One-Shot circuitry. When triggered externally, a One-Shot port generates the waveform only once, halts, re-arms the trigger circuitry and awaits the next trigger pulse.

The Sampling Rate Clock is derived from a programmable clock divider fed by either the 3.6864-MHz Internal Precision Clock or an External Precision Clock received either from the front panel EXT CLK input or the VXIbus on TTLTRG0, 1, 2, or 3. With the Internal Precision Clock, the rate divider can produce up to 1006 software-selectable sampling rates from 204.8 kHz to 3.603 kHz.

For synchronizing waveform generation with an external event, an External Precision Clock and External Trigger can be input from the front panel EXT CLK and EXT TRIG BNC connectors, respectively, or via TTLTRG lines.

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The EXT CLK and EXT TRIG inputs operate independently. EXT TRIG can be used with either the Internal Precision Clock (internally synchronized with EXT TRIG) or the EXT CLK input (user synchronized with EXT TRIG). When using both the EXT CLK and EXT TRIG inputs together, certain timing requirements must be met. Refer to Section 3, Operation.

Under software control, the eight TTLTRG lines of the VXIbus can be enabled to receive external clocks and triggers. TTLTRG0-3 are reserved for receiving an External Precision Clock and TTLTRG4-7 are reserved for External Trigger inputs. By installing a hardware jumper, the Sampling Rate Clock can be driven onto the VXIbus using any TTLTRG line to synchronize this instrument with a compatible Data Acquisition System (DAS) module. Also via a hardware jumper, the front panel EXT TRIG input can be driven onto the VXIbus on any TTLTRG line.

DMA operations are controlled by an on-board Universal DMA Controller (UDC) chip which can transfer data from the VXIbus resident memory to the DAC memory at up to a 0.8 Mbyte/second transfer rate. The UDC can down-load single waveform data tables into DAC data memory. Since each DAC has its own memory, a command is issued to select the DAC memory to receive the data. The UDC is then instructed to down-load the data table and interrupt the host upon completion of the transfer.

1.2 SERVICE AND TECHNICAL SUPPORT

If this product fails to operate upon arrival, contact your Analogic dealer or the Measurement and Control Division (MCD) at the Analogic factory in Peabody, MA, to arrange for an exchange. Upon contacting MCD, you will be given a Return Material Authorization (RMA) number.

To arrange for an exchange, contact MCD Order Entry:

Tel: (508) 977-3000, Ext. 3840 or 3844; FAX: (508) 977-6818

For technical assistance, contact MCD Applications Engineers:

Tel: (508) 977-3000 Domestic calls: Ext. 3876
International calls: Ext. 3011 or 3844

FAX: (508) 977-6814

To arrange for service, contact the Customer Service Office:

Tel: (508) 977-3000 Repairs: Ext. 3612 Parts: Ext. 3614

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Before contacting the Customer Service Office, have the following ready:

- ❑ Model number
- ❑ Serial number
- ❑ Purchase order number
- ❑ Quantity being returned
- ❑ A detailed description of the malfunction
- ❑ Your "Bill To" and "Ship To" addresses

Upon contacting the Customer Service Office, the Service Coordinator will provide you with the following:

- ❑ Customer service order number (CSO)
- ❑ Warranty status of the units being returned
- ❑ Repair charge, if any

The CSO number is your authorization number. Please write this number on your purchase order and shipping label.

Send all authorized returns to:

Analogic Corporation
8 Centennial Drive
Peabody, MA 01960
Attn: Receiving Dock B.
CSO# _____

After the material has been returned, you will receive an acknowledgement copy of the CSO which will be marked with the scheduled return date.

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Section 2
Preparation & Installation

2.1 OVERVIEW

This section provides instructions for setting up hardware jumpers and installing the instrument in a VXI chassis. After unpacking, carefully inspect the hardware for any damage that may have occurred during shipment. If necessary, contact the carrier to file a claim. Save the shipping carton and packing materials if for any reason you need to return the product for repair or replacement. For technical support or to return this product to the factory, refer to Section 1.2 for instructions.

CAUTION:  **This product contains components which are sensitive to electrostatic discharge (ESD). Be sure to follow proper procedures for handling, storing and transporting ESD-sensitive assemblies.**

2.2 HARDWARE JUMPERS

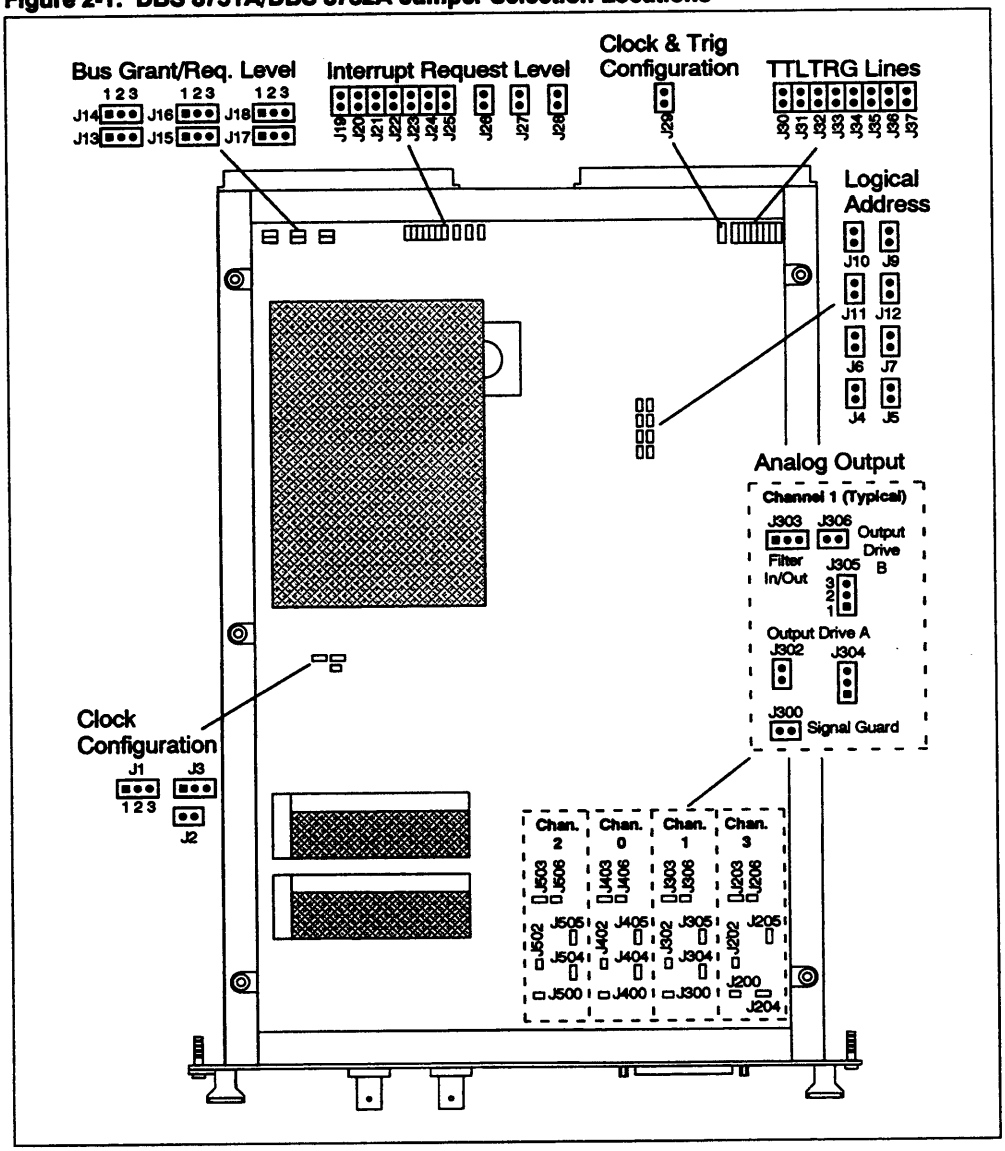
Before installing this instrument in a chassis, check Table 2-1 which summarizes jumper selection options and the selections made at the factory. To make changes, see the referenced Section and Figure 2-1.

Table 2-1. Hardware Jumper Setup Summary

Function	Ref. Sect.	Factory Setting	Jumper Selections			
Logic Addr. (DBS 8751A)	2.2.1	133	J5, J7, J10, J11 & J12 In; J4, J6 & J9 Out			
Logic Addr. (DBS 8752A)	2.2.1	134	J4, J7, J10, J11 & J12 In; J5, J6 & J9 Out			
Bus Grant/Req. Level	2.2.2	3	J13-1 to J14-1, J15-1 to J16-1, J16-2 to J16-3, J13-3 to J14-3, J15-2 to J15-3, J17-2 to J17-3			
Intr. Request Level	2.2.3	2	J24, J27 & J28; J26 Out			
Precision Clock Source	2.2.4	Internal	J1-2 to J1-3, J3-2 to J3-3 and J2 Out			
EXT TRIG to TTLTRG	2.2.5	Open	J29 Out			
TTLTRG Line	2.2.6	None	J30 through J37 Out			
			Chan 0	Chan 1	Chan 2	Chan 3
Output Signal Guard	2.2.7	Ana Gnd	J400 In	J300 In	J500 In	J200 In
Filter	2.2.7	In Line	J403:1-2	J303:1-2	J503:1-2	J203:1-2
Output Drive	2.2.7	Diff.	J402 Out	J302 Out	J502 Out	J202 Out
			J404:1-2	J304:1-2	J504:1-2	J204:1-2
			J405:1-2	J305:1-2	J505:1-2	J205:1-2
			J406 Out	J306 Out	J506 Out	J206 Out

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Figure 2-1. DBS 8751A/DBS 8752A Jumper Selection Locations



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2.2.1 Selecting the Base Address

The Base address of a VXI device is determined by the following:

Base Address = (Logical Address x 64) + 49152

The Logical Address of this instrument can be set from 0 to 255d using jumpers J4-J7 and J9-J12. Table 2-2 lists some examples. These jumpers determine the contents of the Base Address word described in Section 4.1

Table 2-2. Logical Address Selection Examples

	VXIbus Address Lines & Jumper Selections							
Logical Address	VA13 J9	VA12 J10	VA11 J12	VA10 J11	VA9 J7	VA8 J6	VA7 J5	VA6 J4
255	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
254	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN
252	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN
248	OUT	OUT	OUT	OUT	OUT	IN	IN	IN
240	OUT	OUT	OUT	OUT	IN	IN	IN	IN
224	OUT	OUT	OUT	IN	IN	IN	IN	IN
192	OUT	OUT	IN	IN	IN	IN	IN	IN
133	OUT	IN	IN	IN	IN	OUT	IN	OUT
2	IN	IN	IN	IN	IN	IN	OUT	IN

2.2.2 Selecting the Bus Grant/Request Level

As a Bus Master, this instrument uses a "Release-When-Done" type of request. The Bus Grant/Request level is jumper-selectable for levels 0-3 as shown in Table 2-3.

Table 2-3. Bus Grant/Request Jumper Selections

Level	Bus Req.	Bus Grant	BG0 In to BG0 Out	BG1 In to BG1 Out	BG2 In to BG2 Out	BG3 In to BG3 Out
0	J18: 2-3	J13-1 to J13-2 J14-1 to J14-2		J13-3 to J14-3	J15-1 to J16-1	J15-3 to J16-3
1	J18: 1-2	J13-2 to J13-3 J14-2 to J14-3	J13-1 to J14-1		J15-1 to J16-1	J15-3 to J16-3
2	J17: 1-2	J15-1 to J15-2 J16-1 to J16-2	J13-1 to J14-1	J13-3 to J14-3		J15-3 to J16-3
3	J17: 2-3	J15-2 to J15-3 J16-2 to J16-3	J13-1 to J14-1	J13-3 to J14-3	J15-1 to J16-1	

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2.2.3 Selecting the Interrupt Request Level

A host interrupt is received from this instrument when it is in the DMA mode. When interrupting the host, the 8-bit logical address of this instrument is supplied to the VXIbus interrupt handler on bits 0-7. Table 2-4 list the jumper selections for interrupt levels 1-7.

Table 2-4. Interrupt Request Level Jumper selections

Level	J28	J27	J26	J25	J24	J23	J22	J21	J20	J19
1	In	Out	In	In	Out	Out	Out	Out	Out	Out
2	In	In	Out	Out	In	Out	Out	Out	Out	Out
3	In	Out	Out	Out	Out	In	Out	Out	Out	Out
4	Out	In	In	Out	Out	Out	In	Out	Out	Out
5	Out	Out	In	Out	Out	Out	Out	In	Out	Out
6	Out	In	Out	Out	Out	Out	Out	Out	In	Out
7	Out	Out	Out	Out	Out	Out	Out	Out	Out	In

2.2.4 Configuring Precision and Sampling Clocks

The DAC sampling rate clock can be derived internally or externally. Figure 2-2 is a simplified schematic of the clock configuration circuit and Table 2-5 lists the jumper selections for all clock configurations. The internal sampling rate, which is controlled by software, is based on either the 3.6864-MHz internal precision clock or an external precision clock, depending upon how jumper J1 is installed.

NOTES: TTLTRG0-3 are reserved for an external Precision Clock input, TTLTRG4-7 are reserved for external Trigger inputs.

Install J2 to connect the Sampling Rate Clock to a selected TTLTRG line. Install J29 to connect the front panel EXT TRIG input to a selected TTLTRG line. When J29 is installed, J3 must be shorted 2-3. Make sure that the selected TTLTRG line is not used for any other purpose. Both J2 and J29 cannot be installed at the same time.

An External Precision Clock or Sampling Rate Clock can be fed to the front panel EXT CLK BNC connector. To input an External Precision Clock, connect J1-1 to J1-2, J3-2 to J3-3 and leave J2 open. To input an External Sampling Rate Clock, connect J1-2 to J1-3, J3-2 to J3-3 and leave J2 open. An external precision clock may also be received through connector P2 via TTLTRG0, 1, 2 or 3. In this case, connect J1-2 to J1-3, J3-1 to J3-2 and leave J2 open.

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Figure 2-2. Clock Configuration Schematic

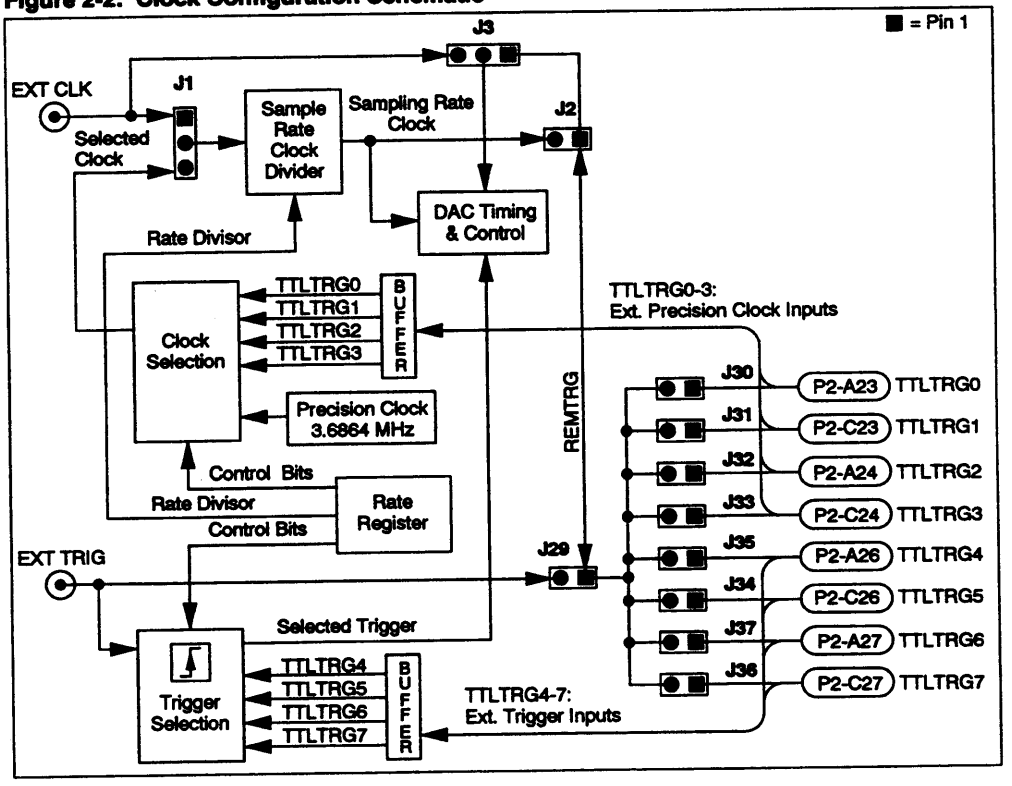


Table 2-5. Clock Configuration Jumper Selections

Function	Source	J1	J2	J3	J29
Internal Precision Clock	Internal Osc.	2-3	OUT	2-3	NA
External Precision Clock	EXT CLK	1-2	OUT	2-3	NA
External Precision Clock	TTLTRG0-3	2-3	OUT	1-2	NA
External Sampling Rate Clock	EXT CLK	2-3	OUT	2-3	NA
External Sampling Rate Clock (Master)	REMTRG	2-3	IN	1-2	OUT
External Sampling Rate Clock (Slave)	REMTRG	2-3	OUT	1-2	OUT

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To synchronize the operation of this instrument with another in a Master-Slave configuration, the sampling clock may be sent to the other instrument on a TTLTRG line. For this configuration, install jumper J2, connect J1-2 to J1-3 and J3-1 to J3-2, and install the appropriate jumper for the selected TTLTRG line. The sampling clock is an active low pulse with a pulse width defined by equation 1 depending upon the source of the Precision Clock. If the on-board 3.6864-MHz Precision Clock is used, the pulse width is 135ns.

$$\text{Pulse width} = \frac{1}{2f_{\text{Prec Clk}}} \qquad \text{[Equation 1]}$$

2.2.5 Connecting EXT TRIG to a TTLTRG line

For triggering another VXI instrument, the front panel EXT TRIG input signal can be connected to a selected TTLTRG line (Table 2-6). By installing jumper J29 and removing J2, and connecting J3-2 to J3-3, the EXT TRIG signal can be routed to the TTLTRG jumper field (J30-J37). Install a jumper for the selected TTLTRG output line. Make sure that the selected TTLTRG line is not used for any other purpose.

Table 2-6. EXT TRIG-to-TTLTRG Jumper Selections

Function	J2	J3	J29	TTLTRG Output
Disconnected	NA	NA	OUT	NA
Connected	OUT	2-3	IN	Install J34, J35, J36 or J37

2.2.6 Selecting a TTLTRG Output Line

A TTLTRG line can be used to drive the Sample Rate Clock or the front panel EXT TRIG input signal onto the VXIbus. To do either, one jumper from Table 2-7 must be installed to physically connect the selected TTLTRG line to the VXIbus.

Table 2-7. TTLTRG Jumper Selections

	TTLTRG Line							
	0	1	2	3	4	5	6	7
One Jumper Only	J30	J31	J32	J33	J35	J34	J37	J36

2.2.7 Configuring the Output Channels

Each DAC channel has two outputs (A & B) and three jumper-selectable options as listed in Table 2-8.

Signal Guard – The signal guard, which also affects both outputs A and B, can be shorted to analog ground.

Output Filter – The output filter is a six-pole Butterworth filter which affects both outputs A and B of each channel. The filter can be connected in line or bypassed.

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Output Drive – The output amplifiers of each channel can be configured for a single-ended or differential output. The DBS 8751 output voltage swing with respect to analog ground is ±3 volts (differential) or ±6 volts (single-ended); and ±5 volts or ±10 volts for the DBS 8752.

Table 2-8. Output Channel Configuration Jumpers

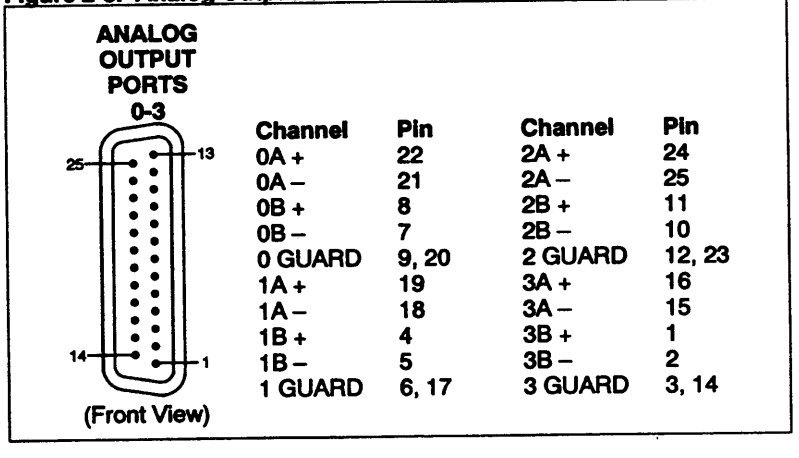
		Chan 0A	Chan 0B	Chan 1A	Chan 1B	Chan 2A	Chan 2B	Chan 3A	Chan 3B
Guard:	None	J400:Out	J400:Out	J300:Out	J300:Out	J500:Out	J500:Out	J200:Out	J200:Out
	A.Gnd	J400:In	J400:In	J300:In	J300:In	J500:In	J500:In	J200:In	J200:In
Filter:	Out	J403:1-2	J403:1-2	J303:1-2	J303:1-2	J503:1-2	J503:1-2	J203:1-2	J203:1-2
	In	J403:2-3	J403:2-3	J303:2-3	J303:2-3	J503:2-3	J503:2-3	J203:2-3	J203:2-3
Drive:	S.E.	J404:2-3	J405:2-3	J304:2-3	J305:2-3	J504:2-3	J505:2-3	J204:2-3	J205:2-3
		J402: In	J406: In	J302: In	J306: In	J502: In	J506: In	J202: In	J206: In
	Diff.	J404:1-2	J405:1-2	J304:1-2	J305:1-2	J504:1-2	J505:1-2	J204:1-2	J205:1-2
		J402: Out	J406: Out	J302: Out	J306: Out	J502: Out	J506: Out	J202: Out	J206: Out

2.3 INSTALLATION

This instrument can be installed in any VXI chassis slot except slot 0. Before installing this module in a VXI slot, make sure that the jumper selections are correct for your application and that the module cover is securely mounted.

The analog output channels are available on a 25-pin D-Type female connector (Figure 2-3). The output cable should be constructed using a standard D-Type 25-pin male connector with a metal-back shell. Analog outputs should be wired using twisted shielded pairs. The GUARDs for each channel can be individually shorted to Analog ground.

Figure 2-3. Analog Output Connections



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2.4 START-UP AND VERIFICATION

2.4.1 Power-Up Reset Status

At power-up, all programmable registers are configured in an unknown state except for the ID Register and the Device Type Register. After completing its power-up sequence, the instrument is in a reset state and the PASS/FAIL indicator is green. If a VXI Resource Manager is invoked, the instrument is recognized and its presence noted.

2.4.2 Example Verification Program

The following program is a simple example for testing the DBS8751/8752 operability. It is NOT a diagnostic test. It can, however, be used as a pattern for other driver type programs.

```
int LA, tmp, ret, Access = 2, Width = 2;

/*
 * Definitions for the  DBS 8751 and DBS 8752
 */

#define NCHAN           4           /* number of on-board channels */
#define MAX_BLOCK_SIZE  256         /* maximum size of DMA block to transfer */
#define CLOCKF          +3.6864e+06 /* clock frequency in MHz */
#define IDENT           0xFFF5      /* DBS 8751/8752 ident. register value */
#define MANF_ID         0xff5       /* Manufacturer's Identification Number */
#define INT_LEVEL       0x01        /* interrupt request level to use */
#define DMA_BLK_SIZE    65535       /* block size for DMA xfers */
#define MODEL_IDb       0x130       /* Device Model code for the DVX 2901 */
#define MODEL_IDc       0x180       /* Device Model code for the DBS 8751 */
#define MODEL_IDd       0x181       /* Device Model code for the DBS 8751A */
#define Access          0x42        /* VXI acc parameters, Intel byte order, non-priv, A24 */
#define Width           0x2         /* word access */
#define L_A             0xe000      /* Logical Address */

/*
 * DBS 8751/8752 DAC COMMANDS
 */
#define WR_H_MAR    0x18    /* write to the HOST MEM ADDR REG. */
#define RD_H_MAR    0x1c    /* read the HOST MEM ADDR REG. */
#define WR_WCTREG   0x10    /* write the DAC word count register */
#define RD_WCTREG   0x14    /* read the DAC word count register */
#define WR_D_MEM    0x08    /* write the DAC memory */
#define RD_D_MEM    0x0c    /* read the DAC memory */
#define STREAM      0X40    /* Stream bit */
#define P2          0x20    /* Data Source selection bit; 1 = P2 */
```


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```
/*
 * 9516 DMA Controller register values
 */
#define MODE                0x0d        /* 9516 master mode reg. */
#define WAIT_ST             0           /* # of wait states for 9516 */
#define CHANNEL_MODE        0x40052L    /* Common Mode pattern */
#define CHANNEL_MODE_W      0x40052L    /* Mode pattern for Write to VME memory */
#define CHANNEL_MODE_R      0x40042L    /* Mode pattern for Read from VME memory */
#define CHAIN_RELOAD        0x1b3
#define ADDRESS_REF         0xc0

/*
 * DBS 8751/8752 register offset definitions
 */
#define ID          0
#define TYPE        2
#define CSR         4
#define RATE        0x0a
#define DACCMD      0x10
#define DACDATA     0x12
#define DMAPTR      0xC
#define DMADAT      0xE

/*
 * DBS 8751/8752 ID and type definitions
 */
#define ANALOGIC_ID     0xff5       /* VXI ID register */
#define ID_MASK         0x0fff      /* ID mask */
#define TYPE_MASK       0xf000      /* upper 4 bits of ID reg. contain type */
#define TYPE_0          0xc000      /* A16/24 type */
#define TYPE_1          0xf000      /* A16 only type */
#define TYPE_2          0xd000      /* A16/32 type */

/*
 * DBS 8751/8752 CSR bit masks
 */

#define SRESET          0x01        /* reset command  */
#define SYSFAIL         0x02        /* 1 == disable driving SYSFAIL line  */
#define EXT_START       0x04        /* Enable External Start */
#define EXT_TRG         0x08        /* external trigger enable  */
#define START           0x10        /* start bit */
#define DAC_4           0x2000      /* enable 4 DACs */

#define TEST_MODE       0x8000      /* enable the Test Mode */
#define INT_EN          0x4000      /* interupt enable */
#define DAC_HOLD        0x02        /* DAC CMD CODE to hold current output */
#define DAC_LOOP        0x00        /* output the table and loop to the beginning */
#define DAC_FLOW        0x01        /* Flow thru operation, DMA or P2 */
```


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```
/*
 * DBS 8751/8752 status masks
 */
#define INT_PEND          0x01    /* interrupt pending */
#define BUFFER_EMPTY      0x02    /* buffer empty */
#define DIAG_PASSED       0x04    /* diagnostics pass */
#define DEVICE_READY      0x80    /* Device ready */
#define COMP_GTE          0x20    /* DAC output is Equal or Greater than */
#define MODID             0x4000  /* MODID */

/*
 * AMD 9516 register offset definitions
 */
#define MMODE   0x38    /* master mode register */
#define CMD     0x2c    /* command register */
#define STR     0x2c    /* status register */
#define CADRBH  0x10    /* current address reg. B hi */
#define CADRBL  0x00    /* current address reg. B lo */
#define BADRBH  0x14    /* base address reg. B hi */
#define BADRBL  0x04    /* base address reg. B lo */
#define CADRAH  0x18    /* current address reg. A hi */
#define CADRAL  0x08    /* current address reg. A lo */
#define BADRAH  0x1c    /* base address reg. A hi */
#define BADRAL  0x0c    /* base address reg. A lo */
#define COPC    0x30    /* current op count */
#define BOPC    0x34    /* base operation count */
#define CMH     0x54    /* channel mode hi */
#define CML     0x50    /* channel mode lo */
#define CAH     0x24    /* chain address hi */
#define CAL     0x20    /* chain address lo */

/*
 * 9516 commands
 */
#define DMARESET    0x0     /* reset 9516 */
#define CHAIN1      0xa0    /* start chaining on channel 1 */
#define CHAIN2      0xa1    /* start chaining on channel 2 */
#define CIP2        0x25    /* clear interrupt on channel 2 */
#define CIP1        0x24    /* clear interrupt on channel 1 */
#define DIE1        0x30    /* disable interrupt on channel 1 */
#define DIE2        0x31    /* disable interrupt on channel 2 */
#define IE1         0x32    /* enable interrupt on channel 1 */
#define IE2         0x33    /* enable interrupt on channel 2 */

/*
 * interrupt enable for channel mode
 */
#define DMA_INT_EOP 0x80    /* DMA interrupt on EOP */
#define DMA_INT_TC  0x200   /* DMA interrupt on term. cnt */
#define BC_TC       0x1000  /* base->current reload on term. cnt. */
#define CHAIN_TC    0x8000  /* chain on TC */
```


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```
/*
 * 9516 status bits
 */
#define TC                      0x01    /* term count */
#define EOP                     0x02    /* end of process termination */
#define NAC                     0x800   /* no autochaining */
#define DMA_INT_PEND            0x2000  /* interrupt pending */

/* Macros for VXIbus transfers */

#define Rvme(x,y)   ret = VXIinReg(LA, x, &tmp); \
                    y = tmp; \
                    if (ret) \
                        printf("Read Error %x\t%x\t%x\n", LA, x, y);

#define Wvme(x,y)   ret = VXIoutReg(LA, x, y); \
                    if (ret) \
                        printf("Write Error %d\t%x\t%x\n", LA, x, y);

#define RMem(x,y)  y = *(LMEM_ADDR + x);
#define WMem(x,y) *(LMEM_ADDR + x) = y;

/* NOTE:  Use the following two definitions if the Memory Destination/Source is
          VMEbus resident memory */

#if 0
   #define RMem(x,y)    ret = VXIin(Access, x | PMEM_ADDR, Width, &tmp); \
                        y = tmp; \
                        if (ret) \
                            printf("MEMRead Error %x\t%x\n", x, y);
   #define WMem(x,y)    ret = VXIout(Access,x | PMEM_ADDR, Width, y); \
                        if (ret) \
                            printf("MEMWrite Error %x\t%x\n", x, y);
#endif

unsigned long MEM_OFFSET;
unsigned long MSIZE;
unsigned int *LMEM_ADDR;
unsigned long PMEM_ADDR;

#define PI      3.1415926

#include "stdio.h"
#include <math.h>
#include <string.h>

main()
{
      int data,dcmd,i,j, stype, patrn;
      float f;
      int wct[4],npts,dac[4];
```


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```
    InitVXIlibrary();

    dac[0] = 0x0;
    dac[1] = 0x1;
    dac[2] = 0x2;
    dac[3] = 0x3;

    printf("\select the waveform desired for all channels \n\n");
    printf("\ 0 = DC \n");
    printf("\ 1 = + full scale \n");
    printf("\ 2 = - full scale \n");
    printf("\ 3 = full scale square wave \n");
    printf("\ 4 = full scale sine wave \n");
    printf("\ 5 = random value \n");
    printf("Enter choice: ");
    scanf("%d",&stype);

/*
 * RESET THE DBS 8751/2
 */
    loop:
    if (kbhit())exit(0);
    dcmd = 0x2002;
    Wvme(CSR,dcmd|0x0001);    /* issue the reset command */
    dcmd = (TEST_MODE|DAC_4|(DAC_LOOP<<11)|(DAC_LOOP<<9)|(DAC_LOOP<<7)
                        |(DAC_LOOP<<5)|dcmd);
    Wvme(CSR,dcmd);           /* Place all DACs in the Loop Mode */

/*
 * SET THE SAMPLING RATE
 *
 *    Possible choices are:
 *      125 Khz = 0x3E2, 100 Khz = 0x3db, 194 Khz = 0x3ed,
 *      204.8KHz = 0x3ee  400 Khz = 0x3f7   50 Khz = 0x3b7
 */
    Wvme(RATE,0xfc00 | 0x03ee);     /* Selected 204.8 KHz */

/*
 * LOAD THE WORD COUNTERS
 * This value determines the frequency at which the waveform table is output,
 * i.e., Sampling Rate divided by Word Count = DAC Table Repeat Frequency.
 *  If RATE = 3ed, then   0x8 = 25 Khz;
 *                        0x14 = 10 Khz;
 *                        0x28 = 5 Khz;
 *                        0X32 = 4 Khz.
 *                        0x64 = 2 Khz;
 *                        0xc8 = 1 Khz
 *
 * If RATE = 3ef, then  0x15 = 10.326 Khz
```


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```
*
* If RATE = 3ee, then    0x08 = 25.6 khz
*                        0x0a = 20.48 Khz
*                        0x0d = 15.7Khz
*                        0x14 = 10.24 Khz
*                        0x19 = 8.192 Khz
*                        0x22 = 6023 hz
*                        0x33 = 4015 hz
*                        0x66 = 2007 hz
*/

/* Load the word count registers for all 4 DACs. This determines the output waveform frequency. */

    wct[0]=0xa;         /* 20.48 Khz @ 204.8Khz sampling rate */
    wct[1]=0x14;        /* 10.24 Khz @ 204.8Khz sampling rate */
    wct[2]=0x20;        /* 6.40 Khz @ 204.8Khz sampling rate */
    wct[3]=0x30;        /* 4.27 Khz @ 204.8Khz sampling rate */

    Wvme(DACCMD,WR_WCTREG|dac[0]);
    Wvme(DACDATA,wct[0]);
    Wvme(DACCMD,WR_WCTREG|dac[1]);
    Wvme(DACDATA,wct[1]);
    Wvme(DACCMD,WR_WCTREG|dac[2]);
    Wvme(DACDATA,wct[2]);
    Wvme(DACCMD,WR_WCTREG|dac[3]);
    Wvme(DACDATA,wct[3]);

/*
 * ZERO THE MEMORY FOR ALL DACs (This is not required, just nice. )
 */
    for (j=0;j<4;j++)
  {
        /* Set up the HMAR & load it with 0 (starting point) */

        Wvme(DACCMD,WR_H_MAR|dac[j]);
        Wvme(DACDATA,0x0);

        /* write the data into the DAC RAM buffer */

        Wvme(DACCMD,WR_D_MEM|dac[j]);
        for (i=0;i<wct[j];i++)
        {
            patrn = 0x0;
            Wvme(DACDATA,patrn);
        }
  }
```


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```
/*
 * LOAD THE MEMORY FOR ALL DACs
 */
      for (j=0;j<4;j++)
      {
      /* Set up the HMAR starting at location 0. */
            Wvme(DACCMD,WR_H_MAR|dac[j]);
            Wvme(DACDATA,0x0);

      /* Load the command to Write Memory */
            Wvme(DACCMD,WR_D_MEM|dac[j]);

      /* Generate the pattern for the selected waveform and write it into the DAC memory */
            switch ( stype )/* Select the desired waveform */
            {
                  case 0:           /* + 1/2 Scale DC */
                  for (i=0;i<wct[j];i++)
                        {
                        patrn = 0xC000;
                        }
                  break;

                  case 1:    /* + full scale */
                  for (i=0;i<wct[j];i++)
                        {
                        patrn = 0x8000;
                        }
                  break;

                  case 2:    /* - full scale */
                  for (i=0;i<wct[j];i++)
                        {
                          patrn = 0x7fff;
                        }
                  break;

                  case 3:    /* full scale square wave */
                  for (i=0;i<wct[j];i++)
                        {
                        if(i<(wct[j]/2))   /* if wct[j] is odd, the waveform will NOT be symmetrical */
                              {
                               patrn = 0x7fff;
                              }
                        else
                              {
                              patrn = 0x8000;
                              }
                        }
                  break;
```


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```
                case 4:    /* full scale sine wave */
                for (i=0;i<wct[j];i++)
                     {
                     f = 0.98*(32767.*sin(2*PI*(float)i/(float)wct[j]));
                     patrn = (int)f;
                     Wvme(DACDATA,patrn);
                     }
                break;

                case 5:    /* random value */
                for (i=0;i<wct[j];i++)
                     {
                     Wvme(DACDATA,(2*rand()));
                     }
                break;

          }
     }

     start:
/*
 * START THE DAC #0
 */
     printf("  next to last dcmd %x  \n",dcmd);
     printf("  last dcmd to start %x  \n",(dcmd|START));

     Wvme(CSR,dcmd|START);
     thend:

     printf("Done !!!\n");

     CloseVXIlibrary();
}
```


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Section 3
Operation

3.1 OVERVIEW

This section provides guidelines for Waveform Generator operation using software controls. It includes references to the programmable registers described in detail in Section 4. If this instrument is to be controlled using a software driver, refer to the Software User's Manual received with the driver for software installation and operating instructions.

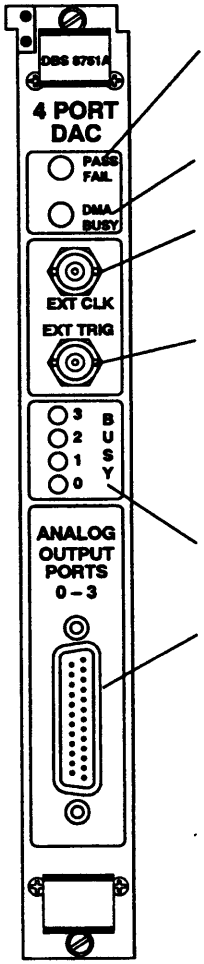
The waveforms generated on the four output channels depend on the data loaded into the 64K-word data table memory for each D/A Converter (DAC) channel. Data is transferred to the DAC data table memories either by a programmed I/O command sequence or a DMA operation. Although all four DAC channels are updated at the same time by the Sampling Rate Clock, each DAC can have a different size data table, allowing the generation of four different waveforms. Waveform generation is controlled by the input clock, trigger function, DAC operating modes, and sampling rate which are all programmable.

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3.2 CONTROLS AND INDICATORS

Figure 3-1 describes the control inputs and indicators on the front panel. For information on configuring the hardware for any of these control functions or on analog output cable wiring, see Section 2.

Figure 3-1. Front Panel Description



Pass/Fail Indicator
Indicates diagnostic test results:
Green = Pass
Red = Failure

DMA Busy Indicator
Green indicates DMA cycle in progress.

External Clock Input (BNC)
Used for an External Precision Clock input or an Absolute Sample Rate Clock input. This input is selected by software control.

External Trigger Input (BNC)
An External Trigger input used to start and stop waveform generation. Internally synchronized with the Internal Precision Clock. Must be user-synchronized with an EXT CLK input (see timing requirements, Figure 3-3). This input is selected by software control.

Channel Busy Indicators
A green indicator indicates an active channel.

Analog Output Connector
Provides access to the four dual output ports through a standard D-Type 25-pin female connector.

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3.3 CLOCK OPTIONS

The rate at which the Waveform Generator samples input data can be determined by using either an internal/external Precision Clock or Sampling Rate Clock. If an internal or external Precision Clock is used, it is fed to an internal Clock Divider which produces the Sampling Rate Clock. If an absolute Sampling Rate Clock is used, it is configured to drive the DACs directly . In this configuration the DACs are driven at the same rate at which the Waveform is updated. All DAC channel outputs are updated at the same time.

The available clock options are listed in Table 3-1 and the relationship between clock sources and sampling rate is depicted in Figure 3-2. Before installing and operating this module, the chosen clock option must first be selected by making the appropriate hardware jumper selections (See Section 2.2.4.).

When using a Precision Clock, the rate divisor needs to be written into Rate Register bits 0 through 9. The Internal Precision Clock is selected by Control Register bit 13. An External Precision Clock can be input either at the front panel EXT CLK connector or on TTLTRG line 0-3 from the VXI backplane. The EXT CLK input is enabled by Control Register bit 3. When using a TTLTRIG line, Rate Register bits 14 and 15 are used to select the TTLTRG line.

Table 3-1. Clock Options

Clock Source	I/O Requirements or Characteristics
Internal Precision Clock	Selected by Rate Register bit 13 set to 1. Rate Register Divisor: 1023 (3.603 kHz) to 18 (204.8 kHz).
Ext. Precision Clock (EXT CLK)	Clock Signal Input: 2.4 to 4.0 MHz, 50% duty cycle, TTL. Rate Register Divisor: 1023 to 18. EXT CLK enabled by Control Register bit 3 set to 1.
Ext. Precision Clock (TTLTRG0-3)	Clock Signal Input: 1.0 to 5.0 MHz, 50% duty cycle. Rate Register Divisor: 1023 to 18. Clock source enabled by Rate Register bit 13 set to 0. TTLTRG line selected by Rate Register bits 14 and 15.
Ext. Sampling Rate Clock (EXT CLK)	Clock Signal Input: TTL, active-low clock pulse; 2.0 µs (min.) pulse width, 5-µs (min.) period. EXT CLK enabled by Control Register bit 3 set to 1.
TTLTRG Sampling Rate Clock (Master)	Frequency dependent upon selected Precision or Sampling Rate Clock.
TTLTRG Sampling Rate Clock (Slave)	Maximum Frequency = 204.8 kHz, Minimum Pulse Width = 120 ns, Minimum Period = 5µs.

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Figure 3-2. Clock Sources and Sampling Rate

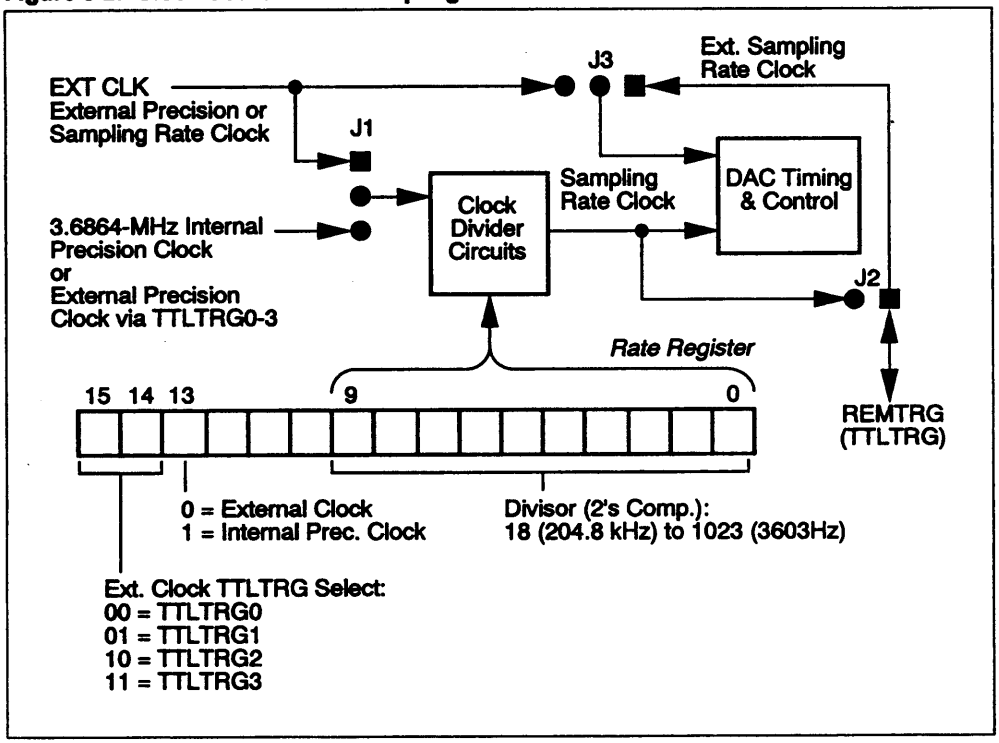
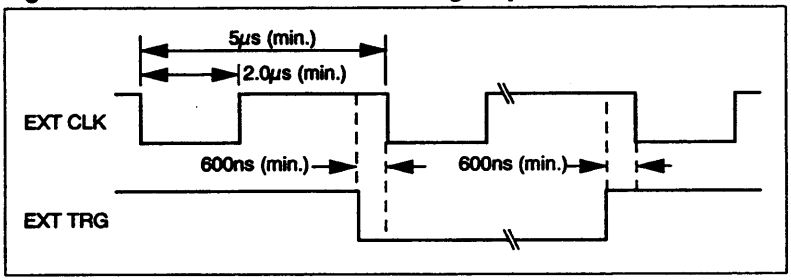


Figure 3-3. EXT CLK to EXT TRIG Timing Requirements



An External Sampling Rate Clock can be input either at the EXT CLK connector or on a TTLTRG line configured as a Remote Trigger (REMTRG) input from another module. See Section 3.4 for information on using REMTRG for master/slave synchronization.

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The EXT CLK and EXT TRIG inputs operate independently. EXT TRIG (waveform external start control) can be used with either the Internal Precision Sampling Clock (internally synchronized with EXT TRIG) or the EXT CLK input (user synchronized with EXT TRIG). When using both inputs, see Figure 3-3 for timing requirements.

NOTE: When using an External Clock (EXT CLK) that is gated by an External Trigger (EXT TRIG), one extra clock pulse must be supplied at the beginning of the waveform output (*i.e.*, 1024 pulses for a complete cycle of the waveform output) to start the process. Note that there is a one-clock delay between the n^{th} pulse on the EXT CLK input and the n^{th} data point in the output data.

3.4 MASTER-SLAVE SYNCHRONIZATION

To synchronize the operation of one Waveform Generator with another in a Master-Slave configuration, the Sampling Rate Clock of a Master module may be fed to a Slave module on a TTLTRG line. Refer to Section 2.2.2 for the appropriate jumper settings. The Sampling Rate Clock is an active-low pulse with a pulse width defined by equation 1 depending upon the source of the Precision Clock. If the 3.6864-MHz Internal Precision Clock is used, the pulse width is 135ns.

$$\text{Pulse width} = \frac{1}{2f_{\text{Prec Clk}}} \qquad \text{[Equation 1]}$$

where $f_{\text{Prec Clk}}$ = Frequency of the selected Precision Clock

3.5 SAMPLING RATE

The DAC sampling rate is based on a Clock Divider Circuit fed by an Internal/External Precision Clock (Figure 3-2) or an External Sampling Rate Clock fed directly to the DAC. Normally, the Internal Precision Clock is selected to establish the range of sampling rates. Using an External Precision Clock enables the instrument to produce sampling rates which cannot be generated by the combined circuitry of the Internal Precision Clock and internal frequency divider.

The Clock Divider Circuit receives a divisor input from bits 0 through 9 of the Rate Register. The divisor is an integer ranging from 18 to 1023. Using the 3.6864 MHz Internal Precision Clock produces rates from 3.603 kHz to 204.8 kHz. Refer to Section 4.4.1 for a description of the Rate Register format.

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3.6 TRIGGERING OPTIONS

NOTE: When using a TTLTRG line, make sure that the selected TTLTRG line is not used by another VXI instrument. When triggered externally, the first data point is generated two sample clock periods after the trigger signal is asserted.

Starting and stopping waveform generation is controlled by the triggering function. Waveform generation can be triggered either internally by software or externally by an External Trigger input signal (Figure 3-4).

Internal triggering is performed using bit 4 of the Control Register. With Control Register bit 2 set to zero (EXT TRIG disabled), bit 4 starts waveform generation when set to a one.

An External Trigger signal can be input from either the Front Panel EXT TRIG BNC connector or from a selected TTLTRG line (4, 5, 6, or 7). The External Trigger input requires a negative-going pulse, 30 ns wide (min.). When enabled by bit 2 in the Control Register, the rising edge of the External Trigger signal starts waveform generation on all channels that are programmed for the Loop or One-Shot Mode. Refer to Section 3.9 for information on DAC modes.

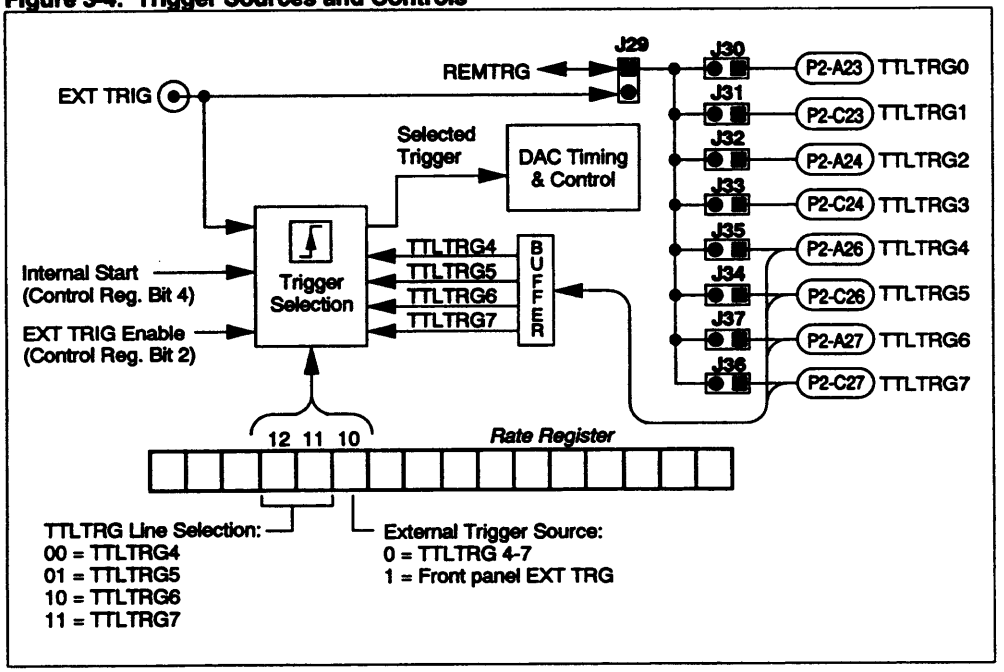
Waveform generation stops for channels in the One-Shot Mode after the data pattern has been cycled once. The next rising edge of the External Trigger restarts the One-Shot channels. Waveform generation stops for all channels when bit 4 (Internal Start) in the Control Register is cleared to 0.

The source of the External Trigger input signal (EXT TRIG connector or TTLTRG line) is controlled by bit 10 in the Rate Register (Section 4.3.1). Selecting TTLTRG 4, 5, 6 or 7 as the supply line is done using bits 11 & 12 in the Rate Register.

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For triggering another VXI instrument via the backplane, the front panel EXT TRIG input signal can be connected to a selected TTLTRG line by installing jumper J29. Make sure that REMTRIG (master/slave remote trigger) is not in use.

Figure 3-4. Trigger Sources and Controls



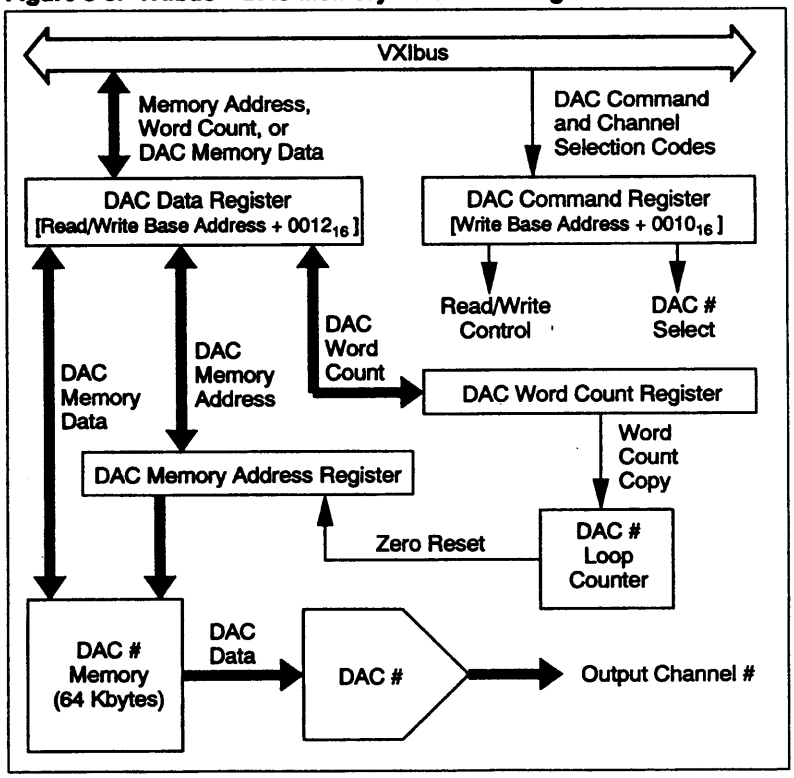
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3.7 LOADING DAC MEMORIES

NOTE: The DBS 8751(2)A provides no manual offset or gain trim adjustments. It is calibrated by storing offset and gain correction data in memory. For the calibration procedure, refer to Appendix B.

The DAC memory in each channel is loaded from the VXIbus using the DAC Command Register (Section 4.4.2) and the DAC Data Register (Section 4.4.3) (Figure 3-5). DAC memories are accessible only in the A16 memory space and DAC input data must be in two's complement format (Table 3-2). Data is transferred to the DAC memories, one channel at a time, under the control of a programmed I/O sequence or a DMA cycle.

Figure 3-5. VXIbus – DAC Memory Data Flow Diagram



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Table 3-2. DAC Input Data Format

DAC Input Data (2's Comp)					Output
0111	1111	1111	1111	=	+ Full Scale
0000	0000	0000	0000	=	0
1000	0000	0000	0000	=	– Full Scale

The DAC Command Register selects a channel and defines the commands to read/write the DAC Memory Address Register, the DAC Word Count Register and the DAC memory of the selected channel. Data is transferred between the VXIbus and each of these three locations via the DAC Data Register. The defined command is executed only when the DAC Data Register is accessed.

Each time the DAC memory is read or written, the contents of the DAC Memory Address Register is incremented. So, when many DAC memory locations need to be accessed, there is no need to write each subsequent address into the DAC Memory Address Register. Each time the memory is accessed, the DAC Memory Address Register is automatically incremented. Thus, repeated access to the DAC Data Register after the DAC Memory Address Register has been loaded results in the sequential access to the memory.

The DAC Word Count Register defines the number of words (65536 max.) to be read from memory and transferred to the DAC. Whenever data is written to this register, the data is copied (complemented) to an incrementing loop counter for the selected DAC. Whenever the loop counter reaches zero, the DAC Memory Address Register is reset to zero and the DAC Word Count is re-copied to the loop counter. The value of the word count and the selected Sampling Rate determine the the output waveform frequency.

Sampling Rate × Word Count = DAC Data Table Repeat Frequency
= Output Waveform Frequency

Whether a DAC memory is filled by either a series of PIO transfers or a DMA operation, the DAC Memory Address Register is set to zero, and the DAC Command Register is loaded with the command to write to the selected DAC memory. The transfer of data begins by either implementing a series of PIO transfers to the memory or by initiating a DMA operation. At this point the selected DAC can be placed into the Loop Mode to begin signal generation.

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NOTE: When writing data to a DAC memory, the DAC being loaded must be in the Loop Mode and bit 4 of the Control Register must be a zero (Stop). Waveforms cannot be generated while loading data via PIO or DMA.

3.7.1 *Using a Programmed I/O (PIO) Data Transfer Sequence*

A PIO data transfer sequence consists of the following basic steps:

(1) Encode the DAC Command Register to write the DAC Memory Address Register for one of the four output channels.

(2) Write the starting DAC memory address into to the DAC Data Register.

(3) Encode the DAC Command Register to write or read the DAC Memory of the selected channel.

(4) Write or read the first word in the DAC Data Register. Each subsequent write or read to the DAC Data Register increments the DAC Memory Address and accesses the next location in the selected DAC memory.

NOTE: Data that is read from DAC memory is held in a temporary register before being passed to the VXIbus via the DAC Data Register. Therefore, the first word read in a transfer sequence is from a previously accessed memory location and must be discarded.

Example 1 – Write Sequence

Action	Results
Write 18_{16} to DAC Command Reg.	Writes DAC 0 Memory Address Register command.
Write 00_{16} to DAC Data Reg.	Loads 00_{16} into DAC 0 Memory Address Register.
Write 08_{16} to DAC Command Reg.	Writes DAC 0 Memory command.
Write Word 1 to DAC Data Register	Loads Word 1 into DAC memory location 00.
Write Word 2 to DAC Data Register	Loads Word 2 into DAC memory location 01.
Write Word 3 to DAC Data Register	Loads Word 3 into DAC memory location 02.
Write Word 4 to DAC Data Register	Loads Word 4 into DAC memory location 03.
Write Word 5 to DAC Data Register	Loads Word 5 into DAC memory location 04.

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Example 2 – Read Sequence

Action	Results
Write 18_{16} to DAC Command Reg.	Writes DAC 0 Memory Address Register command.
Write 00_{16} to DAC Data Reg.	Loads 00_{16} into DAC 0 Memory Address Register.
Write $0C_{16}$ to DAC Command Reg.	Reads DAC 0 Memory command.
Read DAC Data Register	First read is meaningless, discard.
Read DAC Data Register	Reads DAC 0 memory location 00.
Read DAC Data Register	Reads DAC 0 memory location 01.
Read DAC Data Register	Reads DAC 0 memory location 02.
Read DAC Data Register	Reads DAC 0 memory location 03.
Read DAC Data Register	Reads DAC 0 memory location 04.

3.7.2 DMA Data Transfers

DMA transfers are performed using the on-board DMA Controller. DMA operations are similar to PIO except that the Memory Address Register cannot be loaded by the DMA Controller; the Memory Address must be loaded before initiating a DMA operation. Once the starting address is loaded into the Memory Address Register and the Read/Write Memory command is loaded into the DAC Command Register, DMA read/write operations can sequentially access the required number of DAC memory locations. See Section 4.5 for information on programming DMA read/write operations.

3.8 INTERRUPT GENERATION

The Waveform Generator generates an interrupt upon completing a DMA operation. At the end of the hardware interrupt cycle, the Logical Address of the Waveform Generator is placed on the VXIbus by the DMA Controller. Reading the Status Register of the DMA Controller identifies the reason for the interrupt. Refer to Section 4.6 for detailed programming information regarding interrupts.

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3.9 DAC OUTPUT CHANNEL MODES

Each DAC output channel can be individually programmed for the Loop, One-Shot, or Hold operating mode using the Control Register.

In the Loop Mode, the output channel generates the output waveform continuously. Each successive memory location is read from the data table in DAC memory and loaded into the DAC. The Word Count value determines how many words are transferred from DAC memory to the DAC. When all locations have been read, the DAC Loop Counter resets the DAC Memory Address to 0 and the memory is read from the beginning of the data table again. The repeat rate and the sampling rate determine the output waveform frequency. Refer to Section 3.7.

In the One-Shot Mode, only one cycle of the waveform is generated. When triggered internally, a One-Shot port generates the waveform once, after which a command is given to stop and re-arm the One-Shot circuit.

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Section 4
Register-Based Programming

4.1 OVERVIEW

This section contains information on Register-Based Programming which allows you to directly access the hardware registers that control the functions of this instrument. Since these Waveform Generators are Register-Based devices, they support VXIbus register maps, but do not require hardware to support VXIbus communication protocols.

For programming examples, refer to the software driver that was received with the instrument.

4.2 REGISTER ADDRESSING

This instrument has three Basic Configuration Registers (Figure 4-1) and five Device-Dependent Registers which can be located on any 64-byte boundary above $C000_{16}$ in the VXI A16 address space.

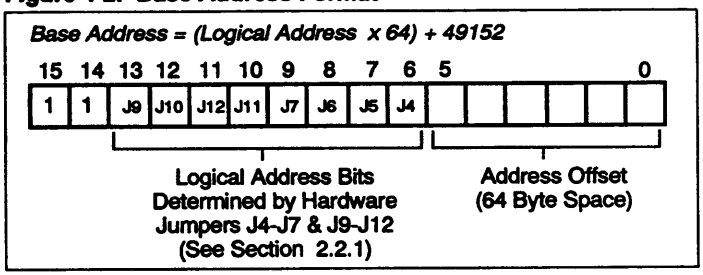
Figure 4-1 Register Map

	Address Offset	Register
DEVICE DEPENDENT REGISTERS	12_{16}	DAC Data Register
	10_{16}	DAC Command Register
	$0E_{16}$	UDC Command/Data Register
	$0C_{16}$	UDC Pointer Register
	$0A_{16}$	Rate Register
BASIC CONFIGURATION REGISTERS	08_{16}	Unassigned
	06_{16}	Unassigned
	04_{16}	Status/Control Register
	02_{16}	Device Type Register
	00_{16}	ID Register

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The Base Address is determined by the user-selectable logical address as shown in Figure 4-2. Bits 15 and 14 are always a one. The Logical Address (bits 13 to 6) is set by jumpers J4 to J7 and J9 to J12. Bits 5 to 0 contain a unique two-digit offset address for selecting each register.

Figure 4-2. Base Address Format



NOTE: This register-based instrument does not have any power-on default settings. All registers, except the ID Register and the Device Type Register, need to be initialized even though you do not intend to use all of the functions.

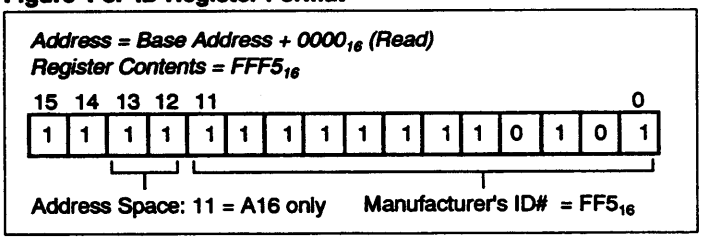
4.3 BASIC CONFIGURATION REGISTERS

The Basic Configuration Registers are used to define and identify the characteristics of the device. They are the ID Register, the Device Type Register and the Status/Control Register.

4.3.1 ID Register

The ID register (Figure 4-3) is a read-only register that identifies the addressing mode used by the device and provides the manufacturer's ID# of the device. Bits 15 and 14 are always a one. Bits 13 and 12 (Address Space) indicates the A16 addressing mode used by the operational registers of this device. Bits 11 through 0 (Manufacturer's ID#) returns the unique identification number of the manufacturer, in this case $FF5_{16}$.

Figure 4-3. ID Register Format

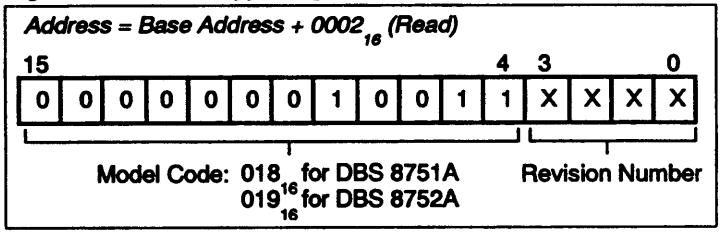


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4.3.2 Device Type Register

The read-only Device Type Register (Figure 4-4) contains the instrument's identification code (bits 15-4) and revision level (bits 3-0).

Figure 4-4. Device Type Register Format

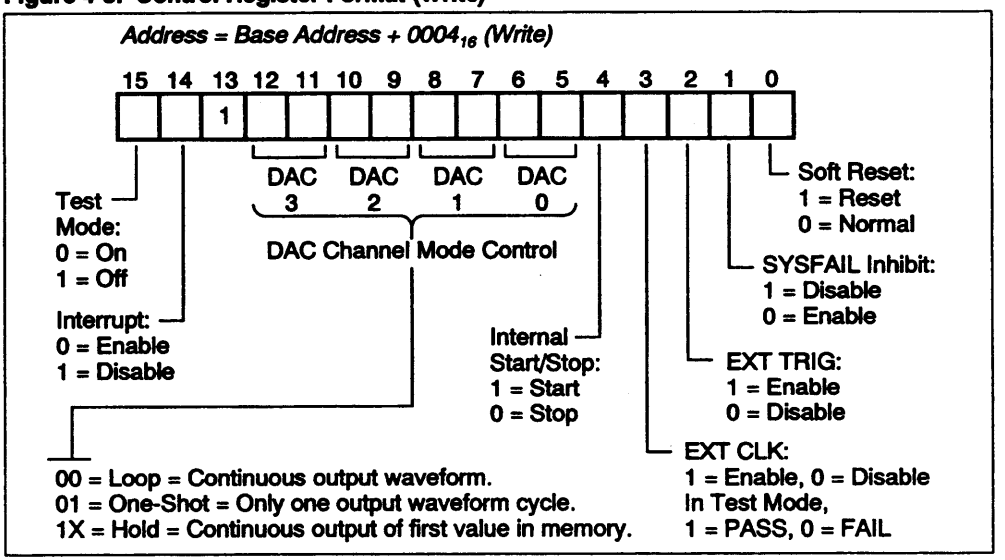


4.3.3 Control/Status Register

The Control/Status Register (Figures 4-5 and 4-6) is a read/write register used for programming functions and reporting module status. At power-on, all bits in the Control Register are set to zero.

The Control Register format is defined in Figure 4-5. Bit 15 (Test Mode) is used for a test mode sequence. When the test is complete, this bit is asserted and the results of the test (Pass/Fail) is stored by setting the EXT CLK enable bit accordingly. Bit 14 (Interrupt) enables the interrupt

Figure 4-5. Control Register Format (Write)

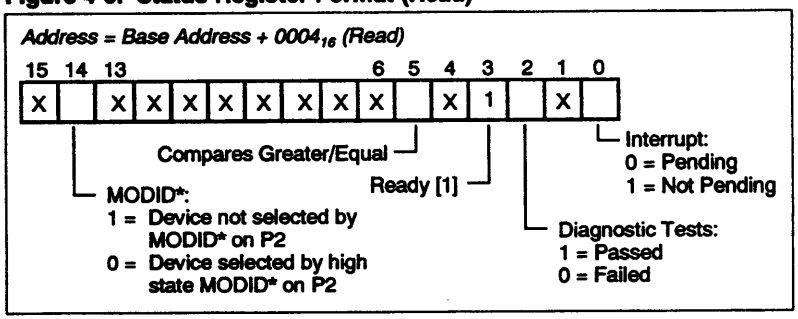


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capability of the device. Bits 12-5 are used to specify the operating mode of each DAC. Bit 4 (Internal Start) starts and stops waveform generation. Bit 3 is used in two ways: (1) If the Test Mode is ON, it sets the Pass/Fail indicator according to the test results, and (2) If the Test Mode is OFF, it enables or disables the EXT CLK input. Bit 2 (EXT TRIG) enables or disables the EXT TRIG input. Bit 1 (SYSFAIL Inhibit) enables or disables the device from driving the SYSFAIL* signal on the VXIbus. Bit 0 (Soft Reset) set to a one forces the device into the reset state which clears the control logic on the card and the Control Register.

The Status Register format is defined in Figure 4-6. Bit 14 (MODID) indicates if the device is selected via signal MODID. Bit 5 (Compares Greater/Equal) is the Analog Output Test comparator output in Test Mode. Bit 3 (Ready) is always a one (1). Bit 2 (Diagnostic Tests) indicates the status of the driver diagnostics. Bit 0 (Interrupt) indicates an interrupt by the instrument is pending.

Figure 4-6. Status Register Format (Read)



4.4 DEVICE-DEPENDENT REGISTERS

The Device-Dependent Registers are specific hardware control registers that can be programmed to control the DAC sampling rate, DAC functions and DMA transfers. The DMA registers (UDC Command/Data Register and UDC Pointer Register) are described in Section 4.5.

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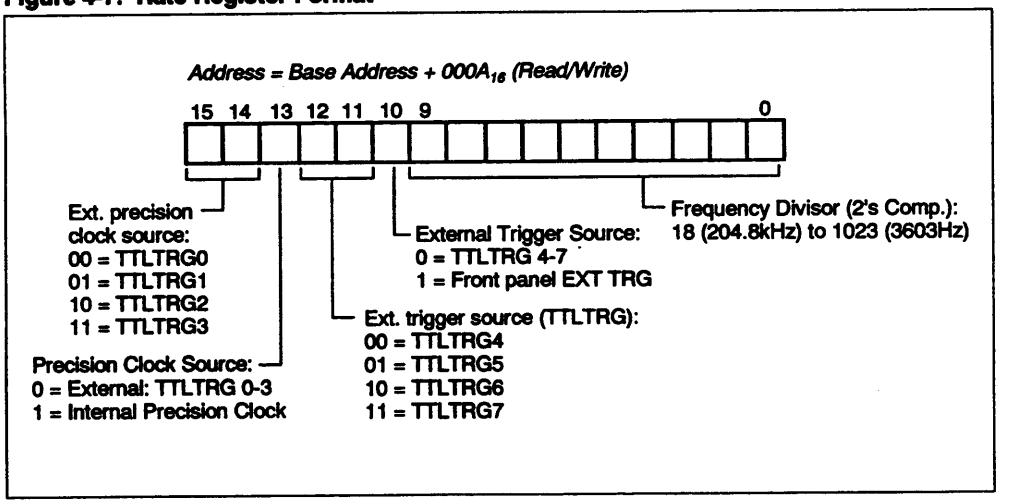
4.4.1 Rate Register

The Rate Register (Figure 4-7) controls the external trigger and clock inputs and contains the frequency divisor sent to the Clock Divider Circuit. Bits 15 and 14 select the TTLTRG line to receive an external clock input from the VXI backplane. Bit 13 selects the clock source. Bit 12 and 11 select the TTLTRG line to receive an external trigger input from the VXI backplane. Bit 10 selects the external trigger input source. Bits 9 - 0 contain the frequency divisor, in two's complement format, which determines the Sampling Clock frequency according to the following relationship:

Sampling Frequency (Hz) = 3686400 ÷ Frequency Divisor

NOTE: The Rate Register must be loaded before loading waveform data into DAC memories.

Figure 4-7. Rate Register Format



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4.4.2 DAC Command Register

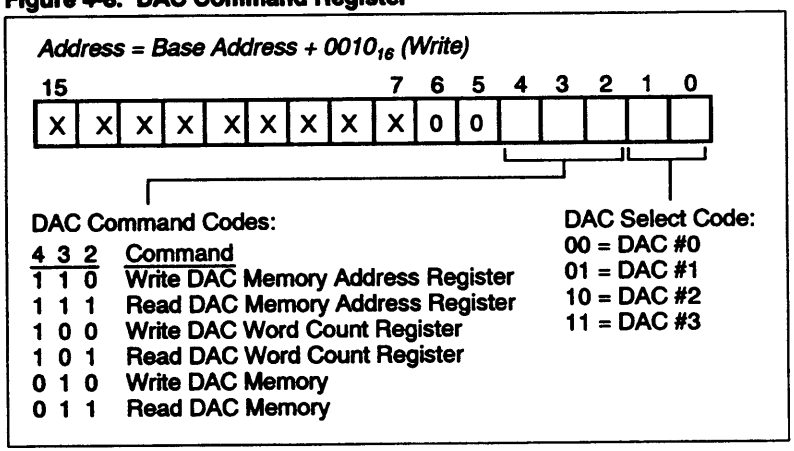
The write-only DAC Command Register (Figure 4-8) defines read/write commands which are used for loading data into each of the four 64-Kbyte DAC memories using a programmed I/O sequence or a DMA operation. The three-bit code in bits 2, 3, and 4 provides access to either a DAC Memory Address Register, a DAC Word Count Register, or a 64-Kbyte DAC Memory for each of the four channels of the Waveform Generator. The channel is selected by bits 0 and 1. The read/write data for each of these three avenues is transferred via the DAC Data Register (Section 4.4.3). The command defined in the DAC Command Register is executed only when the DAC Data Register (Section 4.3.3) is accessed.

The DAC Memory Address Register is a 16-bit register that is used to address a location of the selected DAC memory. When the addressed memory location is read/written, the contents of this register is incremented with each read/write cycle.

The DAC Word Count Register is a 16-bit register that is used to define the number (65536 max.) of words to be read from memory and transferred to the DAC. Whenever data is written to this register, the data is also copied (complemented) to an incrementing loop counter (unaccessible by command) for the selected DAC. Whenever the loop counter reaches zero, the DAC Memory Address Register is set to zero and the DAC Word Count is copied again to the loop counter.

For more information and examples, refer to Section 3.7.

Figure 4-8. DAC Command Register



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4.4.3 DAC Data Register

The DAC Data Register (Base Address + 0012_{16}) is a 16-bit read/write register used to transfer data as specified by the code wriiten to the DAC Command Register (Section 4.3.2). When the DAC Data Register is read or written, the command defined by bits 0-4 of the DAC Command Register is executed.

4.5 DMA CONTROLLER

DMA operations are controlled by the on-board Am9516A Universal DMA Controller (UDC). This section contains only an overview of how the UDC is implemented on the VXI card. For more detailed information on UDC operation, refer to "Direct Memory Access Controller Am9516/ AmZ8016," Advanced Micro Devices #04910A; and "MOS Microprocessors and Peripherals," Advanced Micro Devices, #09067A

NOTE: When the instrument becomes a Bus Master, it accesses the standard A24 address space differently for chaining and data transfer operations. For chaining, this instrument executes a Standard Supervisory Data access by generating address modifier "$3D_{16}$." For data transfers, a Non-Privileged Data Access is executed by generating address modifier "39_{16}."

4.5.1 Implemented Features of the UDC

Although the UDC has two independent DMA channels, only Channel 2 is used in this instrument. This UDC is operated in the Flyby Transfer Mode to transfer data from source to destination in a single step, thus doubling the throughput. The Chaining Mode is used to load or initialize the registers and to automatically reload or reinitialize at the end of DMA operation.

4.5.2 Implemented Registers of the UDC

The UDC has two types of internal registers: Chip-Level registers and Channel-Level Registers. The block diagram in Figure 4-9 shows the Chip-Level registers used by this device: Master Mode, Command and Chain Control. These are used to configure the functions of the UDC and control its operation. The Channel-Level registers used for Channel 2 are shown in Figure 4-10. These control the DMA operations performed by the channel.

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Figure 4-9. UDC Implementation Block Diagram

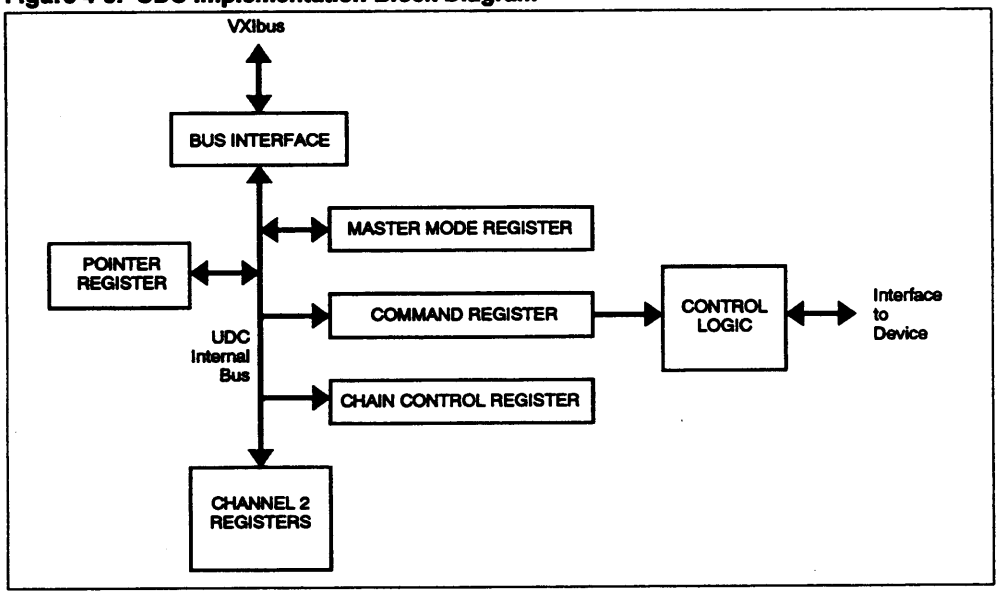
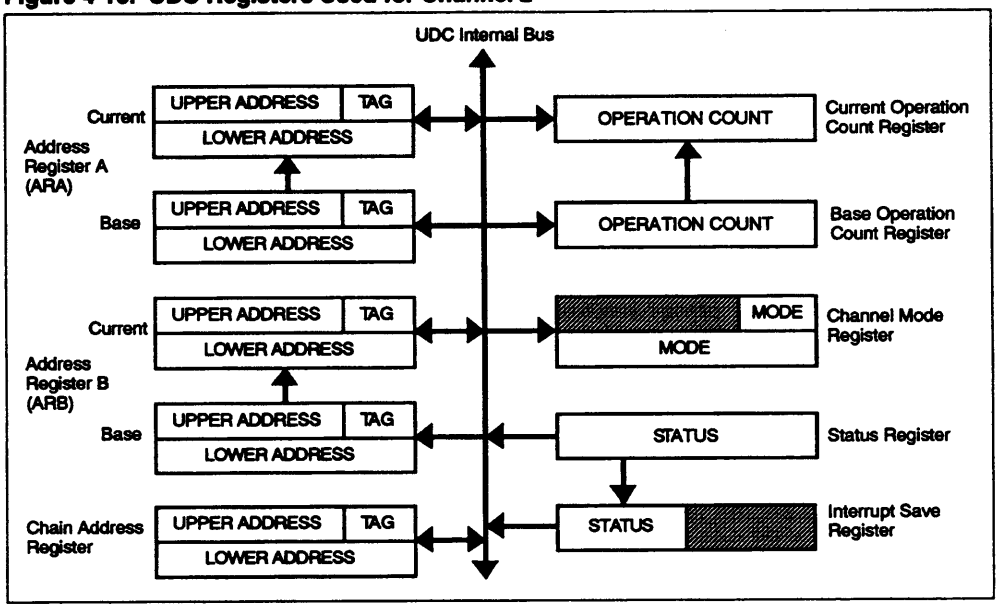


Figure 4-10. UDC Registers Used for Channel 2



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4.5.3 Access to UDC Registers

UDC registers are accessed through the UDC Pointer Register (read/Write, Base Address + $0C_{16}$). The address of the UDC register being accessed must be loaded into the UDC Pointer Register. The applicable Channel 2 registers are listed in Table 4-1 along with access type and register address of each. A read or write operation to the UDC Command/Data Register (Address = Base Address + $000E_{16}$) allows access to the internal UDC register addressed by the UDC Pointer Register.

Table 4-1. Applicable UDC Registers

Register Name	Access Type R = Host Read W = Host Write C = Chain Loadable	Address (Hex) Ch 1/Ch 2
Master Mode	R/W	38
Command Mode	W	2E/2C
Chain Control	C	
Current Address A:	R/W, C	
Upper Addr./Tag Field		1A/18
Lower Address Field		0A/08
Current Address B:	R/W, C	
Upper Addr./Tag Field		12/10
Lower Address Field		02/00
Base Address A:	R/W, C	
Upper Addr./Tag Field		1E/1C
Lower Address Field		0E/0C
Base Address B:	R/W, C	
Upper Addr./Tag Field		16/14
Lower Address Field		06/04
Current Operation Count	R/W, C	32/30
Base Operation Count	R/W, C	36/34
Status Register	R	2E/2C
Interrupt Save	R	2A/28
Interrupt Vector	R/W, C	5A/58
Channel Mode	R/W, C	52/50
Chain Address:	R/W, C	
Upper Addr./Tag Field		26/24
Lower Address Field		22/20

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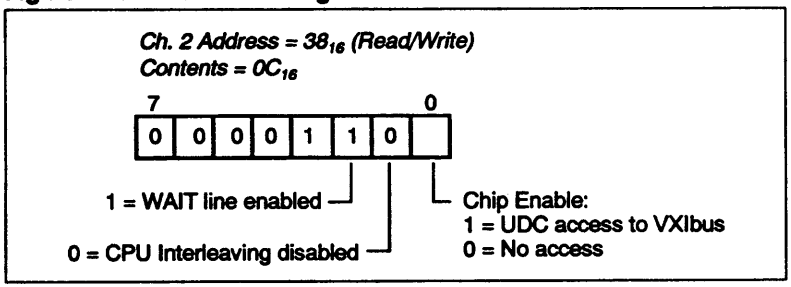
4.5.4 Chip-Level Register Descriptions

The following describes the UDC Chip-Level registers for this device.

4.5.4.1 Master Mode Register

The Master Mode Register (Figure 4-11) controls the chip-level DMA interface. A read or write is allowed at any time except during chaining. System RESET clears this register to all zeroes. When Chip Enable is a 1, the UDC gains access to the VXIbus to begin DMA operations. The remaining bits are assigned as shown for proper operation.

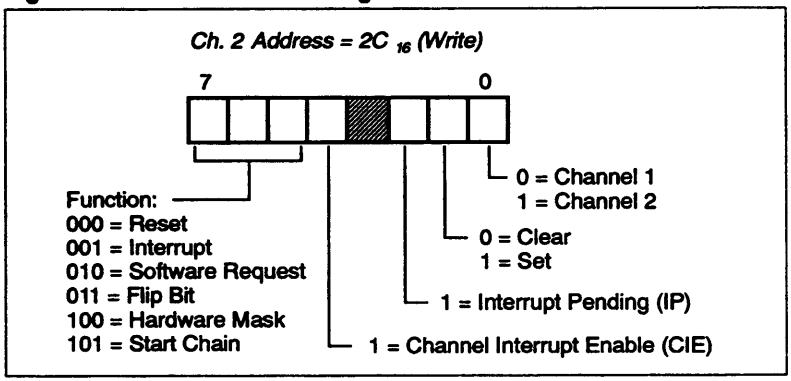
Figure 4-11 Master Mode Register Format



4.5.4.2 Command Register

The Host CPU writes to the Command Register to provide commands for the DMA operation. These commands initiate specific types of DMA operations, including chaining, mask setting/clearing, and setting specific bits to indicate transfer direction. Figure 4-12 shows the register format and Table 4-2 summarizes the commands used for Channel 2.

Figure 4-12. UDC Command Register



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Table 4-2. UDC Command Register Summary – Channel 2

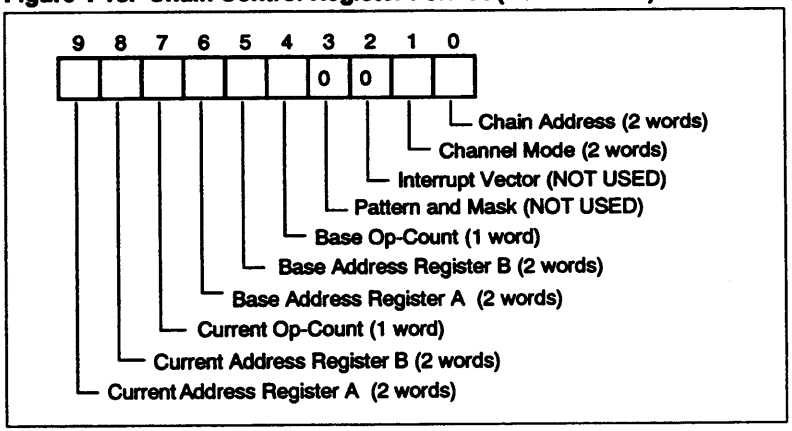
Command	Opcode	Command Description
Reset	0000 0000	Sets the UDC to the same state generated by a Hardware Reset. The Master Mode Register is set to all zeros; the CIE, IP and SIP bits are cleared; the NAC and CA bits in each channel's Status Register are set; and channel activity is forbidden. The Chain Address must be programmed since its state may be indeterminate after a Reset. The lockout preventing channel activity is cleared by issuing a Start Chain command.
Start Chain	1010 0001	Causes the selected channel to clear the NAC bit in the channel's UDC Status Register, and to start a chain reload operation of the channel's registers. These effects take place even if the fetched Reload word is all zeros. This command is only honored if both the CA and SIP bits in the channel's Status Register are clear. If this command is issued while the WFB bit in the UDC Status Register is set, the channel honors the command after one DMA iteration.
Set Software Request Clear Software Request	0100 0011 0100 0001	Sets or clears the Software Request bit in the Channel Mode Register. If the SIP and NAC bits in the UDC Status Register are both cleared, the channel starts executing the programmed DMA operation. The SIP bit is cleared when the channel receives an interrupt acknowledge. One way to clear the NAC bit is to issue a Start Chain command to the channel. If the fetched Reload word is all zeros, the channel's registers remain unchanged and the Software Request bit, if set earlier by command, causes the programmed DMA operation to start immediately. If during chaining new information is loaded into the Channel Mode Register, this new information overwrites the Software Request bit.
Set Hardware Mask Clear Hardware Mask	1000 0011 1000 0001	Sets or clears the Hardware Mask bit in the selected Channel Mode Register. This bit inhibits recognition of an active signal on the channel's DMA Request (DREQ) input; this bit does not affect recognition of a Software Request. If the channel is in single transfer mode, it performs DMA operations upon receipt of a transition on DREQ rather than in response to a DREQ level. Transitions occurring while the Hardware Mask bit is set are stored and serviced when the Hardware Mask is cleared, assuming the Channel has not chained. The UDC requests the system bus 1 1/2 to 2 clocks after receiving any DREQ, after which a minimum of one DMA iteration is unavoidable. DREQ transitions are stored only for the current DMA operation. If the channel performs a chain operation of single transfer mode, any DREQ transition stored for later service is cleared.
Set CIE Ch Set IP Set CIE & IP Clear CIE Clear IP Clear CIE & IP	0011 0011 0010 0111 0011 0111 0011 0001 0010 0101 0011 0101	Sets or clears any combination of the CIE and IP bits in the selected channel's UDC Status Register. Setting bit 4 to a one sets/clears the CIE bit; setting bit 2 to a one sets/clears the IP bit. These bits control the operation of the channel's interrupt structure. Setting the IP bit causes the Interrupt Save Register to be loaded with the current vector and status. The IP bit is cleared to facilitate an efficient conclusion to the processing of an interrupt.
Set Flip Bit Clear Flip Bit	0110 0011 0110 0001	Sets and clears the Flip Bit in the selected Channel Mode Register. It allows the user to reverse the source and destination, thereby reversing the data transfer direction without reprogramming the channel. This command is most useful when repetitive DMA operations are performed by the channel using Base-to-Current reloading for channel reinitialization and using this command to control transfer direction. Chaining new information into the Channel Mode register overwrites the Flip Bit.

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4.5.4.3 Chain Control Register

Chaining allows a channel to load its own control parameters from a Chain Control Table in memory, thereby minimizing the need for Host CPU intervention. When a channel begins a chaining operation, the Chain Control Register (Figure 4-13) is loaded with the Reload Word from the first memory location of the Chain Control Table. The address of this location is taken from the Chain Address Register. The channel retains control of the VXIbus until all of the registers defined in the Reload word have been reloaded. The bits in this Chain Control Register identify all registers that must be loaded from the Chain Control Table following the Reload Word.

Figure 4-13. Chain Control Register Format (Reload Word)



4.5.5 Channel-Level Registers

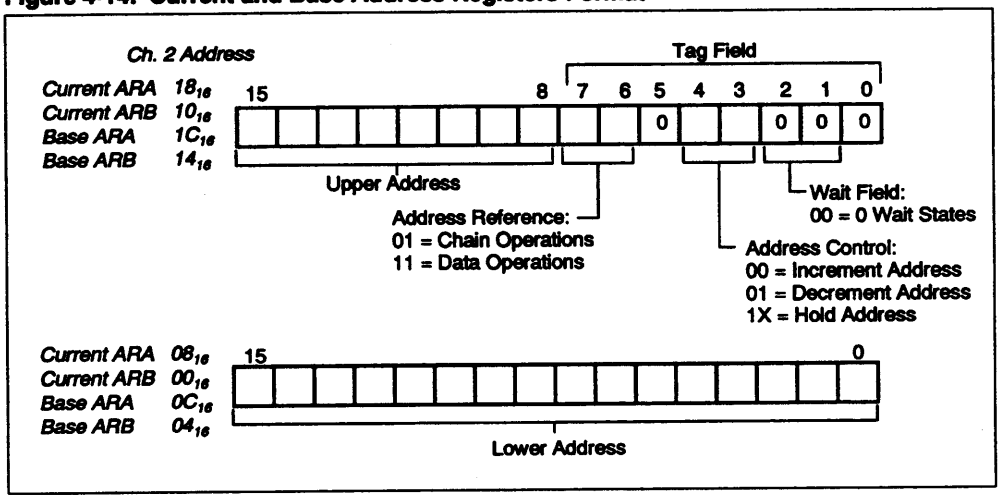
The following describes how the UDC Channel-Level registers are used.

4.5.5.1 Current and Base Address Registers A & B

These four registers (Figure 4-14) are divided into two Current Address Registers (A & B) and two Base Address Registers (A & B). They are referred to as the Current ARA and ARB and the Base ARA and ARB.

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Figure 4-14. Current and Base Address Registers Format



The Current ARA and ARB hold source and destination addresses of the current DMA operation. These can be loaded with the contents of the Base ARA and ARB upon completion of a DMA operation if the Base-to Current reload completion bit is set in the Channel Mode Register. This feature allows auto-reloading of repetitive operations without the overhead of Chaining.

4.5.5.2 Current Operation Count Register

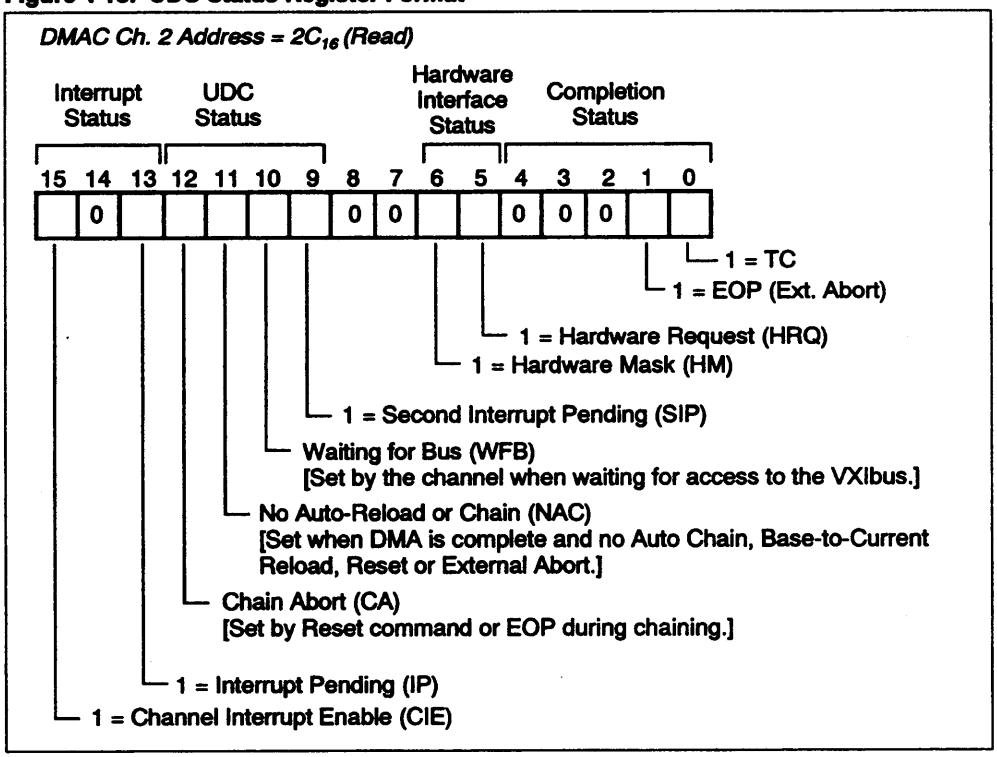
The Current and Base Operation Count Registers are two 16-bit registers that contain the number of words transferred during a DMA operation. When the contents have been decremented to 0000, the TC bit in the Status Register is set, indicating a successful completion of the operation. The maximum number of words (65535) can be transferred by loading the Current Count register with FFFF. The contents of the Base Operation Count Register can be read, written, or copied into the Current Operation Count Register.

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4.5.5.3 *UDC Status Register*

The UDC Status Register (Figure 4-15) contains four fields. The Completion Status field indicates why the most recent DMA operation terminated. Bit 5 of the Hardware Interface field monitors the channel's DMA Request signal. When the Hardware Mask bit is set, it inhibits the DMA response to a low-active signal on the channels DMA Request signal pin. The UDC Status field reflects the current channel state and are accessible to the Host CPU. The Interrupt Status field reflects the status of the current interrupt.

Figure 4-15. UDC Status Register Format



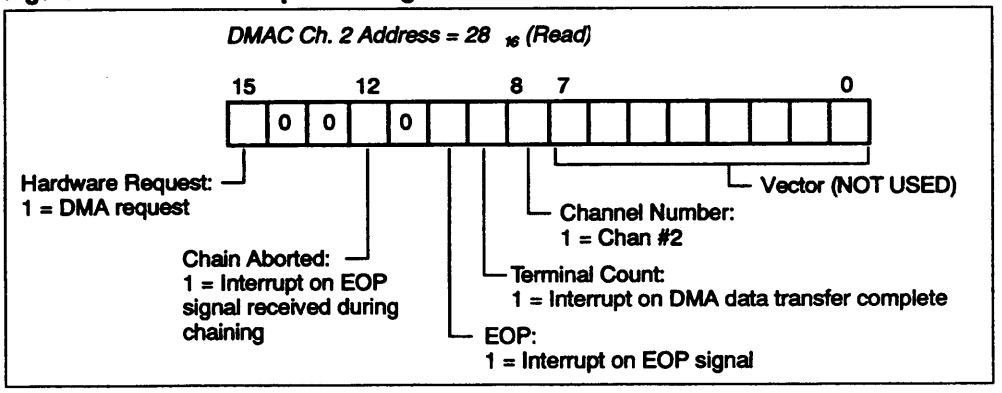
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4.5.5.4 UDC Interrupt Save Register

The 8-bit Interrupt Vector Register contains the vector or identifier put on the bus during an interrupt acknowledge cycle. When an interrupt occurs, because a DMA operation terminated or the EOP line was driven low during chaining, the contents of this register and part of the Channel Status Register are loaded into the 16-bit Interrupt Save Register (Figure 4-16).

The DMA controller has a two-level interrupt queue. When two interrupts are queued in the channel, the Second Interrupt Pending (SIP) bit in the status register is set. When the SIP is set, the Host can read the Interrupt Save Register to determine the source of the interrupt. All further activity on the channel is prohibited until the Interrupt Acknowledge clears the SIP bit. This ensures that the DMA never gets more than two operations ahead of the host processor.

Figure 4-16. UDC Interrupt Save Register Format

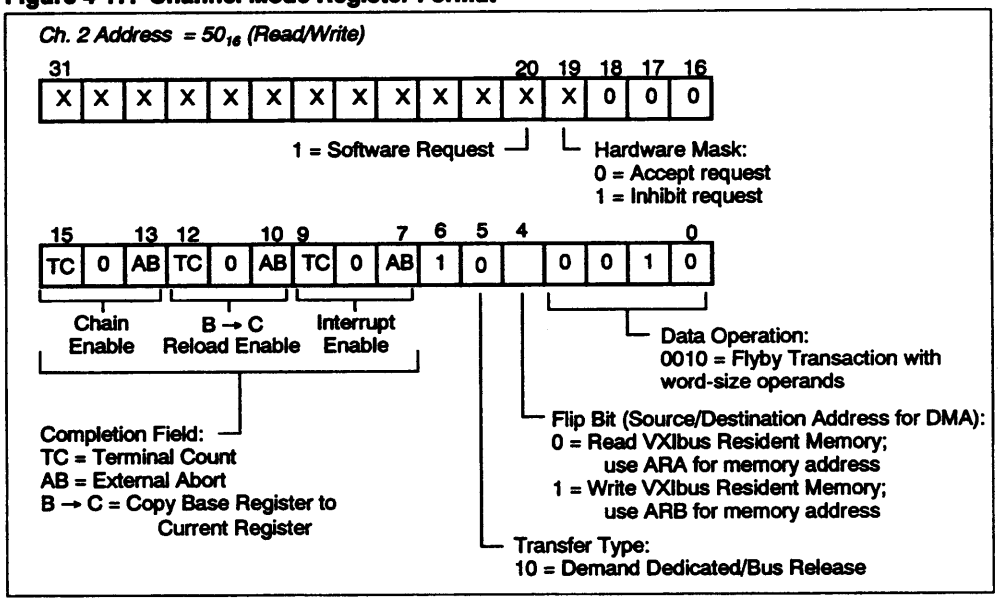


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4.5.5.5 Channel Mode Register

The Channel Mode Register (Figure 4-17) selects the type of DMA operation to be performed, the manner of execution and the action taken upon completion or abnormal termination of the operation. Bit 20 (Software Request) is set when DMA operations are initiated to chain in commands, addresses, etc., for data transfers. It is loaded by writing to the Command Register and is best done via chaining. Bit 19 (Hardware Mask) bit is set only by chaining. Although it can be loaded by writing the Command Register, it is best done via chaining. Bits 15 – 7 (Completion Field) enable three actions based upon how the current operation is terminated. For example, if Chain Enable TC is set when the current operation count reaches TC, the channel is switched to the chain mode to chain in the new Reload word. If Interrupt Enable AB is set when the operation is aborted due to abnormal conditions, the channel generates an interrupt to the host processor. Setting a bit in the B→C Reload field causes the Base Address and Base Operations Count registers to be copied into the current Address and Current Operation Count registers when the terminal condition occurs. This allows continued feeding from a single or circular buffer. Bit 4 (Flip Bit) determines whether ARA or ARB is treated as the source or destination address for the DMA operation.

Figure 4-17. Channel Mode Register Format

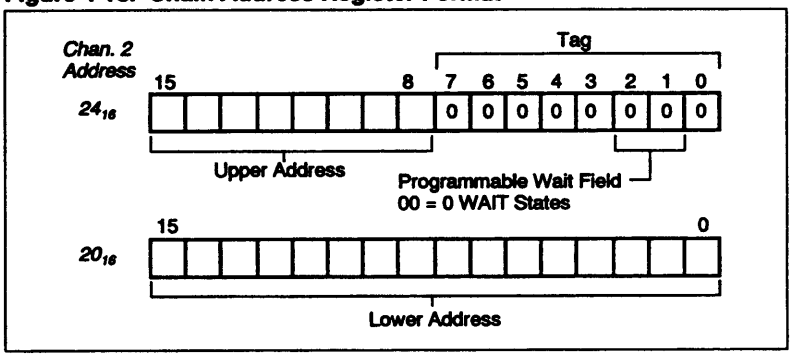


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4.5.5.6 Chain Address Register

The contents of the Chain Address Register (Figure 4-18) point to the Chain Control Table in the VXIbus resident memory where the data to be loaded into the channel's other registers during chaining is located.

Figure 4-18. Chain Address Register Format



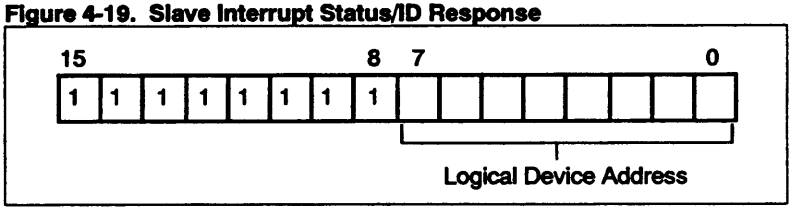
4.6 HOST INTERRUPT

A Host interrupt is received from the Waveform Generator when it is in the DMA mode. Although the UDC has its own interrupt enable bit, the Control Register Interrupt Enable (bit 7) is also used to enable or disable the interrupt. When interrupting the Host, this instrument supplies an 8-bit interrupt vector (Logical Device Address) to the VXIbus interrupt handler.

A DMA interrupt is generated when a DMA operation is completed. Upon execution of the hardware interrupt cycle, the Slave Interrupt Status/ ID Register (Figure 4-19) is returned. To determine the reason for the interrupt, the Host driver reads the UDC Status Register (Figure 4-15). If bit 9 (SIP) is set, the Host reads the Interrupt Save Register (Figure 4-16). A DMA interrupt is dismissed when the Host writes a Clear Interrupt command (CLEAR IP) to the UDC. The Logical Device Address is derived from Base Address jumpers J4-J7 and J9-J12. See Section 2.2.1.

/*

Figure 4-19. Slave Interrupt Status/ID Response



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Section 5
Specifications

Unless otherwise noted, all specifications apply at +25 degrees Celsius.

Analog Output

Number of ports	4
Number of outputs	8 (2 per channel)
Resolution	16 bits
Output Voltage	±6V S.E. / ±3V Diff. (DBS 8751A) ±10V S.E. / ±5V Diff. (DBS 8752A)
Offset	±30 mv max. (DBS 8751A); ±50 mv max. (DBS 8752A)
Output Drive Current	40 mA per output
Slew rate	7 volts per usec min.
Output Impedance	0.5 ohm max.
DC Gain Error	± 0.5%

Filter Characteristics

Corner Frequency	21 kHz.
Attenuation rate	36 dB per octave
Settling time (Step input)	100 usec. typ.
Overshoot (Step input)	30% of FSR typ.
Flatness in passband	± 0.2 dB max. at 0-10 kHz

Dynamic Characteristics

Sampling rate	204.8 kHz to 3.6 kHz in 1006 steps
Channel-to-channel Crosstalk	- 88 dB max.
Signal/Noise (with filter)	+ 84 dB Typ.
Peak Distortion	- 95 dB @ 10 Khz Typ.

NOTE: Peak Distortion represents the ratio between the highest spurious frequency component below the Nyquist rate and the test signal.

Total Harmonic Distortion	- 90 dB @ 10 KHz Typ.

NOTE: Total Harmonic Distortion represents the ratio between the rms sum of all harmonics up to the 20th harmonic and the rms value of the test signal.

Transfer Characteristics

Differential Non-Linearity	60 ppm FSR
Monotonicity	14 bits Guaranteed

Stability (0 Deg to +50 Deg C.)

Required Warm-up Time	15 minutes (for ultimate specifications)
Offset Tempco	12 ppm FSR/Deg C max.
Gain Tempco	70 ppm FSR/Deg C max.
Precision Clock	3.6864 MHz ±0.001%

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Digital Inputs

Logic Levels	TTL/CMOS Compatible Logic "1": 2.0 volts min. Logic "0": 0.8 volts max.
Termination	50 Ohms in series with 200 pf
External Sampling Clock (EXT CLK)	TTL Active low, 2.0 µsec min., 50 ohm load
External Precision Clock (EXT CLK)	2.4 MHz to 4.0 MHz, 50% duty cycle, 50 ohm load
External Precision Clock (TTLTRG0-3)	1.0 MHz to 5.0 MHz, 50% duty cycle
External Trigger	TTL, rising edge

Sampling Modes

Internal	Derived from internal Precision Sampling Clock
External	Derived from a user-supplied 2.0-Mhz to 4.0-Mhz precision clock or an absolute sampling rate clock.

Data Transfer

Input coding	Two's Complement
DMA	On-board controller, 0.8 Mword/sec., typ.

VXI Compliance

Master	A24, D16, RWD, Register-based
Slave	A16, D16, I7
Interrupt	Seven level, jumper selected

Group Isolation

500 volts DC max. 1 minute

Front Panel Indicators

Pass/Fail LED	Green/Red
DMA Transfer Active	Green
DAC #0 Running LED	Green
DAC #1 Running LED	Green
DAC #2 Running LED	Green
DAC #3 Running LED	Green

Power Required

+5 volt supply	+4.75 to +5.25 volts
Power dissipation	20 watts max.

Environmental and Mechanical

Temperature Range	Rated Performance: 0 to 50 Deg C. Storage: -25 to 75 Deg C.
Relative Humidity	0 to 85 % non condensing to 40°C.
Recommended Forced Air Cooling	10 CFM per min.
Dimensions	VXI C-size, single slot
Front Panel Potential	Chassis Ground

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Appendix A
VME/VXIbus Signal List

VME Bus P1 Connector

Pin	Signal Mnemonics		
	Row a	Row b	Row c
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	Not Used	SYSRESET*
13	DS0*	Not Used	LWORD*
14	WRITE	Not Used	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	Not Used	A17
22	IACKOUT*	Not Used	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	Not Used	Not Used	Not Used
32	+ 5V	+ 5V	+ 5V

Not Used means the the VME/VXI signal is not connected on the card.

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VME / VXI Bus P2 Connector

Pin	Signal Mnemonics Row a	Row b	Row c
1	Not Used	+ 5V	Not Used
2	Not Used	GND	Not Used
3	Not Used	Not Used	GND
4	Not Used	Not Used	Not Used
5	LBUSA00	Not Used	LBUSC00
6	LBUSA01	Not Used	LBUSC01
7	Not Used	Not Used	GND
8	LBUSA02	Not Used	LBUSC00
9	LBUSA03	Not Used	LBUSC01
10	GND	Not Used	GND
11	LBUSA04	Not Used	LBUSC00
12	LBUSA05	GND	LBUSC01
13	Not Used	+ 5V	Not Used
14	LBUSA06	Not Used	LBUSC00
15	LBUSA07	Not Used	LBUSC01
16	GND	Not Used	GND
17	LBUSA08	Not Used	LBUSC00
18	LBUSA09	Not Used	LBUSC01
19	Not Used	Not Used	Not Used
20	Not Used	Not Used	LBUSC00
21	Not Used	Not Used	LBUSC01
22	GND	GND	GND
23	TTLTRG0*	Not Used	TTLTRG1*
24	TTLTRG2*	Not Used	TTLTRG3*
25	Not Used	Not Used	GND
26	TTLTRG4*	Not Used	TTLTRG5*
27	TTLTRG6*	Not Used	TTLTRG7*
28	GND	Not Used	GND
29	Not Used	Not Used	Not Used
30	MODID	Not Used	GND
31	Not Used	Not Used	Not Used
32	Not Used	+ 5V	Not Used

Not Used means the the VME/VXI signal is not connected on the card.

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Appendix B
Calibration

INTRODUCTION

The DBS 8751(2)A provides no manual offset or gain trim adjustments. It is calibrated by storing offset and gain correction data in memory. Each output can be calibrated using the equation "Y = Mx + B", where B is the offset correction and M is the gain correction. You may also want to apply a (sin x)/x correction to the waveform data before loading it into the DAC data memory.

Offset and Gain Correction

The calibration procedure starts by setting each DAC output to zero and measuring the offset voltage at the analog output connector with no load applied (Table B-1). Then, each DAC output is set to a voltage less than Full Scale (GCS), corrected by the offset value and measured again with no load. The gain correction factor is calculated last.

(1) Set analog output port P_n (n = 1, 2, 3) to zero (0000_{16}).

(2) Using a seven-digit DVM at the output connector, measure and record the output voltage (B_n).

(3) Set the port to the two's complement of voltage B_n.

(4) Modify the offset output voltage B_n until the measured voltage at the connector is zero.

(5) Set the port to the value K_n = GCS – B_n (See Table B-1 for the value of GCS). Measure the output and record it as Z_n.

(6) Calculate the gain correction factor: $M_n = Z_n \div GCS$.

(7) Correct the (sin x)/x error (Section A.2.2).

Table B-1. Calibration Input Codes

Input (Hex)	DBS 8751A Output	DBS 8752A Output
8001	+5.999695	+9.999695
8198	+5.925292 (GCS)	+9.875488 (GCS)
0000	0	0
7FFF	–5.999695	–9.999695

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(sin x)/x Error Correction

Due to the nature of the sampling and waveform reconstruction process, the (sinx)/x error should be corrected With a sampling rate of f_s, the correction takes the form of Equations 1 and 2. The correction is to be applied over the pass band of the filter (0 to 20 kHz). Values of "K" across the pass band are given in Table B-2.

$$K = \frac{\sin\left(\frac{2\pi f}{f_s}\right)}{\left(\frac{2\pi f}{f_s}\right)} = \frac{f_s \sin\left(\frac{2\pi f}{f_s}\right)}{2\pi f} \qquad \text{[Equation 1]}$$

$$Y = \frac{A \sin 2\pi f}{K} \qquad \text{[Equation 2]}$$

NOTE: In Equation 2, "Y" must always be less than full scale.

Table B-2. K Values Across Pass Band

f_{out} (kHz)	K	dB
0	1.0	0
2	0.99937	–0.0055
4	0.99750	–0.0218
6	0.99436	–0.0491
8	0.98999	–0.0874
10	0.984386	–0.1367
12	0.97756	–0.1971
14	0.96954	–0.2687
16	0.96032	–0.3517
18	0.94994	–0.4460
20	0.93842	–0.5520

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