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DBS907
907LM/907HV

1 GS/s VXI Waveform Digitizer Plug-In Module

Plugs into the Analogic DBS 9905 "C" Size VXI Carrier Module

Introduction

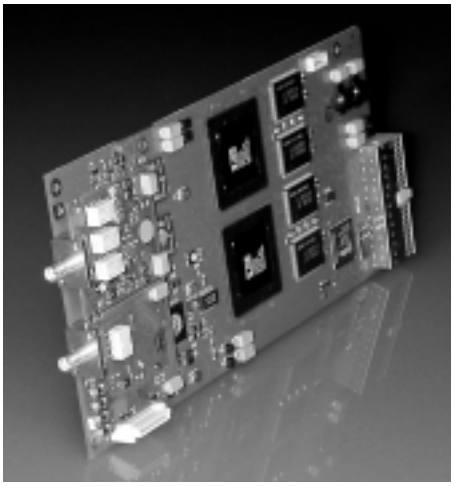
The Analogic DBS907 is a 1 GigaSamples/second Waveform Digitizer that plugs into the DBS 9905 “C” size VXI carrier module. One or two DBS907s can be installed in a single DBS 9905. This mezzanine board concept enables a single VXI chassis slot to provide multiple functions, thereby maximizing VXI resources and decreasing the cost per slot. The DBS907 provides a combination of speed, resolution, and size that, until now, was unavailable, and it builds on the Analogic tradition of providing the highest possible state-of-the-art performance at the lowest price available.

The DBS907’s broad sampling rate range of 100 S/s to 1 GS/s coupled with an input bandwidth of DC to 500 MHz (–3 dB), 8-bit resolution and 2 MegaSamples (8 MS for DBS907 LM) on-board memory position it for use in Telecommunications, Magnetic Media, Automotive, Time-of-Flight Mass Spectroscopy, Computing, Particle Physics, Military, Explosive-Weapons and Ballistic Testing applications. User programmable configuration of the DBS907’s front end further optimizes the digitizer’s performance and can be used to satisfy specific requirements in these and other applications.

General Description

The DBS907 is a single-channel, 8-bit, 1 GS/s Waveform Digitizer with 2 MS (8 MS for DBS907LM) of on-board memory. The DBS907 front end can be programmed for AC or DC coupling and 50Ω or 1 MΩ input impedance, making it easily adaptable for use with either coaxial transmission cable or high impedance probes. The high impedance mode also features very low, 10 pF capacitance that helps minimize the loading effect that can occur when probing high frequency circuits. A programmable amplifier is used to optimize the DBS907’s dynamic range by scaling the input to a Full Scale Range (FSR) that is appropriate for the signal of interest. Available ranges are; 50 mV, 100 mV, 200 mV, 500 mV, and 1V, 2V and 5V on the DBS907 and LM versions; or 10V, 20V and 50V on the DBS907HV. A variable offset of ±2V for all mV ranges or ±20V (±100V on DBS907HV) for the higher FSRs can also be employed to maintain the digitizer’s dynamic range in instances where the signal of interest is not centered around 0V.

A crystal-controlled time base, accurate to ±25 ppm, is used to clock the DBS907’s ADC subsystem. A Trigger Time Interpolator (TTI), with 5 ps resolution max, is also used to measure the time from the trigger to the first sample point. The sampling rate has a range of 100 S/s to 1 GS/s and is programmed in increments of 1, 2, 2.5, 4 or 5 (e.g., 1 MS/s, 2 MS/s, 2.5 MS/s, 4 MS/s, 5 MS/s, 10 MS/s, etc.). For divergent sample rates or to synchronize the ADC clock with the signal of interest, an external clock signal input is available. Data acquisition may be triggered from the input signal itself, the internal trigger, an external signal input or VXI TTLTRG lines. In most cases the trigger condition can be more precisely defined by selecting the trigger slope and trigger level (threshold) as well as a trigger coupling mode, DC or AC LFReject. The trigger level is defined as a set voltage at which the selected trigger source will produce a valid trigger. (NOTE: All trigger circuits have sensitivity levels that must be exceeded in order for reliable triggering to occur.) Regardless of the trigger source, data is captured around the specified trigger event and stored as user-defined, pre- or post-trigger



Features

- ❑ 1 GS/s Sampling Rate
- ❑ 500 MHz Bandwidth
- ❑ 2 MS Acquisition Memory (8 MS Option)
- ❑ Internal Calibration
- ❑ Input Protection
- ❑ Pre- and Post-Triggering
- ❑ High Resolution Trigger Timer Interpolator
- ❑ Low Power Consumption (<15W)
- ❑ VXI Plug & Play Software
- ❑ TV Trigger
- ❑ High Voltage Option
- ❑ Trigger Holdoff

Applications

- ❑ Telecommunications
- ❑ Magnetic Media
- ❑ Ultrasonic
- ❑ Radar
- ❑ ATE
- ❑ Vibration Analysis
- ❑ Time-of-Flight Mass Spectroscopy
- ❑ Beam Instrumentation

VXI bus

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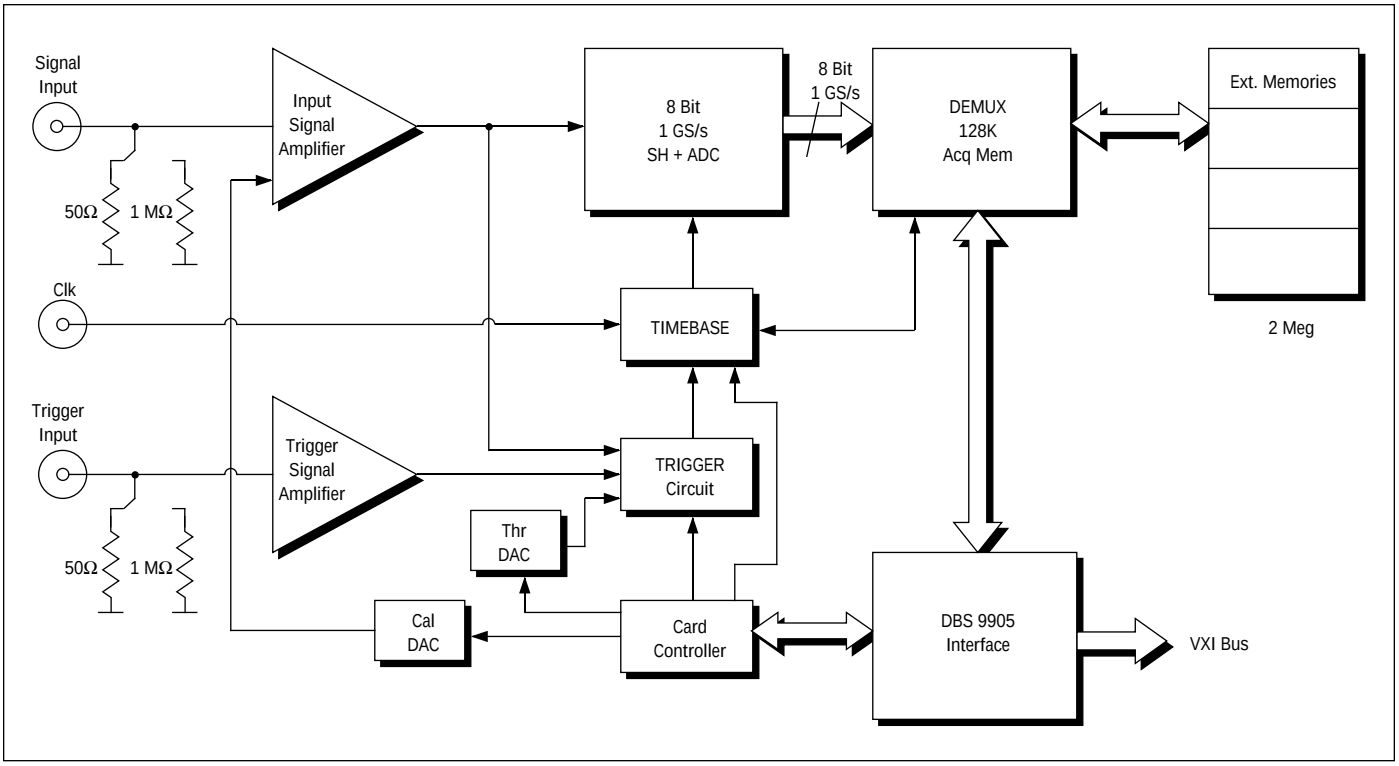


Figure 1. DBS907 Block Diagram.

data. A pre-trigger delay can be adjusted from 0% (all data points acquired after the trigger) to 100% (all data points acquired before the trigger) of the acquisition frame, or anywhere in between. Post-trigger delay can be adjusted between 0 and 200 million samples. Data from the ADC is stored in on-board memory. Trigger hold off is also provided with a range of 65K events maximum at a resolution of one event or 6.5 ms maximum at a resolution of 100 ns. The amount of data stored is programmable and can range from 100 samples to the full 2 MS (8 MS for DBS907LM). TV trigger with support for either 625 lines per frame (50 Hz) or 525 lines per frame (60 Hz) is standard on all DBS907 configurations.

Software

A VXI Plug & Play compliant software driver is supplied that supports all functions of the DBS907 and provides automatic recognition and configuration for all plug-in modules that are installed in the DBS 9905 carrier unit. The source code is included as well as .DLL files to allow easy porting to most popular programming environments. These drivers exceed VXI Plug & Play requirements to help ensure that system integration and software development time are reduced to an absolute minimum.

In addition, a comprehensive set of measurement functions is included with each module: Frequency, Volts amplitude, Volts average, Volts maximum, Volts peak-to-peak, Volts minimum, VAC RMS, VDC, +Pulse Width, –Pulse Width, Rise Time, Fall Time, Period, Duty Cycle, Delay, Volts Base. Volts Top, Overshoot.

Operations supported include: Add, Substract, Multiply, Divide, FFT.

Modes of Operation

The DBS907 has two acquisition modes, Single and Sequence. These modes provide an efficient means of utilizing memory while taking advantage of the DBS907's high sampling rate.

Single Acquisition Mode

Acquired waveforms are the result of a series of ADC measurements (sample points) taken at a uniform clock rate. In this mode the user selects the desired sampling rate and acquisition memory size and sets the number of segments to 1. Each waveform is then recorded using a single trigger.

Sequence Acquisition Mode

In this mode the acquisition memory is divided into a preselected number of segments between two and four thousand. Each segment is then used to store waveforms acquired from successive triggers. In this mode the trigger re-arm time is less than 500 ns, resulting in very low "dead time" (when the digitizer cannot acquire data from a new trigger event). In this mode each trigger event is time stamped. Readout of the individual trigger time stamps makes it possible to determine the time (with 5 ps resolution) between one trigger to any other trigger in the sequential acquisition.

Multi-Module Synchronization

All DBS907 digitizers include a proprietary, high bandwidth, auto-synchronous bus system, ASBus, that distributes both the clock and trigger signals along an optional, module-to-module, plug-in, bus connector. This allows two digitizers to work together sychronously to, in effect, create a 2-channel system.

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DBS907
907LM/907HV
Specifications

SIGNAL INPUT		
Parameter	*Condition*	*Value*
Bandwidth	–3 dB	DC to 500 MHz (907/LM) >250 MHz (907HV)
Full Scale Range (p-p)	Low-level	50 mV, 100 mV, 200 mV, 500 mV
	High-level	1V, 2V, 5V (907/LM) 10V, 20V, 50V (907HV)
Offset Range	≤ 500 mV FSR	±2V range
	≥ 1V FSR	±20V range
	≥ 10V FSR	±100V range
Input Impedance	Programmable	1 MΩ/10 pF; 50Ω ±0.5%
Number of Channels		1 single-ended
Input Coupling	Programmable	AC or DC
Over Voltage Protection	@1 MΩ Input Impedance	100V (DC+peak AC < 10 kHz)
	@50Ω Input Impedance	±5V DC (500 mW) or 5V RMS
	@1 MΩ Input Impedance (HV only)	250V (DC+peak AC < 10 kHz)
Overload Recovery Time	@2% FSR with 2 x FSR positive or negative 100 ns pulse returning to 0V	15 ns (typ.)
Overshoot	With 500 ps rise time pulse	< 20% FSR
Long Term Settling Time	@0.5% of step amplitude (80% FSR)	50 ns (typ.)
Connector Type		SMA or BNC

DIGITAL CONVERSION		
Parameter	*Condition*	*Value*
Conversion Rate	Internal Clock	100 S/s to 1 GS/s
Aperture Uncertainty		± 1 ps
Acquisition Memory Size		2 MS (8 MS for DBS907LM)
Resolution		8 bits (1:256)
Differential Linearity		± 0.7 LSB

TRIGGER (INTERNAL & EXTERNAL)		
Parameter	*Condition*	*Value*
Slope	Programmable	Positive or Negative
Coupling	Programmable	DC or AC (50 kHz LFReject)
Trigger Sensitivity	Internal Trigger	From DC to 250 MHz: levels >15% FSR
	External Trigger	From DC to 250 MHz: levels > 500 mV
Internal Trigger Threshold		FSR ± 60%
Pre-Trigger Delay		0% to 100% of data set
Post-Trigger Delay		0 to 200 MS
Hold Off	Programmable	1 to 65K events or 100 ns to 6.5 ms
Hold Off Resolution		1 event or 100 ns
Bandwidth	(–3 dB)	DC to 500 MHz
Trig. Threshold	Variable	–3V to +3V
Max. Input Voltage		± 5V DC (500 mW)
Impedance	Programmable	1 MΩ or 50Ω
Connector Type		BNC or SMA
TV Trigger	Programmable	525 lines/frame or 625 lines/frame

TIME BASE		
Parameter	*Condition*	*Value*
Clock Accuracy	Internal Clock	< 25 ppm
Acquisition Modes	Single Shot	100 to 2M or 8 Msamples
	Sequence	1 to 4k or 16k segments
Trigger Dead Time	Sequence Mode	< 500 ns
Trigger Time Interpolator	Sequence Mode	5 ps resolution

SYSTEM PERFORMANCE		
Parameter	*Condition*	*Value*
DC Accuracy		< ±2% FSR ±1% FSR typ.
Integral Linearity		< ±1% FSR
ENOB (at 1 GS/s)	DC – 20 MHz	> 6.8
	20 – 100 MHz	> 6.0
SFDR	100 MHz	–44 dB typ.
Temperature Drift	Offset	< 1000 ppm FSR/°C
	Gain	< 200 ppm FSR/°C

EXTERNAL INPUTS FOR CLOCK & REFERENCE		
Parameter	*Condition*	*Value*
External Clock Frequency		10 MHz to 500 MHz
External Reference Clock Freq.		10 MHz
Clock/Ref. Threshold	Variable	–3V to +3V
Clock/Ref Amplitude	Minimum	500 mV pk-pk

DBS907 POWER REQUIREMENTS		
Supply Voltage	***Amps, Max.***	***Watts***
+24 VDC	0.0	0.0
–24 VDC	0.0	0.0
+12 VDC	0.1	1.2
–12 VDC	0.0	0.0
+5 VDC	1.8	9.0
–5.2 VDC	1.2	6.3
–2 VDC	0.2	0.4

RELIABILITY		
Parameter	*Condition*	*Value*
MTBF	Determined by the Generic Parts Count method of MIL-HDBK-217F for a ground benign environment at a temperature of 30°C	>25,000 Hrs

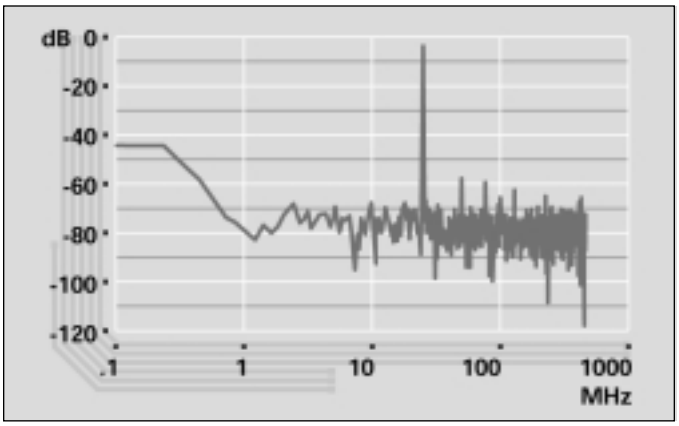
GENERAL		
Parameter	*Condition*	*Value*
Operating Temperature	5% to 90% humidity (non-Condensing)	0°C to 40°C

Specifications subject to change without notice

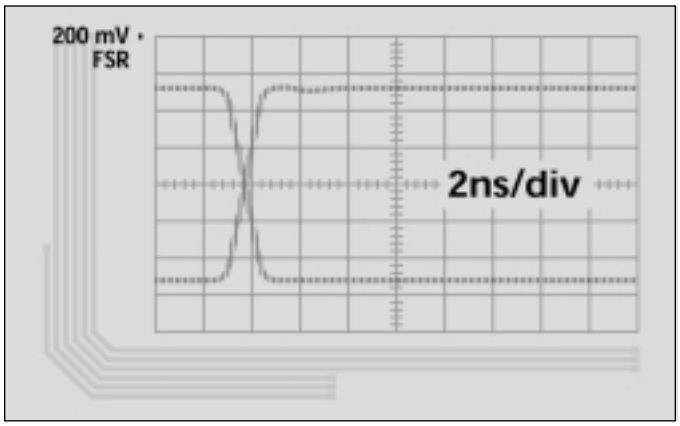
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Quality Performance

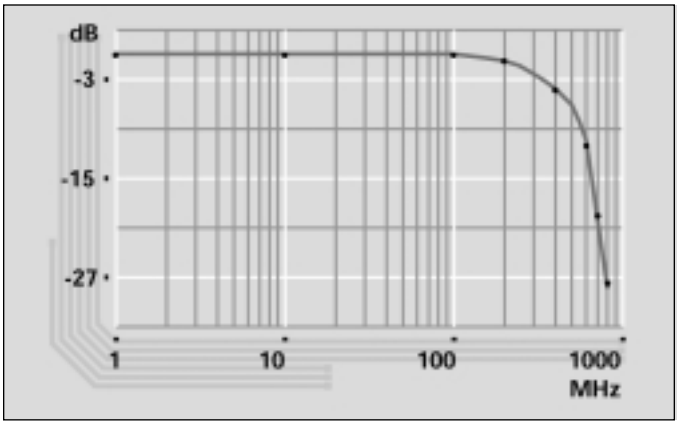
The DBS907's low noise, low harmonic distortion, step response, flat frequency response and effective number of bits (ENOB) are depicted in the following plots.



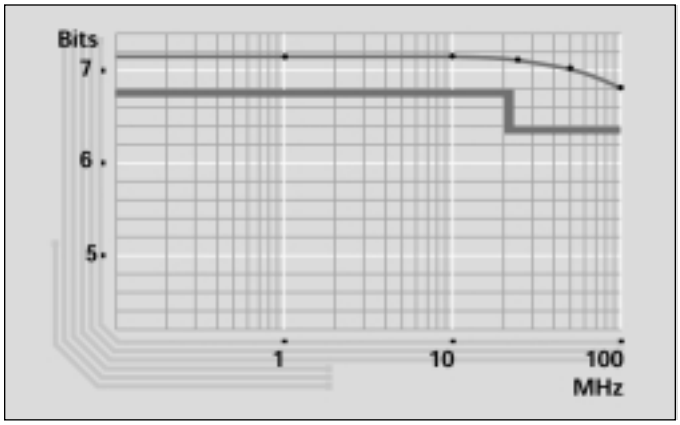
FFT analysis of a pure 25 MHz sinewave, measured at 500 mV full scale, showing very low noise floor and little harmonic distortion.



Positive and negative step responses show little or no overshoot or undershoot.



Frequency response is very flat and system bandwidth reaching well beyond the specified 250 MHz.



Effective bits (top graph) are significantly higher than the minimum guaranteed performance (bottom graph).

Ordering Guide

Model Number	Output Connector	Memory Size
DBS907	SMA	2 MS
DBS907B	BNC	2 MS
DBS907LM	SMA	8 MS
DBS907LMB	BNC	8 MS
DBS907HV	BNC	2 MS

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