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DVX 2504

VME/VXI Data Acquisition System

USER'S MANUAL

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DVX 2504

VME/VXI Data Acquisition System

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P/N 82-5085
Revision 0
February 1, 1992

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TABLE OF CONTENTS

1.0 GENERAL INFORMATION 1-1

2.0 HARDWARE INSTALLATION 2-1

2.1 BOARD CONFIGURATION 2-1
- 2.1.1 VME Slave Address 2-2
- 2.1.2 Internal/External Clock 2-2
- 2.1.3 Internal/External Trigger 2-2
- 2.1.4 DAS Data Output Format 2-3
- 2.1.5 VME Interrupt 2-4
- 2.1.6 TTLTRG Jumpers 2-4
- 2.1.7 Remote Triggering 2-6
- 2.1.8 Analog Signal Guard 2-7

2.2 EXTERNAL SIGNAL INPUT 2-7
- 2.2.1 Analog Signals 2-7
- 2.2.2 Digital Signals 2-8

2.3 VME BUS BACKPLANE CONNECTIONS 2-9
- 2.3.1 Bus Grant In/Out Backplane Jumpers 2-9
- 2.3.2 IACKIN/IACKOUT Backplane Jumper 2-9

3.0 DAS SOFTWARE INSTALLATION ON SUN SYSTEMS 3-1

4.0 PROGRAMMING THE DVX 2504 4-1

4.1 PROGRAMMING OVERVIEW 4-1

4.2 DEFAULT DEVICE CONFIGURATION 4-2

4.3 DRIVER FUNCTION DESCRIPTIONS 4-2
- 4.3.1 OPEN (DEV, FLAG) 4-3
- 4.3.2 CLOSE (FID) 4-3
- 4.3.3 WRITE (FID, BUFFER, COUNT) 4-3
- 4.3.4 READ (FID, BUFFER, COUNT) 4-4
- 4.3.5 IOCTL (FID, CMD, DATA, FLAG) 4-5
  - 4.3.5.1 RESET 4-5
  - 4.3.5.2 RATE__DIVISOR 4-5
  - 4.3.5.3 CLOCK__SOURCE 4-5
  - 4.3.5.4 START__MODE 4-5

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4.3.5.5 RUN __ AD __ DIAGS 4-5
4.3.5.6 GET __ DIAG __ ERROR 4-6
4.3.5.7 THRESHOLD 4-6
4.3.5.8 TRIGGER__POLARITY 4-6
4.3.5.9 READ __ SRAM 4-6
4.3.5.10 TIMEOUT 4-6
4.3.5.11 GET __ ERROR 4-6
4.3.5.12 PRE __ POST __ TRIGGER 4-7
4.3.5.13 THRESHOLD __ TRIG 4-7
4.3.5.14 PRE __ TRIG __ BUF __ SZ 4-7
4.3.5.15 SET __ SIGNAL __ TYPE 4-7
4.3.5.16 READ __ REG 4-7
4.3.5.17 WRITE __ REG 4-7

4.4 ERROR HANDLING 4-8

4.5 DATA ACQUISITION EXAMPLES 4-8
4.5.1 Simple Acquisition 4-8
4.5.2 Pre/Post Data Acquisition 4-12

5.0 FUNCTIONAL DESCRIPTION 5-1

5.1 OVERVIEW 5-1
5.1.1 Analog Front End 5-1
5.1.2 A/D Converter 5-2
5.1.3 Control Sequencer 5-2
5.1.4 VME/VXI Interface 5-3
5.1.5 Power-Up Diagnostic Stimuli 5-4
5.1.6 DC/DC Converter 5-4

5.2 HARDWARE DEVICE REGISTERS 5-4
5.2.1 Device ID Register 5-5
5.2.2 Device Type Register 5-5
5.2.3 Control/Status Register 5-5
5.2.4 Sequence RAM Offset Register 5-6
5.2.4.1 Loading the Scan Sequence RAM 5-7
5.2.4.2 Gain/Channel Word 5-8
5.2.4.3 Channel/Port Word 5-8
5.2.4.4 A Typical Sequence RAM Load Table 5-9
5.2.4.5 SRAM Format For DVX Family 5-10
5.2.4.6 Order of Scan Restrictions 5-10
5.2.4.7 Example of Single Stage Delay 5-11
5.2.4.8 Example of Two Stage Delay 5-13

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5.2.4.9 Example of Three Stage Delay 5-14
5.2.4.10 Example of Five Stage Delay 5-14
5.2.4.11 Example of Single Stage Delay With Sample/Hold Multiplexer 5-16
5.2.5 Memory Device Attribute Register (Base Address + 0008H) 5-18
5.2.6 Sampling Rate Select Register (Base Address + 000AH) 5-18
5.2.7 Threshold Register (Base Address + 0010H) 5-19
5.2.8 FIFO Register (Base Address + 0012H) 5-20
5.2.9 AM9516 DMA Controller (DMAC) Pointer Register (Base Address + 000CH) 5-20
5.2.10 AM9516 DMA Controller (DMAC) Data Register (Base Address + 000EH) 5-22

5.3 DMA OPERATIONS 5-22
5.3.1 Normal Mode 5-22
5.3.2 Post-Trigger Mode 5-23
5.3.3 Pre/Post-Trigger Mode 5-23
5.3.4 DMA Address Modifiers 5-23

5.4 INTERRUPT OPERATIONS 5-24

5.5 AM9516A PROGRAMMING OVERVIEW 5-24
5.5.1 Registers 5-24
5.5.1.1 Chip-Level Registers 5-24
5.5.1.2 Channel-Level Registers 5-25
5.5.2 Commands 5-25
5.5.3 Chaining 5-25
5.5.4 Register Description 5-25
5.5.4.1 Master Mode Register 5-25
5.5.4.2 Command Register 5-26
5.5.4.3 Chain Control Register 5-27
5.5.4.4 Channel Mode Register 5-27
5.5.4.5 Current Address Registers, A & B 5-29
5.5.4.6 Base Address Registers, A & B 5-29
5.5.4.7 Current Operation Count Register 5-29
5.5.4.8 Base Operation Count 5-30
5.5.4.9 Status Register 5-30
5.5.4.10 Interrupt Save Register 5-31
5.5.4.11 Chain Address Register 5-31
5.5.4.12 Chain Control Register 5-31
5.5.5 Simple Example of DMA Operation 5-32
5.5.6 Driver Excerpt For DMA Operations 5-36

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6.0 SPECIFICATIONS 6-1

6.1 ANALOG INPUTS 6-1

6.2 AMPLIFIER CHARACTERISTICS 6-1

6.3 DYNAMIC CHARACTERISTICS 6-1

6.4 TRANSFER CHARACTERISTICS 6-2

6.5 STABILITY (0°C to + 50°C) 6-2

6.6 TRIGGER MODES 6-2

6.7 DATA TRANSFER 6-3

6.8 SEQUENCE CONTROLLER 6-3

6.9 POWER REQUIREMENTS 6-3

6.10 ENVIRONMENTAL 6-3

6.11 DIGITAL INPUTS/OUTPUTS 6-4

6.12 TEST CALIBRATION 6-4

6.13 VME DATA TRANSFER RATES 6-4

7.0 APPENDIX 7-1

7.1 VME/VXI COMPLIANCE 7-1

7.2 CONNECTOR PIN ASSIGNMENTS 7-1
7.2.1 Analog Input Connector J1 7-1
7.2.2 VMEBus P1 Connector 7-2
7.2.3 VME/VXI Bus P2 Connector 7-3

7.3 MECHANICAL OUTLINE 7-4

8.0 WARRANTY 8-1

9.0 SERVICE AND TECHNICAL SUPPORT 9-1

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1.0 GENERAL INFORMATION

This manual describes the operation of the DVX 2504 Data Acquisition System (DAS). It is organized into the following Sections:

Section 2.0 describes how to modify the jumper selectable features.

Section 3.0 covers installing the driver on a Sun Microsystems workstation.

Section 4.0 contains the definitions of all the driver calls used to initiate the acquisition of data.

Section 5.0 is a detailed functional description and contains the necessary depth of information should you choose to write your own driver.

The DVX 2504 card is a 1024 kHz, high resolution, multichannel DAS combining precision measurement and high throughput with the compactness of a dual eurocard (6U) VME (or VXI size B) format. Fully compatible with the VXI specifications, Rev. 1.3, the DAS occupies a single slot in a VME chassis and provides an unparalleled price performance ratio when used either alone or in combination with other VME/VXI -based boards (multiplexers, filters, digital-to-analog converters or array processors) in Analogic's DVX family of cards.

Eight shielded, differential input ports are provided with over-voltage current protection. The DAS is directly expandable to 256 channels with Analogic's family of DVX multiplexer boards. The input port signals are multiplexed via an instrumentation amplifier (IA) and a programmable gain amplifier (PGA) with four software selectable gains (1, 2, 4 and 8) and then fed into a 1024 kHz, 14-bit sampling A/D converter. The order of channels in the scan, the selected gain for each channel, the selection of the channel for data dependent triggering as well as the sampling rate are user programmable.

The converted data is temporarily stored in a 1024 word deep FIFO. When the FIFO is half full, it signals the powerful 2 channel on-board DMA controller to acquire the mastership of the bus. Then the DMA controller executes fast transfers over the VME bus sending data directly from the FIFO into the bus resident system memory until the FIFO is empty. The DMA controller automatically reads the necessary

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information regarding data set size and memory buffer areas from the bus resident memory relieving the controlling microprocessor of monitoring the DMA operations.

Three flexible conversion trigger sources are available:

Internal Trigger: Derived from a precision clock with acquisition started by either the VMEbus resident host processor or the user-supplied External Start command.

User-Supplied External Trigger: Acquisition is started by either the VMEbus resident host processor or the user supplied External Start command.

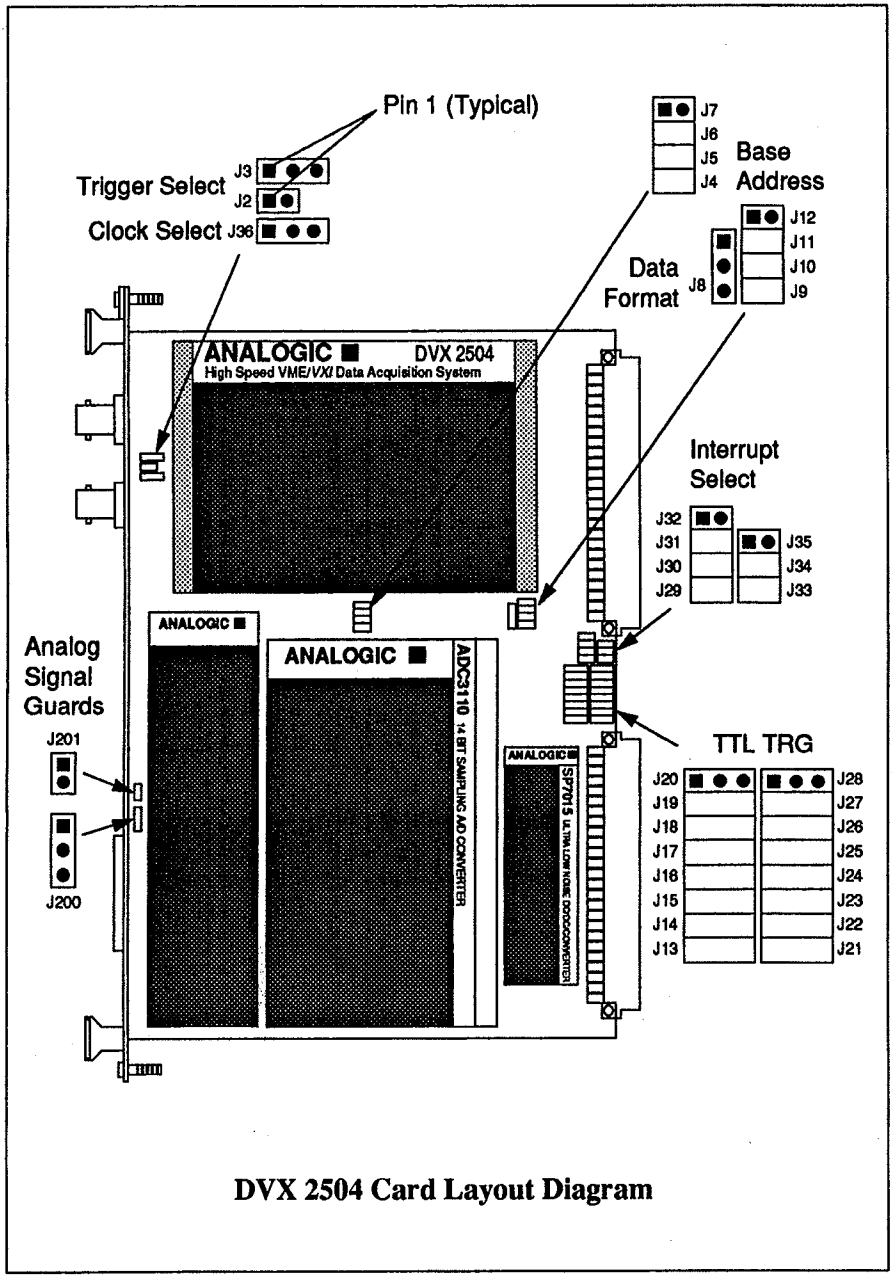
Internally/Externally Derived Trigger: Acquisition is started by the occurrence of a pre-specified data dependent event on a selected channel.

For ease of integration, a fully compatible UNIX (Berkeley 4.2)* software driver provides a set of high level routines for controlling the data acquisition.

** UNIX is a trademark of A.T.& T.*

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DVX 2504 Card Layout Diagram

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2.0 HARDWARE INSTALLATION

Remove the DVX 2504 from the carton and the anti-static bag, and visually inspect it for any shipping damage. Retain the carton and packing. Should the DAS fail to function properly, contact Analogic Customer service for return authorization. Any damage should be reported to the shipping company.

The VXI specification requires a lock-out key on the front panel of a card that uses the A & C rows of pins on the P2 connector. The purpose of the key is to prevent the insertion of the DAS card adjacent to a VXI incompatible card that could cause electrical damage to the card.

CAUTION

The DAS uses rows A & C on the P2 connector. Improper connection of signals on this connector could cause damage to the DAS card.

2.1 BOARD CONFIGURATION

The factory installed jumpers configure the card as follows:

Jumper Installed	Selected Function
J4 - J7 and J9 - J12	Base Address = C000
J2	Master Board (Remote Trigger Pulse origin)
J36-2 to J36-3	Internal Precision Clock
J3-2 to J3-3	External Trigger Input Selected
J8-1 to J8-2	Two's Complement Data Format
J32	Interrupt Level #1
J200-2 to J200-3	Analog Signal Input Guards connected to Analog Ground.
J21-1 to J21-2	ESTB connected to TTLTRG-7
J16-2 to J16-3	EXTSHL connected to TTLTRG-4
J15-1 to J15-2	EXTSH connected to TTLTRG-5

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2.1.1 VME Slave Address

The Base Address of the board is determined by the installation of jumpers according to the following table. The examples given illustrate the base address range; any 64 byte block of addresses from FFC0 thru C000 can be configured.

Base Address	J9	J10	J12	J13	J7	J6	J5	J4
FFCO								
FF80								X
FFOO							X	X
FEOO						X	X	X
FCOO					X	X	X	X
F800				X	X	X	X	X
FOOO			X	X	X	X	X	X
EOOO		X	X	X	X	X	X	X
COOO	X	X	X	X	X	X	X	X

X = jumper installed.

2.1.2 Internal/External Clock

The DAS provides a precision 3.072 MHz clock (±0.001%) for use as the sampling clock. However, the user may wish to use his own external precision clock and divide it down to the desired sample rate. The external clock is connected to the TRIG BNC in the front panel. See Section 2.2.2.

Function	Jumper
On-board precision clock	J36-2 TO J36-3
"TRIG" BNC jack = precision clock	J36-1 to J36-2

2.1.3 Internal/External Trigger

The user may wish to trigger the conversion from an external source rather than use either of the options above. The external trigger initiates the actual sampling of the input analog signal(s) but the internal precision clock is required to run the internal A/D controls. The external trigger is connected to the TRIG BNC on the front panel.

To use an external trigger, jumper J3-2 to J3-3.

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2.1.4 DAS Data Output Format

The data format from the DAS can be configured for Binary, Offset Binary or Two's Complement. The difference between the last two formats is that the most significant data bit in Offset Binary format is the complement of the most significant data bit in the 2's COMPLEMENT format.

For example:

Offset Binary:

MSB			LSB	Value
1111	1111	1111	1111	+ Full Scale
1000	0000	0000	0001	+ 1
1000	0000	0000	0000	Zero
0111	1111	1111	1111	- 1
0000	0000	0000	0000	- Full Scale

2s Complement:

MSB			LSB	Value
0111	1111	1111	1111	+ Full Scale
0000	0000	0000	0001	+ 1
0000	0000	0000	0000	Zero
1111	1111	1111	1111	-1
1000	0000	0000	0000	- Full Scale

The jumpers are installed as follows.

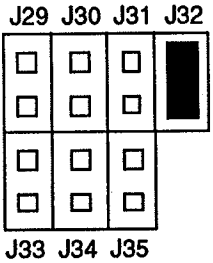
Binary or Offset Binary: J8-2 to J8-3
Two's Complement: J8-1 to J8-2

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2.1.5 VME Interrupt

Since the DAS requires a minimum of attention from the VME host processor after the necessary DMA transfer commands have been issued by the user's application program, there will be little need to closely monitor the acquisition operation. Therefore, the factory assembly of the DAS is set up for interrupt level 1 and the only interrupt jumper installed is J32. Should the user desire to assign the DAS to another interrupt level, the BREQ_INT PAL (Z-14) must be reprogrammed for the desired level and the interrupt jumper removed from J32 and installed at the desired level. A copy of the BREQ_INT PAL equations is included with the Operating System Driver. Jumper assignments are as follows.

Interrupt Level	Jumper
1	J32
2	J31
3	J30
4	J29
5	J33
6	J34
7	J35



2.1.6 TTLTRG Jumpers

When other cards in the DVX/DBS family are used in conjunction with the DAS, it is assumed that the user's backplane conforms to the VXIbus specifications for interconnection wiring between card slots. Failure to comply with the VXIbus electrical specifications may result in damage to, or unreliable operation of the DAS (and the companion cards).

CAUTION

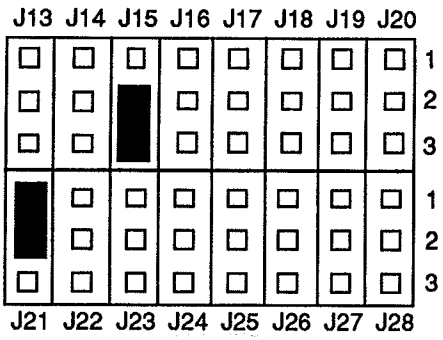
The DAS uses rows A & C on the P2 connector. Improper connection of signals on this connector could cause damage to the DAS card.

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If a companion card is used with the DAS, jumpers are required to pass high speed TTLTRG control signals to the other cards. The following table shows the four control signals that can be connected to the TTLTRG lines and the corresponding connection points for TTLTRG-0 through TTLTRG-7.

Control Signals	TTLTRG– Jumper Connection							
	7	6	5	4	3	2	1	0
REMTRG Remote Trigger	J21 2-3	J22 2-3	J23 2-3	J24 2-3	J25 2-3	J26 2-3	J27 2-3	J28 2-3
ESTB External Strobe	J21 1-2	J22 1-2	J23 1-2	J24 1-2	J25 1-2	J26 1-2	J27 1-2	J28 1-2
EXTSHL Ext. S/H (lo)	J13 2-3	J14 2-3	J15 2-3	J16 2-3	J17 2-3	J18 2-3	J19 2-3	J20 2-3
EXTSH Ext. S/H (Hi)	J13 1-2	J14 1-2	J15 1-2	J16 1-2	J17 1-2	J18 1-2	J19 1-2	J20 1-2

For Example, the diagram below depicts the jumpers installed to connect the EXTSHL signal to TTLTRG-5 and ESTB to TTLTRG-7.



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2.1.7 Remote Triggering

In those installations where there are 2 to 4 DAS cards in the same chassis, the user may wish to have one of the cards be the "master" trigger for all the other DAS cards. In this case, it is assumed that the user's backplane conforms to the VXIbus specifications for interconnection wiring between card slots. Failure to comply with the VXIbus specifications MAY result in damage to or unreliable operation of the DAS (and the companion cards).

In this case, the "master" trigger card should be configured to generate the REMOTE TRIGGER pulse while the "slave" cards should be configured to receive the REMOTE TRIGGER pulse. The REMTRG signal must then be jumpered to one of the TTLTRG lines on the P2 connector. See Section 2.1.6 above. The jumpering of the Master card and the Slave card(s) is defined as follows:

Jumper	Master	Slave(s)
J2	1-2	–
J3	1-2	1-2
J21-J28	2-3	2-3

The user must choose which of the eight TTLTRG lines is to be used to pass the REMTRG signal across the backplane from the Master to the Slave(s) and install the necessary jumper on the Master and the Slave(s).

Jumper	TTLTRG
J21	7
J22	6
J23	5
J24	4
J25	3
J26	2
J27	1
J28	0

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2.1.8 Analog Signal Guard

The analog signal guards (shields) for all channels are connected together to jumpers J200 & J201 which are located between the front panel and the differential multiplexer cover, just above the J1 analog input connector.

The user can connect the signal shields to any one of the following;

J201-1 to J201-2: Digital Gnd (VME backplane ground)

J200-1 to J200-2: Chassis Gnd (via front panel card cage retaining screws)

J200-2 to J200-3: Analog ground

See the label on the differential multiplexer cover for jumper connections.

2.2 EXTERNAL SIGNAL INPUT

2.2.1 Analog Signals

Analog signals should be brought to the DAS via twisted shielded pairs. The signal and the shield wires should be connected according to the table below. A metal back-shell should be used with the standard D type 25 pin male connector. Suggested components are the following:

a) ITT Cannon DB-25P or TRW-Cinch DB25P 25-pin D-type connector

b) AMP #745833-1 metallic backshell

c) Belden #8761 twin conductor shielded cable

	Connector Pin No.		
Port	+ IN	- IN	Guard
0	8	7	9
1	19	18	17
2	11	10	12
3	16	15	14
4	24	25	23
5	1	2	3
6	22	21	20
7	4	5	6

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2.2.2 Digital Signals

Through the TRIG and START front panel BNC jacks, the card accepts two TTL-level input signals.

a. External Trigger (TRIG input jack)

b. External Start (START input jack)

The two input jacks are terminated with a 50 ohm resistor in series with a 220 pf capacitor to ground.

The External Trigger signal directly triggers an A/D conversion. It is an active low pulse supplied by the user through the TRIG input jack. The user must set bit 6 (Ext. Trigger Select) and bit 4 (Start) in the Control Register to enable the externally-triggered conversion.

An External Start signal can be provided by the user through the START input jack. This active-low signal permits the user to externally control the start of an acquisition. The user must set bit 5 (Ext. Start Select) and bit 4 (Start) of the control register to enable an externally initiated acquisition.

If External Trigger is enabled (without enabling External Start), a conversion will occur when the External Trigger is asserted. If External Start is enabled and External Trigger is disabled, conversions will start when External Start is asserted low. If the user supplies both the External Trigger and External Start, the user is responsible for synchronizing the two signals as shown in Figure 2-1

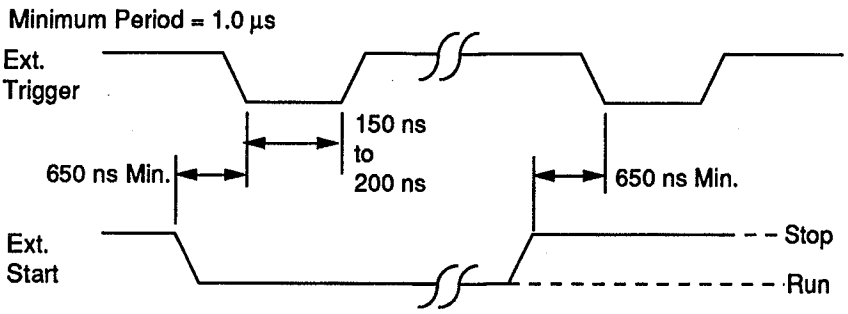


Figure 2-1. External Trigger and Start Synchronization

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To operate the DAS at a sampling rate that is incompatible with the internal precision clock and rate divisor, the board can be jumpered to accept an external clock through the TRIG input jack. The External Clock must be a 50% duty cycle, TTL-level signal within the range of 2.5 to 4.0 MHz. The Rate Register must be loaded with the proper divisor to obtain the desired sampling rate.

Digital Signal Jumper Matrix

Function	Jumper	Position
External Trigger	J36 J3 J2	2-3 2-3 1-2
External Clock and Rate Divisor	J36 J3 J2	1-2 1-2 Open
Internal Clock and Rate Divisor	J36 J3 J2	2-3 2-3 1-2

2.3 VMEBUS BACKPLANE CONNECTIONS

2.3.1 Bus Grant In/Out Backplane Jumpers

The DAS uses only bus request BR3* for requesting VMEbus ownership. Therefore, the BG3IN-BG30UT bypass jumper (or switch) located in the backplane for the slot that the DAS occupies must be removed (open).

Bus grants BG0IN, BG1IN and BG2IN are shorted through to the BG0OUT, BG1OUT and BG2OUT pins, respectively, on the P1 connector.

2.3.2 IACKIN/IACKOUT Backplane Jumper

The DAS requires that the IACKIN-IACKOUT jumper (or switch) located in the backplane of the slot that the DAS occupies must be removed (open).

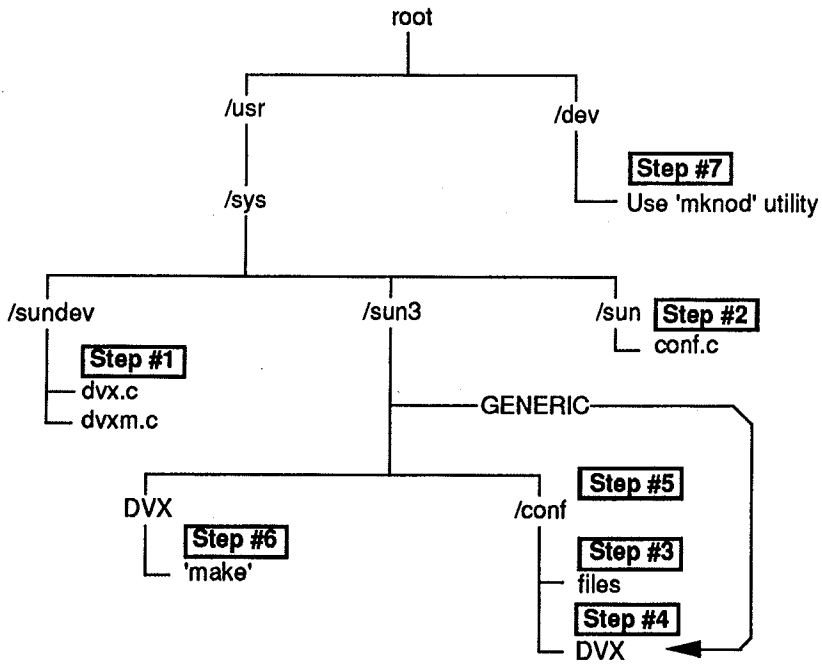
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3.0 DAS SOFTWARE INSTALLATION ON SUN* SYSTEMS

The DAS software is a UNIX device driver (based upon the Berkley Version 4.2) supplied in a source file format. Installation of the software requires reconfiguring the UNIX kernel as described in the following paragraphs.

The following figure shows a typical directory configuration and shows at which level in the structure each step in the following paragaphs takes place. It also shows where certain files referred to in the text are located.



Typical Directory Tree

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STEP 1

Copy the contents of the DVX/UNX release tape to the directory

'/usr/sys/sundev'

using the following command:

tar -xfr / dev / rs0 < cr>

STEP 2

Open the '/usr/sys/sun/conf.c' file and insert the following section near the top of the file:

```
#include "DVX/dvx.h"
#if NDVX > 0
int dvxopen ( ), dvxclose( ), dvxstrategy( ), dvxread( ),
dvxwrite( ); int dvxioctl( );
#else
#define        dvxopen          nodev
#define        dvxclose         nodev
#define        dvxstrategy      nodev
#define        dvxread          nodev
#define        dvxwrite         nodev
#define        dvioctl          nodev
#endif
```

Insert the following section in the Character Device switch table in any free device number location:

```
{
dvxopen,      dvxclose,     dvxread,      dvxwrite,     /* nn */
dvxioctl,     nodev,        seltrue,      0,
0,
}
```

Note the number "nn" in the right hand column, you will need it later.

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STEP 3

Add the following lines to "/usr/sys/sun3/conf/" files:

```
/usr/sys/sundev/dvx.c        optional dvx device-driver
/usr/sys/sundev/dvxm.c       optional dvxm device-driver
```

The file'dvx.c' is the actual driver source code, while the file 'dvxm.c' is a dummy driver used only to allocate memory in VME A24D16 space.

STEP 4

Change directory to "/usr/sys/sun3/" conf and copy the file GENERIC to the file you wish to use for the DAS configuration data base. Add in the following lines to this file:

```
device dvxm0 at vme24d16? csr 0x800000

device dvx0 at vme16d16 ? csr 0xc000 flags 0x800000 priority 1\
        vector dvxintr 0xc8
```

These lines define the particular device hardware configuration to the system by specifying the base address of the board in the appropriate VME address space, the interrupt priority, and the interrupt vector.

The line for 'dvxm0' allocates system memory in VME A24D16 address space for the Scan Sequence RAM; note that the 'flags' parameter in the line for "dvx0' must match the address specified for 'dvxm0'.

The line for device 'dvx0' specified a DAS base address of 0xffc000, an interrupt priority of one, and an interrupt vector of 0xc8; refer to the Hardware Installation Manual if the default settings are not desirable.

The **USER MUST ENSURE** that the addresses and interrupt vectors specified for the DAS do not conflict with those of other devices. Before moving on, check that the following are NOT used by any other device listed in this file:

a) The csr address 0xc000,

b) The interrupt vector 0xc8, and

c) The physical location of the Sequence RAM memory 0x800000.

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STEP 5

Run the 'config' utility to generate the necessary configuration data for the new kernel. For instance 'config DVX' would build the required configuration and place them in the file "/usr/sys/sun3/DVX."

STEP 6

Change directory to"/usr/sys/sun3/DVX" and type 'make' to build your new kernel. When 'make' has finished, change directory to the root and make a backup copy of the original 'vmunix'; copy the new kernel into the root directory and reboot the system.

Observe the following system messages:

'dvxm0 at vme24d16 xxxx'

and

'dvx0 at mve16d16 xxxx vec xxxx'

These indicate that the system has identified the DAS hardware. The driver will turn the PASS/FAIL light on the DAS to green if the startup diagnostics have passed.

If the driver does NOT detect the DAS card, then the only message displayed will be 'dvxm0 at vme24d16xxxx'.

STEP 7

Before using the driver, a device file must be created in the '/dev' directory for the DAS using the 'mknod' utility. For instance the command 'mknod /dev/dvx0 c nn 0' will create the device file 'dvx0' with a major device number of [nn]. Note that the device number used must correspond with the entry "nn" used in the character device table in 'conf.c' (Step 2). User applications access the device via an 'open' call to the appropriate device file.

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4.0 PROGRAMMING THE DVX 2504

4.1 PROGRAMMING OVERVIEW

The Unix device driver enables the host application to configure the hardware and acquire data directly into user process buffers using the DAS on-board DMA controller. Additionally, upon request from the main program, the driver can perform a diagnostic check of the hardware and report the status. All DAS control, acquisition, and diagnostic functions are accessed by the application through standard Unix system calls: 'READ', 'WRITE', and 'IOCTL'.

The following table references DAS hardware functionality with the corresponding DAS Unix driver functions.

DAS UNIX Drivers

Driver	Hardware Function
OPEN	Allocate the device and establish communication
CLOSE	Release the device
WRITE	Initialize the DAS Channel/Gain Sequence RAM
READ	Acquire data from the DAS using DMA
IOCTL	Perform Diagnostic Self Test DAS Hardware Reset Set Sampling Rate Divisor Read Sequence RAM Set Start Mode (internal/external) Set Trigger Threshold Set Trigger Source (external/internal) Set Trigger Polarity Set Data Acquisition Timeout Return Last DAS Specific Error Code Set Trigger Mode (Normal, Post-, Pre-/Post-) Set Input Signal Type Read A DAS Hardware Register Write A DAS Hardware Register Return Diagnostic Status Set Pre-Trigger Buffer Size

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In keeping with Unix driver conventions, all control and setup functions map to subfunctions of the Unix 'IOCTL' system call with the exception of the loading of the Sequence RAM which maps to the 'WRITE' function. The actual acquisition of data from the device is accomplished by the 'READ' Unix system call.

To program the DAS for data acquisition, follow these four simple steps:

(1) Use the Unix 'OPEN' system call to establish communication with the device.

(2) Use 'WRITE' to specify a channel/gain sampling sequence.

(3) Use a series of 'IOCTL' calls to specify the setup configuration.

(4) Use 'READ' to acquire the data into a user buffer.

Any setup specified in steps 1, 2, and 3 will remain valid until the device is released or explicitly changed by the application.

4.2 DEFAULT DEVICE CONFIGURATION

When the DAS is 'opened' by the host application, the DAS default configuration is as follows:

Sampling Rate Divisor: 3 (1024 kHz sampling rate)
Start Mode: Internal
Trigger Mode: Internal
Trigger Threshold: 0
Trigger Polarity : Negative
Timeout for Data Acquisition: Infinite
Internal Threshold Triggering: Disabled
Channel/Gain Sequence RAM Contents: Non-initialized
(User must specify a channel/gain sequence to the driver.)
Pre-Trigger Buffer size: 0

4.3 DRIVER FUNCTION DESCRIPTIONS

The paragraphs below describe each DAS driver call in detail. The calling convention, parameters, and returned status conform to the standard Unix protocol but are listed for completeness.

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4.3.1 OPEN (DEV, FLAG)

The 'OPEN' entry point verifies that the device is physically present in the system; if the device is present the driver attempts to allocate the device to the user and initialize the hardware. If the device is not in the system or another user is currently using the device a [-1] will be returned. Note that the device must first be 'opened' by the user before any subsequent communication can take place.

The 'dev' parameter is a character string which specifies the device file name in the /dev subdirectory of the root. Ask the system manager for the assigned device name or refer to the DAS Unix Driver Installation in Section 3.0 for more detail.

The 'flag' parameter specifies the attributes with which the device should be opened; for the DAS the flag parameter should indicate read/write attributes (the O__RDWR flag defined in the system include files).

If the call to the open routine was successful the driver will return an integer greater than zero which will be used as the 'file id' parameter in subsequent calls to the driver.

4.3.2 CLOSE (FID)

The 'CLOSE' routine deallocates a previously opened DAS device. The 'fid' parameter is the 'file id' returned from a prior open statement.

4.3.3 WRITE (FID, BUFFER, COUNT)

The 'WRITE' procedure will load the scan sequence RAM with a user supplied channel/gain sequence. The user must specify a channel/gain sequence to the driver prior to initiating an acquisition.

The 'fid' parameter is an integer 'file id' obtained by a previous call to the 'OPEN' routine. The 'buffer' parameter is a pointer to an array of structure of type 'SeqRam'.The structure, defined in the included module 'dvx2502io.h', is as follows:

```
struct    SeqRam { short Channel;     /* channel number (0—255) */
          short  Gain;                /* gain (1, 2, 4, 8) */
          short Trigger;              /* trigger control (1 = trigger) */
          }
```


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Each channel to be specified will have one entry in the 'SeqRam' array. The 'Channel' field specifies the channel number to be sampled, the 'Gain' field specifies the gain (1,2,4,8) for that channel, and the 'Trigger' field enables or disables internal threshold triggering on the channel. A one in the 'Trigger' field enables threshold triggering on that specific channel, while a zero disables threshold triggering. Note that only one channel in a sampling sequence may be selected for triggering.

The 'count' parameter indicates to the driver the number of channels specified in the 'SeqRam' array.

The WRITE' function returnS a zero value if successful and a negative value if loading the sequence RAM failed. Causes for failure include:

a.) Specifying threshold triggering on more than one channel.

b.) Exhausting the physical capacity of the sequence RAM.

4.3.4 READ (FID, BUFFER, COUNT)

The 'READ' call starts the acquisition process with previously loaded setup values.

The 'fid' field is the 'file id' returned from a prior call to the 'open' routine.

The 'buffer' field is a pointer to an array which will receive the data from the DAS. NOTE THAT THE USER BUFFER MUST BE AT LEAST 64 BYTES LONG. Failure to assure this condition is met, may lead to fatal system failures.

The 'count' field specifies the total number of bytes to acquire which is two times the number of 16-bit data words desired.

The READ' driver routine will return a zero value if successful or a negative value if an error was encountered. Common causes for an acquisition failure include:

a.) FIFO overflow.

b.) The timeout limit for data acquisition expired before all the data was acquired.

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4.3.5 IOCTL (FID, CMD, DATA, FLAG)

The 'IOCTL' driver routine supports a variety of control and diagnostic functions which are discussed separately below. As with the other driver routines the 'fid' parameter is an integer containing the file identifier for the device. The 'cmd' indicates to the driver the particular IOCTL' function being requested by the user; the include file 'dvx2502io.h' contains the valid subfunction codes for the DAS driver. The 'data' and 'flag' parameters are interpreted differently for each driver subfunction.

4.3.5.1 RESET

The IOCTL RESET command sets the RESET bit in the control/status register and waits 2 seconds for the bit to clear. If the bit is not clear after 2 seconds or if the power-on test bit is 0, an error is returned.

The data parameter is ignored for this function.

4.3.5.2 RATE__DIVISOR

The IOCTL RATE__DIVISOR command loads the DAS rate divisor register with a user specified divisor. The data parameter contains the desired rate. If the specified rate divisor is greater than the allowable 10-bit value, an error is returned in the user structure.

4.3.5.3 CLOCK__SOURCE

The IOCTL CLOCK__SOURCE command sets/clears the external clock select bit in the DAS CSR according to the value passed in the data parameter. A non-zero value sets the bit while a zero value clears the bit. A one in this word specifies an external clock source.

4.3.5.4 START__MODE

The IOCTL START__MODE command sets/clears the external start bit in the DAS CSR according to the value passed in the data parameter. A non-zero value sets the external start bit to a one while a zero value clears the bit. A one in this word selects an external start signal.

4.3.5.5 RUN__AD__DIAGS

The IOCTL RUN__AD__DIAGS command initiates a diagnostic self test of the DAS hardware. If the tests pass, a zero is returned in the 'data' pa-

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rameter, otherwise a non-zero diagnostic error code is returned. Diagnostic error codes are defined in the include file 'dvx2502io.h'.

4.3.5.6 GET__DIAG__ERROR

The IOCTL GET__DIAG__ERROR returns the last diagnostic status code in the data parameter.

4.3.5.7 THRESHOLD

The IOCTL THRESHOLD command loads the DAS threshold register with the trigger threshold value contained in the data parameter. An error is returned if the threshold value is greater than six bits.

4.3.5.8 TRIGGER__POLARITY

The IOCTL TRIGGER__POLARITY command sets/clears the polarity bit in the DAS threshold register. A non-zero value sets the bit while a zero value clears the bit. A one specifies positive edge triggering while a zero specifies negative edge triggering.

4.3.5.9 READ__SRAM

The IOCTL READ__SRAM command returns up to 64 bytes of sequence RAM data to the user and is primarily used for diagnostics. The flag parameter specifies which block of 64 bytes of sequence RAM is returned(0 - 31). The base address of the sequence RAM to be read is calculated as 'flag * 64 .' An error is returned if the specified flag value is greater than 31.

4.3.5.10 TIMEOUT

The IOCTL TIMEOUT command sets the timeout limit for DAS data acquisitions in seconds. The timeout value is passed in the data parameter.

4.3.5.11 GET__ERROR

The IOCTL GET__ERROR command returns a device specific error number which can be interpreted from the error codes supplied in the include file 'dvx2502io.h'. The user should make this call after a negative value is returned from an open, write, read, or ioctl call to obtain the specific cause of the error.

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4.3.5.12 PRE__POST__TRIGGER

The IOCTL PRE__POST__TRIGGER command sets the data collection mode for internal threshold triggering. A zero for the 'data' parameter specifies post trigger data collection only, while a non-zero value specifies both pre- and post-data collection. No error codes are returned.

4.3.5.13 THRESHOLD__TRIG

The IOCTL THRESHOLD__TRIG command enables or disables internal threshold triggering. A zero in the 'data' parameter disables triggering, while a non-zero value enables triggering. No error codes are returned.

4.3.5.14 PRE__TRIG__BUF__SZ

The IOCTL PRE__TRIG__BUF__SZ command sets the PreTrigger buffer size for threshold triggered acquisitions. The size of the buffer expressed in 16-bit words is supplied by the user in the 'data' parameter.

4.3.5.15 SET__SIGNAL__TYPE

The IOCTL SET__SIGNAL__TYPE command allows the user to ground the input to the input buffer, apply a positive or negative voltage reference to the input buffer, or allow the signal at the input connector to pass through the input multiplexer to the input buffer. The 'data' parameter specifies the input type; the include file 'dvx2502io.h' defines values for valid input signal types. An error is returned if the signal type specification is not defined.

4.3.5.16 READ__REG

The IOCTL READ__REG command allows the user to read any DAS register. The 'flag' parameter specifies the register to be read and the 'data' parameter is a pointer to a user variable which receives the data. The include file 'dvx2502io.h' logically defines the valid register assignments. An error is returned if the register to be read is not defined.

4.3.5.17 WRITE__REG

The IOCTL WRITE__REG command allows the user to write data to any DAS register. As with the READ__REG command, the 'flag' parameter

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specifies the register to be read. An error is returned if the register to be written is not defined.

4.4 ERROR HANDLING

Driver error conditions will be flagged by returning a negative number from any of the system calls. The following errors are logically defined in the include file 'dvx2502io.h":

a.) Device not present
b.) Other user owns device
c.) Attempt to write more than 2048 bytes to sequence RAM
d.) Unexpected interrupt
e.) FIFO overflow
f.) Power-on test failure
g.) Invalid channel number
h.) Invalid gain (only one gain per acquisition
i.) Invalid rate divisor
j.) Device timeout
k.) Invalid device model number
l.) Cannot access sequence RAM
m.) Invalid threshold value
n.) Attempt to assign trigger to multiple channels
o.) See dvx2502io.h for the complete list of error codes.

4.5 DATA ACQUISITION EXAMPLES

4.5.1 SIMPLE ACQUISITION

This example shows the ease of setting up a simple acquisition and averaging the data set. The user is prompted to enter the number of channels and the number of samples per channel and to select the type of input signal. This information plus the control parameters are downloaded into the DAS. Acquisition is then started and the acquired data is scaled and the average is computed.

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```
/*
*SIMPLE DATA ACQUISITION PROGRAM USING THE *DVX 2504 A/D
*/
#include <sys/file.h>
#include "dvx2502io.h"              /*DAS I/0 definitions */
#define MAX__SAMPLES 16384
#define SCALE (20./65536.)          /* converter level to voltage scale fact or */

main( )
{
int i,j,k;
int fid;
int sigtype,NCHAN;
extern int errno;
int averr;
int rate;
int thres;
struct SeqRam SeqRam[8];
short dvxdata[MAX __ SAMPLES];
int tsamp,samp;
float avgvolts[8];

        /* NUMBER OF CHANNELS TO SAMPLE */
printf(" \ n \ tEnter Number of Channels: ");
scanf("%d",&NCHAN);
if ( NCHAN > 8 ) {
   printf(" \ nMax. number of channels is 8");
exit(0);
   }
        /* NUMBER OF SAMPLES PER CHANNEL */
printf(" \ n \ tEnter Number of Samples per Channel: ");
scanf("%d",&samp);

tsamp = samp*NCHAN;             /* total number of samples */

if ( tsamp > MAX __ SAMPLES )
{
        printf(" \ nERROR: sample size too big");
        exit(0);
}
```


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```
        /* SPECIFY SIGNAL INPUT TYPE */
printf(" \ n \ t1 = Normal Input");
printf(" \ n \ t2 = Grounded Input");
printf(" \ n \ t3 = Positive Reference");
printf(" \ n \ t4 = Negative Reference");
printf(" \ n \ tEnter Signal Type: ");
scanf("%d",&sigtype);


/*
* SETUP SAMPLING SEQUENCE STRUCTURE FOR THE WRITE TO SRAM
*/

for(i = 0;i < NCHAN;i + + )
{
        SeqRam[i].Channel = i;
        SeqRam[i].Gain = 1;             /*only one gain per acquisition*/
        SeqRam[i].Trigger = 0;
}

/*
*OPEN THE DEVICE
*/
fid = open("/dev/av0", O__RDWR);
if (fid = = -1 ) {
        printf("ERROR %4d, cannot open the device \ n",errno);
        /* get device specific error */
        exit(0);
}
/*
* WRITE THE SRAM SAMPLING SEQUENCE AND GAINS
*/
if ( write(fid,(char *)SeqRam, sizeof(struct SeqRam)* NCHAN) = = - 1 )
{
        ioctl(fid,GET __ ERROR,&averr,0);
        printf("DEVICE ERROR %3d \ n",averr);
        exit(0);
}
```


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```
/*
*SET THE RATE REGISTER
*/
rate = 3;                                   /* divide by 3 */
if (ioctl(fid,RATE __ DIVISOR,&rate,0) = = -1)
{
        ioctl(fid,GET __ ERROR,&averr,0);
        printf("DEVICE ERROR %3d \ n",averr);
        exit(0);
}

/*
* SELECT INPUT SIGNAL TYPE
*/
if (ioctl(fid,SET __ SIGNAL __ TYPE,&sigtype,0) = = - 1)
{
        ioctl(fid,GET __ ERROR,&averr,0);
        printf("DEVICE ERROR %3d \ n",averr);
        exit(0);
}

/*
* GET SOME DATA
*/
if ( read(fid,(char *)dvxdata,tsamp< <1) = = - 1)
{
        ioctl(fid,GET __ ERROR,&averr,0);
        printf("DEVICE ERROR %3d \ n",averr);
        exit(0);
}

        /* CONVERT LEVELS TO VOLTAGE AND AVERAGE */
for (i = 0;i < NCHAN;i + + )
{
        avgvolts[i] = 0.;
        for(j = 0;j < samp;j + + ) avgvolts[i] + = (float)dvxdata[i +j*NCHAN];
        avgvolts[i] /= (float)samp;
        avgvolts[i]* = SCALE;
}

for(i = 0;i < NCHAN;i + + )
        printf(" \ nAverage Voltage Channel %3d = %7.6f ",i,avgvolts[i]);

close(fid);
}
```


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4.5.2 PRE/POST DATA ACQUISITION

In this example, the user is prompted for the number of samples to acquire. Channels #2 and #3, each with a gain of 1, will be scanned continuously and the results stored in the Pre-trigger buffer. Data from channel #2 will be monitored, and when the converted value crosses the threshold of +3/16 of full scale in the positive direction, the DMAC will store all subsequent data points in the Post-trigger buffer. The Pre-trigger data buffer will be half of the total number of samples. The scan sequence will be downloaded along with the sampling rate and the threshold value, and the acquisition will be started. When the voltage on channel #2 increases across the threshold and the Post-trigger buffer is filled, the data will be scaled, the pretrigger data concatenated with the post-trigger data and the values displayed.

```
/* PRE/POST DATA ACQUISITION PROGRAM USING THE
DAS A/D
*/
#include <sys/file.h>
#include "dvx2502io.h"
#define SCALE (20./65536.) /* converter level to voltage scale factor */
#define MAX __ SAMPLES 16384
#define CHAN1 2                    /* define channels to use */
#define CHAN2 3                    /*              ......*/
main( )
{
int i,j,k;
int fid;
extern int errno;
int averr;
int rate;
int thres;
struct SeqRam SeqRam[8];
short dvxdata[MAX __ SAMPLES];
int tsamp,samp;
int offset;
float volts[MAX __ SAMPLES];

/* NUMBER OF SAMPLES PER CHANNEL */
printf(" \ n \ tEnter Number of Samples per Channel: ");
scanf("%d",&samp);


/* total number of samples (we use 2 channels)*/
```


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```
/* SETUP SAMPLING SEQUENCE STRUCTURE FOR THE
* WRITE TO SRAM
*Two channels are used with triggering enabled on the
* 1st channel
*/
SeqRam[0].Channel = CHAN1;
SeqRam[0].Gain = 1;                    /*only one gain per acquisition*/
SeqRam[0].Trigger = 1;                 /* enable trigger */
SeqRam[1].Channel = CHAN2;
SeqRam[1].Gain = 1;
SeqRam[1].Trigger = 0;

/*
* OPEN THE DEVICE
*/
fid = open("/dev/avO", O__RDWR);
if(fid == -1){
        printf("ERROR %4d, cannot open the device \ n",errno);
/* get device specific error */
exit(0);
}
/* WRITE THE SRAM
*/
printf(" \ nSetting up SRAM");
if ( write(fid,(char *)SeqRam, sizeof(struct SeqRam)*2) = = - 1)
{
ioctl(fid,GET__ERROR,&averr,0);
printf("DEVICE ERROR %3d \ n",averr); exit(0);
}
/* SET THE RATE REGISTER
*/
rate = 1000;/* divide by 1000 */
printf(" \ nSetting up rate divisor");
if (ioctl(fid,RATE__DIVISOR,&rate,0) = = - 1)
{
        ioctl(fid,GET__ERROR,&averr,0);
        printf("DEVICE ERROR %3d \ n",averr); exit(0);
}
```


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```
/*
* SELECT TRIGGER POLARITY AS POSITIVE
*/
i=1;
printf(" \ nSetting up trigger polarity");
if (ioctl(fid,TRIGGER __ POLARITY,&i,0) = = - 1)
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVICE ERROR %3d \ n",averr);
exit(0);
}
/*
* ENABLE THRESHOLD TRIGGERING
*/
printf(" \ nEnabling threshold triggering");
if (ioctl(fid,THRESHOLD __ TRIG,&i,0) = = - 1)
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVICE ERROR %3d \ n",averr);
exit(0);
}
/* SET THE TRIGGER THRESHOLD
*/
i = 3d; /* 2's complement of +3/16 F.S. */
printf(" \ nSetting trigger threshold");
if (ioctl(fid,THRESHOLD __ TRIG,&i,0) = = - 1)
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVICE ERROR %3d \ n",averr);
exit(0);
}
/* SET THE PRETRIGGER BUFFER SIZE TO 1/2 THE
*TOTAL NUMBER OF SAMPLES
*/
i = tsamp>>1;
printf(" \ nSetting PreTrigger buffer size");
if (ioctl(fid,PRE __ TRIG __ BUF __ SZ,&i,0) = = - 1)
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVICE ERROR %3d \ n",averr);
exit(0);
}
```


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```
/* GET SOME DATA
*/
printf(" \ nWAITING for TRIGGER");
if ( read(fid,(char *)dvxdata,tsamp< <1) = = - 1 )
{
ioctl(fid,GET __ ERROR,&averr,0);
printf("DEVICE ERROR %3d \ n",averr);
exit(0);
}
/*

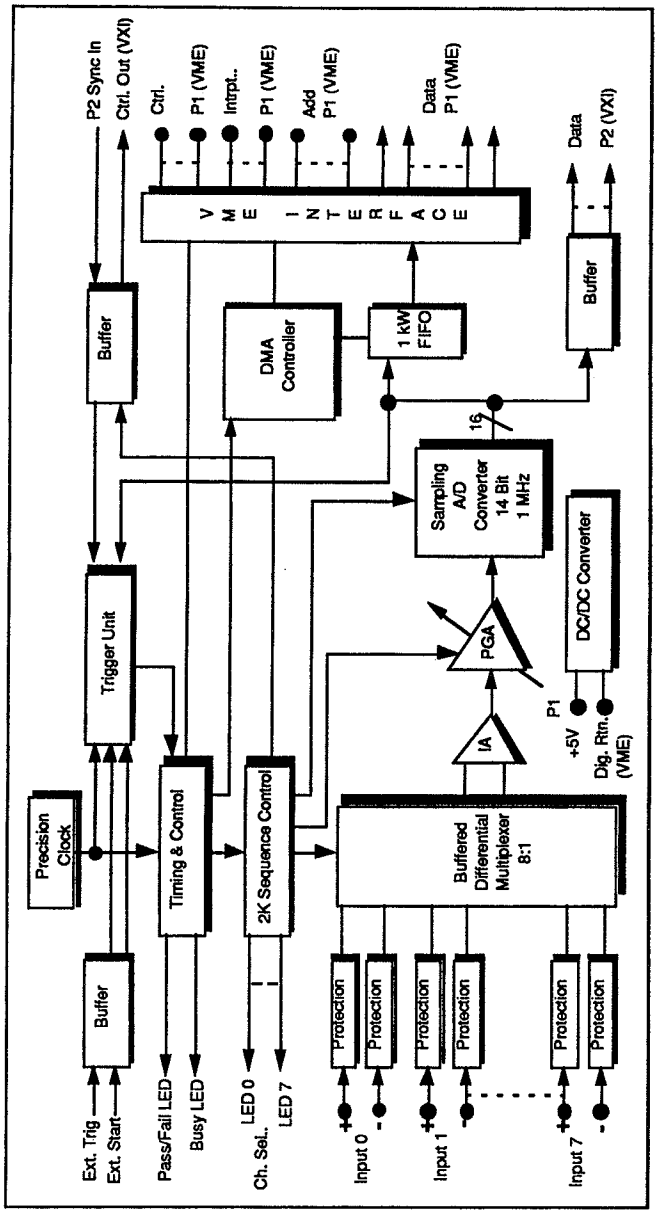
* CONVERT SAMPLES TO VOLTAGE
*/

for(i = 0;i < tsamp;i + + ) volts[i] = (float)dvxdata[i] * SCALE;


/* PRETRIGGER DATA */
for(i=0;i<(tsamp>>1);i+ =2)
printf(" \ n PreTrigger Data Chan[%1d] %4.3f Chan[%1d] %4. 3f",
CHAN1,volts[i],CHAN2,volts[i + 1]);

/* POSTTRIGGER DATA */
for(i = (tsamp> >1);i <tsamp;i + = 2)
printf(" \ n PostTrigger Data Chan[%1d] %4.3f Chan[%1d] %4 .3f",
CHAN1,volts[i + 1],CHAN2,volts[i]);
close(fid);
}
```


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DAS Functional Block Diagram

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5.0 FUNCTIONAL DESCRIPTION

5.1 OVERVIEW

The DVX 2504 occupies a single slot in a standard double height VME chassis or 'C' size VXI chassis. Connectors for 8 differential analog input signals and two digital sampling control signals are available on the front panel. Ten LEDs indicate the 8-bit binary channel code (1 of 256), the Pass/Fail condition of the board and the BUSY condition while acquisition is in progress. On the rear of the card, the P1 connector is fully compatible with the VMEbus specifications and the P2 connector complies with the VXIbus specification.

5.1.1 Analog Front End

Eight differential analog signals can be connected to the card. To minimize the noise pick-up, these signals should be connected with twisted shielded conductor pairs, wired to a 25 pin D type male connector according to the table in Section 2.2.1. The connector should be covered with a metallic backshell.Unused inputs should be connected to ground to prevent them from floating and introducing spurious noise.

The analog inputs are over-voltage protected. Any analog signal exceeding ±12 volts is clamped to an internal supply rail.

The eight differential analog input pairs (Ports) are buffered by high impedance dual-FET op-amps and then differentially multiplexed into a low-noise bipolar input Instrumentation Amplifier (IA). The Common Mode Rejection Ratio of the IA exceeds 75 dB at 60 Hz. The single-ended output of the IA is amplified by a software-controlled Programmable Gain Amplifier (PGA) with gains of 1, 2, 4, or 8.

The programmable gain allows the user to check for maximum signal amplitude. The sequence RAM can be reloaded with a new gain setting so that the signal level of all channels will be optimally amplified to take full advantage of the dynamic range of the A/D converter.

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5.1.2 A/D Converter

A 1024-kHz, 14-bit resolution sampling analog-to-digital converter digitizes the signals amplified by the PGA. The sampling rate of the converter is selectable in 1021 steps from 1024 kHz to 3.000 kHz. The built in sample-and-hold has been optimized for acquisition time, hold mode settling time, noise, and aperture errors up to the maximum sampling rate. Upon completion of the conversion, the digitized results are transferred to a 1024 word FIFO for transfer over the VMEbus, or buffered for transfer to the adjacent card slot via the VXIbus.

5.1.3 Control Sequencer

Before starting an acquisition sequence, the user prepares a gain/channel sequence file which contains:

a) Only one gain selection per acquisition.

b) The port and channel number of each channel to be scanned in the sequence of the scan

c) The trigger flag (if required) marking the channel to be monitored for data dependent triggering.

The user then downloads the file into the Scan Sequence RAM. The Control Sequencer reads the Sequence RAM and synchronizes the DAS card as well as the associated multiplexer cards that can extend the total number of input channels to 256 (32 channels to each of 8 ports).

The sampling trigger and the start acquisition commands can be derived internally or from user supplied signals via the two BNC connectors on the front panel. Internally, the sampling trigger is derived from a precision crystal controlled oscillator (3.072 MHz + 0.001%) and the Start is issued by the user under his program's control. The sampling rate, one of the downloadable parameters, is selected by the user prior to the initiation of the acquisition. Externally, the user can supply both the sampling trigger and the start command by connecting the signals to the BNCs and downloading the necessary selection commands into the Command register.

In the data dependent triggering mode, the Control Sequencer continually scans through the channels. Each time the channel flagged

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for monitoring is sampled, the converted value is compared with the threshold level that was loaded by the user into the Threshold register.

In the Post-trigger mode, when the threshold is crossed in the user defined direction, the triggering event and all subsequent values are stored in the FIFO. Channel #2 of the DMA controller transfers all data to the VMEbus memory. In demultiplexing post-trigger data, the channel data point AFTER the triggering channel is the FIRST data point in the data set (NOT necessarily the first channel in the scan sequence).

In the Pre/Post triggering mode, all conversions are stored in the FIFO from the beginning of the scan. When the threshold is crossed in the user defined direction, the value of the trigger event and all subsequent values are tagged as they are loaded into the FIFO. All pre-trigger data PLUS the trigger event data point, are transferred to the VMEbus memory pre-trigger buffer by channel #1 of the DMA controller and all post-trigger event data are transferred to the post trigger buffer in the VMEbus memory by channel #2. In demultiplexing pre/post triggered data, it is important to note that the pre-trigger data is stored in a circular buffer and that the trigger event aborted the DMA operation on channel #1. The trigger event data point is the LAST point written into the pre-trigger buffer before the operation was aborted. The data point following the trigger event data point is the FIRST point in the post-trigger data buffer. The user must determine from the DMA channel #1, which was the last location in the pre-trigger buffer to be written by reading the registers in the AM9516, and "unroll" the data before concatenating it with the post-trigger data, and then locate the beginning of a scan sequence in the pre-trigger data set.

5.1.4 VME/VXI Interface

In compliance with the both the VMEbus and the VXIbus Specifications, the DAS provides a series of registers and jumper fields to satisfy:

a.) VMEbus slave data transfer
b.) VMEbus master data transfer
c.) VMEbus interrupt operations
d.) VMEbus master bus arbitration
e.) VXIbus software protocol requirements
f.) VXIbus local bus connections
g.) VXIbus TTLTRG bus connections

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This facilitates the transfer of data from the DAS to both VMEbus resident memories and host processors as well as cards in the adjacent card slots. The detailed description of the various registers and jumpers appears below in Section 5.1.

5.1.5 Power-Up Diagnostic Stimuli

The DAS software driver includes diagnostics that are automatically run whenever the system is initialized. In addition, the user can execute them by issuing the RUN_AD_DIAG command. These diagnostics, in addition to testing all of the registers and the scan sequence memory, also select an on-board reference voltage to test the operation of the IA, the PGA, the ADC, the FIFO and the DMA controller. It is also a means of measuring the offset voltage of the entire analog front end (from IA through the ADC). Successful completion of the tests sets the Pass/Fail lamp on the front panel from red to green.

5.1.6 DC/DC Converter

The DAS uses an ultra-low noise DC/DC converter to meet the stringent power demands of the ADC3110 A/D converter. The DC/DC converter draws +5V power from the VME backplane and supplies a filtered +15V, -15V and +5V to the ADC and the analog front end.

5.2 HARDWARE DEVICE REGISTERS

The purpose of this section is to familiarize the user with the operations of the card and to give meaning to some of the driver calls. The user will most likely never need to examine directly the contents of any of the operating registers.

The DAS has 9 control and status registers that can be located on any 64 byte boundary above C000 (hexadecimal) in the VME A24 address space. The Base Address of the card is C000. The 8-bit on-board jumpers, which select the particular 64 byte group of addresses reserved for the DAS, complete the Base address. The registers are accessed as 16-bit words only. See Section 2.1.1 for full range of possible addresses.

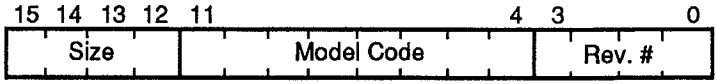
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5.2.1 Device ID Register (Base address + 0000H)

The ID Register is a Read-only register containing Analogic's unique VXI manufacturers code of CFF5 assigned by the VXIbus consortium.

5.2.2 Device Type Register (Base address + 0002H)

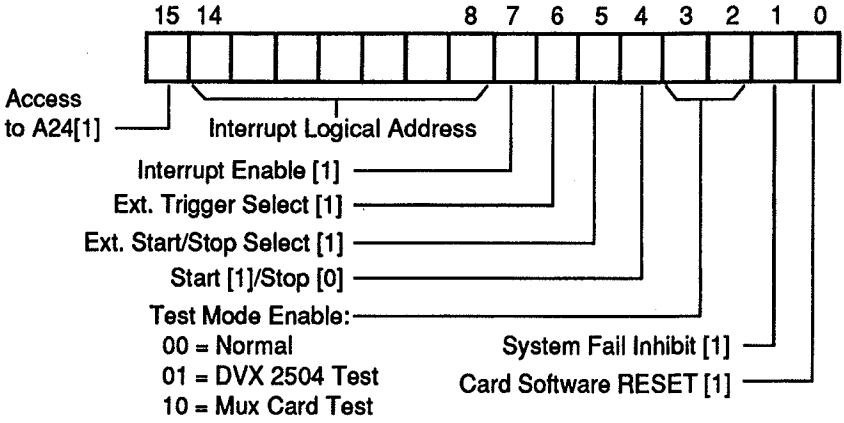
This read-only register contains a memory size code and a model number/revision code. The memory size code complies with the VXI Specification. The content of the Device Type Register for A16/24 devices is defined as follows:



For the DAS, the Size code is hexadecimal 'B', for 4096 bytes of on-board memory that can be accessed in the A24 address space (Note: Only the even numbered bytes contain valid data.) The model code is 16 hex and the revision code is 0. In summary, the content of this register is B160.

5.2.3 Control/Status Register (Base address + 0004H)

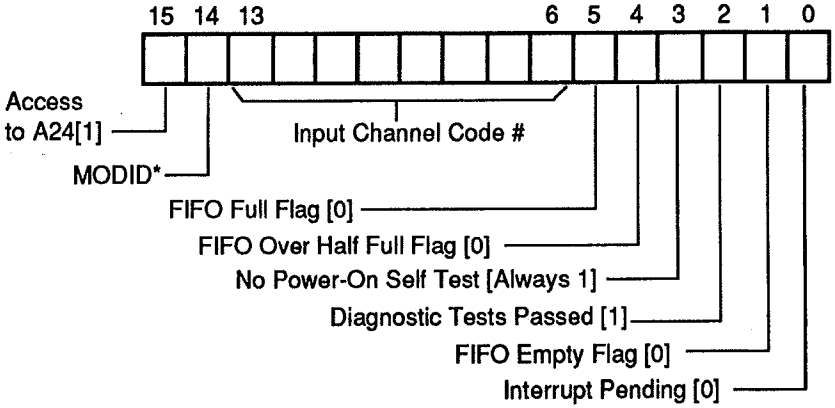
The Control/Status Register (CSR) is a Read/Write register used for controlling the operational modes of the DAS (Write only) and for providing the current board status (Read only). The Control Register (Write-Only) bit assignments are as follows:



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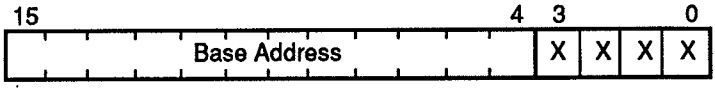
At power-on, all bits in the Control Register are set to Zero and the Pass/Fail lamp is in the Pass condition. When Software RESET is asserted, the control logic on the card and the contents of the FIFO are cleared.

The bit assignments for the Status register (Read only) are as follows:



5.2.4 Sequence RAM Offset Register (Base address + 0006H)

This 16-bit register contains the offset address of the on-board memory that is mapped into an unassigned memory block of the A24 address space of the VME bus. Each offset address points to a single 256 byte block of memory. Since there are 16 such blocks on the DAS card, only the most significant 12 bits of the Offset register are required.



For example, if the Sequence Ram were to be mapped into the A24 space at location 401000H, the Offset register would be loaded with 4010.

The access to the Sequence RAM is controlled by the A24 Enable bit in the Control/Status register (CSR15). When this bit is zero, access is disabled and the SRAM will not respond to VMEbus accesses. After the Offset Register is loaded with the desired offset and A24 Enable is set, the SRAM will respond to the desired address.

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5.2.4.1 Loading the Scan Sequence RAM

The Scan Sequence RAM on the DAS is a 2048 word memory in which ONLY the low byte is implemented. Two words are required for each channel to be scanned.These words contain:

a) The channel code (channel number) of the input on a Multiplexer.

b) The Port number to which the multiplexer is connected.

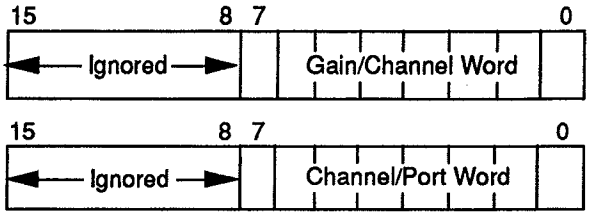
c) The gain setting for the Programmable Gain Amplifier when the channel is sampled.

d) The Trigger ID for when the channel's data is to be monitored for triggering.

e) The Control Code used by the sequencer.

If a multiplexer is NOT connected to a port, then the port is a single channel port. The Channel number is split between the Gain/Channel word and the Channel/Port Word with the most significant two bits of the channel code in the Gain/Channel word with the least significant three in the Channel/Port word. This pair of words is written into the Scan RAM for each port or channel on that port in the desired order of scanning.

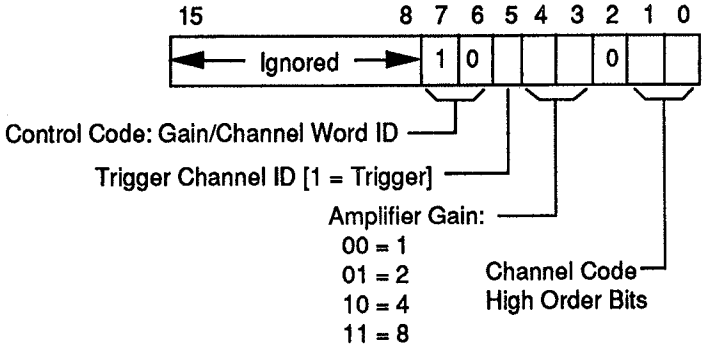
The format of the two words is as follows:



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5.2.4.2 Gain/Channel Word

The Gain/Channel word contains the programmable gain amplifier setting, the high order two bits of the Channel code, the trigger ID bit identifying the channel as the trigger channel for data dependent triggering, and the control bits.



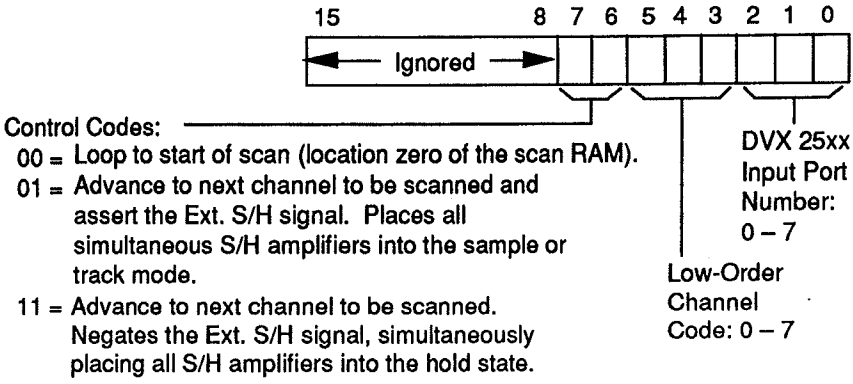
5.2.4.3 Channel/Port Word

The Channel/Port word contains the 3-bit Port address, the 3 least significant bits of the channel code for the channel to be sampled, and the control code bits.

The scan sequence is loaded into the sequence RAM starting at the first location (VMEbus offset address + 0). When the sequencer encounters the loop back code in the Channel/Port word of the last channel in the scan sequence, the address of the SRAM is returned to zero. This last word of the scan table MUST be repeated in the following location of the sequence RAM.

When a Multiplexer card is connected to a Port, it compares the 3-bit port code with the setting of its Port Selection switches and loads the 5-bit channel code into the Channel register when the port code matches the Port Selection code. The code stored in the Channel register selects which analog input signal is connected to the output of the multiplexer card.

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5.2.4.4 A Typical Sequence RAM Load Table

The following example shows the content of the sequence RAM load table for a scan of the DAS ports. There are no multiplexer cards connected to the input ports.

Channel	Port	Gain	Scan Sequence RAM Table (Binary)	
0	0	1	1000 0000	
			1100 0000	
0	3	1	1000 0000	
			1100 0011	
0	7	1	1000 0000	
			1100 0111	
0	0	1	1000 0000	
			1100 0000	
0	2	1	1000 0000	
			1100 0010	
0	5	1	1010 0000	(Trigger Channel)
			1100 0101	
0	6	1	1000 0000	
			0000 0110	(End of Scan - Loop to start.)
			0000 0110	(End of Scan repeated.)

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5.2.4.5 SRAM Format For the DVX Family

When DVX multiplexer cards are connected to one or more of the eight DAS input ports, the method of loading the SRAM in the DAS must be modified to account for the preselection (pipelining or overlapping) of the next channel to be scanned on the multiplexer cards. The Channel register on a multiplexer card must be loaded with the channel code before the sampling process begins. This register (pipeline register) can also be used to provide additional time for the amplifiers and multiplexers to settle before the selected channel's voltage is converted. For aggregate sampling rates below 200 kHz, the single stage of delay caused by the channel register is all that is required for optimum settling time. For aggregate sampling rates between:

a.) 200 to 400 kHz, use 2 stages of delay.
b.) 400 to 600 kHz, use 3 stages of delay.
c.) 600 to 800 kHz, use 4 stages of delay.
d.) 800 to 1024 kHz, use 5 stages of delay.

Before a scan can begin, the channel register on each multiplexer card connected to the DAS must be loaded with the code of the first channel on that multiplexer card to be scanned. This is accomplished by the construction of a Pre-scan table that is loaded into the SRAM, starting an acquisition for a minimum of one complete scan of the pre-scan sequence, and the halting of the acquisition. The FIFO is then cleared, and the SRAM loaded with the complete scan sequence.

5.2.4.6 Order of Scan Restrictions

There are no "order of scan" restrictions on scanning the multiplexer channels when only a single stage of delay is required. However, when two stages are required, the port to which the multiplexer is connected CANNOT be scanned twice in succession. That is, two or more ports must be scanned alternately. This allows an additional sample period of delay for settling. Similarly, when three stages are required, then at least three or more ports must be scanned alternately.

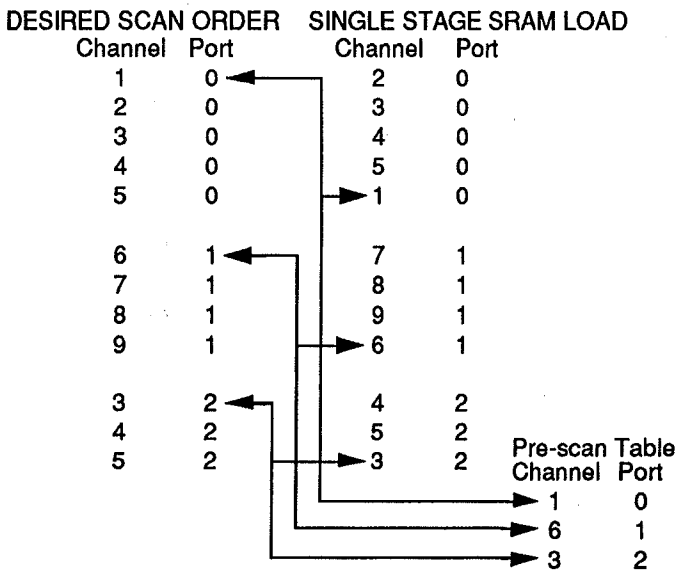
At this point some examples using a DVX 2701 or DBS 8720 multiplexer will help in understanding how ordering the scan increases the amount of time for settling. With the same port/channel pairs, let us configure three scan sequences, one each for 1, 2 & 3 stages of delay.

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5.2.4.7 Example of Single Stage Delay

The desired order of scanning the channels is shown on the left below. It has been broken into three sections with all of the channels on a port in a group for clarity reasons only. The rearranged order of channels which is the format that will be loaded into the Sequence RAM is shown in the center below.

In forming the SRAM load, the order of the ports in the scan MUST be the same as in the DESIRED order.



The code for the first channel to be scanned on each port MUST be loaded into the Channel register on the multiplexer card BEFORE the acquisition of data begins because the first sample of the port will load the channel code of the NEXT channel to be sampled.

Notice that the channel codes for each port in the SRAM load are offset by one step and that the first channel on a port has slipped to the last position for that port. The pre-scan table consists of the channel and port codes for the first occurrence of each port.

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The sequence RAM is loaded with the Pre-scan table and an acquisition sequence is initiated and terminated after a minimum of one pass through the pre-scan table. This preloads the channel code registers on the three multiplexer cards. Data acquired from this scan is discarded.

The channel codes, as reordered above in the Single Delay SRAM Load acquisition table, are then combined with the gain, trigger, and control code bits as shown in Section 5.2.4.4. The resulting composite scan sequence is loaded into the sequence RAM for the acquisition of the data.

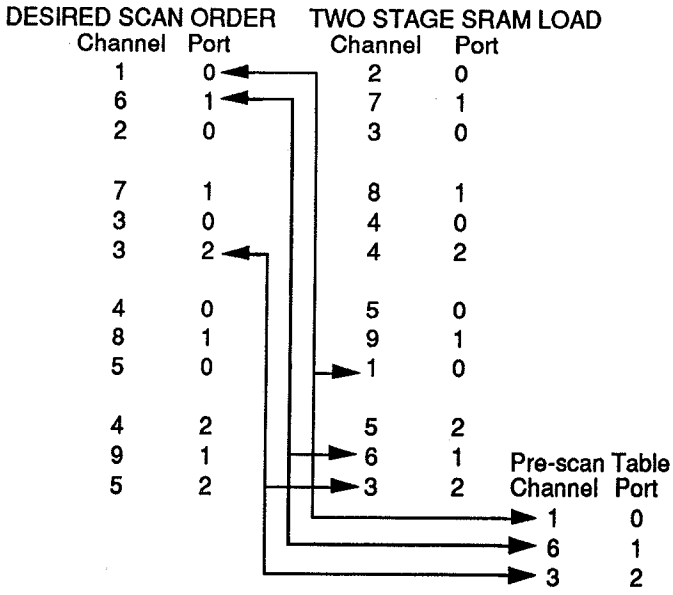
When the acquisition begins, the first channel converted will be Channel 1 on Port 0 (since that code had been pre-loaded), and channel code 2 will be loaded into the channel code register in the multiplexer on Port 0. The process is repeated as channels 2,3, and 4 are converted. When channel 5 is converted, the channel code register is loaded with the channel code 1, leaving the multiplexer set up for reading Channel 1 on Port 0 when the scan sequence is repeated. The same process is repeated for the other two ports.

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5.2.4.8 Example of Two Stage Delay

Now using the same set of channels and ports, let us construct a table with 2 delay stages. Here, note that the total number of channels scanned MUST be an integer multiple of 2, or else a "dummy" channel must be added. Also, the channels per port must be balanced so that in no case will a port be scanned twice in succession.

Notice that the same port code does NOT appear twice in succession but the order of the ports is the same as the desired order and, as before, the first channel on a port has slipped to the last position for that port. The pre-scan table must be loaded with the first channel on each port.

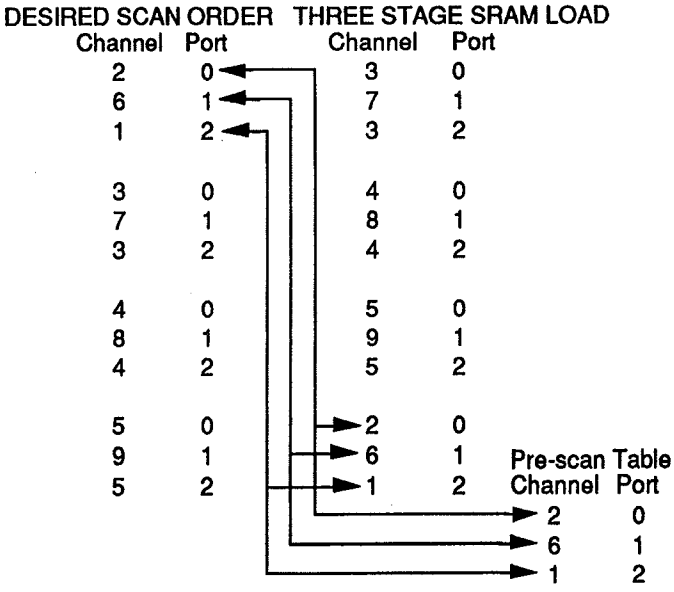


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5.2.4.9 Example of Three Stage Delay

In this case of the 3 stage version of channel/port codes, however, we cannot use the same channel/port order as above because of the requirement to separate each port by at least 2 other port codes. Therefore, channel 1 on Port 0 will be moved to Port 2 (relocating the signal from Multiplexer #0 to Multiplexer #2) as shown below.

Notice that the same port code appears no more frequently than every third sample. As before, the first channel on a port has slipped to the last position for that port. The pre-scan table must be loaded with the first channel on each port.

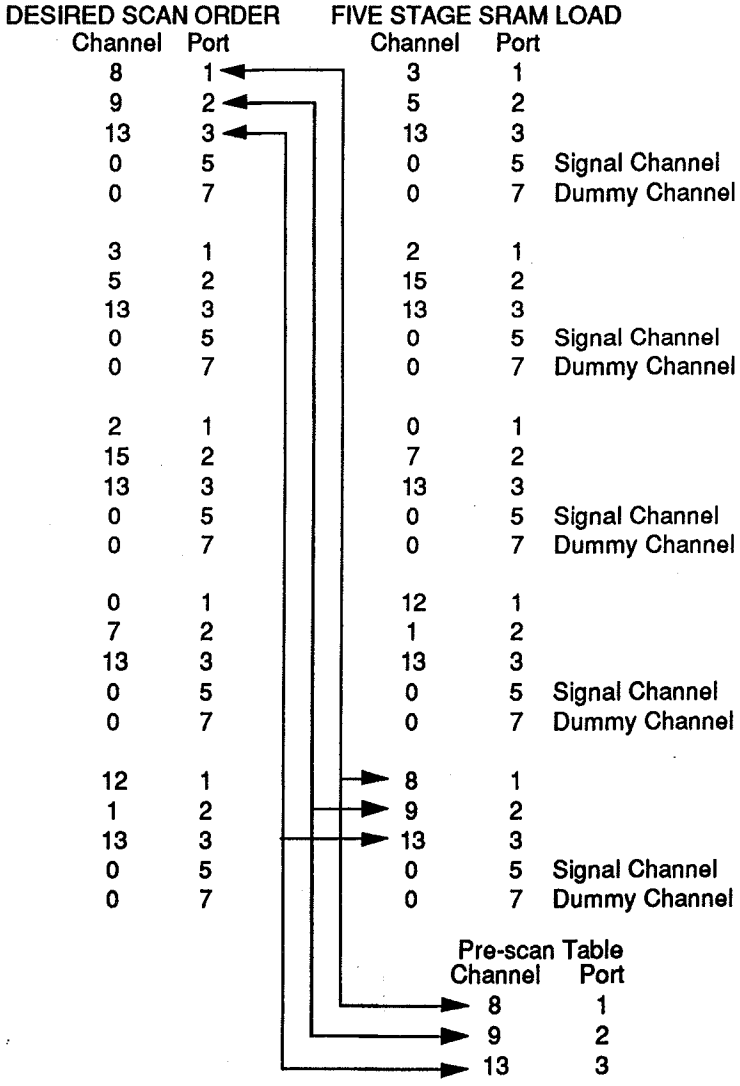


5.2.4.10 Example of Five Stage Delay

The five-stage version requires that each port be separated by at least five other port codes. As shown below, notice that the same port code appears no more frequently than every fifth sample. Just as before, the first channel on a port has slipped to the last position for that port. The pre-scan table must be loaded with the first channel on each port.

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The particular case that is demonstrated makes use of a dummy port, Port 7 and a port carrying a signal, Port 5. Three multiplexers are used, but between five and eight multiplexers could be employed with a five stage delay (at the maximum sample rate of the DVX-2504).



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5.2.4.11 Example of Single Stage Delay With Sample/Hold Multiplexer

When a multiplexer card with simultaneous sample/hold amplifiers is connected to the DAS, the External S/H signal must be driven to place the S/H amplifiers into the 'track' mode to acquire the input signal voltage and then switched into the 'hold' mode for the scan cycle. This is accomplished by setting the control code bits in the Channel/Port word to "01" for asserting the Ext. S/H signal for a period of time and then setting the control code bits to "11" to negate the Ext. S/H signal and start the scan of the channels. The assertion of the Ext. S/H is done at the very beginning of the scan by inserting at the beginning of the SRAM load table the replication of the first entry with the control code for the assertion of the Ext. S/H for as many sample periods as required to reduce the effects of dielectric absorption. See DVX 2601/DBS 8710 User's Manual for details on dielectric absorption.

Then the two words for the first channel to be sampled follow but with the control code bits of the second pair set to 11. This switches the external Sample/Hold circuits to the "hold" mode. The first converted value stored in the FIFO is the conversion for this entry in the scan table.

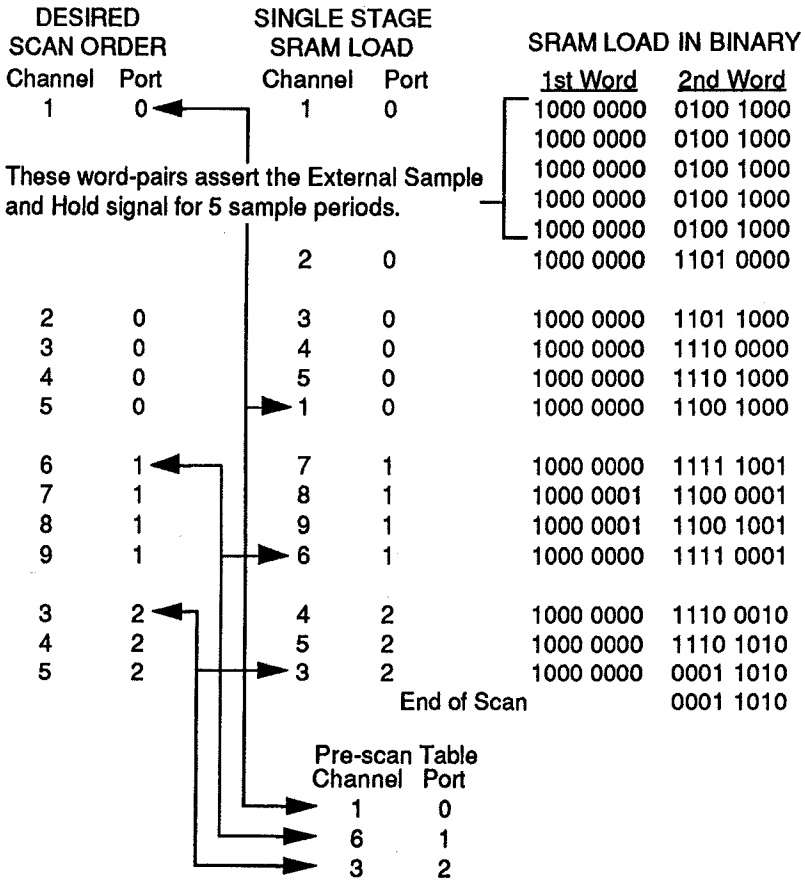
Note that when a Sample/Hold DVX multiplexer card is used, at least one sample cycle per S/H entry per scan loop is lost for the sample period. Therefore loop time = (the number of channels + the number of S/H entries) multiplied by the sample period (Tsamp). In the example below, assuming 5 µs for the sample period,

$$\text{Loop Time} = (12 \text{ channels} + 5 \text{ S/H}) \times \text{Sample Period}$$

$$\text{Loop Time} = 17 \text{ periods} \times 5\ \mu s = 85\ \mu s$$

Sampling Frequency per Channel = 1/Loop time = 1/85 µs = 11.765 kHz

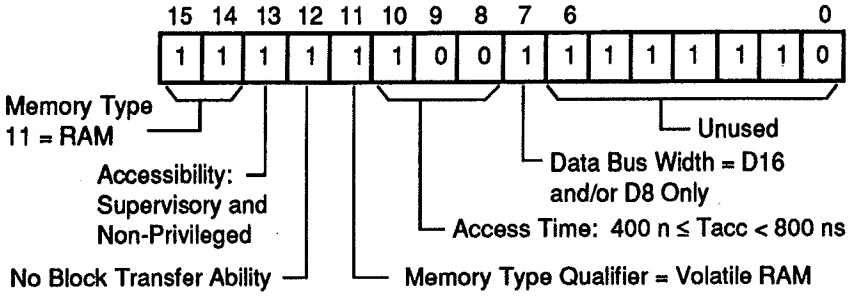
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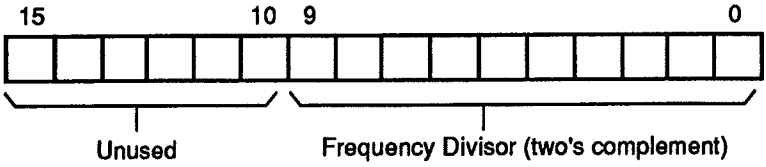
5.2.5 Memory Device Attribute Register (Base address + 0008H)

The attribute register (Read Only) lists the important characteristics of the memory on the card.



5.2.6 Sampling Rate Select Register (Base address + 000AH)

To select one of the possible 1021 sampling rates, the user writes the two's complement of the divisor of the 3.072 MHz precision clock into this Read/Write register.



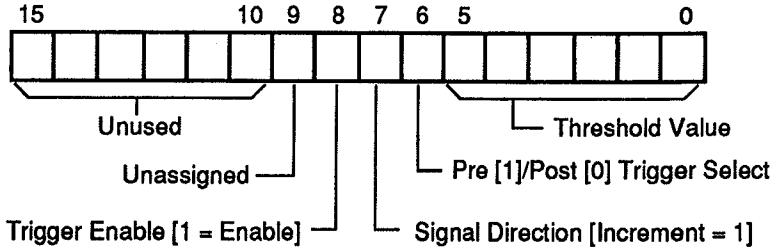
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Typical sampling rates and divisors are as follows:

DIVISOR	SAMPLING FREQUENCY
3	1024.00 kHz
4	768.00 kHz
5	614.40 kHz
6	512.00 kHz
7	438.86 kHz
8	384.00 kHz
12	256.00 kHz
15	204.80 kHz

5.2.7 Threshold Register (Base address + 0010H)

For data dependent triggering of the data acquisition, this register is loaded with the threshold value, the direction of the crossing of the threshold, and whether the mode of acquisition is to be Post triggering or Pre/Post triggering. The bit assignment for the register is:



When data dependent triggering is enabled, the threshold value is compared to the most significant 6 bits of the digitized value of the trigger channel every time that channel is selected. The user is cautioned that the "threshold value" is a BINARY VALUE, whereas the digital output of the ADC to which it will be compared is Offset Binary (regardless of the output data format that has been jumpered).

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In Post [0] triggering mode, the A/D is continuously digitizing while stepping through every channel listed in the sequence, but none of the data is stored in the FIFO. When the digitized value of the triggering channel crosses the threshold in the desired direction, all SUBSEQUENT digitized values are loaded into the FIFO. Channel #2 of the DMA controller is used to transfer the data from the FIFO to system memory.

In the Pre/Post [1] triggering mode, all digitized values are written into the FIFO. When the digitized value of the triggering channel crosses the threshold in the desired direction, the triggering value and all SUBSEQUENT digitized values are tagged as they are loaded into the FIFO. Channel #1 of the DMA controller is used to transfer all untagged (pretrigger) data and the first word (trigger word) of the tagged data into one area of system memory. Channel #2 is used to transfer all of the remaining tagged (post trigger) data into another area of system memory. In this manner, any amount of data before AND after the triggering event can be captured.

5.2.8 FIFO Register (Base address + 0012H)

This Read-Only register allows the direct access to the contents of the FIFO by the host processor without the use of the DMA controller.

5.2.9 AM9516 DMA Controller (DMAC) Pointer Register (Base address + 000CH)

The address of the DMAC's internal register to be accessed must be loaded into the Pointer register. The Pointer register is a Read/Write register. The DAS uses the following registers in the AM9516.

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AM9516 Registers

Register	No.	Access Type*	Address(Hex) Ch. 1/Ch 2
Master Mode Register	1	R/W	38
Chain Control Register	1	C	
Command Register	1	W	2E/2C
Current Address Register A Upper Address & Tag	2	CRW	1A/18
Lower Address	2	CRW	0A/08
Base Address Register A Upper Address & Tag	2	CRW	1E/1C
Lower Address	2	CRW	0E/0C
Base Address Register B Upper Address & Tag	2	CRW	16/14
Lower Address	2	CRW	06/46
Current Operation Count	2	CRW	32/30
Base Operation Count	2	CRW	36/34
Status Register	2	R	2E/2C
Interrupt Save Register	2	R	2A28
Interrupt Vector Register	2	CRW	5A/58
Channel Mode Register (Low)	2	CRW	52/50
Chain Address Register Upper Address and Tag.	2	CRW	26/24
Lower Address	2	CRW	22/20

* C = Chain Loadable
R = Readable by the host CPU
W = Writable by the host CPU

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5.2.10 AM9516 DMA Controller (DMAC) Data Register (Base address + 000EH)

Read or write operations to the DMAC Data Register access the AM9516 register that is pointed to by the code in the DMAC Pointer Register.

5.3 DMA OPERATIONS

The following is a brief discussion of the AM9516A Universal DMA Controller. Details of the operation of the chip may be found in one of the following publications.

a) Advanced Micro Devices Am9516/AmZ8016
Direct Memory Access Controller Manual, 1984
Document #CD-MU-10M-10/84, Order #04910A

b) Advanced Micro Devices MOS Microprocessors and Peripherals 1987-1988 Data Book, 1987, pg 2-66 to 2-118; order #09067A

The AM9516 DMAC has two independent DMA channels for transferring data and instructions. Each channel has its own set of registers as shown in the table above. On the DAS, the AM9516 operates in the "flyby" word mode, writing data from the FIFO into the host memory. It operates in the "chaining" mode to load/initialize its registers and to automatically reload/reinitialize at the end of an acquisition cycle.

The DAS uses the on-board dual channel DMAC in three different ways:

a.) Normal data acquisition

b.) Post trigger acquisition

c.) Pre/Post trigger acquisition

5.3.1 Normal Mode

In the normal mode, DMAC channel #2 is loaded via chaining prior to the start of the A/D. When the FIFO is more than half full, the DMAC #2 acquires the VME bus and transfers data until the FIFO is emptied. It then becomes idle until the FIFO again fills past half full.

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5.3.2 Post-Trigger Mode

In the Post trigger mode, the DMAC channel #2 is loaded as above, but the storing of data into the FIFO after the A/D is started is suspended until the threshold is crossed. The DMAC channel #2 transfers the data as before.

5.3.3 Pre-/Post-Trigger Mode

In the Pre/Post trigger mode, the DMAC channel #1 as well as DMAC channel #2 are used. When the A/D is started, all data acquired are written into the FIFO. DMAC channel #1 will transfer the data into one memory (circular) buffer area. When the threshold is crossed, all the data written into the FIFO are tagged. When the first tagged datum point is read out of the FIFO, it is written to the one memory (circular) buffer area, the DMAC channel #1 operation is terminated and DMAC channel #2 operation is started with the remaining tagged data being written into a second memory buffer area. This allows the continuous capture of an arbitrary amount of data before and after the triggering event.

5.3.4 DMA Address Modifiers

When the DAS becomes bus master, it accesses the A24 (standard) address space differently for the chaining operations and data transfer operations. For chaining commands, the DAS executes a Standard Supervisory Data access by generating the address modifier "3D". For data transfers, however, the DAS executes a Non-privileged Data Access by generating the address modifier "39".

Most VMEbus compatible memories respond to:

a.) Supervisory Program Access Addr. Mod = 3E

b.) Supervisory Data Access Addr. Mod = 3D

c.) Non-privileged Program Access Addr. Mod = 3A

d.) Non-privileged Data Access Addr. Mod = 39

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5.4 INTERRUPT OPERATIONS

The DAS can generate an interrupt to the host CPU on the VME bus for several different conditions. The least significant 7 bits of the interrupt vector to be generated when the DAS acknowledge interrupt servicing are defined by a field within the DAS CSR; the most significant bit of the vector is not programmable and will always be a 1.

The interrupt enable bit in the CSR enables the DAS to interrupt when the FIFO becomes half-full and again when it becomes full. A half-full interrupt is dismissed upon acknowledgement from the host CPU; a full interrupt will not be dismissed until the FIFO goes non-full or the DAS is reset.

Interrupts can also be generated when a DMA operation has been completed or when a trigger condition has been met. The DMA interrupts are enabled by the appropriate register fields in the AM9516 internal register set. The DMA interrupt is dismissed when the CPU writes a Clear Interrupt command to the AM9516.

All interrupts generate the same interrupt vector. Normally, the user will enable only the FIFO interrupts OR the DMA interrupts. It is up to the user to keep a flag on which interrupt is enabled, and to read either the DAS Status Register or the AM9516 Status Register to determine the source of the interrupt.

5.5 AM9516A PROGRAMMING OVERVIEW

The following is an explanation of the programming of the AM9516 DMAC chip as it is used in the DAS. Therefore, only the registers that are meaningful in the DMA operations of the DAS are discussed.

5.5.1 Registers

5.5.1.1 Chip-Level Registers

The Master Mode, Command and Chain Control Registers are used to configure the AM9516A functions and control the chip's operation.

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5.5.1.2 Channels-Level Registers

Each DMA channel has 13 local registers that control its operation but only the following registers are of concern in the DAS:

- Channel Mode Register
- Current Address Register A
- Base Address Register A
- Current Address Register B
- Base Address Register B
- Current Operation Count
- Base Operation Count
- Status Register
- Interrupt Save Register
- Chain Address Register

5.5.2 Commands

The host CPU can write any of 19 commands into the DMA device's Command Register. These commands initiate specific types of DMA operations, including chaining, mask setting and clearing, and the setting of specific bits to indicate transfer direction.

5.5.3 Chaining

Chaining allows a channel to load its own control parameters from a Chain Control Table in memory, thereby minimizing the need for CPU intervention.

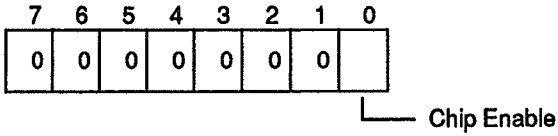
5.5.4 Register Description

The table in Section 5.1.9 lists the registers used, their accessibility, and their addresses. Below is a detailed description of the bit assignments and usage.

5.5.4.1 Master Mode Register

This 8-bit register, which controls the chip level interface, can be read or written at any time except during chaining. System RESET clears it to all zeroes.

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When Chip Enable is a 1, the DMAC gains access to the system bus to begin DMA operations. The other bits are assigned as shown for proper operation of the DAS.

5.5.4.2 Command Register

This register contains the command that the host CPU issues to the DMAC. The following is a table of commands used in the DAS.

Command	OP Code
Reset	0000 0000
Start Ch. #1	1010 0000
Start Ch. #2	1010 0001
Set Software Request Ch. #1	0100 0010
Set Software Request Ch. #2	0100 0011
Clear Software Request Ch. #1	0100 0000
Clear Software Request Ch. #2	0100 0001
Set CIE/IP Ch. #1	001R 0P10
Set CIE/IP Ch. #2	001R 0P11
Clear CIE/IP Ch. #1	001R 0P00
Clear CIE/IP Ch. #2	001R 0P01
Set Flip Bit Ch. #1	0110 0010
Set Flip Bit Ch. #2	0110 0011
Clear Flip Bit Ch. #1	0110 0000
Clear Flip Bit Ch. #2	0110 0001

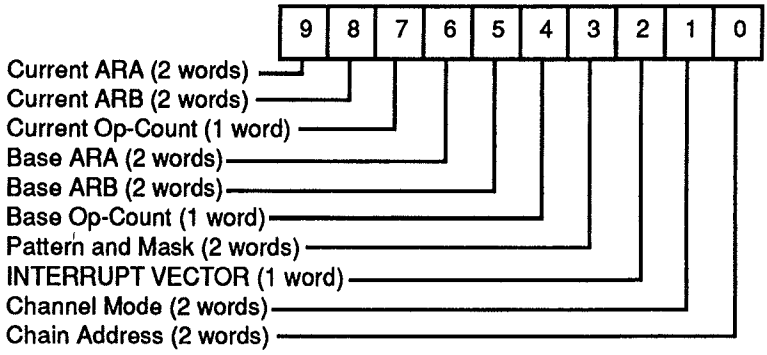
NOTE

R = 1 to perform set/clear on Chain Interrupt Enable (CIE)
R = 0 for no effect on Chain Interrupt Enable (CIE)
P = 1 to perform set/clear on Interrupt Pending (IP)
P = 0 for no effect on Interrupt Pending (IP)

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5.5.4.3 Chain Control Register

When a channel begins a chaining operation, this register is loaded with the Reload word from the memory location indicated by the address in the channel's Chain Address register. The bits in this register identify all of the registers that must be loaded from the table in memory that follows the Reload word.



5.5.4.4 Channel Mode Register

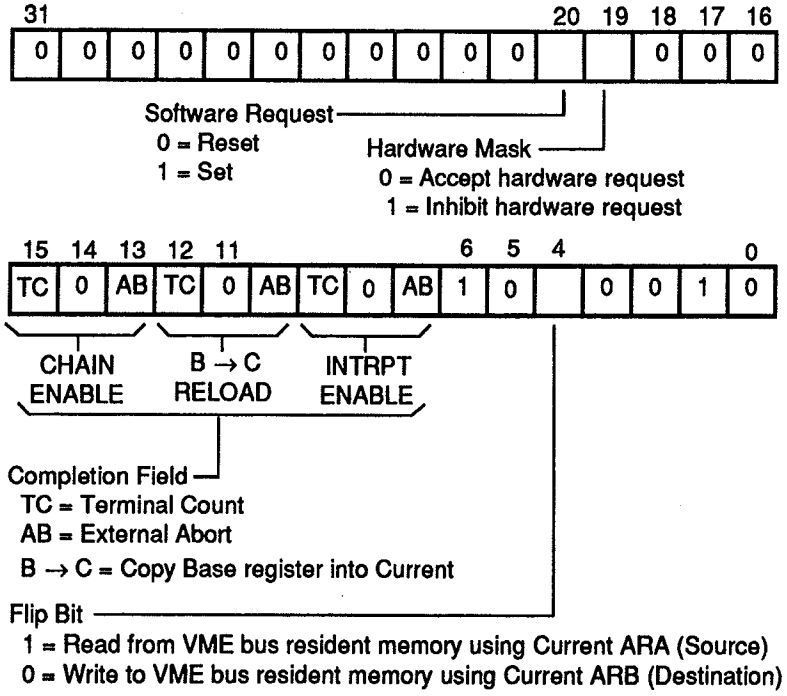
This 32-bit register for each channel selects:

a) The type of DMA operation to be performed.
b) The manner of execution.
c) What action to be taken upon the completion or the abnormal termination of the operation.

The Software Request bit is set when DMA operations are initiated to chain in the commands, address, etc. for data transfers and to chain in subsequent commands, addresses, etc. after the first data operation is complete. Although it can be loaded by writing to the Command Register, it is best done via chaining.

The Hardware Mask bit is to be set ONLY by chaining. Although it can be loaded by writing to the Command Register, it is best done via chaining.

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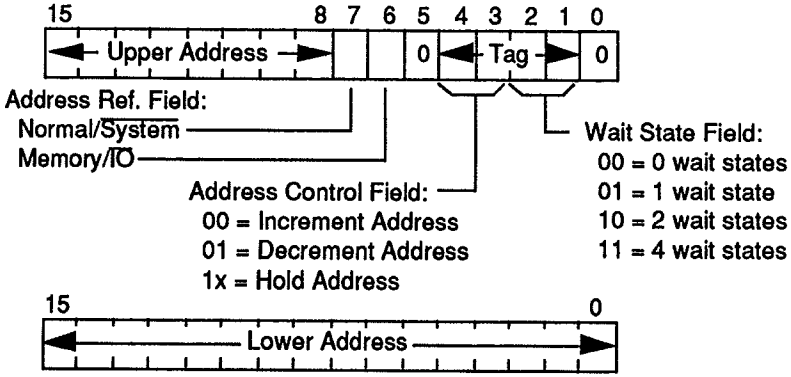
The Completion Field specifies the enabling of the three named actions based upon the manner of termination of the current operation. For example, if the Chain Enable TC bit is set, when the current operation count reaches terminal count, the channel will switch to the chain mode and chain in the new Reload word. If the AB (abort) bit in the INTERRUPT field is set, when the operation is aborted due to abnormal conditions, the channel will generate an interrupt to the host processor. A bit set in the B→C RELOAD field causes the Base Address and Base Operations Count registers to be copied into the current Address and Current Operation Count registers when the terminal condition occurs. This allows the continued writing to a single (or circular) buffer.

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5.5.4.5 Current Address Registers, A & B

For the purposes of this discussion, these registers contain the address of VMEbus resident memory accessed by the data DMA operations. These registers can be loaded with the contents of the Base Address Registers A & B for the auto-loading of repetitive operations without the overhead of chaining in the address.

These registers consist of two 16-bit words, an Upper Address/Tag field and the Lower Address field as shown below. The Upper Address is the most significant byte of the 24-bit memory address and the Lower Address is the remaining portion of the 24-bit address.



5.5.4.6 Base Address Registers, A & B

The Base Address Registers A & B are identical to the Current Address Registers A & B with regard to the content. Operationally, however, they are storage registers whose contents can be read, written, or copied into the Current Address Registers A & B.

5.5.4.7 Current Operation Count Register

This 16-bit register contains the number of words transferred during a DMA operation. With each transfer, the contents are incremented or decremented as specified in the Tag field of the Current Address Register. When the contents have been decremented to 0000, the TC bit in the Status Register is set to 1 indicating a successful completion of the operation. The maximum number of words, 65535, can be transferred by loading the Current Count register with FFFF.

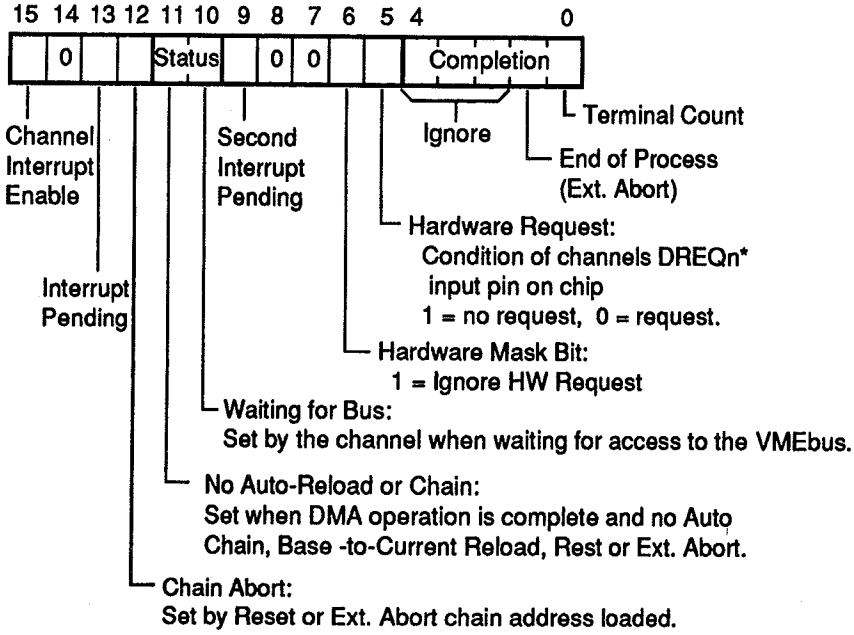
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5.5.4.8 Base Operation Count

This 16-bit register is a holding register which can be read, written, or copied into the Current Operation Count Register.

5.5.4.9 Status Register

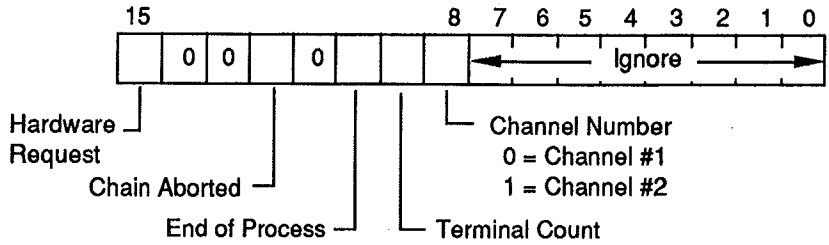
This 16-bit register contains the following fields of information:



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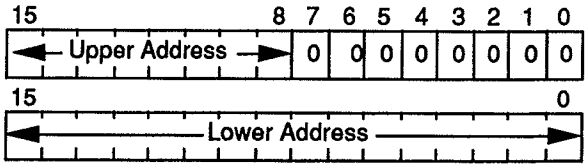
5.5.4.10 Interrupt Save Register

The DMA controller has a two-deep interrupt queue. When two interrupts are queued in the channel, the Second Interrupt Pending (SIP) bit in the status register is set. Once set, all further activity on the channel is prohibited until the Interrupt Acknowledge clears it. This ensures that the DMA never gets more than two operations ahead of the host processor. The content of the Interrupt Save register is shown below.



5.5.4.11 Chain Address Register

The contents of the Chain Address Register point to the Chain Control Table in the VMEbus resident memory where the data to be loaded into the channel's other registers during chaining are located. The contents are shown below.



5.5.4.12 Chain Control Register

The first step in a chaining operation is reading the Reload word from the VMEbus memory location pointed to by the Chain Address Register and storing it in the Chain Control Register. The channel then retains control of the VMEbus until all of the registers defined in the Reload word have been reloaded.

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5.5.5 Simple Example of DMA Operations

The following example written in "C" demonstrates the set-up for the Pre-Post triggering operation of the DMA controller.

```
/*
 *    A simple example for setting up DMA operations
 *    for Pre/Post-triggering acquisition.
 */

#define DMAPointerReg = 0x000c
#define DMACommandReg = 0x000e
#define CSR = 0x0004
#define THRSH = 0x0010
#define OFFSET = 0x0006
#define DevAdr = 0xffc040
#define WordCount = 0x0fff

int DataTablAdrL, DataTablAdrH;
long DataTableAddr, ChainAddr1, ChainAddr2;
int WordCount, IntrVect;
int ChanModeH, ChanModeL;

/*
*   RESET THE 9516A CONTROLLER
*/
{
        /*set the software reset bit */
    WriteReg(DevAdr + CSR,0x0003)
        /* clear the software reset bit and enable the SRAM.*/
    WriteReg(DevAdr + CSR,0x8002)
        /* Load the SRAM A24 Offset Register */
    WriteReg(DevAdr + OFFSET,0x4000)

/*
*   LOAD THE MASTER MODE REGISTER
*/
        /*Load the address of the Master Mode*/
    WriteReg(DevAdr + DMAPointerReg,0x0038)
        /* Load the Mode Command */
    WriteReg(DevAdr + DMACommandReg,0x000d)
```


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```
/*
 *   SET UP THE CHAIN TABLE FOR CHANNEL 2 IN MEMORY

 */
            /* write the Reload word at the top of
               the Chain Table. The Reload word
               calls for loading the following
               registers:
               Current Address Reg. B (2 words)
               Current Operation Count (1 word)
               Channel Mode (2 words) */

     WriteMem (ChainAddr2,0x182)
     DataTablAdrH = (((DataTableAddr + WordCount) > > 8)
                    &&0xff00||0x000000c0)
     DataTablAdrL = (DataTableAddr + WordCount)
                    &&0x0000ffff

  /*
   * write post trigger starting address into chain table
   */
     WriteMem(ChainAddr2 + 1,DataTablAdrH)
     WriteMem(ChainAddr2 + 2,DataTablAdrL)

  /*
   * write word count
   */

     WriteMem(ChainAddr2 + 3,WordCount)
  /*
   * write channel mode words
   */
     ChanModeH = 0x0004;       /* interrupt on Terminal Count after
                                  reading the chaining table */
     ChanModeL = 0x0252;
     WriteMem(ChainAddr2 + 4,ChanModeH)
     WriteMem(ChainAddr2 + 5,ChanModeL)
```


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```
/*
 *
 * SET UP THE CHAIN TABLE FOR CHANNEL 1 IN MEMORY
 */
          /* write the Reload word at the top of
             the Chain Table. The Reload word
             calls for loading the following
             registers:
             Current Address Reg. B (2 words)
             Current Operation Count (1 word)
             Base Address Reg. B (2 words)
             Base Operation Count (1 word)
             Channel Mode (2 words) */

    WriteMem(ChainAddr1 ,0x1d2)
    DataTablAdrH = ((DataTableAddr > > 8)
            &&0xff00||0x00c0)
    DataTablAdrL = DataTableAddr&&0x0000ffff

 /*
  * write pre-trigger starting address into chain table
  */
    WriteMem(ChainAddr1 + 1,DataTablAdrH)
    WriteMem(ChainAddr1 + 2,DataTablAdrL)

 /*
  * write word count
  */

    WriteMem(ChainAddr1 + 3,WordCount)

 /*
  * write the base address into chain table
  */
    WriteMem(ChainAddr1 + 4,DataTablAdrH)
    WriteMem(ChainAddr1 + 5,DataTablAdrL)

 /*
  * write base word count
  */

    WriteMem(ChainAddr1 + 6,WordCount)
```


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```
/*
* write channel mode words
*/
       ChanModeH = 0x0004;
  /* interrupt on terminal count after reading the chaining table */

       ChanModeL = 0x9052
      WriteMem(ChainAddr1 + 7,ChanModeH)
       WriteMem(ChainAddr1 + 8,ChanModeL)

/*
 * SETUP THE THRESHOLD
 */

  /* set the trigger enable, positive transition */
      WriteReg(DevAdr + THRSH,0x01e0)

/*
 START THE 9516 CHAIN LOAD ON CHANNEL 1
 */

  /* Load the address of the Channel #1 Command Register*/
      WriteReg(DevAdr+ DMAPointerReg,0x002e)
  /* Start Ch. #1 Chaining */
      WriteReg(DevAdr + DMACommandReg,0x00a0)

/*
 * START THE 9516 CHAIN LOAD ON CHANNEL
 */
  /* Load the address of the Channel #2 Command Register*/
      WriteReg(DevAdr+ DMAPointerReg,0x002c)
  /* Start Ch. #2 Chaining */
      WriteReg(DevAdr+ DMACommandReg,0x00a1)

/*
 * START ACQUISITION
 */

  /*Start the ADC sampling */

      WriteReg(DevAdr + CSR,0x8012)
}
```


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5.5.6 Driver Excerpt for DMA Operations

The following is an excerpt from the DAS driver that performs the setup of the DMA controller.

```
/*
 *#define DEBUG
 */

#include <dvx.h>
#include <sys/types.h>
#include < sys/errno.h >
#include <sys/param.h>
#include < sys/buf.h >
#include <sys/ulser.h>
#include < sys/uio.h >
#include < machine/psl.h >
#include <sundev/mbvar.h>
#include < sundev/dvx2502io.h >
#include <sundev/dvx2502.h>

/* maximum DMA block size for this device*/
#define                         AV__MAX__BLK__SIZE   0x10000
#define                         CLOCK__TICK    15

/*
* allocate buffers
*/
struct buf dvxbuf[NDVX];

/*
* system structure definitions
*/

struct AV25deviceAV25device[NDVX];
int dvxattach( ),dvxintr( ),dvxprobe( );
struct mb__device*dvxinfo[NDVX];
struct mb__driver dvxdriver = {
        dvxprobe,0,dvxattach,0,0,dvxintr,
        sizeof(struct AV__regs),"dvx",dvxinfo,0,0,0};

/*---The following program performs the setup of the AM9516A for straight DMA,
Pre- and Post-trigger data acquisition.---*/
```


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```
/*
* dvxstrategy:
*
* DMA strategy routine
*
*/

dvxstrategy(bp)
register struct buf*bp;
{
register struct mb__device*md;
register struct AV25device*av;
register struct AV__regs*regs;
register struct ChainBlk*cbp;
register struct ChainBlk*cb; }
int unit;
int s,i,j,k;
short *addr,*addrl;
long CHANNEL__MODE;

#ifdef DEBUG
short *caddr;
printF("/nDVXstrategy:");
#endif

        /*get unit number from buf structure */
unit = minor(bp→b__dev);
md = dvxinfo[unit];av
= &AV25device[unit];

        /*register base address*/
regs = (struct AV__regs*)md→md__addr:

        /*chain reload block*/
        /*Post-trigger*/
cb = (struct ChainBlk *)&AV25device[unit].ChainBlk[0];
        /*Pre-trigger*/
cbp = (struct ChainBlk *)&AV25device[unit].ChainBlk[l];

        /*raise priority level*/
s = splx(pritospl(md→md__intpri));
```


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```
/*
* sleep while resources in use
*/
while(av→busy)
        sleep((caddr__t)av,AVPRI);

/*
* ready to start DMA
*/
        av→busy = 1;
        av→bp = bp;
/*
* clear out the FIFO with a reset
*/
        i = regs→offset;                        /* save offset reg. */
        j = regs→ratediv;                       /* save rate reg */
        k = regs→thresh;                        /* save threshold reg. */
        regs→csr = AV__RESET;                   /* apply the RESET */
        regs→cst = av control__reg;
        regs→offset = i;                        /* restore the offset reg. */
        regs→ratediv = j;
        regs→thresh = k;

                                        /* grab bus resources */
        av→mbinfo = mbsetup(md→md-hd,bp,0);

        addrl = addr = (short *)MBI__ADDR(av→mbinfo);

#ifdef DEBUG
caddr = (short *)(int)addr + 0xff00000);
print("/nDVXstrategy: Unit = %x, DMA Virt. Addr = %x",unit,addr);
#endif

        /* check pre trigger buffer size */
        if (regs→thresh & AV__TRIG__SEL)
        if ( ((bp→b__bcount>>1)< = av PreTrigBufSz)
        ||(av→PreTrigBufSz==0))
{
```


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```
        av→error = EINVALIDPREBUFSZ;
        dvxbuf[unit].b__flags  = B__ERROR;
        mbrelse(md→md__hd,&av mbinfo);
        av→busy = O;
        (void) splx(s);
        iodone(&dvxbuf[unit]);
        return;
}
        /*check for 24 bit address */
if( (int)addr & 0xff000000 )
{
/*ERROR if physical address is > than 24 bits */
        av→error = EINVALIDDMAADDRESS;
        dvxbuf[unit].b__flags |= B__ERROR;
        mbrelse(md→md__hd, &av→mbinfo);
        av→busy = 0;
        (void) splx(s);
        iodone(&dvxbuf[unit]);
        return;
}

/*
*set up chain reload block in device structure for pre trigger chan.
*/
        if(regs→thresh & AV__TRIG__SEL)
        {

#ifdef DEBUG
print("/nDVXstrategy: Setting up Pre-Trigger DMA channel");
#endif
                                        /* chain reload word */
        cpb→LoadCtl = CHAIN__RELOAD;

                                        /* DMA word count */
        cpb→BCount = cpb→Count = av→PreTrigBufSz;

                                        /* current and base addresses */
        cpb→AddrL = cbp→BAddrL=(short)((int)addr & 0xffff);
        cbp→AddrH = cbp→BAddrH=(short)(((int)addr>> 8)&0xff00)
        | ADDRESS__REF|(WAIT__STATES<<1);
```


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```
        /* channel mode register */
cbp→ModeH = (short)( (CHANNEL__MODE>>16)&0xffff);
cbp→ModeL = (short)( CHANNEL__MODE & 0xffff );
cbp→ModeL | = BC__TC; /* base to current reload on term. cnt

                                        /*load 9516 chain address register */
        regs→am9516ptr = AM__CAR__LOW+2;
        i = (int)addr + sizeof(struct ChainBlk);
        regs→am9516dat = (short)(i & 0xffff );

        regs→am9516ptr = AM__CAR__UP+2;
        regs→am9516dat =
        (short)((((int)i>>8)&0xff00)|(WAIT__STATES<<1));

        addr = (short *)((unsigned int)addr+av→PreTrigBufSz<<1);
        }
/*
*set up chain reload block in device structure for post channel
*/
                                        /* chain reload word */
        cb→LoadCtl = CHAIN__RELOAD;

                                        /* DMA word count */
        cb→BCount = cb→Count = (bp b__bcount>>1);

                                        /* current and base addresses */
        cb→AddrL = cb→BAddrL = (short)((int)addr & 0xffff);
        cb→AddrH = cb→BAddrH = (short)(((int)addr>>8)&0xff00)
                                        |ADDRESS__REF|(WAIT__STATES<<1);

                                        /* channel mode register */
        cb→ModeH = (short)( (CHANNEL__MODE>>16) & 0xffff);
        cb→ModeL = (short)(CHANNEL__MODE & 0xffff);
        cb→ModeL | = INT__TC;/* interrupt on terminal count */

                                        /*load 9516 chain address register */
        regs→am9516ptr = AM__CAR__LOW;
        regs→am9516dat = (short)((int)addr1 & 0xffff);
```


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```
#ifdef DEBUG
printf("/nDVXstrategy: Chain Addr Lo Addr = %x
Dat = %x",AM__CAR__LOW,regs→am9516 dat);
#endif
        regs→am9516ptr = AM__CAR__UP; regs→am9516dat = (short)
        ((((int)addr>>8)&0xff00)
        |(WAIT__STATES<<1) );

#ifdef DEBUG
print("/nDVXstrategy: Chain Addr Hi Addr = %x
Dat = %x",AM__CAR__UP,regs→am9516dat);
#endif
/*
* move the 9516 parameters into the top of the user's buffer
/*
        uiomove((caddr__t)cb,(sizeof(struct ChainBlk)<<1),

        UIO__READ,av→uio);
#ifdef DEBUG
print("/nDVXstrategy:Phys Addr = %x, Data = %x",caddr,caddr[0]);
print("/nDVXstrategy:Phys Addr = %x, Data = %x",caddr,caddr[1]);
#endif

                                        /* bootstrap the 9516 to begin DMA */
        /* point to command register */
        regs→am9516ptr = AM__CMDR;
        if ( regs→thresh & AV__TRIG__SEL)
        /* start channel 1 chaining */
        regs→am9516dat = ST__CHAIN__1;
        /* start channel 2 chaining */
        regs→am9516dat = ST__CHAIN__2;
                                        /* start up the converter if the external start
mode is NOT
                                        selected */
        if ( (av→control__reg & AV__XSTART__STOP) = = 0)
                                        av→control__reg | = AV__START__STOP;
                                        regs→csr = av control__reg;
        }
(void)splx(s);                                          /* restore CPU
priority */
}
```


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6.0 SPECIFICATIONS

6.1 ANALOG SIGNAL INPUT

Differential Input Voltage ..... ±10V
Input Bias Current ..... 5 nA max.
Input Resistance ..... 100 MΩ typ.
Input Capacitance ..... 70 pF max.
Common Mode Voltage ..... ± 10V max.
Input Overvoltage Protection ..... ± 25V max.
Connector Type ..... D type 25 pin

6.2 AMPLIFIER CHARACTERISTICS

Gain Accuracy Per Range ..... ± 0.02%
Gain Ranges 1, 2, 4, 8
Offset ..... 55 mV max.
Slew Rate ..... 18 V/µs max.
CMRR ..... 86 dB @ 60 Hz
Settling Time ..... 975 ns (typ.) to 0.008%
of 10-volt input step @ gain = 1

6.3 DYNAMIC CHARACTERISTICS

Aggregate Conversion Rate ..... 1024 Ksamp/s max.
Noise* ..... (0.5 LSB + 300 µV) rms
Differential Crosstalk ..... –83 dB max. @ 20 kHz
S/H Aperture Delay ..... 20 ns (typ.)
S/H Aperture Jitter ..... 10 ps rms max.
S/H Feedthrough ..... –75 dB max. @ 20 khz
Peak Distortion ..... –82 dB (typ.) @ 50 kHz
Total Harmonic Distortion ..... –80 dB (typ.) @ 50 kHz

* Referred to input over 700 kHz equivalent noise bandwidth.

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6.4 TRANSFER CHARACTERISTICS

Resolution ..... 14 bits (including sign)
Accuracy for 10V Range of ADC..... ±.006% of reading
Quantization Error ..... ±0.5 LSB max.
Integral Non-Linearity..... ±0.006% FSR max.
No Missing Codes ..... Guaranteed 0°C to +50°C
Monotonicity ..... Guaranteed

6.5 STABILITY (0°C TO + 50°C)

Required Warm-Up Time..... 15 Minutes
Offset Tempco ..... 200 µV/°C max.
Gain Tempco ..... 20 ppm FSR/°C max.
Differential Non-Linearity Tempco .... ±1 ppm FSR/°C max.
Precision Clock ..... 3.072 MHz + 0.001%

NOTE

Unless otherwise noted all specifications apply at +25°C.

Peak Distortion represents the ratio between the highest spurious frequency component below the Nyquist rate and the signal.

Total Harmonic Distortion represents the ratio between the rms sum of all harmonics up to the 20th harmonic and the rms value of the signal.

6.6 TRIGGER MODES

Internal..... Derived from an on-board precision clock or received from a Master Trigger module within the system.
External ..... Supplied by the User.
Data Dependent..... Generated at the occurrence of a predefined value on a monitored channel.

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6.7 DATA TRANSFER

Output coding .....Two's complement, Offset Binary, Binary.

Via VMEbus.....16-bit word transfer by means of an on-board DMAcontroller using a 1024 word FIFO buffer.

Interrupts .....Level 7, jumper configurable.

Via VXIbus .....2 successive byte transfers to the adjacent slot on the left (towards slot 0).

6.8 SEQUENCE CONTROLLER

Number of steps.....2048
Gain change capability.....Once per acquisition
Number of addressable channels .....256 max.
Sampling rate .....3.000 kHz to 1024 kHz in 1021 steps.

6.9 POWER REQUIREMENTS

5-Volt Supply.....5.0 ± 5% Vdc
Power Dissipation .....22W max.

6.10 ENVIRONMENTAL

Operating Temperature Range .....0° to +50°C
Storage Temperature .....-25 °to +75 °C
Relative Humidity .....0 to 85% non-condensing up to +40 °C
Recommended Forced Air Cooling ....10 CFM

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6.11 DIGITAL INPUTS/OUTPUTS

Logic Levels, TTL/CMOS Compatible:
- Logic "0" ..... 0.8V max.
- Logic "1" ..... 2.0V min.

External Trigger ..... TTL Active Low, 50 Ohms
125 ns min., 175 ns max.,
External Start ..... TTL Active Low, 50 Ohms
Multiple Channel S/H Command ..... TTL (on P2) Active High
Sample & HOLD Complement ..... TTL (on P2) Active Low
Remote Trigger ..... TTL (on P2) Active High

6.12 TEST CALIBRATION

Reference Voltage ..... 1.170 Volts ± 12%

6.13 VME DATA TRANSFER RATES

Actual data transfer rates for the DMA operations are highly dependent upon system configuration and system operation. The latency of the VME bus resident memory boards, the relative position of the DAS on the bus request daisy chain, the length of time other bus masters retain control of the bus, and other factors degrade the maximum data rates achievable on the VME bus. The DAS can sustain an average data rate of 1.2 million words per second when there is no contention for the VME bus mastership. The user can approximate the expected transfer rate by calculating the minimum transfer time per word as 600 ns plus the maximum write cycle time of the target bus memory.

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7.0 APPENDIX

7.1 VME / VXI COMPLIANCE

The DAS conforms to the VMEbus Specification Rev. C.1 and has the following compliance code:

MA24, MD16, SAD016, SAD024, SD16, 11-7 (ROAK & RORA)

The DAS conforms to the VXIbus Specification Rev. 1.3 for register based cards. It is a class 1 (TTL) user of the P2 connector based local buses A and C.

7.2 CONNECTOR PIN ASSIGNMENTS

7.2.1 Analog Input Connector J1

Pin #	Signal	Pin #	Signal
1	Input 5 +	14	Input 3 Guard
2	Input 5 –	15	Input 3 –
3	Input 5 Guard	16	Input 3 +
4	Input 7 +	17	Input 1 Guard
5	Input 7 –	18	Input 1 –
6	Input 7 Guard	19	Input 1 +
7	Input 0 +	20	Input 6 Guard
8	Input 0 –	21	Input 6 –
9	Input 0 Guard	22	Input 6 +
10	Input 2 +	23	Input 4 Guard
11	Input 2 –	24	Input 4 –
12	Input 2 Guard	25	Input 4 +
13	Not Used		

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7.2.2 VME Bus P1 Connector

	Signal Mnemonics		
Pin	Row a	Row b	Row c
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	Not Used	SYSRESET*
13	DS0*	Not Used	LWORD*
14	WRITE	Not Used	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	Not Used	A17
22	IACKOUT*	Not Used	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	Not Used	Not Used	Not Used
32	+ 5V	+ 5V	+ 5V

Not Used means the the VME/VXI signal is not connected on the card.

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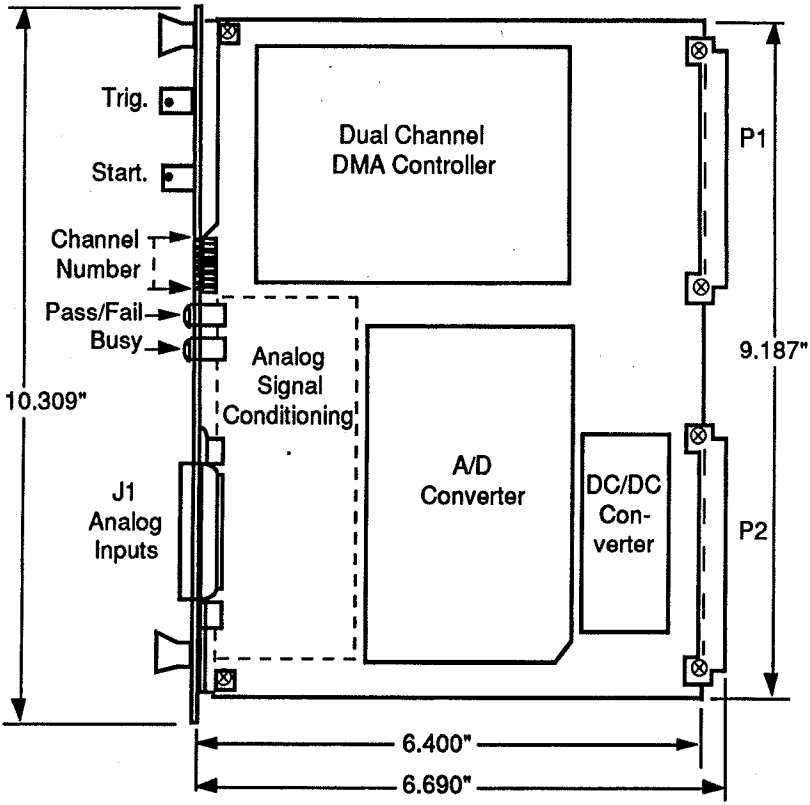
7.2.3 VME / VXI Bus P2 Connector

Pin	Signal Mnemonics Row a	Row b	Row c
1	Not Used	+ 5V	Not Used
2	Not Used	GND	Not Used
3	Not Used	Not Used	GND
4	Not Used	Not Used	Not Used
5	LBUSA00	Not Used	LBUSC00
6	LBUSA01	Not Used	LBUSC01
7	Not Used	Not Used	GND
8	LBUSA02	Not Used	LBUSC00
9	LBUSA03	Not Used	LBUSC01
10	GND	Not Used	GND
11	LBUSA04	Not Used	LBUSC00
12	LBUSA05	GND	LBUSC01
13	Not Used	+ 5V	Not Used
14	LBUSA06	Not Used	LBUSC00
15	LBUSA07	Not Used	LBUSC01
16	GND	Not Used	GND
17	LBUSA08	Not Used	LBUSC00
18	LBUSA09	Not Used	LBUSC01
19	Not Used	Not Used	Not Used
20	Not Used	Not Used	LBUSC00
21	Not Used	Not Used	LBUSC01
22	GND	GND	GND
23	TTLTRG0*	Not Used	TTLTRG1*
24	TTLTRG2*	Not Used	TTLTRG3*
25	Not Used	Not Used	GND
26	TTLTRG4*	Not Used	TTLTRG5*
27	TTLTRG6*	Not Used	TTLTRG7*
28	GND	Not Used	GND
29	Not Used	Not Used	Not Used
30	MODID	Not Used	GND
31	Not Used	Not Used	Not Used
32	Not Used	+ 5V	Not Used

Not Used means the the VME/VXI signal is not connected on the card.

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7.3 MECHANICAL OUTLINE



DVX 2504 Outline

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8.0 WARRANTY

Seller warrants that the DVX 2504 Data Acquisition System will conform to written specifications, drawings, and other descriptions made by the seller, including any modification thereof. The Seller warrants the goods against faulty workmanship and defective materials. If any goods fail to conform to these warrantees, the Seller will, as its sole and exclusive liability hereunder, repair or replace such goods if they are returned within the following warranty period:

WARRANTY PERIOD

Twelve (12) months from date of shipment from manufacturer.

These warranties are made upon the express condition that:

1) Analogic is given prompt written notice upon discovery by Buyer of such nonconformity, with a detailed explanation of the alleged deficiencies;
2) Such goods are returned to the Seller at the expense of the Buyer;
3) Examination of such goods by Seller discloses that the nonconformity actually exists and was not caused by accident, misuse, neglect, alteration, improper or unauthorized repair, or improper testing, and
4) Such goods have not been modified, altered, or changed by any person other than the Seller or its duly authorized repair agents.

Analogic will have 30 days to repair or replace such goods.

THESE WARRANTIES EXCLUDE ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, ORAL OR WRITTEN, INCLUDING WITHOUT LIMITATION WARRANTIES OF MERCHANTABILITY AND OR FITNESS FOR A PARTICULAR PURPOSE. SELLER WILL NOT IN ANY EVENT BE LIABLE FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES.

IN ACCEPTING THIS WARRANTY, THE PURCHASER OR BUYER AGREES TO WAIVE ANY AND ALL OTHER CLAIM OR RIGHT TO WARRANTY, OR IF SUCH BE THE CASE, ANY CLAIM OF WARRANTY FROM ANALOGIC CORPORATION. SHOULD THE SELLER BE OTHER THAN ANALOGIC CORPORATION, THE BUYER AGREES TO LOOK ONLY TO THE SELLER FOR ITS WARRANTY CLAIM OR CLAIMS.

No terms, conditions, understanding, or agreements purporting to modify the terms of this warranty shall have any legal effect unless made in writing and signed by a corporate officer of the Seller.

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9.0 SERVICE AND TECHNICAL SUPPORT

Should your DAS require service or repair, contact Analogic Service Department, either by telephone, telex, or facsimile, with the following information available:

a.) Model and serial number
b.) Quantity of each item being returned
c.) Description of malfunction
d.) Customer's "Bill To" address
e.) Customer's "Ship To" address
f.) Purchase Order number

Contact our Customer Service Office at one of the following numbers:

In North America:

Telephone	(508) 977-3000
Spare Parts Only	x3617, x3614
Repairs Only	x3612, x3613, x3615, x3616
Telex	68-17288 anal uw
Facsimile	(508) 532-8913
International: Analogic GmBH	Tel: 49-6122-70060
Analogic Ltd	Tel: 44-3-44-860111

At this time, the Service Coordinator will be able to inform you of the Customer Service Order (CSO) number, the Warranty or NonWarranty status of the units being returned, and the repair charge, if any. This CSO number will be utilized as your Return Authorization number. Please reference this number on your Purchase Order and shipping label.

After the material has been returned, you will receive the Customer Acknowledgement copy of the CSO, with the scheduled return date.

All material should be sent to the following address:

Analogic Corporation
8 Centennial Drive
Peabody, MA 01960

Attn: Receiving Dock B CSO:

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