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FAST SERIES

1 MHz Sampling Rate Data Acquisition Boards

for the PC/AT (Optional DSP Interface)

FAST12-1, FAST12-1 (SSH), FAST14-1, FAST16-1

Introduction

Analogic's FAST series of PC/AT-compatible data acquisition boards offers a wide range of capabilities for high speed/high performance applications. This versatile family is offered in 12-, 14-, and 16-bit versions with optional on-board sample memory or DSP interconnection. All the models perform to exacting specifications at a 1 MHz peak sample rate, or 250 kHz/channel across all four channels.

FAST12 (except the -4S version), FAST14, and FAST16 offer software programmable input ranges, as well as a 4-channel low-noise multiplexer, in a single PC/AT slot. In addition, an optional 8-channel sample-and-hold companion board (Model SSH-8) supports either eight or sixteen inputs of simultaneous data acquisition. On-board sample memory is available in 1, 2, 4 or 8 Megasample versions to facilitate transient data capture in real time.

A digital signal processing (DSP) interconnection is offered in either of the most popular DSP Interface Standards: DSP~Link™ or DT-Connect™. This option consists of a daughterboard that replaces the sample memory option for the FAST series and interconnects to a companion DSP board in an adjacent slot.

The FAST12-1-n-4S provides the capability to sample four channels simultaneously (SSH), and convert with 12-bit resolution, at a 250 kHz/channel rate. A single input can be sampled at 1 MHz. It offers a cost-effective and efficient solution for many applications.

Software support is provided in the form of routines to run, test, and set up the hardware functions on the board. In addition, C language libraries (Microsoft and Borland) are available to facilitate the rapid inclusion of these boards in specific applications.

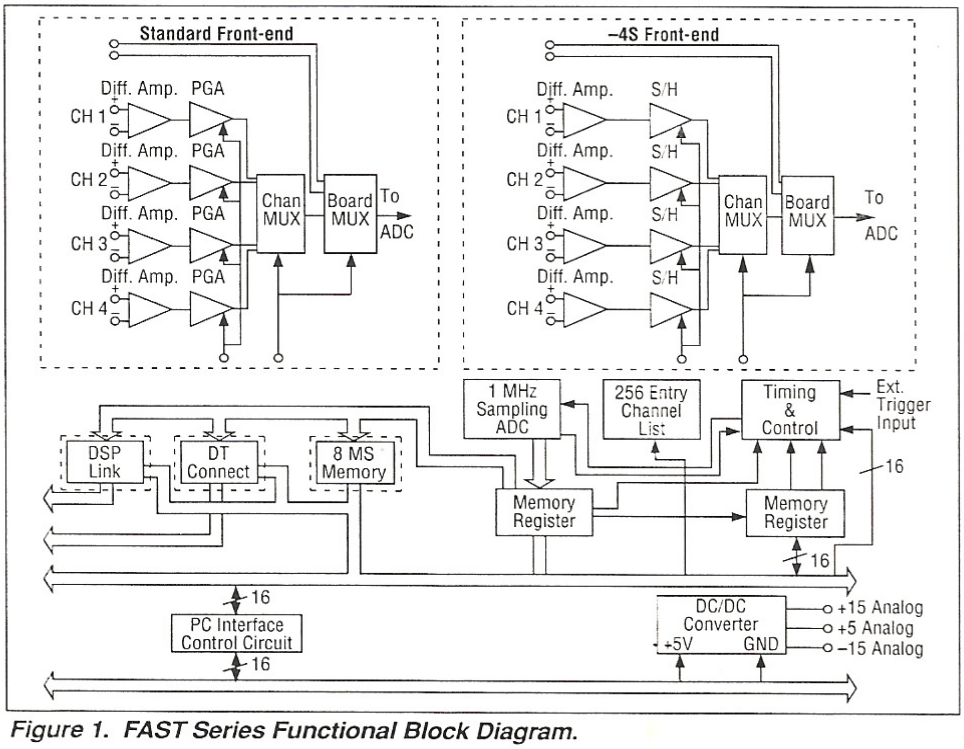
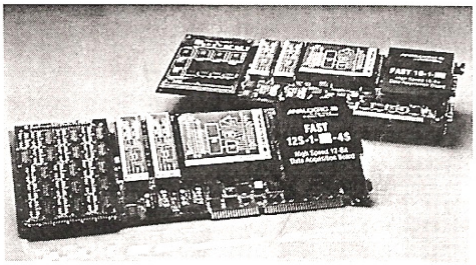


Figure 1. FAST Series Functional Block Diagram.



Features

- ❑ PC/AT-compatible
- ❑ 12-, 14- and 16-bit Resolution
- ❑ 1 MHz Sampling Rate
- ❑ Optional DSP Interface
- ❑ Four Differential Input Channels
- ❑ 4-Channel SSH Option
- ❑ Programmable Input Ranges
- ❑ Up to Eight Megasample On-board Memory
- ❑ 256-Entry Channel List
- ❑ Flexible Triggering Modes
- ❑ DMA Data Transfer
- ❑ Software Calibration
- ❑ C Libraries
- ❑ Application Software Support
  - TestPoint™
  - DASY*Lab*™

Applications

- ❑ Vibration Analysis
- ❑ Sonar
- ❑ Automatic Test Equipment
- ❑ CCD Imaging
- ❑ Waveform Analysis
- ❑ Transient Analysis
- ❑ Speech Processing
- ❑ Spectral Analysis

DSP~Link™ is a trademark of Spectrum Signal Processing, Inc.

DT-Connect™ is a trademark of Data Translation, Inc.

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FAST SERIES
Specifications[1]

	FAST12-1	FAST14-1	FAST16-1
ANALOG INPUT			
Number of Channels	Four Differential	Four Differential	Four Differential
Max. Input Without Damage			
Power On	±35V	±35V	±35V
Power Off	±20V	±20V	±20V
Input Voltage Ranges			
Unipolar	+2.5V, +5.0V, +10V (special order)	+2.5V, +5.0V, +10V (special order)	+2.5V, +5.0V, +10V
Bipolar	±2.5V, ±5V, ±10V	±2.5V, ±5V, ±10V	±2.5V, ±5V, ±10V
Input Bias Current	5 nA Typ.	5 nA Typ.	5 nA Typ.
Input Resistance	100 MΩ Typ.	100 MΩ Typ.	100 MΩ Typ.
Input Capacitance	50 pF Typ.	50 pF Typ.	50 pF Typ.
Common Mode Rejection	80 dB Min. DC to 120 Hz	80 dB Min. DC to 120 Hz	72dB Min. DC to 120 Hz
ADC TRANSFER CHARACTERISTICS			
Resolution	12 bits	14 bits	16 bits
Quantization Error	±0.5 LSB	±0.5 LSB	±0.5 LSB
No Missing Codes	Guaranteed	Guaranteed	Guaranteed
Relative Accuracy	±0.012% FSR Max.	±0.006% FSR Max	±0.003% FSR Max.
Absolute Accuracy [2]	±0.03% FSR Max.	±0.03% FSR Max.	±0.12% FSR Max.
Noise [3]	0.25 LSB RMS Max.	0.7 LSB RMS Max.	1.0 LSB RMS Max.
ADC DYNAMIC CHARACTERISTICS			
Maximum Sampling Rate	1 MHz Min.	1 MHz Min.	1 MHz Min.
Crosstalk [4]	–90 dB Max.	–90 dB Max.	–90 dB Max.
S/H Feedthrough	–84 dB Max.	–84 dB Max.	–84 dB Max.
Channel/Channel Timing Skew	N/A	N/A	N/A
Signal to Noise Ratio [5]	72 dB Min.	73 dB Min.	84 dB Min.
Peak Distortion [6]	–75 dB Max.	–78 dB Max.	–90 dB Max.
Total Harmonic Distortion [7]	–72 dB Max.	–76 dB Max.	–88 dB Max.
Full Power Bandwidth	500 kHz Typ.	500 kHz Typ.	500 kHz Typ.
Slew Rate	32 V/µs	32 V/µs	32 V/µs
Settling Error at Max. Rate	.02% of 1/2 FSR	.02% of 1/2 FSR	.02% of 1/2 FSR
STABILITY			
Offset Tempco	±200 µV/°C Max.	±150 µV/°C Max.	±100 µV/°C Max.
Gain Tempco	±50 ppm/°C Max.	±35 ppm/°C Max	±20 ppm/°C Max.
Differential Linearity TC	±2 ppm/°C Max.	±1 ppm/°C Max.	±1 ppm/°C Max.
Reference TC	±5 ppm/°C Typ.	±5 ppm/°C Typ.	±5 ppm/°C Typ.
Warm-Up Time	10 Minutes	10 Minutes	10 Minutes
TRIGGER			
Trigger Modes Programmable	Host Software	Host Software	Host Software
16 – 32 Bit Counter	Internal	Internal	Internal
External	TTL, Positive/Negative Slope	TTL, Positive/Negative Slope	TTL, Positive/Negative Slope
Analog (Memory Options Only)	Level or slope, 8-bit Resolution	Level or slope, 8-bit Resolution	Level or slope, 8-bit Resolution
External Trigger Loading	1 TTL Load	1 TTL Load	1 TTL Load
External Minimum Pulse Width	200 ns	200 ns	200 ns
TIME BASE			
Sampling Period	1 µs to 7 Min. in 100 ns Increments	1 µs to 7 Min. in 100 ns Increments	1 µs to 7 Min. in 100 ns Increments
Time Base Delay (Memory Options Only)	100% Pre-trigger to 100% Post-trigger	100% Pre-trigger to 100% Post-trigger	100% Pre-trigger to 100% Post-trigger
ENVIRONMENTAL			
PC/AT Bus Required Voltage	+5V ±5%	+5V ±5%	+5V ±5%
Current	6A Max.	6A Max.	6A Max.
Power Consumption	30W Max.	30W Max.	30W Max.
Operating Temperature	+5°C to +50°C	+5°C to +50°C	+5°C to +50°C
Storage Temperature	–25°C to +85°C	–25°C to +85°C	–25°C to +85°C
Relative Humidity	40%, Noncondensing to +50°C	40%, Noncondensing to +50°C	40%, Noncondensing to +50°C
Mounting Bracket Potential	Ground	Ground	Ground
Physical Size	Full Size, Single slot PC/AT Card	Full Size, Single slot PC/AT Card	Full Size, Single slot PC/AT Card
RFI/EMI Compatibility	Guaranteed	Guaranteed	Guaranteed

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	FAST12-1 (SSH)
ANALOG INPUT	
Number of Channels	Four Differential (SSH)
Max. Input Without Damage	
Power On	±35V
Power Off	±20V
Input Voltage Ranges	
Unipolar	+10V
Bipolar	±5V
Input Bias Current	5 nA Typ.
Input Resistance	100 MΩ Typ.
Input Capacitance	50 pF Typ.
Common Mode Rejection	72 dB Min. DC to 120 Hz
ADC TRANSFER CHARACTERISTICS	
Resolution	12bits
Quantization Error	±0.5 LSB
No Missing Codes	Guaranteed
Relative Accuracy	±0.012% FSR Max.
Absolute Accuracy [2]	±0.03% FSR Max.
Noise [3]	0.25 LSB RMS Max.
ADC DYNAMIC CHARACTERISTICS	
Maximum Sampling Rate	1 MHz Min.
Crosstalk [4]	–90 dB Max.
S/H Feedthrough	–84 dB Max.
Channel/Channel Timing Skew	±2.5 ns Max.
Signal to Noise Ratio [5]	72 dB Min.
Peak Distortion [6]	–75 dB Max.
Total Harmonic Distortion [7]	–72 dB Max.
Full Power Bandwidth	500 kHz Typ.
Slew Rate	32 V/µs
Settling Error at Max. Rate	.02% of 1/2 FSR
STABILITY	
Offset Tempco	±200 µV/°C Max.
Gain Tempco	±50 ppm/°C Max.
Differential Linearity TC	±2 ppm/°C Max.
Reference TC	±5 ppm/°C Typ.
Warm-Up Time	10 Minutes
TRIGGER	
Trigger Modes Programmable	Host Software
16 – 32 Bit Counter	Internal
External	TTL, Positive/Negative Slope
Analog (Memory Options Only)	Level or slope, 8-bit Resolution
External Trigger Loading	1 TTL Load
External Minimum Pulse Width	200 ns
TIME BASE	
Sampling Period	1 µs to 7 Min. in 100 ns Increments
Time Base Delay (Memory Options Only)	100% Pre-trigger to 100% Post-trigger
ENVIRONMENTAL	
PC/AT Bus Required Voltage	+5V ±5%
Current	6A Max.
Power Consumption	30W Max.
Operating Temperature	+5°C to +50°C
Storage Temperature	–25°C to +85°C
Relative Humidity	40%, Noncondensing to +50°C
Mounting Bracket Potential	Ground
Physical Size	Full Size, Single slot PC/AT Card
RFI/EMI Compatibility	Guaranteed

NOTES:

1. Unless otherwise noted, all specifications apply at +25°C and power supply at +5.0V.
2. Referred to on-board reference. Absolute accuracy before calibration is –0.7% to ±0.2% FSR maximum.
3. Combined thermal noise of input amplifier, S/H amplifier, and ADC noise, not including quantization noise. Referred to ±5V voltage range.
4. Measured with a ±5V sinusoidal 20 kHz input signal.
5. Signal-to-Noise Ratio represents the logarithmic ratio between the RMS value of the signal and the total RMS noise below the Nyquist rate. The total RMS noise is computed by: (1) summing the noise power in all frequency bins not correlated with the test signal; (2) estimating the total noise power contained in all harmonically related frequency bins; and (3) computing the RMS noise from the sum of (1) and (2), measured with a ±5V 20 kHz input signal.
6. Peak Distortion represents the logarithmic ratio between the highest spurious frequency component below the Nyquist rate and the input signal. Note that in computing peak distortion, the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed (see Note 5). Measured with a ±5V 20 kHz input signal.
7. Total Harmonic Distortion represents the logarithmic ratio between the RMS sum of all harmonics up to the 100th harmonic and the RMS value of the input signal. Note that in computing THD, the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed (see Note 5). Measured with a ±5V 20 kHz input signal.

Specifications subject to change without notice.

HARDWARE DESCRIPTION

Analog Input Section (standard)

Each differential analog input to the FAST Series contains a multiplexer that, under software control, switches from the input signal to a reference, determined by the range of the channel, for auto-calibration. The input buffers consist of a pair of high input impedance, low bias current amplifiers. Each buffer drives one side of a well-balanced differential amplifier, which then drives a programmable gain amplifier (PGA) that, under software control, sets the range of the channel. Both the differential amplifier and PGA have been carefully designed for low-noise and fast-settling characteristics. The outputs of the PGAs drive a 4:1 high-speed channel select multiplexer. This is followed by a high-speed buffer amplifier that drives a 3:1 board select multiplexer that allows switching between the Master board (FAST front end) and two slave boards (SSH-8).

The board select multiplexer is connected to the input of a two-pass, sub-ranging sampling A/D converter. State-of-the-art 1 MHz, 12-, 14- or 16-bit converters with a proven track record of high reliability were chosen to provide the high performance the FAST Series requires.

Analog Input Section (SSH version)

FAST 12-1-1-4S provides a 4-channel simultaneous sample-and-hold (SSH) on the board. This feature supports sampling of very high speed signals at 1 MHz for one channel or 250 kHz/channel for four channels.

Channel List

Complex channel sequencing is simplified by use of a unique Channel List stored in on-board RAM. This list is a 256-channel entry that specifies the sequence in which input channels are to be sampled. The list, from 1 to 256 valid entries, is advanced by the internally generated ADC sampling signal at a maximum rate of 1 MHz. An entry includes: CHANNEL CODE; NULL BIT; SSH BIT; and RECYCLE BIT.

CHANNEL CODE: Indicates next channel to be sampled.

NULL BIT: A logic "1" indicates a nonconversion or "dead time" at this point in the sequence.

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SSH BIT: A logic "1" indicates that this channel and the next channel will be sampled at the ADC sampling signal rate. A logic "0" indicates that this is the last channel to be sampled. The next channel will wait for a pacing signal before sampling begins. When used with a S/H slave board, the SSH BIT has a second function. A logic "1" tells the slave board to remain in HOLD. The next channel will be converted at the maximum rate. A logic "0" tells the slave to go into SAMPLE and begin acquiring new data at the completion of this channel's conversion.

RECYCLE BIT: A logic "1" indicates the last channel in the cycle. Following this last conversion, the Channel List will be recycled to the beginning at entry #0. If the SSH BIT is set to "1", the Channel List will be sequenced, again, from entry #0. If the SSH BIT is set to "0" with a logic "1" RECYCLE BIT, the converter will wait for the next Trigger and/or Pacing Signal, depending on the mode of operation.

Control Signals

The FAST Series offers three first trigger options and four second trigger options. First Trigger is used (1) to initiate a conversion sequence; and (2) as an enable (depending on the mode of operation selected). The first trigger can be selected to be an external TTL input, on-board 16- or 32-bit timer, or a programmable software bit. For all modes of operation, the first trigger initiates a conversion sequence; i.e., samples will be converted when the first trigger occurs. Subsequent conversions depend on the mode selected.

The second trigger is used to signal the end of the conversion sequence (see FREE RUN and GATED MODE). It has four available options, the three mentioned for the first trigger, and an analog voltage (available with memory options only) from one of the four input channels.

Pacing is used to initiate conversions in modes of operation where the trigger is used as a gate.

Modes of Operation

The FAST Series boards may interface to the PC/AT as a programmed I/O device or via Direct Memory Access (DMA). They offer four modes of operation for data acquisition: Normal Trigger Mode; scan count Mode; Free Run Mode; and Gated Mode.

NORMAL MODE: Acquisition and conversion are controlled and paced by trigger only.

SCAN COUNT MODE: This is the only mode using the Scan Counter. The Scan Counter is programmable from 1 to 255 scans through the channel list. Acquisition and conversion are controlled by the pacing signal after it has been enabled by a trigger signal. As previously stated, the first trigger initiates the first set of conversions determined by the channel list. All subsequent conversions are governed by the pacing signal and the channel list. Conversions continue, initiated by the pacing signal, until the Scan Counter is decremented to "0" or until the on-board memory generates a "Memory Full" signal.

In both Normal Trigger Mode and Scan Count Mode, after two samples are collected, a "data ready" signal will be generated, and data stored in on-board memory can be transferred to the PC via PIO or DMA. Data can be transferred "on the fly" as it is acquired, or the memory could be programmed not to transfer data until memory is full, or after a specific number of samples has been taken.

FREE RUN MODE: Again, the trigger signal is the enabl with the pacing signal controlling acquisition and conve sion. The first trigger starts the initial set of conversions determined by the channel list. Subsequent conversions are governed by the pacing signal and the channel list. I the Free Run Mode, the channel listing sequence contin ues until the second trigger ends the sequence. At thi time, a pre-programmed number of samples are taken an data can now be transferred to the PC. This mode is use to capture data around an event (pre- and post-triggere data). In this mode, data transfer to the PC is not allowe until the second trigger occurs. On-board memory is al lowed to overwrite itself without an error condition.

GATED MODE: This mode of operation is the same as the Free Run Mode except that data stored in on-board memory can be transferred to the PC memory at any time, and an error condition is generated if the on-board memory overflows.

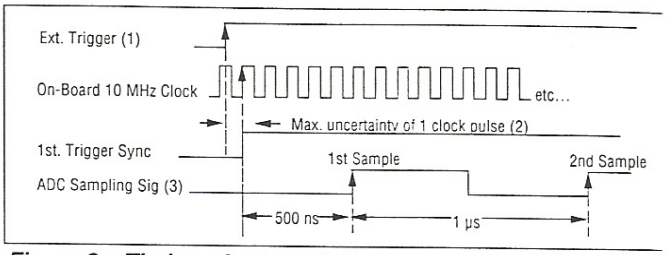


Figure 2a. Timing of external trigger to that of the on-board timing signals in all Modes.

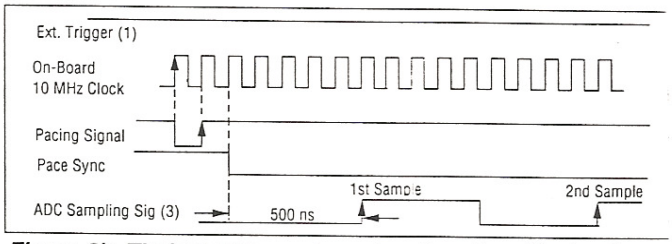


Figure 2b. Timing of the on-board pacing signal in the three Paced Modes.

NOTES:

1. The external trigger can be configured in software to activate first trigger sync on either a positive or negative edge.
2. First trigger sync is generated in coincidence with rising edges of the external trigger and the on-board 10 MHz clock.
3. The ADC sampling signal, once synchronized, will initiate an ADC sample precisely every 1 µs as controlled by the channel list.

Noise Immunity

Noise immunity within the FAST Series board is achieved, maintaining true stated resolution, by use of proven high frequency layout techniques, including short leads and interconnects, guarded signal lines, and the use of separate power and ground planes within the printed circuit board's eight layers. Noise immunity is further enhanced by careful use of on-board DC-to-DC converters to generate all required supply voltages.

Typical Examples

To program FAST Series boards, both the Channel List and the selected mode of operation must be taken into consideration. Typical examples of this are described on the next page.

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Figure 3a illustrates a channel list programmed to sample all entries (eight in this example) at the full conversion rate of the A/D converter when the first pacing signal is issued. Figure 3b illustrates a channel list with an alternating SSH bit. With this channel list, channels 1 and 2 will be converted at the maximum rate of the A/D converter. The board will then wait for the next pacing signal to sample channel 3 only. On the next pacing signal, channel 2 will be sampled once; then there will be a "dead time" of one conversion period (Null Bit = "1"); then channel 3 will be sampled. Note that in the Normal mode, the first trigger becomes the pacing signal (Figures 4a and 4b); in the Scan Count Mode, the pacing signal is first gated by the first trigger (Figures 5a and 5b and Figures 6a and 6b). The examples shown are after the channel list has sequenced through at least once. For the pacing modes, the first trigger starts the conversions which continue automatically per the channel list definitions. All subsequent conversions for the paced modes are controlled by the pacing signal only.

CHANNEL LIST				
Entry Number	RECYCLE Bit	SSH Bit	Null Bit	Channel
0	0	1	0	1
1	0	1	0	2
2	0	1	0	3
3	0	1	0	2
4	0	1	1	x
5	0	1	0	3
6	0	1	0	1
7	1	0	0	2
–	x	x	x	x

Figure 3a. All channels converted at the maximum rate of the A/D converter.

CHANNEL LIST				
Entry Number	RECYCLE Bit	SSH Bit	Null Bit	Channel
0	0	1	0	1
1	0	0	0	2
2	0	0	0	3
3	0	1	0	2
4	0	1	1	x
5	0	0	0	3
6	0	1	0	1
7	1	0	0	2
–	x	x	x	x

Figure 3b. Alternate SSH bit. An entry following a logic "0" SSH bit must wait for a pacing signal before a conversion will take place.

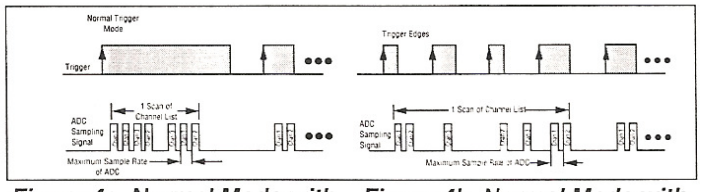


Figure 4a. Normal Mode with channel list of Figure 3a.

Figure 4b. Normal Mode with channel list of Figure 3b.

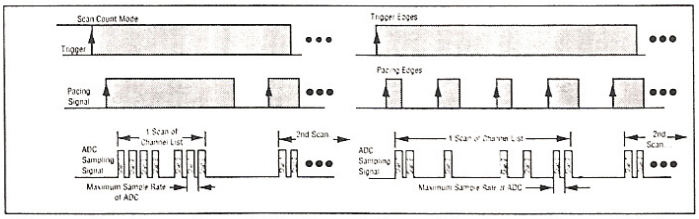


Figure 5a. Scan Count Mode with channel list of Figure 3a.

Figure 5b. Scan Count Mode with channel list of Figure 3b.

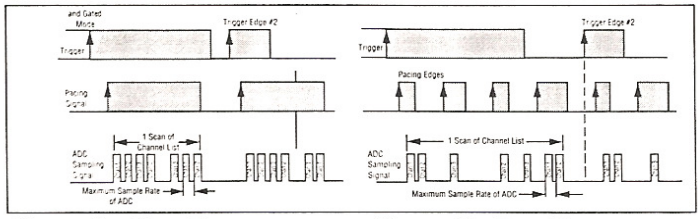


Figure 6a. Free Run or Gated Mode with channel list of Figure 3a.

Figure 6b. Free Run or Gated Mode with channel list of Figure 3b.

FAST SERIES PERFORMANCE TESTING

As part of our continuing effort to maintain our customers' confidence, Analogic supplies a data sheet indicating that 100% testing was performed on each device prior to shipping. Such data sheets reflect testing performed in both the "Frequency Domain" and the "Amplitude Domain."

Time Domain Testing

Time Domain Testing is performed by proprietary automatic test equipment that includes a 22-bit duty-cycle digital-to-analog converter. The data sheet provides the end customer with detailed results on integral linearity, A/D converter noise, absolute accuracy, conversion time, power supply current, and power supply rejection. Following is a list of the Analogic major definitions as tested with our "Amplitude Domain" test systems.

A/D CONVERTER NOISE: Errors at the output code caused by signals present other than the signal source. In FAST Series boards, this specification includes noise from the differential amplifier through and including the A/D converter.

INTEGRAL LINEARITY: A measure of the maximum deviation of the output digital codes from the best-fit straight line through the transfer function, expressed as a percentage of the full scale range. A least squares algorithm is used to determine best fit.

DIFFERENTIAL LINEARITY: A measure of the maximum deviation of any particular code width from the ideal code width, expressed as a fraction of an LSB.

$$\text{Differential Linearity} = \left| \frac{V_{MAX} - V_{LSB}}{V_{LSB}} \right| \text{ LSBs}$$

where: V_{MAX} = maximum (or minimum) code width

ABSOLUTE ACCURACY: A measure of the largest static difference between the actual output code and that predicted by the ideal transfer function; a worst case summation of all error sources, expressed as a percentage of full scale.

Absolute Accuracy measurements must be referenced to a standard traceable to the NIST with at least an order of magnitude more accurate than the unit under test.

A/D CONVERSION TIME: Time measured from the rising edge of EOC (the time when the S/H goes into hold) to the falling edge of EOC. The maximum limit is based on allowing sampling rates up to 1 MHz, including a S/H.

Frequency Domain Testing

Frequency Domain Testing is performed within the PC environment. The power of the processor provides us with a

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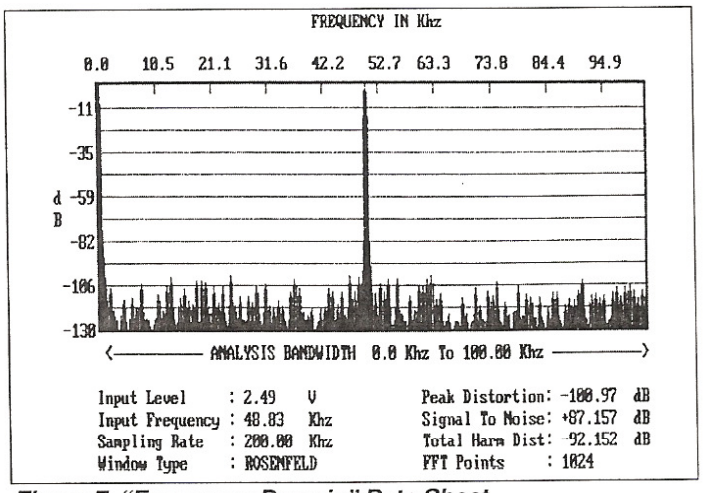


Figure 7. "Frequency Domain" Data Sheet

great deal of flexibility in both gathering and formatting the data. While a Rosenfeld window is applied on a standard basis, other types of windows (such as Blackman-Harris and Blackman) are available for custom testing. The number of samples can be varied from 512 to 8192, and the system can average up to 64 FFTs. A typical data sheet depicting testing over frequency is shown in Figure 7.

Memory

The optional on-board memory, based on the conversion mode of operation chosen, can be used as either a circular buffer or a single-sweep first-in-first-out (FIFO).

In the Free Run Mode, following a gated pacing signal, data will continuously be written to on-board memory, looping around from the bottom to top and writing over the original data until a second trigger occurs. As previously discussed, a pre-programmed number of samples will be taken at this point.

In all other conversion modes, the memory takes on the function of a large FIFO memory device. As data fills the FIFO, the application software can remove data on a first-in-first-out basis. If the program removes the data fast enough, the memory would never fill and data collection would continue indefinitely or as dictated by the channel list. If data is filling the memory faster than the program can transfer it to the host computer, a "memory full" signal is generated and conversion stops.

DSP Board Interface

DSP-Link and DT-Connect are external input/output data ports and software protocols that permit the direct connection of the FAST Series to processor boards for accelerated signal processing. These external ports provide direct high-speed 16-bit communication between the FAST Series and auxiliary boards, and can be used in either single word or block transfer mode. This set of auxiliary pathways completely eliminates host system bottlenecks. In addition, a 4K sample FIFO is included to buffer data between the two boards.

Software Description

A user-friendly Setup Program is provided with each FAST Series board. This program allows the end-user to interactively specify the following operational board parameters:

Board Select (Master or SSH-8 board)	DMA Channel
Interrupt Level	Conversion Mode
Trigger Source	Channel Listing
Analog Input Voltage Range	ADC Sampling
Number of Data Points	Rate

The board parameters selected in the Setup program are saved in a configuration file named "FAST_CFG.CFG". This configuration file may then be used to initialize the board from an application program containing the FAST library functions.

High Level Language libraries are available for custom application programming in addition to set up, demonstration, and diagnostic programs, which support all hardware functions of the FAST Series. The high-level language interface for the Analogic FAST Series simplifies programming in any of the following languages:

Microsoft C 5.1 or later.

Borland C

Ordering Guide

Specify: *FAST* ___ – ___ – ___ – ___

- 12—12-Bit Resolution
- 14—14-Bit Resolution
- 16—16-Bit Resolution
- 1—1 MHz Sample Rate
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