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PC-BASED
DATA ACQUISITION
SYSTEM

16-400503 Version 5.00

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Table of Contents

CHAPTER ONE: Introduction 1-1
1.0 Overview 1-1
1.1 Analog Inputs 1-2
1.2 Analog-to-Digital Conversion 1-3
1.3 A/D Stability 1-6
1.4 A/D Signal Dynamics 1-8
1.5 Digital-to-Analog Conversion 1-9
1.6 Analog Outputs 1-9
1.7 Digital Input/Output 1-10
1.8 Counter-Timer 1-11
1.9 HSDAS-12 Block Diagram 1-12
1.10 DAS Connector Assignments 1-13
1.11 DAS Connector Assignments (10157 Mother Board) 1-14
CHAPTER TWO: Getting Started with the DAS Board 2-1
2.0 Getting Started 2-1
2.1 Compatibility 2-1
2.2 Backing up the DAS Diskettes 2-2
2.3 Installing the DAS Board 2-2
2.3.1 The PC/AT I/O Channel 2-3
2.3.1.1 DAS Address Jumpers 2-4
2.3.2 DMA Control Jumpers 2-6
2.3.3 Interrupt Control Jumpers 2-7
2.3.4 Digital-to-Analog Range Control Jumpers 2-8
2.3.5 Additional Function Jumpers 2-10
2.3.6 Miscellaneous Jumpers 2-11
2.3.7 Installing the DAS Board 2-12
2.4 Installing the DAS_MENU Setup Program 2-13
2.5 Installing the DAS-LIB Library 2-13
2.6 Choosing the Right Software 2-14

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CHAPTER THREE: DAS_MENU Setup Programs 3-1
3.0 Overview 3-1
CHAPTER FOUR: DAS Software Library Compatibility 4-1
4.0 Overview 4-1
CHAPTER FIVE: D/A Conversion 5-1
5.0 Overview 5-1
5.1 Introduction to DAC Operation 5-1
5.2 DAC Modes of Operation 5-2
5.2.1 Mode 0: PIO PIO 5-2
5.2.2 Mode 0: DAC PIO via Timer Update 5-4
5.2.3 Mode 1: PIO DMA 5-6
5.2.4 Mode 2 DMA DMA 5-9
5.2.5 Mode 4: RdRAM PIO 5-12
5.2.6 Mode 5: RdRAM DMA 5-14
5.2.7 Mode 6: RdRAM RdRAM 5-17
5.2.8 Mode 7: WrRAM RdRAM or RdRAMWrRAM 5-19
CHAPTER SIX: A/D Conversion 6-1
6.0 Overview 6-1
6.1 A/D Mode Control 6-1
6.2 Single-Ended or Differential A/D Inputs 6-3
6.3 A/D Input Channel Selection 6-4
6.4 Unipolar/Bipolar Analog Inputs 6-6
6.5 A/D Converter Pacing and Burst Mode 6-8
6.5.1 Programming On-board A/D Pacing 6-13
6.5.2 Programming External A/D Pacing 6-14
6.6 A/D Triggering 6-14
6.6.1 Software Triggering 6-14
6.6.2 External Triggering 6-15
6.7 A/D Pre-/Post-Event Mark 6-15
6.7.1 Analog Event Mark Trigger 6-16
6.7.2 External (Digital) Event Mark Trigger 6-16

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CHAPTER SEVEN: Registers 7-1
7.0 Overview 7-1
7.1 D/A Mode Register 7-1
7.2 A/D Mode Register 7-7
7.3 Control Register 7-15
7.4 Interrupt Control 7-21
7.5 Status Register 7-29
7.6 Range Control Registers 7-35
7.7 Storage Control Registers 7-37
7.8 A/D Control Register 7-40
7.9 RAM Control Register 7-47
7.10 Counter-Timer Registers 7-51
7.10.1 Counter-Timer Control Word 7-51
7.10.2 Counter-Timer Count Registers 7-53
CHAPTER EIGHT: The 82C54 Counter-Timers 8-1
8.0 Overview 8-1
8.1 82C54 Counter-Timer Functional Description 8-1
8.1.1 General 8-1
8.1.2 Counter-Timer Control Register 8-2
8.1.3 Counters 0, 1, and 2 8-2
8.2 82C54 Operational Description 8-5
8.2.1 General 8-5
8.2.2 Programming the 82C54 8-5
8.2.3 82C54 Write Operations 8-5
8.2.4 82C54 Read Operations 8-6
8.2.5 82C54 Mode Definitions 8-13
8.2.6 Operation Common to All Modes 8-19
CHAPTER NINE: The LSDAS-16-AC 9-1
9.0 Overview 9-1
9.1 Getting Started 9-1
9.2 DAS_MENU Setup Programs 9-2
9.3 DAS Software Library Compatibility 9-2
9.4 D/A Conversion 9-2
9.5 A/D Conversion 9-2
9.6 Registers 9-3
9.7 The 82C54 Counter-Timers 9-4

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APPENDIX A: DAC Operation Examples 10-1
A.0 Overview 10-1
A.1 D/A Mode 0 10-1
A.2 D/A Mode 1 10-3
A.3 D/A Mode 2 10-7
A.4 D/A Mode 4 10-11
A.5 D/A Mode 5 10-14
A.6 D/A Mode 6 10-18
A.7 D/A Mode 7 10-21

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CHAPTER ONE: Introduction

This manual is to be used with the following products:

HSDAS-12	400kHz 12-bit Data Acquisition Board
MSDAS-12	200kHz 12-bit Data Acquisition Board
LSDAS-12	100kHz 12-bit Data Acquisition Board
HSDAS-16	200kHz 16-bit Data Acquisition Board
LSDAS-16	50kHz 16-bit Data Acquisition Board

IMPORTANT

With the exception of the ADC subsystem, the above products are similar in all aspects of operation. Therefore, all information in this manual can be applied to any of the above products unless otherwise indicated. Whenever it becomes necessary to explain operating parameters by using examples, the HSDAS-12 will be used. As the user, it is important to remember that your system might have a different sampling rate, and the information contained in this manual may be adjusted accordingly.

1.0 Overview

The xSDAS-xx (DAS) products from Analogic Corporation are high speed, multifunction, plug-in data acquisition boards for the IBM PC/AT and compatibles. These boards contain a multimode 12- or 16-bit analog-to-digital converter (ADC) with sixteen input channels, two 12-bit digital-to-analog (DAC) output channels with optional 32K sample DAC input buffer memory, a multi-configuration 16-bit parallel digital I/O (DIO) port, and a flexible multichannel timer for triggering and pacing. Data from the ADCs is collected in a 128-sample FIFO memory area for data buffering. All data transfers to and from the DAS may be program-driven or via Direct Memory Access (DMA). All functions are contained in a single, full-length, PC/AT bus-compatible board and are fully software programmable. The board's base address, interrupt service level, and DMA addresses are fully jumper-selectable.

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1.1 Analog Inputs

The technical specifications for the analog inputs are as follows:

Number of Input Channels	16 single-ended, 8 differential
Input Voltage Range	
Unipolar	2.5V, 5.0V, 10.0V
Bipolar	+2.5V, +5.0V, +10.0V
Maximum Input Voltage for Proper Operation	
Signal and Common Mode	+11V
Input Current per Channel	1nA typical 100nA maximum
Input Fault Current	20mA for input signals less than +15V and greater than -15V
Input Impedance (in parallel with)	100MΩ minimum 50pF maximum
Maximum Input Voltage without damage)	35V (power on) 20V (power off)

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1.2 Analog-to-Digital Conversion

The DAS takes data from the sixteen analog input channels and buffers it into an analog-to-digital conversion (ADC) subsystem. Trigger signals for the ADC(s) are available from three sources: a programmable on-board timer; a software-generated signal from the host PC; or from a user-supplied external signal, which can be programmed as a positive or negative level, or edge-sensitive. The ADC(s) may be autocalibrated under software control to eliminate gain and offset errors. Data from the ADC subsystem is fed into a 128-sample FIFO buffer that allows asynchronous data transfer from the ADC(s) to the host computer. Data is transferred to the host through Direct Memory Access (DMA) or programmed I/O.

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The following specifications apply to the ADC subsystem of the DAS-12 boards:

Resolution	12 bits
Differential Non-Linearity	±1/2 LSB maximum, ±1/4 LSB typical
Integral Non-Linearity	+1/2 LSB maximum; ±1/4 LSB typical
Relative Accuracy	+0.03% maximum, +0.015% typical
Absolute Accuracy	+0.1% typical, ±0.2% maximum
Inherent Quantization Error	± 1/2LSB
Monotonicity	Guaranteed 0°C to 70° with no missing codes
Noise	0.5 LSB RMS typical, 1.0 LSB RMS maximum
Channel Crosstalk	-80dB maximum at 1kHz
Channel Feedthrough at 1kHz	-100dB typical, -90dB minimum

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The following specifications apply to the ADC subsystem of the DAS-16 boards:

Resolution	16 bits
Integral Non-linearity	±2 LSB
Relative Accuracy	±0.003% of FS maximum
Absolute Accuracy (Note 1)	±0.015% of FS maximum uncalibrated
Monotonicity	Guaranteed
Noise (Note 2)	1 LSB RSM maximum
Channel Crosstalk (Note 3)	-86dB at 1kHz maximum
Channel Feedthrough	-90dB at 1kHz maximum

Notes:

1. Gain and offset errors can be autocalibrated to within LSB of the appropriate reference.

2. Two (2) LSBs maximum for the 0-2.5V range.

3. The proportion of a 1kHz signal applied to a non-selected channel input appearing on the selected channel output:

$$20 \log \frac{Vout}{Vin}$$

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1.3 A/D Stability

The following ADC subsytem stability characteristics apply to the DAS-12 boards:

Gain Temperature Coefficient — 5 ppm/°C typical, 10 ppm/°C maximum

Offset Temperature Coefficient:

Range	Typical	Maximum
10.0V	2.5 ppm/°C	10 ppm/°C
+10.0V	5.0 ppm/°C	20 ppm/°C
5.0V	3.0 ppm/°C	6 ppm/°C
+ 5.0V	6.0 ppm/°C	30 ppm/°C
2.5V	5.0 ppm/°C	25 ppm/°C
+ 2.5V	10.0 ppm/°C	50 ppm/°C

Differential Non-Linearity Temperature Coefficient — +0.3 ppm/°C typical, +0.6 ppm/°C maximum

Integral Non-Linearity Temperature Coefficient — +2ppm/°C

Power Supply Sensitivity (+5V Logic) — + 5 ppm/% typical, +10 ppm/% maximum

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The following ADC subsystem stability characteristics apply to the DAS-16 boards:

Gain Tempco	15ppm/°CFull scale voltage may be autocalibrated to onboard reference voltage.
Offset Tempco	
0.2 LSB/°C	On the +10V range
1.5 LSB/°C	On the 0-2.5V range; may be autocalibrated.
Voltage Reference Tempco	5ppm/°C

Recalibration is recommended once per month for continuous operation at 25°C, for every 10°C change in ambient temperature, or at every Power On.

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1.4 A/D Signal Dynamics

The following are the dynamic characteristics of the ADC subsystem for the DAS-12 boards:

Maximum Throughput Rate	400kHz (HSDAS-12) 200kHz (MSDAS-12) 100kHz (LSDAS-12)
Maximum Throughput each ADC	100kHz
Aperture Delay	25ns
Aperture Uncertainty	100ps plus uncertainty of Control Logic
Common Mode Rejection Ratio (Differential Channels)at 60Hz to 1kHz	80dB typical, 70dB minimum
Full Power Bandwidth	32kHz
Small Signal Bandwidth	2MHz
Total Harmonic Distortion	-72dB typical
Signal-to-Noise Ratio	70dB

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The following are the dynamic characteristics of the ADC subsystem of the DAS-16 boards:

Maximum Throughput Rate	200kHz (HSDAS-16) 50kHz (LSDAS-16)
Aperture Delay	30ns (HSDAS-16) 25ns (LSDAS-16)
Common Mode Rejection	80dB at 60Hz
Total Harmonic Distortion	-90dB maximum; settling error +0.005% FSR maximum
Signal-to-Noise Ratio	88dB

1.5 Digital-to-Analog Conversion

The DAS digital-to-analog subsystem contains two 12-bit voltage-output digital-to-analog converters (DACs). Data is delivered to the DACs for conversion through a DAC holding register which can be loaded one of three ways: by way of programmed I/O from the host PC; under DMA; or from the optional on-board buffer RAM. Triggering and pacing of the DACs may be program-driven, internally-generated by an on-board timer, or externally-supplied by the user.

1.6 Analog Outputs

Each digital-to-analog converter (DAC) drives an integral deglitcher to prevent digital input data transients from appearing at the analog outputs. Analog output voltage ranges are jumper-selectable, and each DAC feeds a high-speed output buffer amplifier. The following specifications apply to the D/A subsystems in all members of the DAS family of boards:

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Number of Output Channels	2
Resolution	12 bits
Output Voltage Ranges (Jumper-Selectable)	5V, 10V (unipolar) +5V, +10V (bipolar)
Output Accuracy	+0.025%
Differential Non-Linearity	+1 LSB
Monotonicity	Guaranteed 0°C to 70°C
Voltage Settling Time	5μs to 0.01% of full scale
Voltage Slew Rate	13V/μs
Gain Error	+2LSB
Offset Drift	+10 ppm/°C
Gain Drift	+10 ppm/°C

1.7 Digital Input/Output

A programmable 16-bit parallel digital I/O port is available to the user through an external connector. The port can be configured as "16 bits in" or "16 bits out," or it can be configured as "8 bits in" and "8 bits out." The latter configuration allows the user to input 8 bits and output 8 bits simultaneously. The following specifications apply to all DAS boards:

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Number of bits	16
Input Loading	1 LSTTL Load
Input Pull-Up Resistor	10kΩ
Output Source Current	2.6mA maximum
Output Sink Current	24mA maximum

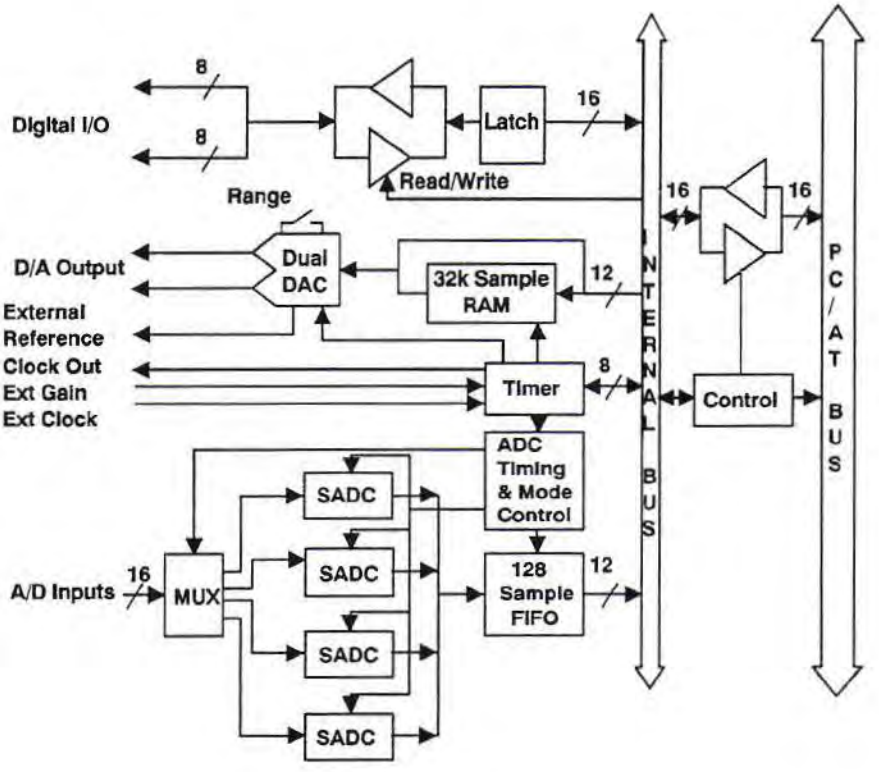
1.8 Counter-Timer

There are six 16-bit timers on the DAS board. One of these timers is available to the user through an external connector.

Number of bits	16
Inputs	Gate,clock
Output	Pulse, squarewave
Maximum Count Rate	5MHz
Functions	Event counting, frequency measurement, pulse output, time proportional output
Interrupt Sources	Output positive transition

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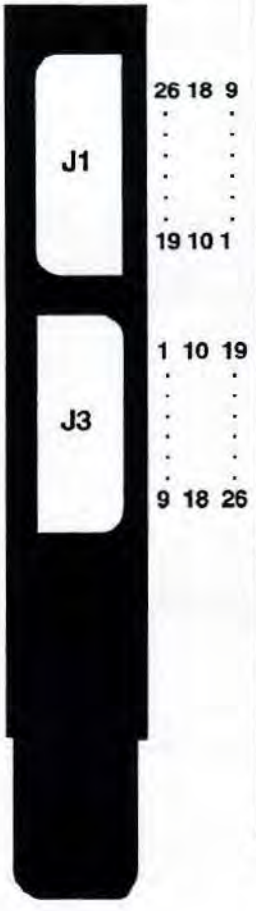
1.9 HSDAS-12 Block Diagram



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1.10 DAS Connector Assignments

End View

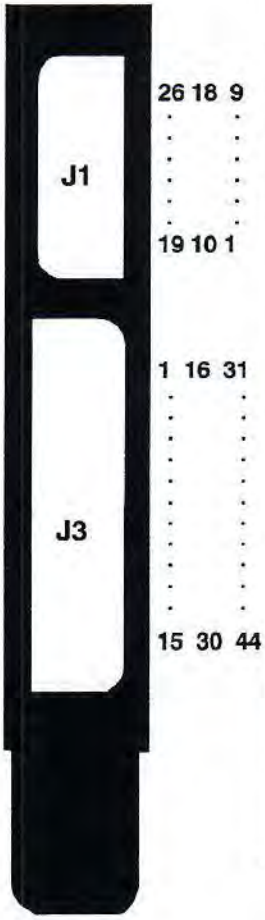


Pin	Function	Description
J1		
1	CH9_HIIN	ADC Channel 9 / Differential Channel 1 Low
2	CH10_HIIN	ADC Channel 10 / Differential Channel 2 Low
3	CH11_HIIN	ADC Channel 11 / Differential Channel 3 Low
4	CH12_HIIN	ADC Channel 12 / Differential Channel 4 Low
5	CH13_HIIN	ADC Channel 13 / Differential Channel 5 Low
6	CH14_HIIN	ADC Channel 14 / Differential Channel 6 Low
7	AGND	Analog Ground
8	EXT REF 0	External Reference for D/A converter 0
9	DAC0 OUT	Output of D/A Converter Zero
10	CH1_HIIN	ADC Channel 1 High
11	CH2_HIIN	ADC Channel 2 High
12	CH3_HIIN	ADC Channel 3 High
13	CH4_HIIN	ADC Channel 4 High
14	CH5_HIIN	ADC Channel 5 High
15	CH6_HIIN	ADC Channel 6 High
16	AGND	Analog Ground
17	EXT REF 1	External Reference for D/A Converter 1
18	DAC1 Out	Output of D/A Converter One
19	CH7_HIIN	ADC Channel 7 High
20	CH15_HIIN/CH7_LO	ADC Channel 15 / Differential Channel 7 Low
21	CH8_HIIN	ADC Channel 8 High
22	CH16_HIIN/CH8_LO	ADC Channel 16 / Differential Channel 8 Low
23	REMOTE GROUND	
24	AGND	Analog Ground
25	EALMINT	External Alarm Interupt
26	EXTTRIG	Ext A/D Trigger
J3		
1	XD0	
2	XD1	Digital I/O
3	XD2	Data
4	XD3	
5	XD4	
6	XD5	
7	XD6	
8	XD7	
9	XD8	Digital Ground
10	XD9	External A/D Trigger
11	XD10	
12	XD11	
13	XD12	
14	XD13	
15	XD14	
16	XD15	
17	DGND	Digital Ground
18	+5V	
19	EPACE	External A/D Pacing
20	TMRGATE	Gate Signal for Externally Available Counter Timer
21	TMRCLK	Clock Signal to Externally Available Counter timer
22	TMROUT	Output from Externally Available Counter Timer
23	A/DMXCK	A/D External MUX Clock
24	MXDONE	A/D MUX Done
25	DA0W	D/A Channel 0 MUX Write
26	DA1W	D/A Channel 1 MUX Write

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1.11 DAS Connector Assignments (10157 Mother Board)

End View



Pin	Function	Description
J1		
1	CH1_HIIN	ADC Channel 1
2	CH2_HIIN	ADC Channel 2
3	CH3_HIIN	ADC Channel 3
4	CH4_HIIN	ADC Channel 4
5	CH5_HIIN	ADC Channel 5
6	CH6_HIIN	ADC Channel 6
7	CH7_HIIN	ADC Channel 7
9	CH8_HIIN	ADC Channel 8
10	REMOTE	Remote Ground
11	CH9_HI/CH1_LO	ADC Channel 9 / Differential Channel 1 Low
12	CH10_HI/CH2_LO	ADC Channel 10 / Differential Channel 2 Low
13	CH11_HI/CH3_LO	ADC Channel 11 / Differential Channel 3 Low
14	CH12_HI/CH4_LO	ADC Channel 12 / Differential Channel 4 Low
15	CH13_HI/CH5_LO	ADC Channel 13 / Differential Channel 5 Low
16	CH14_HI/CH6_LO	ADC Channel 14 / Differential Channel 6 Low
17	CH15_HI/CH7_LO	ADC Channel 15 / Differential Channel 7 Low
18	CH16_HI/CH8_LO	ADC Channel 16 / Differential Channel 8 Low
19	AGND	Analog Ground
20&26	AGND	Analog Ground
J3		
1	XD1	
2	XD2	Digital I/O Data
15	XD15	
16	XD0	
17	DGND	
18	+5V	
19	+5V	
20	+5V	
23	GND	Digital Ground
24	GND	Digital Ground
26	ETRIG	External A/D Trigger
27	EPACE	External A/D Pacing
28	TMRGATE	Gate Signal for Externally Available Counter Timer
29	TMRCLK	Clock Signal to Externally Available Counter timer
30	TMR0UT	Output from Externally Available Counter Timer
31	EALMINT	External Alarm Interupt
32	AGND	
33	AGND	Analog Ground
34	DAC0OUT	D/A Convertor 0 Out
35	AGND	Analog Ground
36	DAC1OUT	D/A Converter 1 Out
37	AGND	Analog Ground
38	EXTREF0	External Reference for D/A Converter 0
39	AGND	Analog Ground
40	EXTREF1	External Reference for D/A Converter 1
41	AGND	Analog Ground
42	AGND	Analog Ground

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CHAPTER TWO: Getting Started with the DAS Board

2.0 Getting Started

You need to take several steps before using a DAS board, the first is to examine its probable uses in your application. This chapter discusses the installation of the DAS board and its software and provides a brief commentary on how to choose the right software.

2.1 Compatibility

The DAS System includes the DAS board, several floppy diskettes, and this manual. The software runs under MS-DOS Version 3.3 and higher, and the board requires an IBM PC/AT or compatible. The DAS Systems have been confirmed to operate with the following IBM PC/AT-compatible computers:

ALR
AST Premium 386
COMPAQ
CompuAdd
Fountain
Gateway
IBM
NEC
Uniq 286
Zenith
Zeos

NOTE

The DAS boards have never failed to function on a new compatible machine. The above list of computers is not exhaustive. Further, if you should find a PC/AT-compatible computer you believe does not operate the DAS board, please call our "Hot Line" number listed in the front of this manual. **WE WANT TO KNOW!**

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2.2 Backing up the DAS Diskettes

The DAS diskettes are not copy-protected and should be copied onto backup diskettes immediately. This can be done by using the DOS DISKCOPY command:

- Place the DAS_MENU diskette in Drive A.
- At the DOS prompt, type DISKCOPY A: A: (The DISKCOPY Program will prompt you for the rest of the steps).

Repeat above for all of your DAS board diskettes.

or --

- Place the DAS_MENU diskette in Drive A.
- Place a blank, formatted diskette in Drive B.
- At the DOS prompt, type COPY A:*.* B:*.*

Repeat these steps for all DAS diskettes.

Place the original diskettes in a safe environment, and work with the backup diskettes.

2.3 Installing the DAS Board

The DAS board uses sixteen consecutive address locations in the PC/AT bus I/O space. The base address is user-adjustable. This flexibilit resolves conflicts with other peripheral devices.

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2.3.1 The PC/AT I/O Channel

The I/O Bus in an IBM PC/AT-class machine has addresses ranging from 0000-FFFF Hex. Of these addresses, the range from 100-3FF Hex are available to the user. The DAS board can reside at any 16-bit boundary in the range 200 Hex-3F0 Hex. The rest are reserved for general operation of the computer itself. In the user-available range, there are commonly used areas. Table 2.1, taken from IBM's ***Technical Reference,*** describes some of the most commonly used addresses and their applications.

TABLE 2.1 - PC/AT I/O ADDRESS MAP

Hex Range	Device
200-207	Game I/O
20C-20D	Reserved
21F	Reserved
278-27F	Parallel Printer Port 2
2B0-2DF	Alternate EGA
2E1	GPIB (Adapter 0)
2E2 & 2E3	Data Acquisition (Adapter 0)
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-363	PC Network (Low Address)
364-367	Reserved
368-36B	PC Network (High Address)
36C-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC; Bisynchronous 2
390-393	Cluster
3A0-3AF	Monochrome Display and Printer Adapter
3C0-3CF	Enhanced Graphics Adapter
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

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2.3.1.1 DAS Address Jumpers

Jumpers W32-W36 (Figure 2.1) control the base address of the DAS board. Factory settings place the DAS board at I/O address 300 Hex. Usually, this is a good choice. However, if there is a conflict, by moving the jumpers, the address can be adjusted within the range 200 Hex to 3F0 Hex in increments of 10 Hex. To determine the address reflected by the jumper setting, begin with the number 0 and use the following chart.

A9 is always 1	**Add 200 Hex.**
A8 is jumper-selectable	**Add 100 Hex** when jumper W36 is not present.
A7 is jumper-selectable	**Add 80 Hex** when jumper W35 is not present.
A6 is jumper-selectable	**Add 40 Hex** when jumper W32 is not present.
A5 is jumper-selectable	**Add 20 Hex** when jumper W33 is not present.
A4 is jumper-selectable	**Add 10 Hex** when jumper W34 is not present.
A3...A0 are not selectable	**Assume they are 0** for base address calculation.

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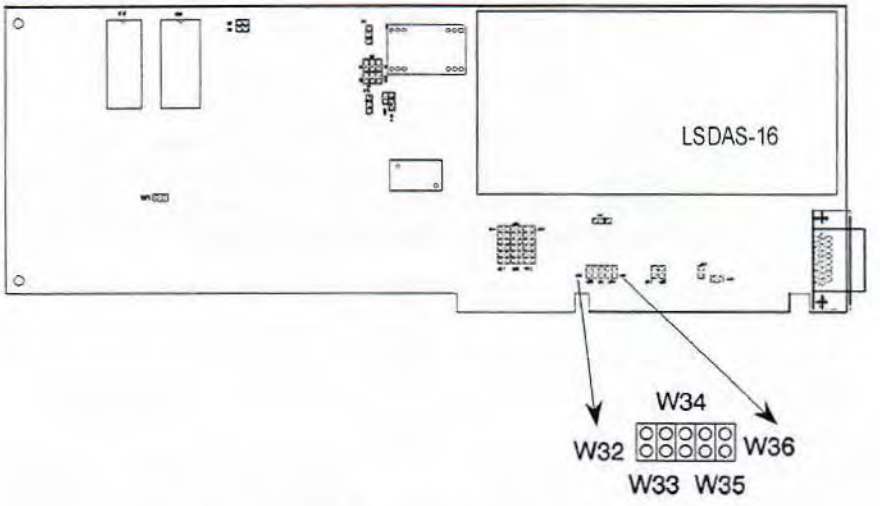
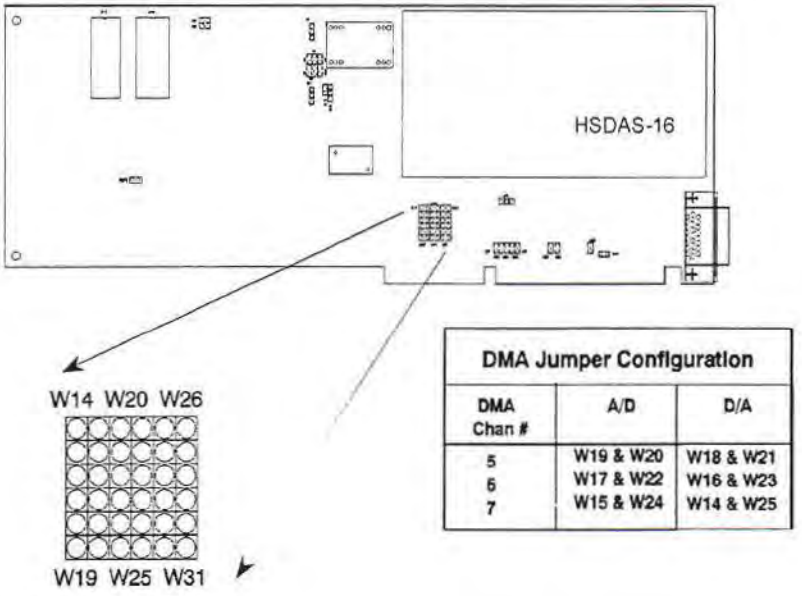


Figure 2.1: Base Address Jumpers

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2.3.2 DMA Control Jumpers

As with the base address, the DMA control levels can be adjusted to allow for multiple DAS boards and to resolve conflicts with other products. The factory sets the A/D to DMA Channel 5 and the D/A to DMA Channel 6. Note that DMA is a true "handshaking" process that requires both a request and an acknowledge signal. For this reason, the DAS has two jumpers for each DMA channel used. Figure 2.2 shows the location of the DMA jumpers and explains their settings. For more information on DAS DMA control, see Chapter Seven under **The Control Register**.



DMA Jumper Configuration

DMA Chan #	A/D	D/A
5	W19 & W20	W18 & W21
6	W17 & W22	W16 & W23
7	W15 & W24	W14 & W25

Figure 2.2: DMA Control Jumpers

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2.3.3 Interrupt Control Jumpers

The factory ships each DAS board with W30 installed (Interrupt Level 11). To avoid conflicts, users should either install the jumper for a desired interrupt level or remove it. In addition, the software available from Analogic for the DAS board does not contain interrupt handlers. A user who wishes to write custom interrupt handlers can expect the DAS to generate an interrupt request signal on one of Interrupt Lines 3, 5, 7, 10, 11, or 15. The interrupt signal transitions from low to high to generate an interrupt. The interrupt line used to signal the PC's CPU depends on the placement of the interrupt level jumper. Figure 2.3 helps users make this choice. It illustrates the placement of the jumper relative to the desired interrupt level. For more information on DAS-generated interrupts, see Chapter Seven under **Interrupt Control Register**.

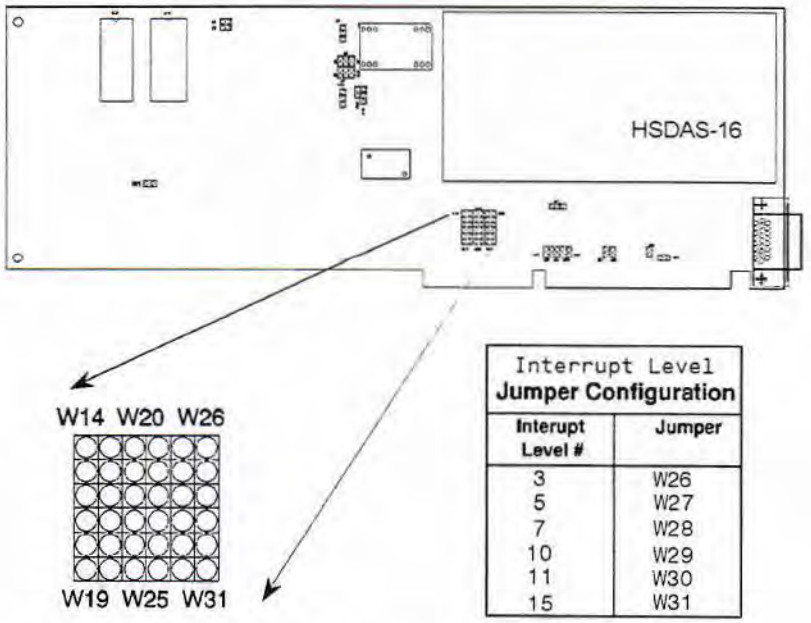


Figure 2.3: Interrupt Level Jumpers

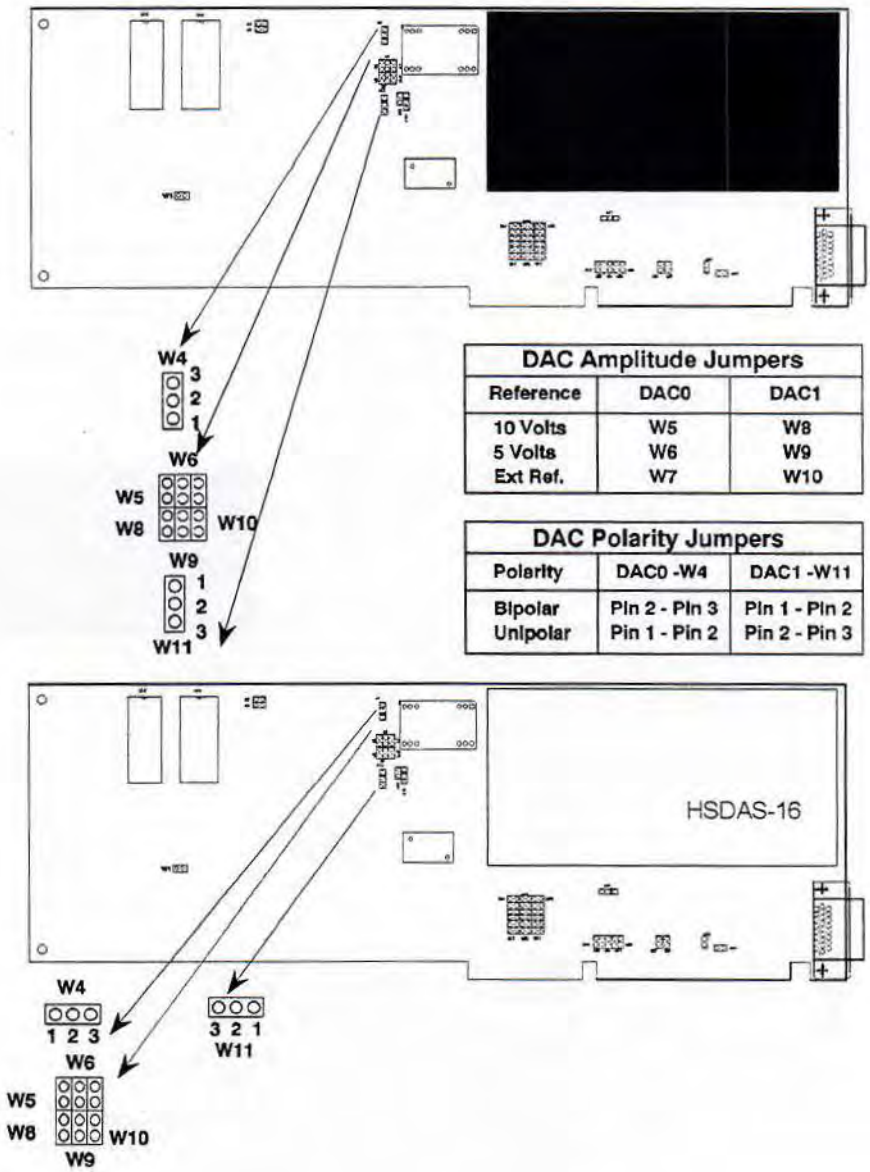
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2.3.4 Digital-to-Analog Range Control Jumpers

The DAS has two digital-to-analog converters (DACs). The output range and polarity for each DAC is jumper-selectable and should be set before the DAS board is installed in the host PC.

DACs: The reference voltage for each DAC is jumper-selectable. Internal reference signals of 5 volts and 10 volts are available, or users can choose their own external reference signal. Any of these ranges can be selected as bipolar or unipolar. Figure 2.4 indicates the location of the jumpers and describes their placement.

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DAC Amplitude Jumpers

Reference	DAC0	DAC1
10 Volts	W5	W8
5 Volts	W6	W9
Ext Ref.	W7	W10

DAC Polarity Jumpers

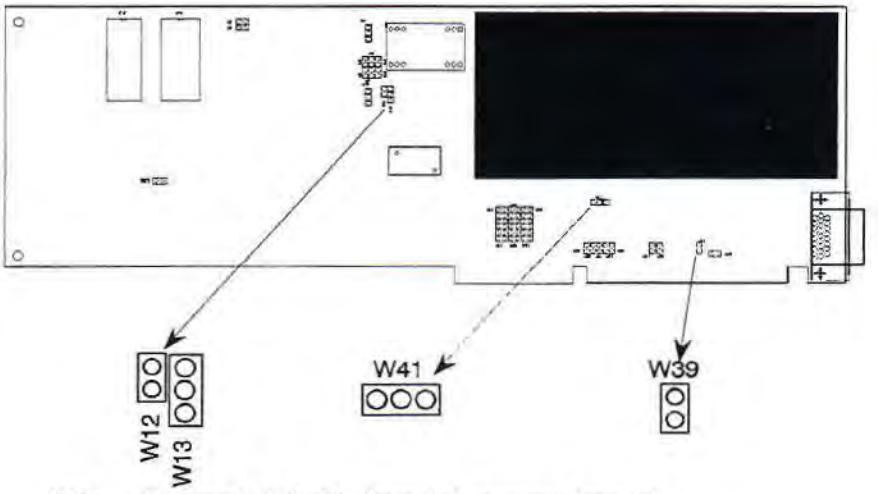
Polarity	DAC0 -W4	DAC1 -W11
Bipolar	Pin 2 - Pin 3	Pin 1 - Pin 2
Unipolar	Pin 1 - Pin 2	Pin 2 - Pin 3

Figure 2.4: DAC Range Jumpers

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2.3.5 Additional Function Jumpers

Jumpers W12 and W13 are used to configure a 32-bit internal pacing clock source for the A/D converter sub-system. This is accomplished by strapping the 16-bit A/D counter/timer to the 16-bit user available counter/timer. To implement a 32-bit pacing clock, install W12 and position W13 at pins 2 to 3. W39 is used in conjunction with W12 and W13. W39 sets a bit in the boards status register. This bit is used to tell the software how to program the A/D pacing clock (16 or 32-bit). W41 can be repositioned to provide status, or interrupt, on FIFO half-full as opposed to "Data Available" (single sample in FIFO). This jumper option is not available on the HSDAS-16. See Figure 2.5 for jumper positions and definitions.



W12 Removed (default). Installed, connects internal board clock to TMRCLK-J3 pin 21.

W13 Installed pin 1 to pin 2 for 16-bit A/D pacing clock (default). Installed pin 2 to pin 3 for 32-bit A/D pacing clock.

W39 Installed for 16-bit A/D pacing clock (default). Remove for 32-bit A/D pacing clock.

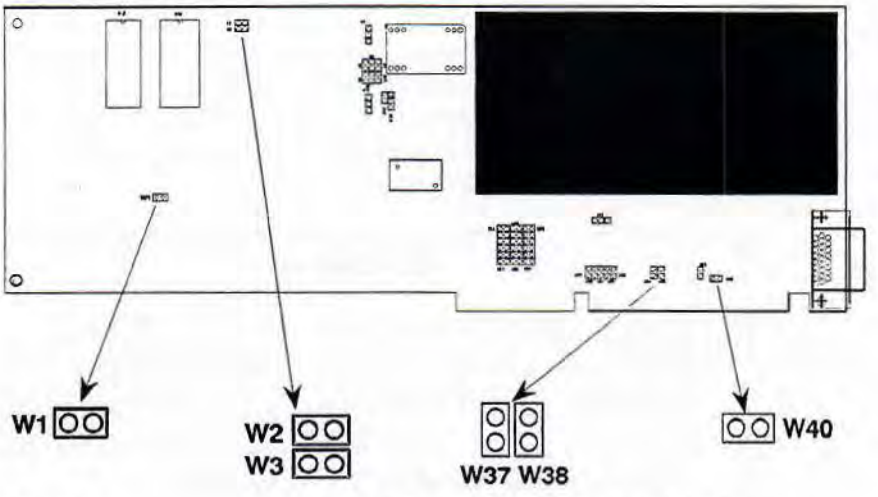
W41 Installed pin 1 to pin 2 for Interrupt when "Data Available" goes true (default). Installed pin 2 to pin 3 for Interrupt on "FIFO Half-Full".

Figure 2.5: Additional Functions Jumpers

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2.3.6 Miscellaneous Jumpers

The jumpers displayed in Figure 2.6 are not user-adjustable. The jumpers' settings are displayed so that, if they are inadvertently moved or removed, they can be replaced for proper operation. See Figure 2.6 for details on jumper locations and installation states.



Function	Jump #	Factory Config
Scope Ground	W1	Removed
Analog - Digital Gnd	W2	Installed
Analog - Digital Gnd	W3	Removed
Osc Disconnect	W37	Installed
Status Register	W38	Installed for DAS-12 Removed for DAS-16
Scope Ground	W40	Removed

Figure 2.6: Miscellaneous Jumpers

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2.3.7 Installing the DAS Board

To install a DAS board, **TURN OFF THE POWER** to your computer and remove the cover. See the Guide to Operations or User's Reference Manual that came with your computer if you are unfamiliar with this process. Select an empty, full-length, extended-connector slot in the option-board connector area of the computer. Remove the cover plate from the back of the slot by undoing the retaining screw and sliding the cover upwards. Carefully install the DAS board into the free slot by inserting the front end of the board into the guide at the front of the computer's chassis. Slide the board down to the bottom of the slot, and firmly press the board's connector into the slot in the backplane until it stops. Replace the retaining screw and the computer's cover.

WARNING!

NEVER OPEN THE COVER OR ATTEMPT TO EXCHANGE ANY PARTS OF YOUR COMPUTER WITHOUT FIRST TURNING OFF THE POWER; TO DO SO COULD CAUSE IRREPAIRABLE DAMAGE TO BOTH THE COMPUTER AND THE COMPONENT INVOLVED.

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2.4 Installing the DAS_MENU Setup Program

Each DAS board is shipped from the factory with software that includes the DAS_MENU setup program for your DAS board as well as several simple example programs.

Insert the diskette in your floppy disk drive and type:

A: <ret>

then

INSTALL <ret>

The Installation Program will prompt you for information about your computer. Then it will verify the conditions and install the software you request.

2.5 Installing the DAS-LIB Library

If you have purchased the DAS-LIB library, you need only insert the DAS-LIB Libraries/Installation diskette in your floppy disk drive and type:

A: <ret>

then

INSTALL <ret>

The installation program is interactive and will prompt you for all required information about your computer. The program then verifies the integrity of the software on your diskette and installs it.

When the Installation Program has completed, you may wish to run the simple example programs that are also provided.

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2.6 Choosing the Right Software

As discussed in Chapter One, the DAS System is a complex, self-contained data acquisition system -- PLUS A LOT MORE! Choosing the appropriate method of driving the DAS board is as important a descision as the one you made in purchasing the board itself.

The DAS boards have software support from several major data acquisition software houses. Laboratory Technologies Corporation's ***Labtech Notebook***, HEM Data Corporation's ***Snapshot***, and DSP Development Corporation's ***DADiSP*** are just a few of the well-established third-party products that support the DAS boards. All of these products provide different types of easy-to-learn/operate user interfaces. The authors recommend the use of a mature, established user interface product.

In cases where third-party software does not meet the needs of an application, we again suggest that the application developer take control of the DAS at a software level. Analogic Corporation has developed the DAS-LIB library for the DAS boards. In addition, included with the DAS board is the DAS_MENU setup program, which can be run stand-alone or may be spawned from another program. Using DAS-LIB in conjunction with DAS_MENU provides the application developer with an easily-navigated interface that allows the user to state the desired configuration of the DAS hardware without knowing any details of the hardware. The DAS_MENU program also performs error and conflict checking to protect the user against the subtleties and complexities involved with programming the DAS board.

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CHAPTER THREE: DAS_MENU Setup Programs

3.0 Overview

The software setup program DAS_ MENU provides the capability to create configuration files. These configuration files allow convenient setup of DAS boards using DAS-LIB functions. The operation of the DAS_MENU program is described in detail in the DAS_MENU User's Manual.

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CHAPTER FOUR: DAS Software Library Compatibility

4.0 Overview

The software library DAS-LIB provides complete support for DAS series boards at a variety of levels. This library is a replacement of the earlier High Level Language (HLL) library. The DAS-LIB library is not compatible with HLL or its configuration files, due to the greatly expanded capabilities of DAS-LIB. DAS-LIB supports both Microsoft and Borland C compilers. The DAS-LIB library is described in detail in the DAS-LIB Programmer's Reference.

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CHAPTER FIVE: D/A Conversion

5.0 Overview

The DAS boards have dual, 12-bit digital-to-analog converters (DACs) which are controlled through the D/A Mode Register (see Chapter Seven). This chapter discusses the Update Timing, Data Sources, and Operational Modes for the DACs, which are determined by several bits in the D/A Mode Register.

5.1 Introduction to DAC Operation

There are seven modes of operation for the two DACs (set by Bits 3, 2, and 1 in the D/A Mode Register). These modes are divided into two sections: Modes 0, 1, and 2 are non-RAM modes; Modes 4, 5, 6, and 7 are RAM modes.

Each D/A converter can receive digital input data from one of two sources:

1. Its holding register
2. On-board RAM

DAC0 has a 12-bit holding register, and DAC1 has a 12-bit holding register. Each of these holding registers can be updated from the host computer in one of two ways:

1. PIO (programmed I/O), namely an OUT Instruction in ASSEMBLY Language
2. DMA, using a DMA channel to transfer data from a computer memory buffer to the holding register

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The holding registers and RAM can be updated according to a pacingscheme, which depends on the mode (Bits 3, 2, and 1), CS bit (Bit 0), and Pacing Bits (Bits 15-8 and Bits 5 and 4) in the D/A mode register. On-board timers can be programmed to control the update timing for each DAC (refer to Chapters Seven and Eight), or they can be asynchronously updated via the application's software.

To summarize, we have two DACs, each is updated from either its holding register or on-board RAM at a periodic updating rate, which is programmable or asynchronous at a rate determined by the application's software. The DAC holding registers and RAM can be loaded via programmed I/O or DMA. For all the DAC operating modes, the DACs are loaded from one of two sources, either the holding registers or the onboard RAM.

5.2 DAC Modes of Operation

The DAC Mode Bits (Bits 3, 2, and 1) and the CS Bit (Bit 0) in the D/A Mode Register determine the source of the digital input data for each DAC. The following subsections discuss each DAC Mode of Operation and show a step-by-step example of each mode's setup and execution.

NOTE
Unless otherwise specified, all bits referred to in the discussions in this chapter are in the D/A Mode Register. See Chapter Seven for a detailed explanation of the D/A Mode Register.

5.2.1 Mode 0: PIO PIO

This mode updates the holding registers via a programmed I/O operation (an OUT Instruction in ASSEMBLY Language). Updating of the DACs can be selected to be via software or a timer. Typical programming operation for software updating is as follows:

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1. ➲ Set Mode (Bits 3, 2, and 1);

   ➲ CS (Bit 0);

   ➲ DAC Trigger Select (Bits 12 and 8) for each D/A converter;

   ➲ DAC Update Source Select (Bits 14 and 13 and Bits 10 and 9) for each D/A converter.

2. Set D/A Mode Reset Bit to 1 to enable the D/A Converters (Bit 5 in the Control Register).

3. Set the Enable Update Request Bits (Bits 15 and 11) for each D/A converter.

   NOTE
   This must be done after setting Bit 5 in the Control Register to 1.

4. The D/A converters are now ready to receive digital data via PIO (an ASSEMBLY Language OUT Instruction).

5. The DACs will be updated automatically after the data is sent to the holding register via the ASSEMBLY Language OUT Instruction.

6. Poll the DAC Ready Bits (Bits 4 and 3 in the Status Register) for ready condition before sending the next piece of data via the OUT Instruction. It takes no longer than 5us for the DACs to settle to within 0.01% of the programmed output value.

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5.2.2 Mode 0: DAC PIO via Timer Update

1. ➲ Set Mode (Bits 3, 2, and 1);

   ➲ CS (Bit 0);

   ➲ Update Type (Bits 12 and 8);

   ➲ Update Source Select (Bits 14 and 13, and Bits 10 and 9).

2. Set up timer(s), one timer for each D/A converter (refer to Chapters Seven and Eight).

3. Set D/A Mode Reset to 1 (Bit 5 in the Control Register).

4. Send the first words of data for both DACs to their holding registers via PIO (ASSEMBLY Language OUT Instruction).

   NOTE
   The data is now in the holding registers waiting to be transferred to the D/A Converters. Updating the DAC is done when its timer times out (counts to 0) and generates an update pulse. The DACs can only be updated if the Enable Update Request Bits (11 and 15) are set to 1 (which has not been done yet).

5. Set the DAC Timer Interrupts to 1 (Bits 1, 0 in the Interrupt Control Register) and wait for the DAC Timer Interrupt Status Bits (Bits 1 and 0 in the Status Register) to go to 1. Check the DAC Timer Interrupt Status Bits by polling the Status Register. These bits indicate when each timer has generated an update pulse. Now the DAC Timers are synchronized with our application's software.

6. Clear the DAC Timer Interrupt Status Bits by resetting Bits 1 and 0 in the Interrupt Control Register to 0 then back to 1 again.

7. Set the Enable Update Request Bits (Bits 15 and 11 in D/A Mode Register) to 1.

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NOTE
On the next timer pulse, the DACs will be updated with the data in the holding registers.

8. Poll the Status Register for DAC Timer Interrupt Status Bits. When these bits go to 1, clear them by resetting Bits 1 and 0 in the Interrupt Control Register to 0 and back to 1 again.

9. Poll the Status Register for DAC Ready Bits (Bits 4 and 3). When these bits go to 1, the D/A Converters have "settled" and are ready for new input data.

10. Send next data via PIO (ASSEMBLY Language OUT Instruction).

11. Continue to poll the Timer Interrupt Status Bits, clear them, and send new data.

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TABLE 5.1 - D/A UPDATE PACING SELECTION: MODE 0

(Many = Timer1, Timer2, or A/D Pacer Signal)

CS=0

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mod	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
0	X	Software	Software
1	0	Many	Software
1	1	Many	Many

CS=1

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mode	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
X	0	Software	Software
0	1	Software	Many
1	1	Many	Many

X = Don't Care

5.2.3 Mode 1: PIO DMA

In this mode, the D/A Converter designated by the CS Bit (Bit 0) is updated via DMA, while the other DAC is updated via PIO. The DAC channel selected by the CS Bit must be programmed to be paced via a timer, while the other DAC channel can be programmed to be paced via software or a timer. The data is transferred to the holding registers; then the DACs are updated according to the pacing selected.

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The following steps should be taken to set up DAC Mode 1 operation:

1. ➲ Set Mode (Bits 3, 2, and 1);

   ➲ CS (Bit 0);

   ➲ Update Type (Bits 12 and 8);

   ➲ Update Source Select (Bits 14 and 13, and Bits 10 and 9).

2. Set up the timer(s), one timer for each D/A Converter (refer to Chapters Seven and Eight).

3. Set D/A Mode Reset to 1 (Bit 5 in the Control Register).

4. Send the PIO DAC's data to its holding register.

5. Set up the DMA channel; set the DAC DMA Enable Bit (Bit 12 in the Control Register) to 1.

6. Start the DAC DMA process by setting Bit 13 in the Control Register to 1. This transfers the first word into the appropriate DAC holding register.

7. Set the DAC Terminal Count Interrupt and DAC Timer Interrupt Status Bits (Bit 3, and either Bit 1 or Bit 0 in the Interrupt Control Register, depending on CS Bit chosen above) to 1.

8. Poll the Status Register and wait for the DAC Timer Interrupt Status Bit (either Bit 1 or Bit 0 in the Interrupt Control Register, depending on CS Bit chosen above) to go to 1. The transition to 1 tells the application's software that the timer has counted down to 0 and gives the application a known state for the D/A Pacing Signal.

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9. When the Timer Interrupt Status Bit goes to 1, clear it by resetting its corresponding Interrupt Enable Bit (either Bit 1 or Bit 0 in the Interrupt Control Register, depending on CS Bit chosen above) to 0 and back to 1 again.

10. Set the Enable Update Request Bits (Bits 15 and 11 in the D/A Mode Register). The next timer pulse will cause the data in the holding registers to be ransferred to the DACs.

11. Poll the Status Register for the DAC Timer Interrupt Status Bit (either Bit 1 or Bit 0, depending on the CS Bit chosen above).

12. When this bit goes to 1, clear it by resetting its corresponding Enable Interrupt Bit to 0 and back to 1 again.

13. Poll the Status Register for DAC Ready Bits (Bits 4 or 3, depending on the CS bit chosen above). When this bit goes to 1, the D/A Converter has "settled" and it is ready for new input data. Send new data via an ASSEMBLY Language OUT Instruction.

NOTE
The DMA DAC's holding register will be updated automatically.

14. Poll the Status Register for the DAC Terminal Count Interrupt Status' transition to 1 (Bit 2 in the Status Register).

15. Continue to poll the Timer Interrupt Status Bits, clear them, poll the DAC Ready Bits and send new data.

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TABLE 5.2 - D/A UPDATE PACING SELECTION: MODE 1

(Many = Timer1, Timer2, or A/D Pacer Signal)

CS=0

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mod	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
X	0	Many	Software
X	1	Many	Many

CS=1

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mode	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
0	X	Software	Many
1	X	Many	Many

X = Don't Care

5.2.4 Mode 2 DMA DMA

This mode updates the DAC holding registers via the DMA process. If the DACs are programmed for Mode 2 operation. the updating of the holding registers and DACs can only be done via a timer. If CS (Bit 0 in the D/A Mode Register) is set to 0, DAC 0 is updated at a constant interval. If CS is set to 1, then DAC 1 is updated at a constant interval.

The DACs are updated via the same DMA channel. This implies two things:

1. The DACs should be paced by the same timer.

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2. The data in the buffer must be interleaved so the appropriate data goes to the appropriate DAC.

   A. Set Mode (Bits 3, 2, & 1);

      - CS (Bit 0);
      - Update Type (Bits 12 and 8);
      - Update Source Select (Bits 14 and 13, and Bits 10 and 9).

   B. Enable the D/A Subsystem by setting Bit 5 in the Control Register to 1.

   C. Set up the Timer.

   D. Set up the DMA channel; enable DAC DMA operation by setting Bit 12 in the Control Register to 1.

   E. Start the DAC DMA process by setting Bit 13 in the Control Register to 1. This transfers the first two words to the DAC holding registers.

   F. Enable the DAC Terminal Count Interrupt and DAC Timer Status bits.

   G. Poll the Status Register until either of the DAC Timer Interrupt Status Bits are set to 1. Clear it when it goes to 1 by resetting its corresponding Enable Bit in the Interrupt Control Register to 0 and back to 1 again. This synchronizes the DMA process to the D/A Pacing Timer.

   H. Enable the DAC pacing by setting the Enable Update Request Bits (Bits 15 and 11 in the D/A Mode Register) to 1.

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I. Wait for the DMA operation to finish by polling the DAC Terminal Count Interrupt Status Bit (Bit 2 in the Status Register).

TABLE 5.3 - D/A UPDATE PACING SELECTION: MODE 2

(Many = Timer1, Timer2, or A/D Pacer Signal)

CS=0 and 1

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mod	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
X	X	Many	Many

D/A Update Pacing cannot be via software D/A Mode 2

X = Don't Care

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5.2.5 Mode 4: RdRAM PIO

This mode updates the D/A converter selected by the CS Bit with digital input data from the onboard RAM memory. The other D/A converter receives input data by PIO (programmed I/O). The DAC selected by the CS bit must be paced via a Timer. The other DAC can be programmed for pacing by either software or a timer. The DAC programmed to be updated from RAM can cycle continuously to give a periodic waveform. The addressing for the RAM is done via a down counter that can reload the starting address when it reaches 0. Assuming the RAM has already been loaded with the data, the following sequence will update both DACs (for discussion on loading the RAM, see Mode7: WrRAM RdRAM).

1. ➲ Set Mode (Bits 3, 2, and 1);
   ➲ CS (Bit 0);
   ➲ Update Type (Bits 12 and 8);
   ➲ Update Source Select (Bits 14 and 13, and Bits 10 and 9).
2. Set D/A Mode Reset to 1 (Bit 5 in the Control Register).
3. Initialize the starting address for the DAC RAM in the proper timer channel. DAC0 uses Timer 2, Channel 0 for RAM addressing, while DAC1 uses Timer 2, Channel 1.

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4. Disable CPU control of the address counter by setting Bit 4 of the D/A Mode Register to 1. This allows the RAM Address Counter to be decremented automatically each time the DAC is updated. Essentially, this gives the D/A subsystem control of the RAM addressing scheme.

5. Enable the RAM mode by setting the RAM Mode Reset Bit (Bit 6 in Control Register) to 1.

6. Set up a Timer Channel for DAC pacing.

7. Enable DAC pacing by resetting the DAC Enable Bit (Bit 5 in the DA Mode Register) to 0.

8. Enable the DAC Update Request for both DACs by setting Bits 15 and 11 in the D/A Mode Register to 1.

9. Send data to the DAC holding register for the PIO DAC using the ASSEMBLY Language OUT Instruction.

10. Poll the DAC Ready Bit in the Status Register. When this bit goes to one, send more data.

NOTE
The DAC that is being updated from RAM runs automatically via the timer.

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TABLE 5.4 - D/A UPDATE PACING SELECTION: MODE 4

(Many = Timer1, Timer2, or A/D Pacer Signal)

CS=0

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mod	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
X	X	Many	Software
X	1	Many	Many

CS=1

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mode	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
0	X	Software	Many
1	X	Many	Many

X = Don't Care

5.2.6 Mode 5: RdRAM DMA

This mode allows the D/A converter chosen by the CS Bit (Bit 0 in the D/A Mode Register) to be updated from the onboard RAM memory and the other DAC channel to be updated from a buffer in the host computer's memory via DMA. In this mode, the DACs must be programmed to be updated via a timer.

1. ➲ Set Mode (Bits 3, 2, and 1);
   ➲ CS (Bit 0);
   ➲ Update Type (Bits 12 and 8);
   ➲ Update Source Select (Bits 14 and 13, and Bits 10 and 9).

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2. Enable D/A operation by setting the D/A Mode Reset Bit (Bit 5 in the Control Register) to 1.

3. Initialize the starting address for the DAC RAM in the proper timer channel. DAC0 uses Timer 2, Channel 0 for RAM addressing, while DAC1 uses Timer 2, Channel 1.

4. Disable CPU control of the address counter by setting Bit 4 of the D/A Mode Register to 1. This allows the RAM address counter to be decremented automatically each time the DAC is updated. Essentially, this gives the D/A subsystem control of the RAM addressing scheme.

5. Enable the RAM mode by setting the RAM Mode Reset Bit (Bit 6 in Control Register) to 1.

6. Set up timer(s) for updating both DACs.

7. Enable the DACs by resetting the DAC Enable Bit (Bit 5 of D/A Mode Register) to 0.

8. Enable the DAC that is selected to be updated with data from RAM by setting the Enable Update Request Bit (either Bit 15 or Bit 11 in the D/A Mode Register) to 1.

9. Set up the DMA channel; enable DAC DMA operation by setting Bit 12 in the Control Register to 1.

10. Start the D/A DMA process by setting the DAC DMA Start Bit (Bit 13 in the Control Register) to 1. This transfers the first word to the DMA DAC's holding register.

11. Enable the DAC DMA Terminal Count and the DAC Timer Interrupt Status Bits by setting Bits 2 and either Bit 1 or 0 in the Interrupt Control Register. If DAC0 is the DMA Channel, use Bit 0. If DAC1 is the DMA Channel, use Bit 1.

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12. Poll the Status Register and wait for the DAC Timer Interrupt Status Bit corresponding to the bit described in Step 11 to go to 1. The transition to 1 tells the application's software that the timer has counted down to 0 and gives the application a known state for the D/A Pacing Signal.

13. When the Timer Interrupt Status Bit goes to 1, clear it and re-enable it by resetting the bit chosen in Step 11 to 0 to clear it, then back to 1 again to re-enable it.

14. Enable the DAC to be updated via DMA by setting either Bit 15 or 11 in the D/A Mode Register to 1 (depending on whether the DMA DAC is DAC1 or DAC0).

15. Poll the Status Register for the DAC Terminal Count Interrupt Status Bit; wait for it to go to 1.

16. When the Terminal Count Interrupt Status Bit goes to one, clear it and the Timer Interrupt Status Bit by resetting their corresponding Bits in the Interrupt Control Register to 0 and back to 1 again.

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TABLE 5.5 - D/A UPDATE PACING SELECTION: MODE 5

(Many = Timer1, Timer2, or A/D Pacer Signal)

Mode 5 CS=0 and 1

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mod	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
X	X	Many	Many

D/A Update Pacing cannot be via software D/A Mode 5

X = Don't Care

5.2.7 Mode 6: RdRAM RdRAM

In this mode both DACs are updated from RAM (different areas or the same area of RAM) at the same time. Whichever DAC is chosen by the CS bit determines the timer that is used for updating.

1. Set Mode (Bits 3, 2, and 1);
   - CS (Bit 0);
   - Update Type (Bits 12 and 8);
   - Update Source Select (Bits 14 and 13, and bits 10 and 9).
2. Set D/A Mode Reset to 1 (Bit 5 in the Control Register).
3. Initialize the starting address for the DAC RAM in the proper Timer Channels. DAC0 uses Timer 2, Channel 0 for RAM addressing, while DAC1 uses Timer 2, Channel 1.

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4. Disable CPU control of the address counter by setting Bit 4 of the D/A Mode Register to 1. This allows the RAM address counter to be decremented automatically each time the DAC is updated. Essentially, this gives the D/A subsystem control of the RAM addressing scheme.

5. Enable the RAM mode by setting the RAM Mode Reset Bit (Bit 6 in the Control Register) to 1.

6. Set up a Timer Channel for DAC pacing.

7. Enable DAC pacing by resetting the DAC Enable Bit (Bit 5 in the DA Mode Register) to 0.

8. Enable the DAC Update Request bit by setting either Bit 15 or 11 in the D/A Mode Register (chosen by the CS Bit) to 1. Both DACs will be automatically updated at the pace selected. The circuitry will continuously loop and output the waveform stored in RAM.

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TABLE 5.6 - D/A UPDATE PACING SELECTION: MODE 6

(Many = Timer1, Timer2, or A/D Pacer Signal)

CS=0 and 1

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mod	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
X	X	Many	Many

D/A Update Pacing cannot be via software D/A Mode 6

X = Don't Care

5.2.8 Mode 7: WrRAM RdRAM or RdRAMWrRAM

This mode is typically used to load RAM with the waveform data that is used in Modes 4, 5, or 6. The CS Bit (Bit 0 in the D/A Mode Register) selects which DAC channel's RAM is to be written to (CS=0: data is written to DAC0 RAM; CS=1: data is written to DAC1 RAM). The same data goes to the RAM and to the DAC unless the DACs are disabled.

The DACs can be updated asynchronously via software, or automatically via DMA. However, both DACs are updated at the same time, and the DAC channel chosen by CS is the pacing used to update.

1. ➲ Set Mode (Bits 3, 2, and 1);
   ➲ CS (Bit 0);
   ➲ Update Type (Bits 12 and 8);
   ➲ Update Source Select (Bits 14 and 13, and Bits 10 and 9).
2. Set D/A Mode Reset to 1 (Bit 5 in the Control Register).

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3. Initialize the starting address for the DAC RAM in the proper Timer Channels. DAC0 uses Timer 2, Channel 0 for RAM addressing, while DAC1 uses Timer 2, Channel 1. The DAC chosen by the CS will have data written in to RAM memory. The other DAC reads out of RAM memory.

4. Enable the RAM mode by setting the RAM Mode Reset Bit (Bit 6 in the Control Register) to 1.

5. Enable the Update Request Bits (Bits 15 and 11 in the D/A Mode Register).

6. If the DAC data is coming to the RAM via PIO, then send the first word (using an ASSEMBLY Language OUT Instruction); then wait for the Timer Interrupt Status Bit to go to 1. Remember to enable it by setting Bit 0 or 1 (depending on the CS Bit) in the Interrupt Control Register. If DMA is used, then set up the DMA channel, enable it, and start it.

After data has been stored in RAM, switch to one of the other modes to read it out of RAM.

If both DAC channels are to be read from RAM, then the two areas of RAM must be loaded separately.

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TABLE 5.7 - D/A UPDATE PACING SELECTION: MODE 7

(Many = Timer1, Timer2, or A/D Pacer Signal)

CS=0

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mod	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
0	X	Software	Software
1	X	Many	Many

CS=1

DAC0 (Bit 8)	DAC1 (Bit 12)	Pacing Mode	Pacing Mode
Upd Typ Sel	Upd Typ Sel	DAC0	DAC1
X	0	Software	Software
X	1	Many	Many

X = Don't Care

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CHAPTER SIX: A/D Conversion

6.0 Overview

The DAS boards have a 16-input channel analog-to-digital sub-system that is controlled through the A/D Mode Register and the A/D Control Extended Register (see Chapter Seven). Chapter Six discusses Channel Control, Mode, Pacing, and Triggering Control.

6.1 A/D Mode Control

The HSDAS-12 has four high-accuracy, fully software-programmable, 100kHz/12-bit analog-to-digital converters (ADCs). In combination, these converters give the HSDAS-12 a 400kHz maximum aggregate sampling rate.

The MSDAS-12 has two 100kHz, 12-bit ADCs. In combination, these converters give the MSDAS-12 a 200kHz maximum. The LSDAS-12 has one 100kHz, 12-bit ADC for a maximum aggregate sampling rate of 100kHz.

The LSDAS-16 has one 50kHz, 16-bit ADC for a maximum aggregate sampling rate of 50kHz. The architecture of the HSDAS-16 ADC subsystem is entirely different from that of the other DAS products. However, input multiplexing is similar, thus making the same modes available to the user. This is a 16-bit ADC with an aggregate sampling rate of 200kHz.

The ADCs can be programmed for use in any of five different modes by setting Bits 0, 1, and 2 in the A/D Mode Register (see Section 7.2):

Mode =0: Any one of the sixteen single-ended or eight differential channels can be sampled at the DAS board's maximum rate.

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Mode= 1: Any two of the sixteen single-ended or eight differential channels on a two-channel boundary (i.e.: Channels 1 and 2, 3 and 4, etc., through Channels 15 and 16) can be sampled at a maximum of one-half the board's top speed per channel.

Mode = 2: Any four of the sixteen single-ended or eight differential channels on a four-channel boundary (i.e.: Channels 1-4, 5-8, 9-12, or Channels 13-16) can be sampled at a maximum of one-fourth of the board's top speed per channel.

Mode = 3: Either of the two groups of eight of the sixteen single-ended or all of the eight differential channels on the eight-channel boundary (i.e., either Channels 1-8 or Channels 9-16) can be sampled at a maximum one-eighth of the board's top speed per channel.

Mode = 4: All sixteen channels can be sampled at a maximum of one-sixteenth of the board's top speed per channel.

NOTE
Differential operation requires two input lines per channel; therefore, only eight differential channels can be sampled. This means that differential operation in Mode 4 is illegal.

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6.2 Single-Ended or Differential A/D Inputs

The sixteen analog input lines can be used as sixteen single-ended or eight differential input channels maximum. For single-ended operation, the input channels are grouped as described in Section 6.1. Differential input operation requires two input lines per channel. They are matched as follows:

INPUT CHANNELS Single-Ended	INPUT SIGNALS Differential
Channel 1	Channel 1 High
Channel 2	Channel 2 High
Channel 3	Channel 3 High
Channel 4	Channel 4 High
Channel 5	Channel 5 High
Channel 6	Channel 6 High
Channel 7	Channel 7 High
Channel 8	Channel 8 High
Channel 9	Channel 1 Low
Channel 10	Channel 2 Low
Channel 11	Channel 3 Low
Channel 12	Channel 4 Low
Channel 13	Channel 5 Low
Channel 14	Channel 6 Low
Channel 15	Channel 7 Low
Channel 16	Channel 8 Low

Bit 8 in the A/D Control Register determines the single-ended/differential status of the analog input channels (see Chapter Seven).

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6.3 A/D Input Channel Selection

A/D Mode selection determines how many channels can be sampled (see Section 6.1). Once the number of channels has been determined, the channels themselves must be identified to the DAS. The four least significant bits in the A/D Extended Control Register (Channel Select Bits) determine which channel or group of channels will be sampled. The Channel Select Bits represent the sixteen input channels in binary format. This means that Channel 1 is sampled in Mode 0 by setting the Channel Select Bits to 0, 0, 0, 0. Similarly, Channel 5, in Mode 0 can be sampled by setting the Channel Select Bits to 0, 1, 0, 0.

If Mode 2 is selected, four channels will be sampled. The Channel Select Bits should be set to the lowest channel number in the group. For example, if Channels 5, 6, 7, and 8 are chosen for sampling, the Channel Select Bit should be 5.

A/D MODE 1

Bits 3, 2, 1, 0	Channel
0,0,0,0	1, 2
0,0,1,0	3, 4
:	:
1,1,1,0	15,16

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A/D MODE 2

Bits 3, 2, 1, 0	Channel
0,0,0,0	1, 2, 3, 4
0,1,0,0	5, 6, 7, 8
1,0,0,0	9, 10, 11, 12
1,1,0,0	13, 14, 15, 16

A/D MODE 3

Bits 3, 2, 1, 0	Channel
0,0,0,0	1, 2, 3, 4, 5, 6, 7, 8
1,0,0,0	9, 10, 11, 12, 13, 14, 15, 16

A/D MODE 4

Bits 3, 2, 1, 0	Channel
0,0,0,0	1, 2, 3, 4, 5, 6, 7, 8,
1,0,0,0	9, 10, 11, 12, 13, 14, 15, 16

Output data from the ADCs is transferred to the host computer's memory through a 128-sample FIFO buffer. Transfers to the host can be programmed as Direct Memory Access (DMA) or Programmed I/O (PIO).

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6.4 Unipolar/Bipolar Analog Inputs

Each of the four analog-to-digital converters can be independently programmed to convert a unipolar or bipolar signal. Bits 7, 6, 5, and 4 in the A/D Control Extended Register control the bipolar/unipolar programming of ADC 3, 2, 1, & 0 respectively (see Chapter Seven). Depending on the A/D Mode (see Section 6.1) used, differrent channels are sampled by different ADCs as follows:

A/D MODE 0:

ADC 0, 1, 2 and 3	Any one of all sixteen single-ended channels; OR any one of all eight differential channels.

A/D MODE 1:

ADC 0 and 2	Any one of single-ended Channels 1, 3, 5, 7, 9, 11, 13, or 15; OR any one of differential Channels 1, 3, 5, or 7.
ADC 1 and 3	Any one of single-ended Channels 2, 4, 6, 8, 10, 12, 14, or 16; OR any one of differential Channels 2, 4, 6, or 8.

A/D MODE 2:

ADC 0	Any one of single-ended Channels 1, 5, 9, or 13; OR any one of differential Channels 1 or 5.
ADC 1	Any one of single-ended Channels 2, 6, 10, or 14; OR any one of differential Channels 2 or 6.
ADC 2	Any one of single-ended Channels 3, 7, 11, or 15; OR any one of differential Channels 3 or 7.
ADC 3	Any one of single-ended Channels 4, 8, 12, or 16; OR any one of differential channels 4 or 8.

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A/D MODE 3:

ADC 0	Single-ended Channels 1, then 5 OR 9, then 13; OR differential Channels 1, then 5.
ADC 1	Single-ended Channels 2, then 6 OR 10, then 14; OR differential Channels 2, then 6.
ADC 2	Single-ended Channels 3, then 7, OR 11, then 15; OR differential Channels 3, then 7.
ADC 3	Single-ended Channels 4, then 8, OR 12, then 16; OR differential Channels 4, then 8.

A/DMODE4:

ADC 0	Single-ended Channels 1, then 5, then 9, then 13.
ADC 1	Single-ended Channels 2, then 6, then 10, then 14.
ADC 2	Single-ended Channels 3, then 7, then 11, then 15.
ADC 3	Single-ended Channels 4, then 8, then 12, then 16.

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All unipolar signals must be positive at the input to the ADC. When in unipolar mode, any negative portion of a waveform will be "clipped" and will generate a coded equivalent of 0.

6.5 A/D Converter Pacing and Burst Mode

The DAS boards can be programmed to sample an input waveform at different rates. The term "pacing" refers to the clock signal which tells the A/D converters to sample data. "Pacing" differs from "Triggering," which refers to the signal that tells the A/D subsystem to "remember" the converted data by buffering it through the onboard FIFO.

NOTE

The pacing examples that follow describe the HSDAS-12. If your DAS board is not an HSDAS-12, then the hardware and sampling rates in the following examples might not apply. However, the same theory can be applied to all DAS products.

The A/D pacing signal initiates a conversion of data in the ADCs differently, depending on the A/D Mode. In Modes 0, 1 and 2, all four ADCs are used once each during a sampling cycle, while in Modes 3 and 4, each ADC samples more than one channel during a cycle.

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MODE 0 Pacing Example:
If the end-user is programming the HSDAS-12 to sample Channel 4 at 300kHz, Mode 0 must be chosen. This means that all four ADCs will be sampling Channel 4 in sequence as shown in Figure 6.1. In Mode 0, each of the four ADCs must have its own pacing pulse. So for the 300kHz per channel example, the pacing signal must be programmed for 300kHz.

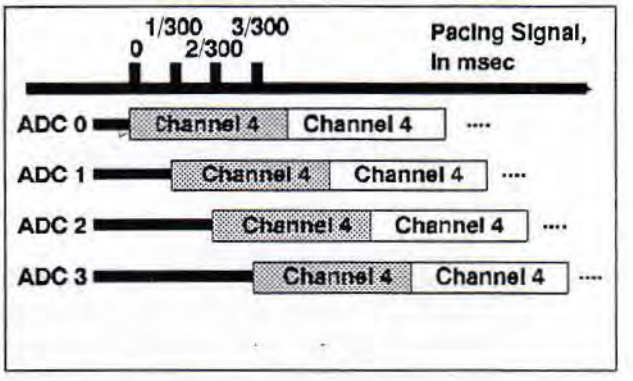


Figure 6.1: A/D Mode 0 Pacing

A/D Mode 1 Pacing Example
The HSDAS-12 can be programmed to sample two channels at a maximum rate of 200kHz. In Mode 1, two ADCs are triggered together, each sampling one of the channels; then the other two ADCs are triggered as shown in Figure 6.2. In this case, Channels 3 and 4 are sampled at 150kHz per channel, and the pacing signal must be programmed at 150kHz.

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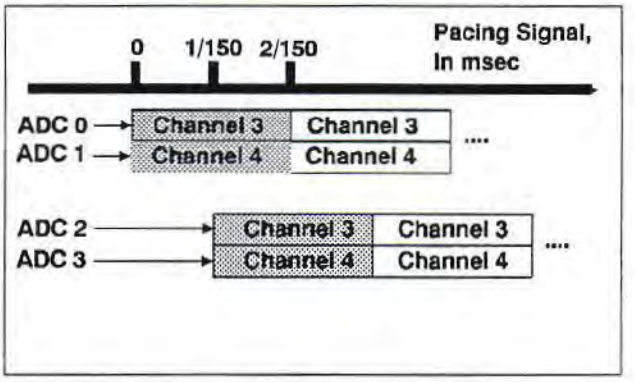


Figure 6.2: A/D Mode 1 Pacing

A/D Mode 2 Pacing Example

Sampling four input channels simultaneously with the HSDAS-12 requires programming the board in Mode 2. In this mode, all four ADCs are triggered together and can sample data at a maximum of 100kHz per channel. Figure 6.3 shows Channels 5, 6, 7, and 8 being sampled at a rate of 80kHz per channel.

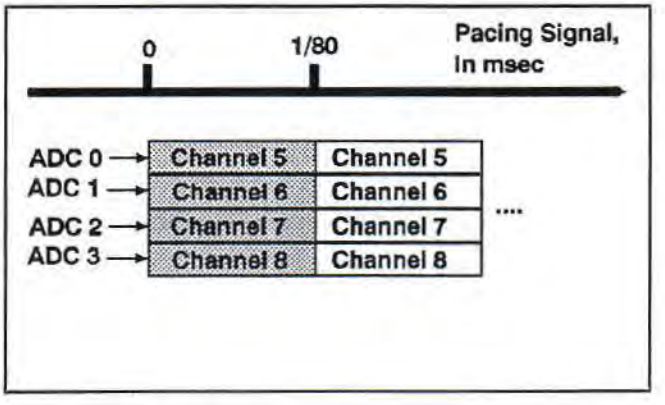


Figure 6.3: A/D Mode 2 Pacing

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A/D Mode 3 Pacing Example:
Since there are only four ADCs, and in Mode 3, eight channels are sampled together, each ADC must sample two channels during a sampling cycle. In Modes 3 and 4, the A/D subsystem samples in "burst mode." This means that one pacing pulse triggers the entire sampling cycle. Each ADC can sample at a maximum rate of 100kHz; therefore, when running in Mode 3 (a burst mode), the maximum pacing frequency for proper operation is 50kHz. Figure 6.4 shows a complete sampling cycle for Mode 3 operation, sampling Channels 1 through 8 at 40kHz per channel. Note that the ADCs take a "burst" of data, then wait for another pacing pulse.

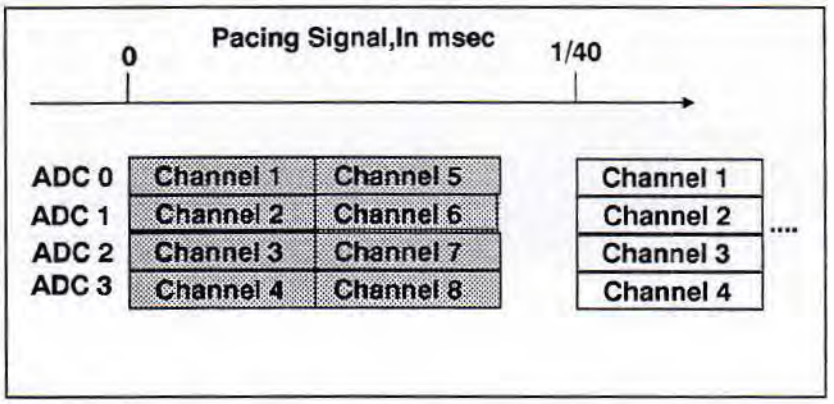


Figure 6.4: A/D Mode 3 Pacing

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Mode 4 Pacing Example:
A/D Mode 4 operation samples all sixteen channels. This means each ADC must sample four different channels during a sampling cycle. As with Mode 3, Mode 4 A/D sampling is in "burst mode," which means that only one pacing pulse is needed to trigger multiple samples for each ADC. Since each ADC can take samples at a maximum of 100kHz, the maximum pacing rate for Mode 4 A/D operation is 25kHz. Figure 6.5 illustrates the sampling configuration for A/D Mode 4 at 20kHz. Again, note that, because the pacing speed is lower than the maximum, the ADCs convert a "burst" of data, then wait for another pacing pulse.

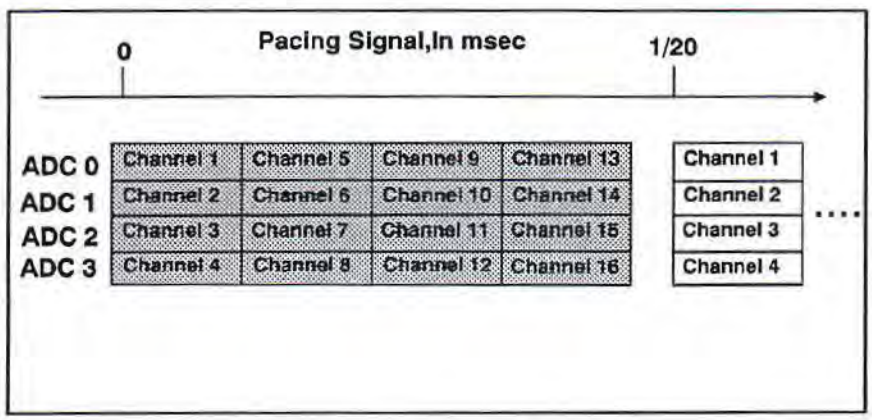


Figure 6.5: A/D Mode 4 Pacing

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6.5.1 Programming On-board A/D Pacing

The on-board A/D pacing signal is programmed by setting Counter-Timer 1, Channel 0 to the appropriate value (see Chapter Eight). The formula for this value is derived by taking the on-board clock speed and dividing it by the required pacing speed:

All DAS-12s: 6.8MHz/Pacing Speed = Counter-Timer Value

All DAS-16s: 5MHz/Pacing Speed = Counter-Timer Value

For example, for a pacing speed of 25kHz, a counter-timer value of 272 is required. This number translates to 0000000100010000 Binary or 0110 Hex.

NOTES:

A/D Mode 0: The smallest number that can be programmed into the pacing counter-timer for proper operation is 17 (decimal), which produces 400kHz.

A/D Mode 1: The smallest number that can be programmed into the pacing counter-timer for proper operation is 34 (decimal), which produces a 200kHz pacing signal.

A/D Mode 2: The smallest legal number for the pacing timer-counter is 68 (decimal), which produces 100kHz.

A/D Mode 3: The smallest legal number for the pacing timer-counter is 136 (decimal), which produces 50kHz.

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A/D Mode 4: The smallest legal number for the pacing timer-counter is 272 (decimal), which produces 25kHz.

6.5.2 Programming External A/D Pacing

Pin 19 on the 26-pin connector, J3 (see Section 1.10), is the input point for the external pacing signal. The DAS boards require an edge-producing TTL signal for external pacing. This must be selected using Bits 3 and 4 in the A/D Mode Register. The direction of the edge must be programmed either positive or negative going, by setting Bit 5 (see Chapter Seven). The external signal provided by the end-user must observe the same frequency constraints as the internal pacing signals described earlier in this section.

6.6 A/D Triggering

Triggering refers to the signal which allows the flow of data from the ADCs into the on-board FIFO. In effect, the triggering signal tells the DAS to "remember" the converted values. There are two types of triggering signals: (1) Software and (2) External. The trigger type is selected by setting Bit 9 in the A/D Mode register (see Chapter Seven).

6.6.1 Software Triggering

Software triggering is achieved by setting the Software Trigger Enable Bit (Bit 13) in the A/D Mode Register (see Chapter Seven). When this bit is 1, sampled data will be strobed into the on-board FIFO. Data will continue to flow into the FIFO until the Software Trigger Enable Bit is reset to 0.

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6.6.2 External Triggering

A/D conversions can be triggered externally. Bits 10 and 11 in the A/D Mode Register program positive or negative, level or edge sensitivity (see Chapter Seven) to connector J1 Pin 26 (see Section 1.10). If the trigger is programmed for level sensitivity, data will flow into the FIFO as long as the trigger signal is at a TTL-compatible high for positive level, or at TTL low for negative level triggering. The flow of data will stop when the satisfying external level is removed. If the external triggering is programmed for edge sensitivity, then the flow of data to the FIFO will begin when the appropriate transition occurs in the external trigger signal and will stop only when the Enable A/D External Trigger Bit (Bit 12 in the A/D Mode Register) is set to 0.

6.7 A/D Pre-/Post-Event Mark

The A/D Event Mark is a mark in the FIFO indicating an event at the time a particular sample was taken. Since the FIFO is 9-bits wide and the sampled data is stored in an 8-bit format, the most significant bit is left free. This bit is used to report an event. There are two types of reportable events selected by Bit 8 in the A/D mode register. The first is the intersection of the "analog" input to ADC0 and a value previously programmed into a specified D/A converter. The second reportable event is the occurrence of a "digital" signal in the external A/D trigger.

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6.7.1 Analog Event Mark Trigger

The Analog Event Mark Trigger compares a value programmed into the DAC specified by Bit 7 in the D/A mode register (see Chapter Seven) to the sampled analog input to ADC0. Section 6.3 describes which input channels are handled by which A/D converters as a function of A/D Mode. Bit 14 in the A/D Mode Register controls the direction of this intersection (see Chapter Seven).

If the Event Mark trigger polarity is programmed as positive edge and DAC0 is selected and programmed to 3.6 volts. then the first time an analog channel being sampled by ADC0 passes through 3.6 volts going up, the report bit will be set to 1. The Enable Analog Event Mark Trigger (Bit 15) and the Enable Event Mark Trigger (Bit 7) must be reset to 0 (clear) and set back to 1 before another report can occur.

6.7.2 External (Digital) Event Mark Trigger

Bit 8 in the A/D mode register set to 0 specifies the External A/D Trigger line (see Section 6.6.2) as the source for the Event Mark Trigger. Using the same bits to program this line as described in Section 6.6.2, an Event Mark can be generated for a positive or negative, level or edge in the External A/D Trigger line. As with Analog Event Mark Trigger, the Enable Event Mark Trigger Bit must be reset to 0 and back to 1 again before another report can be generated.

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CHAPTER SEVEN: Registers

7.0 Overview

DAS boards use sixteen consecutive addresses in the I/O space of the PC/AT bus. The base address is user-adjustable by selecting Address Jumpers as described in Chapter Two. The DAS uses the sixteen address locations as follows:

Address	Read/Write	Register
Base + 0	Rd	A/D Data
	Wr:	DAC0 Data
Base + 2	Wr	DAC1 Data
Base + 4	Wr:	D/A Mode Reg.
Base + 6	Wr:	A/D Mode Reg.
Base + 8	Wr:	Extended Reg.
Base + A Hex	Wr:	Control Reg.
Base + C Hex	Wr:	Interrupt Control Reg.
	Rd:	Status Reg.
Base + E Hex	Rd/Wr:	Digital I/O

7.1 D/A Mode Register

Base Address + 4

The D/A Mode Register is a 16-bit register accessed by writing to the address defined by Base + 4 (see Chapter Five for a discussion of D/A Conversion). Bit 5 in the Control Register is the D/A Mode Reset/Enable. This bit must be set to 1 for the D/A subsystem to operate.

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En U Req DAC1	DAC1 Updat Sel 1	DAC1 Updat Sel 0	DAC1 U Tp Select	En U Req DAC 0	DAC0 Updat Sel 1	DAC0 Updat Sel 0	DAC0 Up Tp Select	Anlg Trgr SrcSel	X	$\overline{DAC}$ En	$\overline{EN}$ CPU	DAC Mode Bit 2	DAC Mode Bit 1	DAC Mode Bit 0	CS
15							8	7							0

Bit 15: Enable Update Request DAC1

0 DAC1 Disable/Clear
1 DAC1 Enable

Bit 15 is reset to 0 at power-up.

Bit 15 is the software update signal for DAC1. Bit 15 is used only when Bit 12 is reset to 0. Bit 15, when set to 1, will cause DAC1 to convert the digital value currently programmed. For another update signal to be issued to DAC1, Bit 15 must be reset back to 0 and set again to 1. If Bit 12 is set to 1 (internal timer), the updating signal for DAC1 will be specified by Bits 14 and 13, and Bit 15 is not used. Resetting Bit 5 in the Control Register will set this bit to 0. Bit 5 in the Control Register must be set to 1 to enable this bit.

Bits 14, 13: DAC1 Update Select

0,0 Timer 1, Channel 1
0,1 A/D Pace Source
1,X Timer 2, Channel 2

Bit 14 is set to 1 at power-up; Bit 13 is reset to 0 at power-up.

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Bits 14 and 13, in combination, specify which internal updating signal for DAC1 is to be used. These two bits are used only when Bit 12 is set to 1. If the combination of Bits 14 and 13 is set to 01, the update signal is the same as the pacing signal for the A/D subsystem. This can be used to synchronize DAC1 and the A/D subsystem. If DAC0 and DAC1 are programmed to be updated from the same timer source (i.e., Timer 1, Channel 1), then updating of the two DACs is synchronized. Clearly, the DACs can be programmed with separate timer sources, which can be used to provide two completely independent waveforms.

Bit 12: DAC1 Update Type Select

0 Asynchronous Update (Software)
1 Internal Timer (selected by Bits 13 and 14)

Bit 12 is reset to 0 at power-up.

Bit 12, when reset to 0, causes DAC1 to convert its programmed digital value to analog each time Bit 15 is set to 1. If Bit 12 is set to 1, the signal that tells DAC1 to convert data comes from an internal timer, which is specified by Bits 14 and 13.

Bit 11: Enable Update Request DAC0

0 DAC0 Disable/Clear
1 DAC0 Enable

Bit 11 is reset to 0 at power-up.

Bit 11 is the software update signal for DAC0. Bit 11 is used only when Bit 8 is reset to 0. Bit 11, when set to 1, will cause the output level of DAC0 to convert the digital value currently programmed. If Bit 8 is set to 1 (internal timer), the updating signal for DAC0 will be specified by Bits 10 and 9, and Bit 11 is not used. Resetting Bit 5 in the Control Register will set this bit to 0. Bit 5 in the Control Register must be set to 1 to enable this bit.

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Bits 10, 9: DAC0 Update Select

0,0	Timer 1, Channel 1
0,1	A/D Pace Source
1,X	Timer 2, Channel 2

Bit 10 is set to 1 at power-up; Bit 9 is reset to 0 at power-up.

Bits 10 and 9, in combination, specify which internal updating signal for DAC0 is to be used. These two bits are used only when Bit 8 is set to 1. If the combination of Bits 10 and 9 is set to 01, the update signal is the same as the pacing signal for the A/D subsystem. This can be used to synchronize DAC0 and the A/D subsystem. If DAC0 and DAC1 are programmed to be updated from the same timer source (i.e., Timer 1, Channel 1), then updating of the two DACs is synchronized. Clearly, the DACs can be programmed with separate timer sources, which can be used to provide two completely independent waveforms.

Bit 8: DAC0 Update Type Select

0	Asynchronous Update (Software)
1	Internal Timer (selected by Bits 9 and 10)

Bit 8 is reset to 0 at power-up.

Bit 8, when reset to 0 causes DAC0 to convert its programmed digital value to analog each time Bit 11 is set to 1. If Bit 8 is set to 1, the signal that tells DAC0 to convert data comes from an internal timer, which is specified by Bits 10 and 9.

Bit 7: Analog Event Mark Trigger Select

0	Event Mark Trigger Level set by DAC0
1	Event Mark Trigger Level set by DAC1

Bit 7 is reset to 0 at power-up.

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The DAS board can be programmed to compare an analog input signal to a value programmed into a DAC. When the analog input signal crosses this programmed value, a mark can be placed in the data buffer so that the input stream of data can be analyzed both before and after the mark (see Chapter Six for a description of Pre- and Post-Event Marking). Bit 7 designates which DAC will be compared with the analog input signal.

Bit 6: Unused

Bit 5: DAC Enable

0 Enable Updating DACs 0 and 1
1 Disable Updating DACs 0 and 1

Bit 5 is reset to 0 at power-up.

Bit 5 enables the D/A converters. **Bit 5 must be reset to 0 for D/A conversion to occur**.

Bit 4: Enable CPU

0 CPU has control of Timer 2 Channels 0 and 1, Gate and Clk

1 RAM Sequencer has control of Timer 2, Channels 0 and 1, Gate and Clk

Bit 4 is reset to 0 at power-up.

When Bit 4 is set to 1, the DAS produces an analog output waveform, or waveforms, independent of the host computer. For this function, optional DAC RAM must be installed and programmed. If Bit 4 is reset to 0, the D/A conversion process is synchronized with the CPU of the host computer. For programming information on internal timers, see Chapter Eight.

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Bits 3, 2, 1: DAC Mode (see Chapter Five)

0,0,0	Mode 0
0,0,1	Mode 1
0,1,0	Mode 2
1,0,0	Mode 4
1,0,1	Mode 5
1,1,0	Mode 6
1,1,1	Mode 7

Bits 3, 2 and 1 are reset to 0 at power-up.

D/A Mode specifies the data source for D/A Conversion and is discussed in Chapter Five.

Bit 0: Channel Select (see Chapter Five)

0 Mode 0, 2, 3, 6 (DAC0 lowest priority);
Mode 4, 5 (DAC0 Read RAM);
Mode 1 (DAC0 DMA).

1 Mode 0, 2, 3, 6 (DAC1 lowest priority);
Mode 4, 5 (DAC1 Read RAM);
Mode 1 (DAC1 DMA).

Bit 0 is reset to 0 at power-up.

Bit 0 specifies the D/A converter with a constant interval between conversions. If Bit 0 is reset to 0, DAC0 will convert its programmed data at a rate exactly equal to its timing rate. This means the time between conversions will remain constant. DAC1, in this case, will convert its data before or after DAC0. On average, DAC1 will also convert its data at a rate equal to its pacing signal; however, there may not be an equal time between each conversion.

If Bit 0 is set to 1, DAC1 will convert with an equal time between each conversion, and, depending on the status of DAC1, DAC0 may have a longer or shorter period of time between each conversion.

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7.2 A/D Mode Register

(Base Address + 6)

The A/D Mode Register is a 16-bit register accessed by writing to the address defined by Base + 6. Bit 7 in the Control Register (see Section 7.3) is the A/D Mode Reset/Enable. This bit must be set to 1 for the A/D subsystem to operate.

En Anl Event Mrk Trgr	Anl Evnt Mrk Trgr Polrty	B/W Trgr En	En A/D Ext Trgr	Ext Trgr Polrty	Ext Trgr Type	Trgr Select	Evt Mrk Trgr Select
15							8

En Evt Mark Trig	S/W Pace	Ext Pace Polrty	A/d Pace Sel 1	A/D Pace Sel 2	A/D Mode Bit 2	A/D Mode Bit 1	A/D Mode Bit 0
7							0

Bit 15: Enable Analog Event Mark Trigger

0 A/D Analog Event Mark Disable/Clr
1 A/D Analog Event Mark Enable

Bit 15 is reset to 0 at power-up.

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The Event Mark is a function that allows the user to mark the A/D data stream so it can be analyzed based on where this mark occurred. An Event Mark is a "1" in the ninth bit of the FIFO at the data sample where the mark occurred. When the data sample with the mark is loaded into the FIFO, Bit 12 in the Status Register is set to 1. When the eight bits indicating the data for that sample are transferred to the host computer, Bit 11 in the Status Register is set to 1, and the DMA process is halted, so the application's software knows the event occurred and can make note of the location of the mark.

An event can be either "analog," which is the intersection of the value of an analog input channel and a preprogrammed value in a D/A converter, or it can be the occurrence of an external TTL signal. If the Event Mark chosen (see Bit 8) is "analog," Bit 15 enables the comparison of the analog input signal to the preprogrammed value in a D/A converter (refer to Section 7.1 for which DAC is chosen by Bit 7 in the D/A Mode Register; Chapter Six describes the Event Mark Function in detail).

Bit 14: Analog Event Mark Trigger Polarity

0 Positive-going
1 Negative-going

Bit 14 is reset to 0 at power-up.

The Event Mark in a data stream can be programmed to occur as an analog input passes through a preprogrammed value in a D/A converter (the DAC used for this is specified by Bit 7 in the D/A Mode Register; refer to Section 7.1). The Event Mark will only occur once and only as the analog input is moving in a specified direction. If Bit 14 is reset to 0, the analog input must have a positive slope as it passes through the preprogrammed value for a mark to be inserted in the data stream. If Bit 14 is set to 1, the analog input must have a negative slope as it passes through the preprogrammed value for a mark to be inserted in the data stream (Chapter Six describes the Event Mark Function in detail).

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Bit 13: Software Trigger Enable

0 Disable
1 Enable

Bit 13 is reset to 0 at power-up.

A/D Trigger enables the flow of converted data to the host computer. If Bit 13 is reset to 0, converted data will not flow to the host computer. If Bit 13 is set to 1, converted data will flow to the host computer. For this function to work, Trigger Select (Bit 9) must be reset to 0.

Bit 12: Enable A/D External Trigger

0 Disable/Clear
1 Enable

Bit 12 is reset to 0 at power-up.

As described for Bit 13, A/D Trigger enables the flow of converted data to the host computer. Bit 12 enables the external A/D Trigger signal. If Bit 12 is reset to 0, the external A/D Trigger signal will have no effect on the flow of data and data will not flow to the host computer. If Bit 12 is set to 1, the external (TTL-compatible) A/D Trigger signal controls the flow of data to the host computer as specified by Bits 11 and 10. For this function to work, Trigger Select (Bit 9) must be set to 1.

NOTE

Chapter Six should be thoroughly reviewed prior to programming A/D conversion.

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Bits 11, 10: External Trigger Polarity, Type (TTL-Compatible)

0,0	Positive Edge
0,1	Positive Level
1,0	Negative Edge
1,1	Negative Level

Bits 11 and 10 are reset to 0 at power-up.

As described for Bits 13 and 12, A/D Trigger enables the flow of data to the host computer. If the External A/D Trigger is to be used, a type and a polarity must be programmed to activate the flow of converted data to the host computer.

If "level" type of A/D Trigger is selected, data will flow to the host computer during the presence of the selected level and will stop flowing when the level is removed. For example, if Bits 11 and 10 are programmed 0 and 1, which indicates positive level triggering, data will flow from the A/D subsystem to the host computer when the External A/D Trigger line is driven to TTL high. Data flow will stop when the External A/D Trigger line is driven to TTL low.

In the case of "edge-sensitive" external A/D triggering, the trigger enable bit (Bit 12) must be reset to 0 for the data flow to stop. For example, if Bits 11 and 10 are set to 1 and 0, which indicates negative edge triggering, data will begin flowing when the External A/D Trigger line moves from TTL high to TTL low. Data will continue to flow until Bit 12 is reset to 0 regardless of what TTL conditions occur on the External A/D Trigger line.

Bit 9: Trigger Select

0	Software
1	External

Bit 9 is reset to 0 at power-up.

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A/D triggering enables the flow of converted data to the host computer. A/D triggering can be through software or through an externally-provided TTL signal. If Bit 9 is reset to 0, A/D triggering will be through software specified by Bit 13. If Bit 9 is set to 1, A/D triggering will be through an external TTL signal as specified by Bits 12, 11, and 10.

Bit 8: Event Mark Trigger Select

0 Digital (External)
1 Analog

Bit 8 is reset to 0 at power-up.

Event marking allows the user to mark the A/D data stream so it can be analyzed based on where the event occurred. A mark in the data stream can be generated by comparing an analog input signal and a value programmed into a D/A converter (see Bits 15, 14, and 7); this is called "Analog Event Mark Triggering" and is specified by setting Bit 8 to 1. The analog channel that is to be used as a trigger must be enabled for storage. The trigger channel is always the first channel to be converted by A/D Converter 0. See Chapter Five for a description of which channels go to which ADCs.

NOTE

Use of the MENUS Program (see Chapter Three) simplifies the selection of the trigger channel and performs all necessary error checking.

Another triggering method for an event mark is called "Digital Event Mark Triggering," which is the occurrence of a TTL event on the External A/D Trigger line. This is the same line used for External A/D Triggering (see Bits 12, 11, and 10). If Bit 8 is reset to 0, an event mark will be inserted in the data sample taken immediately after the event occurs. The external line can be programmed positive level, negative level, or edge-sensitive (see Bits 12, 11, and 10).

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NOTE
If External A/D Triggering is used for A/D conversion, and Digital Event Mark Triggering is used at the same time, the mark will always appear in the first piece of converted data.

If a level type of A/D Trigger is selected (see Bits 11 and 10), an event mark will occur when the selected level appears. For example, if Bits 11 and 10 are programmed to 0 and 1, which indicates positive level triggering, the mark will be inserted when the External A/D Trigger line is driven to TTL high.

In the case of edge-sensitive external A/D triggering, the event mark will be inserted into the data stream when the edge occurs. For example, if Bits 11 and 10 are set to 1 and 0, which indicates negative edge triggering, the mark will occur when the External A/D Trigger line moves from TTL high to TTL low.

NOTE
For Event Mark Triggering to work, Bit 7 and Bit 11 in the Interrupt Control Register must be set to 1.

For multiple event marks in a data stream:

Digital Event Mark Triggering: If additional event marks are to be inserted into the data stream by way of Digital Event Mark Triggering, Bit 7 and Bit 12 (as well as Bit 11 in the Interrupt Control Register) must be reset to 0 and then set back to 1 again before another mark can occur.

Analog Event Mark Triggering: If additional event marks are to be inserted into the data stream by way of Analog Event Mark Triggering, Bit 7 and Bit 15 (as well as Bit 11 in the Interrupt Control Register) must be reset to 0 and then back to 1 again before another mark can occur.

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Bit 7: Enable Event Mark Trigger

0 Disable/Clear
1 Enable

Bit 7 is reset to 0 at power-up.

Bit 7 must be reset to 0, then set back to 1 again before an event mark can be triggered into the data stream.

Bit 6: Software Pace

0 Clear
1 Set

Bit 6 is reset to 0 at power-up.

A/D Pacing tells the A/D converter to convert its analog input. There is only one pacing signal for all four of the A/D converters (HSDAS-12). This signal is cycled through the A/D converters differently, depending on the A/D Mode of operation. (For a detailed description of these modes of operation, see Chapter Six.) There are three types of A/D Pacing signal: Software, Timer, and External.

Selecting Software Pacing (see Bits 4 and 3) allows the user to switch Bit 6 between 0 and 1 to create their own pacing waveform.

NOTE

The circuitry associated with the software pacing pulse (the time at which Bit 6 is set to 1) behaves the same as a "one-shot." This means that the application need not be concerned how long Bit 6 is held at 1.

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Bit 5: External Pace Polarity

0	Positive Edge
1	Negative Edge

Bit 5 is reset to 0 at power-up.

Bits 4, 3: A/D Pace Select

0,0	Power up/Reset
0,1	Software
1,0	Timer
1,1	External

Bits 4 and 3 are reset to 0 at power-up.

A/D Pacing tells the A/D converter to convert its analog input. There is only one pacing signal for all four of the A/D converters (HSDAS-12). This signal is cycled through the A/D converters differently, depending on the A/D Mode of operation. (See Chapter Six for a detailed description of these modes of operation.) Bits 4 and 3 determine the origin of the A/D pacing signal. If Bits 4 and 3 are programmed 0, 1 then A/D pacing is by software (see Bit 6). If Bits 4 and 3 are programmed 1, 0, then the A/D pacing signal originates at Timer 1, Channel 0 (see Chapter Six). If Bits 4 and 3 are programmed 1, 1, then the pacing signal is generated externally and is expected at Pin 19 on the J3 connector (see Section 1.10).

Bits 2, 1, 0: Mode Select

0,0,0	Mode 0
0,0,1	Mode 1
0,1,0	Mode 2
0,1,1	Mode 3
1,0,0	Mode 4

Bits 2, 1, and 0 are reset to 0 at power-up.

A/D Mode selection is subject to numerous criteria. Review Chapter Six thoroughly before making this selection.

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7.3 Control Register

(Base Address + A Hex)
The Control Register is a 16-bit register accessed by writing to the address defined by Base + A Hex.

A/D DMA Start	A/D DMA En	DAC DMA Start	DAC DMA En	Ext. Reg. Dir Control MSB LSB	X	Board Master Reset	A/D Mode Reset	RAM Mode Reset	D/A Mode Reset	Extended Register Address Bit 4 Bit 0
15						8	7			0

Bit 15: A/D DMA Start
0Stop
1Start

Bit 15 is reset to 0 at power-up.

Bit 15 starts the DMA process for the A/D subsystem. If Bit 15 is set to 1, the A/D subsystem will initiate a DMA transfer of data from the onboard FIFO to the host computer's memory. If Bit 15 is reset to 0, the DMA process for the A/D subsystem is halted. (See Chapter Six for a detailed description of this process.)

Bit 14: A/D DMA Request Enable
0 Disable
1 Enable

Bit 14 is reset to 0 at power-up.

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Bit 14 controls the DAS board's ability to request service from the host computer's DMA Controller for the A/D subsystem. Setting up the DMA Controller is a function of the computer's DMA Controller chip and the configuration of the specific host PC. If Bit 14 is set to 1, the DAS can request DMA service from the host computer. (The DMA channel used for this function depends on the DMA Control Jumper setting, which is described in Chapter Two.)

Bit 13: D/A DMA Start

0 Stop
1 Start

Bit 13 is reset to 0 at power-up.

Bit 13 starts the DMA process for the D/A subsystem. If Bit 13 is set to 1, the D/A subsystem will initiate a DMA transfer of data to the DAC holding registers. If Bit 13 is reset to 0, the DMA process for the D/A subsystem is halted. (See Chapter Five for a detailed description of this process.)

Bit 12: D/A DMA Request Enable

0 Disable
1 Enable

Bit 12 is reset to 0 at power-up.

Bit 12 controls the DAS board's ability to request service from the host computer's DMA Controller for the D/A subsystem. Setting up the DMA Controller is a function of the computer's DMA Controller chip and the configuration of the specific host PC. If Bit 12 is set to 1, the DAS can request DMA service from the host computer. (The DMA channel used for this function depends on the DMA Control Jumper setting, which is described in Chapter Two.)

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Bit 11: External Register Direction Control - Most Significant Byte

0 In
1 Out

Bit 11 is reset to 0 at power-up.

Bit 11 controls the direction of the most significant byte of the 16-bit Digital I/O port. If Bit 11 is set to 1, then a write to Base + 0E Hex will go to the MSB of the Digital I/O.

NOTE

The most significant byte of Digital I/O is found on Pins 9, 10, 11, 12, 13, 14, 15 and 16 on the J3 connector. These pins correspond to Digital I/O Bits 8, 9, 10, 11, 12, 13, 14, and 15 respectively.

Bit 10: External Register Direction Control - Least Significant Byte

0 In
1 Out

Bit 10 is reset to 0 at power-up.

Bit 10 controls the direction of the least significant byte of the 16-bit Digital I/O port. If Bit 10 is set to 1, then a write to Base + 0E Hex will go to the LSB of the Digital I/O.

NOTE

The least significant byte of Digital I/O is found on Pins 1, 2, 3, 4, 5, 6, 7 and 8 on the J3 connector. These pins correspond to Digital I/O Bits 0, 1, 2, 3, 4, 5, 6, and 7 respectively.

Bit 9: Unused

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Bit 8: Board Master Reset

0 Reset
1 Enable/Power-up

Bit 8 is set to 1 at power-up.

Bit 8 is the DAS Board Master Reset Bit. This bit must be set to 1 for any portion of the DAS to operate.

NOTE

This bit does not need to be reset to 0 and set back to 1 for any reason. However, if this bit is reset to 0 and then set back to 1 again, all bits in all registers on the DAS will assume their power-up state. This may be useful if the programmer is seeking a normalized state for the whole board.

Bit 7: A/D Mode Reset

0 Reset
1 Enable

Bit 7 is reset to 0 at power-up.

Bit 7 is the Mode Reset Bit for the A/D subsystem. This bit must be set to 1 for proper operation of the A/D Subsystem.

NOTE

If any A/D parameters are to be changed, this bit should be reset to 0 and then set back to 1 after these parameters are changed. These parameters include, but are not limited to, A/D Pacing Type (Bits 4 and 3 in the A/D Mode Register), A/D Trigger Type (Bit 9 in the A/D Mode Register), or Event Mark Trigger Type (Bit 8 in the A/D Mode Register).

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Bit 6: RAM Mode Reset

0 Reset
1 Enable

Bit 6 is reset to 0 at power-up.

Bit 6 is the RAM Mode Reset Bit. This bit must be set to 1 for proper operation of the D/A subsystem when the onboard RAM is to be used.

NOTE

If any parameters are to be changed that involve the use of the onboard RAM, this bit should be reset to 0 and set back to 1 again to normalize the RAM system. For example, if the DAC Mode is set to one that involves the RAM, Bit 6 should be reset to 0, then set back to 1 again. In addition, whenever the DAC Mode is changed or reset involving the DAC RAM, the RAM address timers must be reprogrammed.

Bit 5: D/A Mode Reset

0 Reset
1 Enable

Bit 5 is reset to 0 at power-up.

Bit 5 is the Mode Reset Bit for the D/A subsystem. This bit must be set to 1 for proper operation of the D/A Subsystem.

NOTE

If any D/A parameters are to be changed, this bit should be reset to 0, then set back to 1 after these parameters are changed. These parameters include, but are not limited to, DAC Update Type (Bits 14 and 13, and Bits 10 and 9 in the D/A Mode Register), Analog Event Mark Trigger Select (Bit 7 in the D/A Mode Register), or DAC Mode (Bits 3, 2, and 1 in the D/A Mode Register). In addition, if either of the D/A converters are being run from DAC RAM, the RAM timers must be reprogrammed after a D/A Mode Reset.

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Bits 4, 3, 2, 1, and 0: Extended Register Address

0-3 Hex	A/D Range Control Registers
4-7 Hex	A/D Storage Control Registers
8 Hex	A/D Control Register
C Hex	RAM Control Register

More information on Counter-Timers is found in Chapter Eight.

10 Hex	Timer 1, Channel 0
11 Hex	Timer 1, Channel 1
12 Hex	Timer 1, Channel 2
13 Hex	Timer 1, Control Register
18 Hex	Timer 2, Channel 0
19 Hex	Timer 2, Channel 1
1A Hex	Timer 2, Channel 2
1B Hex	Timer 2, Control Register

Bits 4, 3, 2, 1, and 0 are all reset to 0 at power-up.

The DAS board has an internally extended addressing scheme that affords the board additional registers without consuming additional space in the host computer's I/O plane. By setting Bits 4, 3, 2, 1, and 0, different extended registers are mapped into the board's Base Address + 8. Since these five bits can represent Hex Extended Addresses 0 through 1F Hex, there can be 32 registers located at Base + 8 in the host computer's I/O plane. These 32 address registers are used as described above.

If Bits 4, 3, 2, 1, and 0 are programmed to 0, 0, 0, 0, 0 (which equals 0 Hex), or any values from 0 through 3 Hex, the A/D Range Control Registers can be written to at the Base Address + 8. (A description of the A/D Range Control Registers can be found later in this chapter.)

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If Bits 4, 3, 2, 1, and 0 are programmed to 0, 0, 1, 0, 0 (which equals 4 Hex), or any values from 4 through 7 Hex, the A/D Storage Control Enable Registers can be written to at the Base Address + 8. (A/D Store Enable Registers are described in detail later in this chapter.)

If Bits 4, 3, 2, 1, and 0 are programmed to 0, 1, 0, 0, 0 (which equals 8 Hex), then the A/D Control Register can be written to at the Base Address + 8. (The A/D Control Register is described in detail later in this chapter.)

If Bits 4, 3, 2, 1, and 0 are programmed to 0, 1, 1, 0, 0 (which equals 0C Hex), the RAM Control Register can be written to at the Base Address + 8. (RAM Control Register is described in detail later in this chapter.)

If Bits 4, 3, 2, 1, and 0 are programmed to 1, 0, 0, 0, 0 (which equals 10 Hex) or any values from 10 Hex through 13 Hex, the registers associated with Counter-Timer 1 can be written to or read from at the Base Address + 8. The registers associated with Counter-Timer 2 are accessed by programming Bits 4, 3, 2, 1, and 0 to values from 18 Hex through 1B Hex. (Counter-Timer Registers are described in detail later in this chapter; the Counter-Timer's operation is discussed in Chapter Eight.)

7.4 Interrupt Control

(Base Address + C Hex)

The Interrupt Control Register is a 16-bit register accessed by writing to the address defined by Base + C Hex.

Board Int Mask	En Board Int Mask	En FIFO Ovfl Int	A/D Trg Int Mask	En A/D Trg Int	A/D TC Int Mask	En A/D TC Int	A/D OAV Int Mask	Ext Alm Int Pol	En Ext Alm Int	Ex Ext Ctr Int	Cal Sel	DAC TC Int Mask	En DAC TC Int	En DAC1 Tmr Int	En Dac0 Tmr Int
15							8	7							0

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An interrupt is a "one shot" type of signal. If a state in the DAS can generate an interrupt and the related interrupt is clear, the interrupt line will generate a signal to the host computer's CPU. In addition, the related interrupt status bit in the Status Register of the DAS will be set. At this point, the interrupt cannot occur again until it has been cleared as specified below.

The interrupt signal for any given line can be suppressed (masked). This means that the interrupt line will not signal the CPU. However, the corresponding bit in the Status Register will still be set and, as an interrupt status bit, must be cleared before it can be reissued.

The operation of any interrupt is subject to the proper installation of the Interrupt Level Jumper described in Chapter Two. The placement of this jumper determines which interrupt level the DAS signals the host CPU on. Once the interrupt has occurred, the application software's interrupt driver must poll the Status Register to determine which DAS signal caused the interrupt.

Bit 15: Board Interrupt Mask

0	Mask
1	Enable

Bit 15 is reset to 0 at power-up.

Bit 15 is logically "ANDed" with all other interrupt signals on the DAS. This bit must be set to 1 to allow the host computer's CPU to be interrupted by the DAS. If this bit is reset to 0 and Bit 14 is set to 1, then all interrupt lines are held at their current level. This is useful when a disabling of the interrupt flow is needed. (For example, to service an interrupt, it may be necessary to stop the DAS from interrupting again.)

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Bit 14: Enable Board Interrupt Request

0 Disable
1 Enable

Bit 14 is reset to 0 at power-up.

Bit 14 must be set to 1 for any interrupts to be requested by the DAS. Bit 14 disconnects the interrupt plane on the DAS from the interrupt plane on the host computer. This means that when Bit 14 is reset to 0, the values of the interrupt lines on the host computer are undetermined. To disable the interrupt lines from the DAS while maintaining the values on the lines, leave Bit 14 set at 1, and reset Bit 15 to 0.

Bit 13: Enable FIFO Overflow Interrupt

0 Disable/Clear
1 Enable

Bit 13 is reset to 0 at power-up.

Bit 13 enables or clears the FIFO Interrupt Line. To enable the FIFO Interrupt Line, reset Bit 13 to 0 to clear the FIFO Interrupt Line and Status Bit, then set Bit 13 to 1 to enable the FIFO Overflow Interrupt. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1. The FIFO overflow cannot be masked individually. To mask this signal, the application must mask the whole DAS by using Bit 15. This will inhibit the interrupt transmission while still allowing Bit 13 in the Status Register to be set.

Bit 12: A/D Trigger Interrupt Mask

0 Mask
1 Enable

Bit 12 is reset to 0 at power-up.

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Bit 12 disables the flow of A/D Trigger Interrupt data to the host computer's CPU while still allowing Bit 12 in the Status Register to be set. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1.

Bit 11: Enable A/D Trigger Interrupt

0	Disable/Clear
1	Enable

Bit 11 is reset to 0 at power-up.

Bit 11 clears the A/D Trigger Interrupt. If an A/D Trigger or an A/D Event Mark has occurred, this bit must be reset to 0 and back to 1 to clear the Interrupt Line and Bits 11 and 12 in the Status Register. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1, and Bit 10 must be set to 1 to enable this specific bit.

Bit 10: A/D Terminal Count Interrupt Mask

0	Mask
1	Enable

Bit 10 is reset to 0 at power-up.

If Bit 10 is reset to 0, the only way for an application to be notified of an A/D DMA transfer completion is for the application to poll the Status Register. If Bit 10 is reset to 0, the DMA Terminal Count for A/D data transfer will not generate an interrupt, but will still set Bit 9 in the Status Register. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1.

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Bit 9: Enable A/D Terminal Count Interrupt

0	Disable/Clear
1	Enable

Bit 9 is reset to 0 at power-up.

Bit 9 clears the A/D Terminal Interrupt line and Bit 9 in the Status Register. When this bit is reset to 0, the value of the interrupt is pulled low to 0, and Bit 9 in the Status Register is reset to 0. Bits 9 and 10 must be set to 1 for this interrupt line to activate an interrupt service routine in the host computer. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1.

Bit 8: A/D Data Interrupt Mask

0	Mask
1	Enable

Bit 8 is reset to 0 at power-up.

Bit 8 enables the A/D Data Available Interrupt. If there is data in the A/D subsystem's FIFO and this bit is set to 1, the DAS will generate an interrupt. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1. There is no need to clear this interrupt -- it is cleared automatically when the FIFO data is read.

Bit 7: External Alarm Interrupt Polarity

0	Positive Edge
1	Negative Edge

Bit 7 is reset to 0 at power-up.

Pin 25 on the J1 connector is the External Alarm Interrupt signal; it is an edge-sensitive, TTL-compatible signal. The DAS can be programmed to generate an interrupt on either a rising or a falling edge. Bit 7 selects which edge is used. If Bit 7 is set to 1, an interrupt will be generated on a transition from TTL high to TTL low. If Bit 7 is reset to 0, an interrupt will be generated on a transition from TTL low to TTL high.

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Bits 6, 14, and 15 must all be set to 1 for an interrupt to be generated. After an interrupt has been generated, it must be cleared by resetting Bit 6 to 0 and then setting it back to 1 again to re-enable it. There is no mask facility for the External Alarm Interrupt. If an application requires an External Alarm Interrupt to generate only a status bit setting, the whole DAS-12 must be masked by resetting Bit 15 to 0.

Bit 6: Enable External Alarm Interrupt

0	Disable/Clear
1	Enable

Bit 6 is reset to 0 at power-up.

Bit 6 clears the interrupt line and Bit 6 in the Status Register. Each time an interrupt occurs, this bit must be reset to 0 and back to 1 again before another External Alarm Interrupt can occur. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1.

Bit 5: Enable External Counter Interrupt

0	Disable/Clear
1	Enable

Bit 5 is reset to 0 at power-up.

Bit 5 clears the External Counter Interrupt line and Bit 5 in the Status Register. Each time the externally available counter reaches 0 and this Bit is set to 1, an interrupt is generated. If another interrupt is required, Bit 6 must be reset to 0 and back to 1 again before another External Counter Interrupt can occur. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1.

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Bit 4: Calibration Select

0	A/D Converter
1	D/A Converter

Bit 4 is reset to 0 at power-up.

Bit 4 selects which subsystem is to be calibrated (A/D calibration is discussed in the A/D Control Register Description in Section 7.8). Briefly, A/D offset calibration is accomplished by tying an internal ground signal to the inputs of the A/D converters, converting the signal to digital data and using these values to calibrate future data. A/D gain calibration is accomplished by tying internal reference voltages (2.5V, 5V, and 10V) to the inputs of the A/D converters. These known voltages are converted, and the differences between the results and the reference voltages are used to calibrate future data.

Once the A/D converters have been calibrated, Bit 4 should be switched from 0 to 1 to allow for calibration of the D/A converters.

When Bit 4 is set to 1, the output from the D/A converter selected by Bit 7 in the D/A Mode Register is tied to A/D Channel 0. Programming a value into the D/A converter, and then sampling A/D Channel 0 and applying the calibration constants that were found during the A/D calibration will provide the real output value of the D/A converter. This real value must be compared to the programmed value to calculate a calibration constant for the D/A converter.

Bit 3: D/A Converter Terminal Count Interrupt Mask

0	Mask
1	Enable

Bit 3 is reset to 0 at power-up.

If Bit 3 is reset to 0, the only way for an application to be notified of a D/A DMA transfer completion is for the application to poll the Status Register. If Bit 3 is reset to 0, the DMA Terminal Count for D/A data transfer will not generate an interrupt, but will still set Bit 2 in the Status Register. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1.

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Bit 2: D/A Converter Terminal Count Interrupt

0 Disable/Clear
1 Enable

Bit 2 is reset to 0 at power-up.

Bit 2 clears the D/A Terminal Count Interrupt line and Bit 2 in the Status Register. When this bit is reset to 0, the value of the interrupt is pulled low to 0, and Bit 2 in the Status Register is reset to 0. Bits 2 and 3 must be set to 1 for this interrupt line to activate an interrupt service routine in the host computer. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1.

Bit 1: Enable D/A Converter 1 Timer Interrupt

0 Disable/Clear
1 Enable

Bit 1 is reset to 0 at power-up.

When D/A Converter 1 is programmed to be updated by a signal from a Counter-Timer (see Chapter Four), the selected timer will count down to 0 and generate an update pulse. If Bit 1 is set to 1, when this update pulse comes, the host computer's CPU will be interrupted, and Bit 1 in the Status Register is set to 1. This is useful for synchronizing different aspects in the application. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1. This interrupt cannot be individually masked. If the application needs to use this function by polling Bit 1 in the Status Register, the whole DAS board interrupt structure must be masked by resetting Bit 15 to 0.

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Bit 0: Enable D/A Converter 0 Timer Interrupt

0 Disable/Clear
1 Enable

Bit 0 is reset to 0 at power-up.

When D/A Converter 0 is programmed to be updated by a signal from a Counter-Timer (see Chapter Four), the selected timer will count down to 0 and generate an update pulse. If Bit 0 is set to 1, when this update pulse comes, the host computer's CPU will be interrupted and Bit 0 in the Status Register is set to 1. This is useful for synchronizing different aspects in the application. For this interrupt to be transmitted to the host computer, Bits 15 and 14 must also be set to 1. This interrupt cannot be individually masked. If the application needs to use this function by polling Bit 0 in the Status Register, the whole DAS board interrupt structure must be masked by resetting Bit 15 to 0.

7.5 Status Register

(Base Address + C Hex)

The Status Register is a read-only, 16-bit register accessed by reading the address defined by Base + C Hex.

A/D Type Bit 1	A/D Type Bit 0	FIFO O Flow Int	A/D Event Marker	A/D Marker Int Stat	ADC # Bits	A/D TC Inv Status	A/D DAV Int Stat
15							8

A/D Pacing Status	Ext Alarm Int	Ext Cntr Int	DAC1 Ready	DAC0 Ready	DAC TC Inv Status	DAC1 Timer Int	DAC0 Timer Int
7							0

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Bits 15, 14: A/D Type

0,0	LSDAS
0,1	MSDAS
1,X	HSDAS

Bits 15 and 14 indicate the type of board present. These bits are set at power-up.

Bit 13: FIFO Status

0	No Overflow
1	Overflow

Bit 13 is reset to 0 at power-up.

Bit 13 indicates whether an overflow occurred since the last read of data by the application program. If this bit is read as a 1, data has been lost.

Bit 12: A/D Event Marker

0	No
1	Yes

Bit 12 is reset to 0 at power-up.

Bit 12 is set to 1 when an event mark has been strobed from an A/D converter into the high byte of the A/D holding register. This bit must be cleared before another event can be marked. This is done by resetting Bit 11 in the Interrupt Control Register to 0. The event mark process must be re-enabled by setting Bit 11 in the Interrupt Control Register back to 1 (see Section 7.4).

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Bit 11: A/D Event Marker Interrupt Status

0 Not Read
1 Read

Bit 11 is reset to 0 at power-up.

Bit 11 is set to 1 when an event mark has been read from the DAS. The same mechanism must be used to reset this bit as Bit 12 above.

Bit 10: DAS-12/DAS-16 Identifier

0 12 Bit Converters
1 16 Bit Converters

Bit 10 indicates the type of A/D converters used. When this bit is reset to 0, there are 12-bit A/D converters on board. When this bit is used in conjunction with Bits 15 and 14 above, the maximum speed of the board can be determined. In the case of the HSDAS-12, this bit will be reset to 0 at power-up, and Bits 15 and 14 will be set to 1 and 0 respectively; this indicates a maximum aggregate A/D sampling rate of 400kHz at twelve bits.

Bit 9: A/D Terminal Count Interrupt Status

0 No
1 A/D Terminal Count occurred

Bit 9 is reset to 0 at power-up.

Bit 9 is an indication the DMA processor has finished with A/D data transfer. When Bit 9 is set to 1, A/D transfer of data has completed. For another A/D terminal count signal to be issued, Bit 9 in the Interrupt Control Register must be reset to 0 to clear the Terminal Count Status. Bit 9 in the Interrupt Control Register must be set back to 1 again to enable the A/D Terminal Count Status. When this is done, the DMA controller must be reprogrammed and started again.

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Bit 8: Data Available Interrupt Status

0 No
1 Yes

Bit 8 is reset to 0 at power-up.

Bit 8 indicates that there is data in the A/D subsystem's FIFO that is available for delivery to the host computer. When the application software has read the data, this bit is automatically reset back to 0. As soon as new data is available for delivery, the process begins again.

Bit 7: 16-bit/32-bit Pacing Clock

0 16-bit pacing clock
1 32-bit pacing clock

Bit 7 will monitor the status of Jumper W39. W39 should be installed for the 16-bit pacing clock (factory default), removed for 32-bit pacing clock.

Bit 6: External Alarm Interrupt

0 No
1 Yes

Bit 6 is reset to 0 at power-up.

Bit 6 indicates the occurrence of an external alarm signal. When Bit 6 is set to 1, a signal has been received on the External Alarm Interrupt line (Pin 25 on Connector J1). The external interrupt line is edge-sensitive; whether this is edge-positive or edge-negative is programmed by setting Bit 7 in the Interrupt Control Register. This interrupt status must be reset before another external alarm can be received. This is done by resetting Bit 6 in the Interrupt Control Register to 0 to clear the status. Bit 6 in the Interrupt Control Register must be set back to 1 to enable the process.

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Bit 5: External Counter Interrupt

0 No
1 Yes

Bit 5 is reset to 0 at power-up.

Bit 5 indicates the occurrence of a zero count in the externally available counter. When Timer 1/ Channel 2 goes to 0, Bit 5 is set to 1. For another External Counter Interrupt to occur, Bit 5 in the Interrupt Control Register must be reset to 0 to clear the bit; then it must be reset to 1 again to enable the External Counter Interrupt Bit again.

Bit 4: D/A Converter 1 Ready

0 Not Ready
1 Ready

Bit 4 is set to 1 at power-up.

D/A converters need some finite amount of time to set their output level to the value programmed at their input. This time is called "settling time." The settling time for the D/A converters on the DAS is specified as follows:

It takes no longer than 5 microseconds for the D/A Converters to settle to within 0.01% of the programmed output value.

Bit 4 indicates the settling status for DAC1. If Bit 4 is zero, the output of DAC1 has not settled to its new value. When Bit 4 goes to 1, the data at the output of DAC1 is ready to be read. This bit moves between 0 and 1 automatically, based on the DAC1 update signal (see Chapter Five).

Bit 3: D/A Converter 0 Ready

0 Not Ready
1 Ready

Bit 3 is set to 1 at power-up.

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D/A converters need some finite amount of time to set their output level to the value programmed at their input. This time is called "settling time." The settling time for the D/A converters on the DAS-12 is specified as follows:

It takes no longer than 5 microseconds for the D/A converters to settle to within 0.01% of the programmed output value.

Bit 3 indicates the settling status for DAC0. If Bit 3 is 0, the output of DAC0 has not settled to its new value. When Bit 3 goes to 1, the data at the output of DAC0 is ready to be read. This bit moves between 0 and 1 automatically, based on the DAC0 update signal (see Chapter Five).

Bit 2: D/A Converter Terminal Count Interrupt Status

0 No
1 D/A Terminal Count occurred

Bit 2 is reset to 0 at power-up.

Bit 2 is an indication that the DMA processor has finished with D/A data transfer. When Bit 2 is set to 1, D/A transfer of data is complete. For another D/A terminal count signal to be issued, Bit 2 in the Interrupt Control Register must be reset to 0 to clear the Terminal Count Status. Bit 2 in the Interrupt Control Register must be set back to 1 again to enable the D/A Terminal Count Status.

Bit 1: D/A Converter 1 Timer Interrupt

0 No
1 Yes

Bit 1 is reset to 0 at power-up.

When D/A Converter 1 is programmed with a timer as an update source (Timer 1, Channel 1; or Timer 2, Channel 2), the selected timer counts down to 0 and generates an update pulse. When this pulse occurs, it is recorded in Bit 1. For another update pulse to be issued to DAC1, Bit 1 in the Interrupt Control Register must be reset to 0 and set back to 1 again to clear and re-enable the DAC1 Timer Interrupt Bit.

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Bit 0: D/A Converter 0 Timer Interrupt

0 No
1 Yes

Bit 0 is reset to 0 at power-up.

When D/A Converter 0 is programmed with a timer as an update source (Timer 1, Channel 1; or Timer 2, Channel 2), the selected timer counts down to 0 and generates an update pulse. When this pulse occurs, it is recorded in Bit 0. For another update pulse to be issued to DAC0, Bit 0 in the Interrupt Control Register must be reset to 0 and set back to 1 again to clear and re-enable the DAC0 Timer Interrupt Bit.

7.6 Range Control Registers

(Base + 8 and Extended Register = 00 Hex)

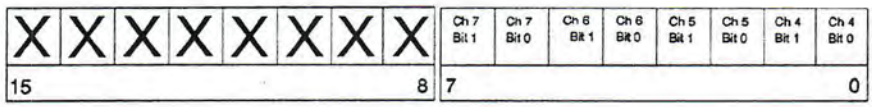
A/D Range Control Register 1:

X	X	X	X	X	X	X	X	Ch 3 Bit 1	Ch 3 Bit 0	Ch 2 Bit 1	Ch 2 Bit 0	Ch 1 Bit 1	Ch 1 Bit 0	Ch 0 Bit 1	Ch 0 Bit 0
15							8	7							0

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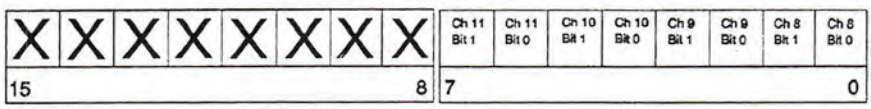
(Base + 8 and Extended Register = 01 Hex)

A/D Range Control Register 2:



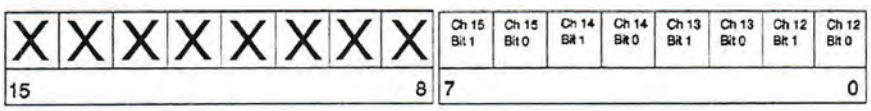
(Base + 8 and Extended Register = 02 Hex)

A/D Range Control Register 3:



(Base + 8 and Extended Register = 03 Hex)

A/D Range Control Register 4:



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The power-up states for these registers are undefined. This means that the Range Control Register Bits for all A/D input channels to be used must be programmed after each power-up.

As indicated in the diagrams above, each A/D input channel has two corresponding bits in a Range Control Register. Each pair of bits corresponds to one channel's range selection. For example, for A/D Input Channel 6, Bits 5 and 4 in A/D Range Control Register 2 control the input range as follows:

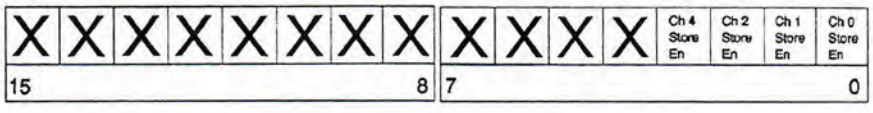
Example

Bits 5, 4:	A/D Channel 6 Input Range Control	
0, 0	0	→ 2.5 Volts Unipolar
	-2.5	→ 2.5 Volts Bipolar
0, 1	0	→ 5.0 Volts Unipolar
	-5.0	→ 5.0 Volts Bipolar
1, X	0	→10.0 Volts Unipolar
	-10.0	→10.0 Volts Bipolar

7.7 Storage Control Registers

(Base + 8 and Extended Register = 04 Hex)

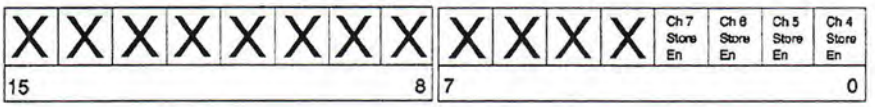
A/D Storage Control Register 1:



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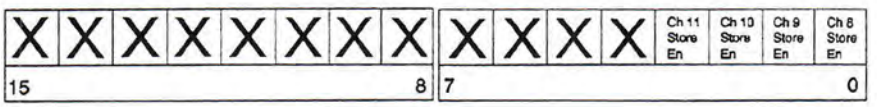
(Base +8 and Extended Register = 05 Hex)

A/D Storage Control Register 2:



(Base + 8 and Extended Register = 06 Hex)

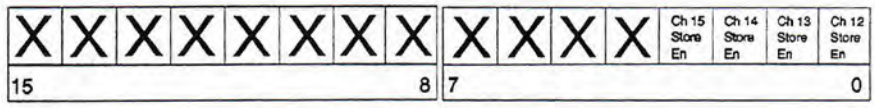
A/D Storage Control Register 3:



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(Base + 8 and Extended Register = 07 Hex)

A/D Storage Control Register 4:



The power-up states for these registers are undefined. This means the Storage Control Register Bits for all A/D input channels to be used must be programmed after each power-up.

As indicated in the diagrams above, each A/D input channel has one corresponding bit in a Storage Control Register. The bit corresponding to each channel to be used must be set to 1 to enable storage of the converted data for that channel. If the bit corresponding to a given channel is reset to 0, then the converted data will not be passed on to the FIFO and will not get stored in the host computer's memory.

NOTE
If Analog Triggering is to be used by the application, the channel used for triggering must be enabled for storage.. (See Chapter Six for more on triggering.)

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7.8 A/D Control Register

(Base + 8 Hex and Extended Register = 8)
The A/D Control Register is a 12-bit register accessed by writing to the address defined by Base + 8 Hex. This extended register is selected when the five least significant bits of the Control Register (Section 3.3) are set to 01000 Binary (8 Hex). (See Section 7.3 for more on Extended Registers.)

Bit 7 in the Control Register is the A/D Mode Reset/Enable. This bit must be set to 1 for the A/D subsystem to operate. (See Chapter Six for a detailed discussion of A/D Conversion.)

X	X	X	X	Cal / Run	Zero / Gain	Con Reset	S-End / Diff	Uni / Bipol Ch 3	Uni / Bipol Ch 2	Uni / Bipol Ch 1	Uni / Bipol Ch 0	Ch 3	Ch 2	Ch 1	Ch 0
15							8	7							0

Bit 11: A/D Calibrate/Run
0 Enable Calibrate
1 Enable Run

Bit 11 is reset to 0 at power-up.

Bit 11 switches the A/D subsystem between Calibrate and Run Modes. Through software it is possible to generate two calibration constants, which can be used to correct any errors in data that may occur. The DAS is designed with a built-in constant offset and gain error. This way, if the A/D converters drift over time, the calibration constants will always be negative.

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Offset calibration is done by resetting Bit 11 to 0 and resetting Bit 10 to 0. This causes ground to be forced into the input of each A/D converter. When this ground signal is converted, it will not result in a 12-bit value of 0; the negatives of the resulting values (one value for each converter) are the calibration constants. These values are used by whatever application software may be controlling the DAS.

Gain calibration is done by resetting Bit 11 to 0 and setting Bit 10 to 1. This causes a reference voltage equal to the range selected to be forced to the input of each A/D converter. For example, if the A/D converter is programmed for a 5V range, a 5V reference will be forced to the input of each A/D converter. This input is converted, and the value at the output represents the reference voltage multiplied by the gain. There is one value for each A/D converter. These values are used by the applications software to calibrate future data.

NOTES

1. Calibration constants must be generated for each range value used. If an application is going to use a 5V and a 10V range (unipolar and bipolar have the same calibration constants), calibration constants must be generated in both 5V and 10V modes.

2. A/D calibration also requires that Bit 4 in the Interrupt Control Register be reset to 0.

3. The HSDAS-16 A/D subsystem is different from the other DAS boards. In order to calibrate the HSDAS-16 correctly, the board must be set up for A/D Input Type; single-ended (see Bit 8) and Channel 8 must also be selected (see Bits 3, 2, 1, and 0).

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Bit 10: A/D Calibration Type

0 Calibrate A/D Offset
1 Calibrate A/D Gain

Bit 10 is reset to 0 at power-up.

Bit 10 selects the calibration constant that is to be generated. If Bit 10 is reset to 0, the A/D offset constants are to be generated. If Bit 10 is set to 1, the A/D gain constants are to be generated.

Bit 9: A/D $\overline{\text{CONRST}}$

0 Reset A/D Converters
1 Enable A/D Converters

Bit 9 is set to 0 at power-up.

Bit 9, when reset to 0, resets the A/D converters. When Bit 9 is set to 1, the A/D converters are enabled for conversion. This bit must be set to 1 for A/D conversion of any type to occur.

NOTE

1. A/D converters should only be reset immediately before a calibration is performed. The act of resetting the converters can itself effect calibration, and therefore can change the calibration constants.

2. A 0.5 second delay is required for A/D converter reset.

Bit 8: A/D Type

0 Single-Ended
1 Differential

Bit 8 is set to 0 at power-up.

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Bit 8 selects the analog input type that will be used. All A/D converters must run with the same type. If Bit 8 is reset to 0, the A/D subsystem will accept sixteen single-ended inputs. If Bit 8 is set to 1, the A/D subsystem will accept eight differential inputs. Pinouts for these different input modes are described in the diagram in Section 1.10.

Bit 7: Unipolar/Bipolar Converter 3

0 Unipolar
1 Bipolar

Bit 7 is reset to 0 at power-up.

If Bit 7 is reset to 0, then A/D Converter 3 is run in unipolar mode. This means all values below 0V that appear at the input of A/D Converter 3 will be clipped and converted to a value of 0. If Bit 7 is set to 1, A/D Converter 3 will accept bipolar waveforms at the input. (See Chapter Six for a detailed description of which input channels go to which A/D converters.)

NOTE

1. If the input waveform is out of range, the converted data will be clipped.

2. HSDAS-12 only (4 ADCs).

Bit 6: Unipolar/Bipolar Converter 2

0 Unipolar
1 Bipolar

Bit 6 is reset to 0 at power-up.

If Bit 6 is reset to 0, A/D Converter 2 is run in unipolar mode. This means all values below 0V that appear at the input of A/D Converter 2 will be clipped and converted to a value of 0. If Bit 6 is set to 1, A/D Converter 2 will accept bipolar waveforms at the input. (See Chapter Six for a detailed description of which input channels go to which A/D converters.)

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NOTE

1. If the input waveform is out of range, the converted data will be clipped.

2. HSDAS only (4 ADCs).

Bit 5: Unipolar/Bipolar Converter 1

0 Unipolar
1 Bipolar

Bit 5 is reset to 0 at power-up.

If Bit 5 is reset to 0, A/D Converter 1 is run in unipolar mode. This means all values below 0V that appear at the input of A/D Converter 1 will be clipped and converted to a value of 0. If Bit 5 is set to 1, A/D Converter 1 will accept bipolar waveforms at the input. (See Chapter Six for a detailed description of which input channels go to which A/D converters.)

NOTE

1. If the input waveform is out of range, the converted data will be clipped.

2. HSDAS-12 (4 ADCs) and MSDAS-12 (2 ADCs).

Bit 4: Unipolar/Bipolar Converter 0

0 Unipolar
1 Bipolar

Bit 4 is reset to 0 at power-up.

If Bit 4 is reset to 0, A/D Converter 0 is run in unipolar mode. This means all values below 0V that appear at the input of A/D Converter 0 will be clipped and converted to a value of 0. If Bit 4 is set to 1, A/D Converter 0 will accept bipolar waveforms at the input. (See Chapter Six for a detailed description of which input channels go to which A/D converters.)

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NOTE
If the input waveform is out of range, the converted data will be clipped.

Bits 3, 2, 1, 0: Channel Select
In binary code, these bits select the input channel (or first channel in the input group). For example, if only Channel 14 is being sampled, Bits 3, 2, 1, and 0 should be set at 1, 1, 0, and 1 (D Hex), respectively. If a group of channels is being sampled (i.e., Channels 5, 6, 7, and 8), Bits 3, 2, 1, and 0 should be set at 0, 1, 0, and 0.

NOTE
Channels 1-16 are represented by Hex Codes 0-F. Strict attention must be paid to the conversion.

Channels Selected in Single-ended Mode

Bits 3, 2, 1, 0	Mode 0	Mode 1	Mode 2 Channels	Mode 3	Mode4
0000	1	1- 2	1- 4	1- 8	1-16
0001	2	1- 2	1- 4	1- 8	1-16
0010	3	3- 4	1- 4	1- 8	1-16
0011	4	3- 4	1- 4	1- 8	1-16
0100	5	5- 6	5- 8	1- 8	1-16
0101	6	5- 6	5- 8	1- 8	1-16
0110	7	7- 8	5- 8	1- 8	1-16
0111	8	7- 8	5- 8	1- 8	1-16
1000	9	9-10	9-12	9-16	1-16
1001	10	9-10	9-12	9-16	1-16
1010	11	11-12	9-12	9-16	1-16
1011	12	11-12	9-12	9-16	1-16
1100	13	13-14	13-16	9-16	1-16
1101	14	13-14	13-16	9-16	1-16
1110	15	15-16	13-16	9-16	1-16
1111	16	15-16	13-16	9-16	1-16

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Channels Selected in Differential Mode

Bits 3,2, 1, 0	Mode 0 Channels	Mode 1 Channels	Mode 2 Channels	Mode 3 Channels
0000	1	1-2	1-4	1-8
0001	2	1-2	1-4	1-8
0010	3	3-4	1-4	1-8
0011	4	3-4	1-4	1-8
0100	5	5-6	5-8	1-8
0101	6	5-6	5-8	1-8
0110	7	7-8	5-8	1-8
0111	8	7-8	5-8	1-8

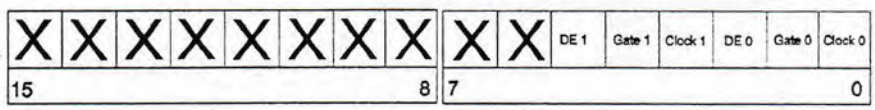
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7.9 RAM Control Register

(Base + 8 Hex and Extended Register = 0C Hex)

The RAM Control Register is a 6-bit register accessed by writing to the address defined by Base + 8 Hex. This extended register is selected when the five least significant bits of the Control Register (Section 7.3) are set to 01100 Binary (0C Hex). For more on extended registers, see Section 7.3.

Bit 6 in the Control Register is the RAM Mode Reset/Enable. This must be set to 1 for the D/A subsystem to operate from RAM. (See Chapter Five for a detailed discussion of D/A Operation.)



NOTE
All of the bits described in this section are valid for use only when Bit 4 (EN CPU) is reset to 0.

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Bit 5: Delay DAC 1 Update

0 Disable/Clear DAC1 Update Delay
1 Enable DAC1 Update Delay

Bit 5 is reset to 0 at power-up.

Counter-Timer 2/Channel 1 can be programmed to count down a value to 0 before DAC1 will accept an update signal. This is useful for inserting a delay between the waveforms from the two DACs. If Bit 5 is set to 1, Counter-Timer 2/Channel 1 will count down the value programmed in it before enabling the update signal to D/A Converter 1. If Bit 5 is reset to 0, the delay count is disabled, and DAC1 is updated immediately when an update signal is programmed.

Bit 4: Gate 1 (Timer 2, Channel 1)

0 Disable
1 Enable

Bit 4 is reset to 0 at power-up.

Bit 4 controls the Gate signal for Counter-Timer 2/ Channel 1. If Bit 4 is reset to 0, then the clock signal for Counter-Timer 2/Channel 1 is disabled and it will not count. This means no delay can be programmed for DAC1 (see Bit 5), and DAC1, running from on-board RAM, will have a constant output as the RAM address will not increment (see Chapter Five).

Bit 3: Clock 1

0 Off
1 On

Bit 3 is reset to 0 at power-up.

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Bit 3 is the clock signal for Counter-Timer 2/ Channel 1. This clock signal controls the updating of the count value in this channel. (See Chapter Eight for a detailed description of Counter-Timer Operation.) When writing a count to each of the counter channels in the 82C54 Counter-Timers, the application actually writes to a holding register, not the counting element. For DAC1, when writing an address to the RAM counter (Timer 2, Channel 1), Bit 4 (Gate 1) must be reset to 0 to disable the counter, and Bit 0 must be reset to 0 to initialize the clock signal. A count value must be written to the counter (actually the holding register), and Gate 1 is now set to 1 to allow the clocking of the counter. One clock pulse should be generated by setting Bit 3 to 1 and then resetting it to 0 again to strobe the value from the holding register to the counting element. The counter is now ready for RAM operation of the DAC.

Bit 2: Delay DAC 0 Update

0 Disable/Clear DAC0 Update Delay
1 Enable DAC0 Update Delay

Bit 2 is reset to 0 at power-up.

Counter-Timer 2/Channel 0 can be programmed to count down a value to 0 before DAC0 will accept an update signal. This is useful for inserting a delay between the waveforms from the two DACs. If Bit 2 is set to 1, Counter-Timer 2/Channel 0 will count down the value programmed in it before enabling the update signal to DAC0. If Bit 2 is reset to 0, the delay count is disabled and D/A converter 0 is updated immediately when an update signal is programmed.

Bit 1: Gate 0 (Timer 2, Channel 0)

0 Disable
1 Enable

Bit 1 is reset to 0 at power-up.

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Bit 1 controls the Gate signal for Counter-Timer 2/ Channel 0. If Bit 1 is reset to 0, then the clock signal for Counter-Timer 2/Channel 0 is disabled and it will not count. This means no delay can be programmed for DAC0 (see Bit 2), and it means that DAC0, running from onboard RAM, will have a constant output as the RAM address will not increment (see Chapter Five).

Bit 0: Clock 0

0	Off
1	On

Bit 0 is reset to 0 at power-up.

Bit 0 is the clock signal for Counter-Timer 2/ Channel 0. This clock signal controls the updating of the count value in this channel. (See Chapter Eight for a detailed description of the Counter-Timer Operation.)

When writing a count to each of the counter channels in the 82C54 Counter-Timers, the application actually writes to a holding register, not the counting element. For DAC0, when writing an address to the RAM counter (Timer 2, Channel 0), Bit 1 (Gate 0) must be reset to 0 to disable the counter, and Bit 0 must be reset to 0 to initialize the clock signal. A count value must be written to the counter (actually the holding register), and Gate 1 is now set to 1 to allow clocking of the counter. One clock pulse should be generated by setting Bit 0 to 1 and then resetting it to 0 again to strobe the value from the holding register to the counting element. The counter is now ready for RAM operation of the DAC.

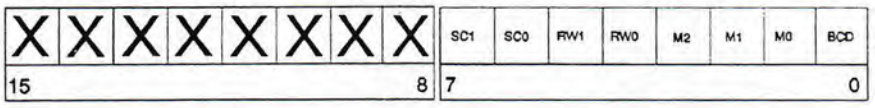
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7.10 Counter-Timer Registers

7.10.1 Counter-Timer Control Word

(Base + 8 and Extended Register = 13 Hex, Timer 1 or 1B Hex, Timer 2)

Each of the two groups of counter-timers has its own control word. This word uses only the least significant byte. The state of each bit in these registers is undetermined at power-up. This means the counter-timers must be programmed at each use. In addition, each time any mode that uses the counter-timers is changed, the counter-timers involved must be reprogrammed. (Review Chapter Eight before programming the counter-timers.)



Bits 7, 6: Select Counter

0, 0	Select Counter 0
0, 1	Select Counter 1
1, 0	Select Counter 2
1, 1	Read-Back Command (see Chapter Eight)

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There are three independent counters in each timer. Bits 7 and 6 designate which counter is to be operated on (see Chapter Eight).

Bits 5, 4: Read/Write

0, 0	Counter Latch Command (see Chapter Eight)
0, 1	Read/Write (least significant byte only)
1, 0	Read/Write (most significant byte only)
1, 1	Read/Write (least significant byte, then most significant byte)

Bits 5 and 4 can be used to latch the current count in the into the Output Latch (see Chapter Eight), or these two bits can be used to request a special format in the read/write order of data.

Bits 3, 2, 1: Counter Mode

0, 0, 0	Mode 0
0, 0, 1	Mode 1
X, 1, 0	Mode 2
X, 1, 1	Mode 3
1, 0, 0	Mode 4
1, 0, 1	Mode 5

Counter-Timer Modes are fully described in Chapter Eight.

NOTE

Mode 2 should always be used for A/D pacing and DAC updating.

Bit 0: BDC Flag

0	Binary Counter (16 bits)
1	Binary Coded Decimal

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Each of the three counters in each of the two timers on the DAS can be set as a BCD counter or a normal binary counter. Resetting Bit 0 to 0 configures the counter indicated by Bits 7 and 6 to be a binary counter. Setting Bit 0 to 1 configures the counter to a BCD counter.

7.10.2 Counter-Timer Count Registers

Counter/Timer Data		Counter/Timer Data	
Bit 15	Bit 8	Bit 7	Bit 0
15	8	7	0

(Base + 8 and Extended Register = 10-1F Hex)

The power-up state for each of these registers is undetermined. This means that each counter used in any subsystem of the DAS12 must be programmed before it can be used.

There are two groups of three 16-bit Counter-Timer Registers. They are: Timer 1, Channels 0 through 2; and Timer 2, Channels 0 through 2. Each of the count registers contains the count number for the corresponding counter-timer and can be accessed by writing to the board's Base Address + 8 when the Extended Register Address is set as described in Section 7.3 (Bits 0-4). The mode for each counter must be preprogrammed (see Section 7.10.1). Based on the selection of the Read/Write Mode, the count must be written to the individual counter in a certain sequence of bytes (see Chapter Eight for more details).

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CHAPTER EIGHT: The 82C54 Counter-Timers

8.0 Overview

The DAS board has two Intel 82C54 timers, each with three channels, used as follows:

- o Timer 1/Channel 0: A/D pacing
- o Timer 1/Channel 1: D/A update signal
- o Timer 1/Channel 2: Externally available
- o Timer 2/Channel 0: RAM Address DAC0
- o Timer 2/Channel 1: RAM Address DAC1
- o Timer 2/Channel 2: D/A update signal

These timers are programmed through registers accessed by reading or writing to the board's Base Address + 8, with the Extended Register Address set as shown in Chapter Seven. Since the two timers as well as the three channels within each timer are identical, only one channel in one timer will be functionally described.

The following is paraphrased from the Microprocessor and Peripheral Handbook (Volume II: Peripheral), copyright INTEL CORPORATION 1988.

8.1 82C54 Counter-Timer Functional Description

8.1.1 General

The 82C54 is a programmable interval counter-timer. It solves one of the most common problems in any microcomputer system -- that is, the generation of accurate time delays under software control. The following are some other counter-timer functions, common to microcomputers, that can be implemented with the 82C54:

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- Real-time clock
- Event counter
- Digital "oneshot"
- Programmable rate generator
- Squarewave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

8.1.2 Counter-Timer Control Register

The Control_Register for the 82C54 is accessed by writing to the DAS board Base_Register_+_8 when the Extended_Register_Address is set at 13 Hex (for Timer 1), or when the Extended Register Address is set to 1B Hex (for Timer 2). The data written to this address is stored in the Control_Word_Register in the 82C54 and is interpreted as the Control_Word used to define the operation of the counters.

The Control Word Register can only be written to.

8.1.3 Counters 0, 1, and 2

The counters are fully independent: each may operate in a different mode.

The Control Word Register is not part of the counter itself, but its contents determine how the counter operates.

The **Status Register** (Figure 8.1), when latched, records the contents of the Control Word Register and the status of the **Output and Null Count Flag**.

Inside the 82C54, the actual counting element is a 16-bit presettable synchronous down-counter.

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Output latches are 8-bit latches, which normally follow the counting element. However, if a suitable counter latch command is sent to the 82C54, the output latches "remember" the present count until read by the CPU and then return to following the counting element. One latch is enabled at a time by the control logic to drive the internal bus. This is how the 16-bit counter communicates over the 8-bit internal bus. Note that the counting element itself cannot be read: whenever reading the count, it is the output latches that are read.

Similarly, there are two 8-bit registers called **Count Registers**. When a new count is written to the counter, it is stored in the Count Register and later transferred to the **Counting Element**. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the Counting Element simultaneously. Both count registers are cleared when the counter is programmed, so if the counter is programmed with only a 1-byte count, the other byte will be 0. Note that the Counting Element cannot be directly written to; whenever a count is written, it is written to the Count Register.

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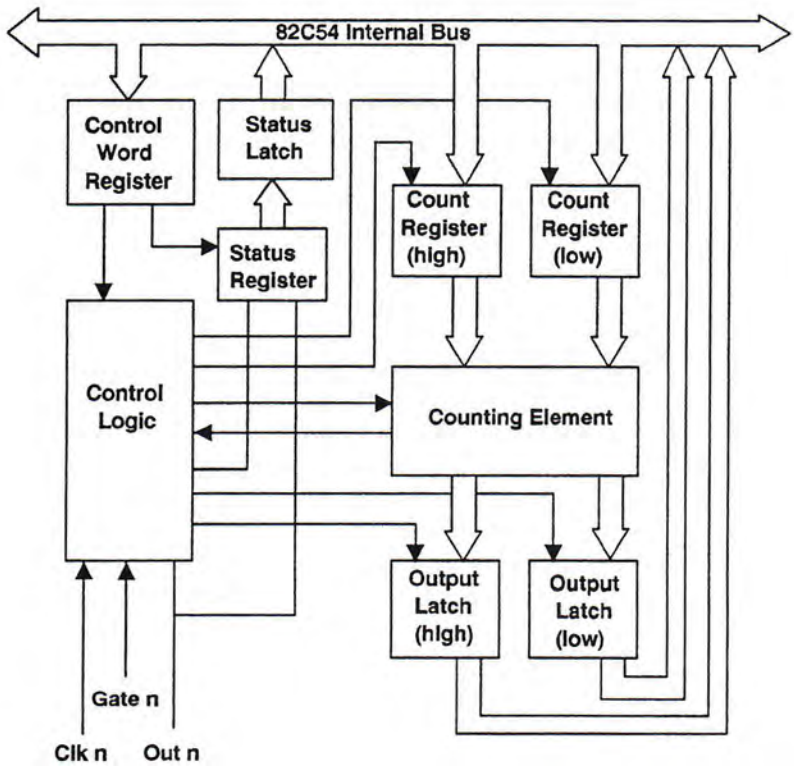


Figure 8.1: 82C54 Timer Block Diagram

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8.2 82C54 Operational Description

8.2.1 General

After power-up, the state of the 82C54 Timer is undefined. The mode, count value, and output of all counters are undefined. The operation of each counter is determined when it is programmed. Each counter must be programmed before it can be used. Unused counters need not be programmed.

8.2.2 Programming the 82C54

Counters are programmed by writing a Control Word and an Initial Count (Control Word Format is described in Chapter Seven). Control words determine which counter is being programmed. Once the Control Word has been programmed, initial counts are programmed for each counter by writing to the counter register's address (described in Chapter Seven). The format of the initial count is determined by the control word used.

8.2.3 82C54 Write Operations

The programming for the 82C54 is very flexible. Only two conventions need to be remembered:

1. For each counter, the Control Word must be written before the initial count is written.

2. The Initial Count must follow the Count Format specified in the Control Word (least significant byte only, most significant byte only; or least significant byte, then most significant byte).

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Since the Control Word register and the counters have separate addresses and each control word specifies the counter it applies to (SC0, SC1), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a counter at any time without affecting the counter's programmed mode in any way. Counting will be affected as described in the Timer Mode Definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write 2-byte counts, the following precaution applies: a program must not transfer control between writing the first and second byte to another routine that also writes into the same counter. Otherwise, the counter will be loaded with an incorrect count.

8.2.4 82C54 Read Operations

It is often desirable to read the value of a counter without disturbing the count in progress. There are three possible methods for reading the counters: a simple Read Operation; the Counter Latch Command; and the Readback Command. Each is explained below.

Read Operation

The first method is to perform a simple Read Operation. To read the counter accessed by the address specified in the Extended Register Address (see Chapter Seven), the CLK input of the selected counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

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Counter Latch Command

The second method for reading the counter uses the "Counter Latch Command." Like a Control Word, this command is written to the Control Word Register, which is selected by setting the Extended Control Register Address to either 13 Hex or 1B Hex and writing to the DAS board's Base Address + 8. Also, like a Control Word, the Bits SC0 and SC1 select one of the counters, but Bits 4 and 5 in the Counter-Timer Control Word distinguish the Counter Latch Command from the Control Word.

The selected counter's output latch "remembers" the count at the time the Counter Latch Command is received. The count is held in the latch until it is read (or until the counter is reprogrammed). The count is then unlatched automatically, and the output latch returns to "following" the counting element. This command allows the reading of the counters on-the-fly without affecting counting in progress. Multiple counter latch commands may be used to latch more than one counter. Each counter's output latch holds its value until it is read. Counter latch commands do not affect the programmed mode of the counter in any way.

If a counter is latched and, some time later, latched again before the count is read, the second counter latch command is ignored. The count read will be the count latched at the time the first counter latch command was issued. With either method, the count must be read according to the programmed format; specifically, if the counter is programmed for 2-byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read, write, or programming operations of other counters may be inserted between the reading of each byte of the output latch.

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Another feature of the 82C54 is that "reads" and "writes" of the same counter may be interleaved. For example, if the counter is programmed for 2-byte counts, the following sequence is valid:

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a counter is programmed to read/write 2-byte counts, the following precaution applies: **A program must not transfer control between reading the first byte and reading the second byte to another routine, which also reads from that same counter; otherwise, an incorrect count will be read.**

Readback Command

The third method of reading data from the counters uses the Readback Command. This command allows the user to check the Count Value, the Programmed Mode, and Current State of the "OUT" Line and Null Count Flag of the selected counter(s).

The command is written to the counter-timer's Control Word Register and has the format shown in Figure 8.2. The command applies to the counters selected by setting their corresponding bits (D3, D2, and D1) to 1.

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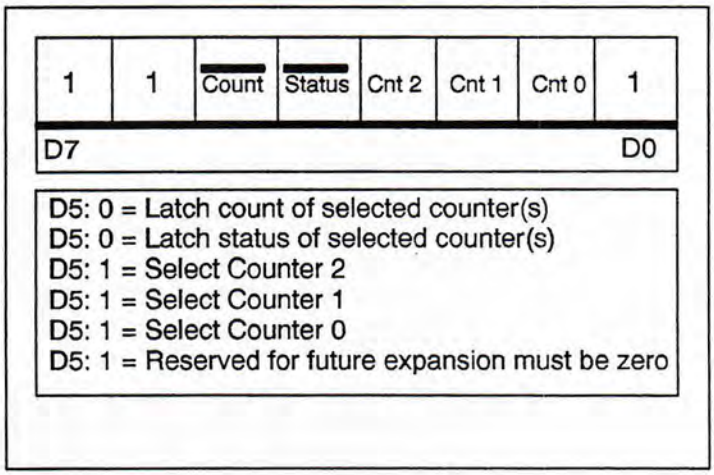


Figure 8.2: Readback Command Format

The Readback Command may be used to_latch multiple counter output latches by setting COUNT Bit (D5) to 0 and selecting the desired counter(s). The single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or until the counter is reprogrammed). That counter is automatically unlatched when read, but the others remain latched until they are read. If multiple count readback commands are issued to the same counter without reading the count, all but the first readback command are ignored -- i.e., the count that will be read is the count at the time the first readback command was issued.

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The Readback Command may also be used to latch status information of selected counter(s) by setting STATUS Bit (D4) to 0. Status must be latched to be read; Status is accessed by a read from that counter.

The Counter Status Format is shown in Figure 8.3. Bits D5 through D0 contain the counter's programmed mode exactly as written in the last Mode Control Word. Output Bit D7 contains the current state of the "out" line (see Figure 8.1). This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

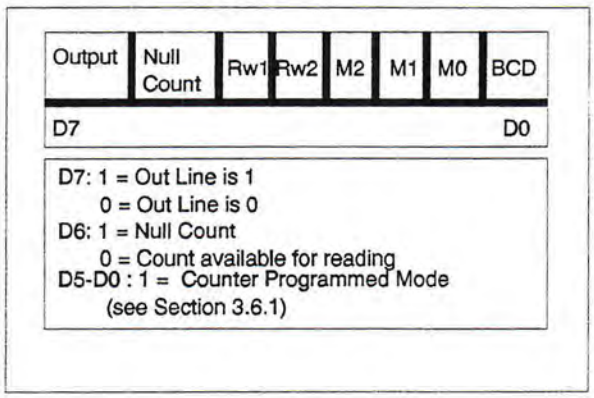


Figure 8.3: Status Byte Format

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Null Count Bit D6 indicates when the last count written to the counter register has been loaded into the counting element. The exact time this happens depends on the mode of the counter and is described in Section 8.2.5 "Mode Definitions"; but until the count is loaded into the counting element, it cannot be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 8.4

THIS ACTION:	CAUSES:
A. Write to the control word register (1)	Null Count = 1
B. Write to the count register (CR); (2)	Null Count = 1
C. New count is loaded into CE (Cr CE);	Null Count = 1

(1) Only the Counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.
(2) If the Counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

Figure 8.4: Null Count Operation

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If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored -- i.e., the status that will be read is the status of the counter at the time the first status readback was issued. Both the count and the status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS Bits (D5 & D4) to 0. This is functionally the same as issuing two separate readback commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status readback commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This sequence is illustrated in Figure 8.5.

Command								Description	Results
1	1	0	0	0	0	1	0	Read-Back count and status of Counter 0 or Counter 1	
1	1	1	0	0	1	0	0		
1	1	1	0	1	1	0	0	Read-Back status of Counter 2 & 1 but not for Counter 0	
1	1	0	1	1	0	0	0		
1	1	0	0	0	1	0	0		
1	1	1	0	0	0	1	0		Command ignored status already latched for Counter 1

Figure 8.5: Readback Command Sequence Example

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If both a count and status of a counter are latched, the first read operation of that counter will return the latched value of the status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for 1- or 2-byte counts) return the latched count. Subsequent reads return unlatched counts.

8.2.5 82C54 Mode Definitions

The following are defined for use in describing the operation of the Intel 82C54:

CLK PULSE -- a rising edge, then a falling edge (in that order) of a Counter CLK input.

TRIGGER -- a rising edge of a counter's GATE input.

COUNTER LOADING -- the transfer of a count from the Count Register to the Counting Element (refer to the Functional Description).

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Mode Control Word is written, the "OUT" line is initially low, and will remain low until the count reaches 0. The "OUT" line goes high and remains high until a new count or a new Mode 0 Control Word is written into the counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

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After the control word and initial count are written to a counter, the initial count will be loaded on the next CLK pulse. The CLK pulse does not decrement the count, so for an initial count of N, "OUT" does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the counter, it will be loaded on the next CLK pulse, and counting will continue from the new count. If a 2-byte count is written, the following occurs:

1. Writing the first byte disables counting. OUT is set low immediately (no CLK pulse required).

2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter, as this has already been done.

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Mode 1: Hardware Retriggerable Oneshot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the oneshot pulse, and will remain low until the counter reaches 0. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and Initial Count, the counter is armed. A trigger results in loading the Counting Element and setting the "OUT" line low on the next CLK pulse, thus starting the oneshot pulse. An initial count of N will result in a oneshot pulse, N CLK cycles in duration. The oneshot is retriggerable; hence, OUT will remain low for N CLK pulses after any trigger. The oneshot pulse can be repeated without reprogramming the counter with the same initial count. GATE has no effect on OUT.

If a new count is written to the counter during a oneshot pulse, the current oneshot is not affected unless the counter is retriggered. In that case, the Counting Element is loaded with the new count, and the oneshot continues until the new count expires.

Mode 2: Rate Generator

This mode functions like a Divide-by-N Counter. It is typically used to generate a realtime clock interrupt. OUT will initially be high. When the Initial Count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counting Element reloads the Initial Count, and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an Initial Count of N, the sequence repeats every N CLK cycles.

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GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counting Element with the Initial Count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus, the GATE input can be used to synchronize the counter.

After writing a Control Word and Initial Count, the Counting Element will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counting Element will be loaded with the new count on the next CLK pulse and counting will continue from the new count; otherwise, the new count will be loaded after the current counting cycle. In Mode 2, a count of 1 is illegal.

Mode 3: Squarewave Mode

Mode 3 is typically used for baud-rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the Initial Count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a squarewave with a period of N CLK cycles.

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GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counting Element with the Initial Count on the next CLK pulse. Thus the GATE input can be used to synchronize the counter.

After writing a Control Word and an Initial Count, the Counting Element is loaded on the next CLK pulse. This allows the counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counting Element will be loaded with the new count on the next CLK pulse and counting will continue from the new count; otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even Counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counting Element is reloaded with the Initial Count. The above process is repeated indefinitely.

Odd Counts: OUT is initially high. The Initial Count minus one (an even count) is loaded on one CLK pulse and is then decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low, and the Counting Element is reloaded with the Initial Count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the counting element is loaded with the Initial Count minus one. The above process is repeated indefinitely; so, for odd counts, OUT will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

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Mode 4: Software-Triggered Strobe

OUT will be initially high. When the Initial Count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the Initial Count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and Initial Count, the Counting Element will be loaded on the next CLK pulse. This CLK pulse does not decrement the count; so, for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the Initial Count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse, and counting will continue from the new count. If a 2-byte count is written, the following happens:

1. Writing the first byte has no effect on counting.

2. Writing the second byte allows the new count to be loaded into the Counting Element on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

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Mode 5: Hardware-Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the Initial Count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and an Initial Count, the Counting Element will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count; so, for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger results in the Counting Element being loaded with the Initial Count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on count.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counting Element will be loaded with the new count on the next CLK pulse, and counting will continue from there.

8.2.6 Operation Common to All Modes

When a control word is written to a counter, all control logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

GATE

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4, the GATE input is level-sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5, the GATE input is rising-edge-sensitive. In these modes, a rising edge of GATE

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(trigger) sets an edge-sensitive flip-flop in the counter. This flip-flop is then sampled on the next rising edge of CLK; the flip-flop is reset immediately after it is sampled. In this way, a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive. In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following the write of a new count value.

Counter

New counts are loaded, and counting elements are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is the equivalent of 216 for binary counting and 104 for BCD counting.

The Counting Element does not stop when it reaches 0. In Modes 0, 1, 4, and 5, the counter "wraps around" to the highest count (either FFFF Hex for binary counting, or 9999 for BCD counting) and continues counting. Modes 2 and 3 are periodic; the Counting Element reloads itself with the Initial Count and continues counting from there.

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CHAPTER NINE: The LSDAS-16-AC

9.0 Overview

The LSDAS-16-AC from Analogic Corporation is a high speed, multi-function, plug-in data acquisition board for the IBM PC/AT and compatibles. This board contains a 16-bit analog-to-digital converter with sixteen input channels, a multi-configuration 16-bit parallel digital I/O (DIO) port and a multichannel timer for triggering and pacing. This board differs from the standard LSDAS-16 in its lack of digital-to-analog capability. In each section of this chapter, the differences between the LSDAS-16 and LSDAS-16-AC will be shown. Sections 1 - 8 of this chapter correspond to chapters 1-8 of this manual. For more detail on specifications for this board, this section will refer you back to the appropriate chapter.

9.1 Getting Started

The LSDAS-16-AC has the same compatibility as all the other DAS products. Setting up the base address for the PC/AT also requires the same procedure. There is a difference when setting the jumper configuration for the board. A summary of the jumpers is as follows:

DAS Address Jumpers - Same
DMA Control Jumpers - Same
Interrupt Control Jumpers - Same
D/A Range Control Jumpers - not available
Additional Function Jumpers - Same
Miscellaneous Jumpers - Same

The installation of the DAS board is the same. This also holds true for the software, including the LS16LIB Library and DAS_MENU Setup Program. Refer to chapter 2 for details concerning hardware and software installation.

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9.2 DAS_MENU Setup Programs

The software setup program DAS_MENU provides the capability to create configuration files. The LSDAS-16-AC should be configured as if it were a LSDAS-16 standard board. This will allow convenient setup of the DAS boards using LS16LIB functions. See the DAS_MENU User's manual for the operation of the program in detail.

9.3 DAS Software Library Compatibility

The software library LS16LIB provides complete support for the LSDAS-16-AC at a variety of levels. This library is a replacement of the DAS-LIB library. The supporting library is also available in the Microsoft version called LS16LIBM. Since there are hardware differences between the LSDAS-16-AC and other DAS boards, there are certain library functions not compatible with this board. These library functions are described in the DAS-LIB manual shipped with this product. These functions may not be used with the LSDAS-16-AC board. Since the required circuitry for these functions has been removed, these functions would fail. A brief description of the functions not available are as follows.

(1) All functions operating the Digital to Analog converters.
(2) All functions using the external analog trigger.

9.4 D/A Conversion

This board has no digital-to-analog conversion capability.

9.5 A/D Conversion

The LSDAS-16-AC has one 50khz, 16-bit ADC for a sampling rate of 50khz. Since the analog-to-digital sub-system architecture is that of the LSDAS-16, the entire operation except for A/D Pre-/Post-Event Mark is the same. The differences in triggering are listed here. For complete detail specifications refer to chapter six.

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Analog Event Mark Trigger - Not Available
Since the Analog Event Mark Trigger compares a value programmed into the DAC, the Analog Trigger function is not available.

9.6 Registers

DAS boards use sixteen consecutive addresses in the I/O space of the PC/AT bus. The base address selection is described in Chapter Two. The LSDAS-16-AC register definitions are the same as an LSDAS-16. except the removal of the registers pertaining to the Digital-to-Analog converters. There are bits in some registers that are used in the D/A conversion which are not used. The following bits should be used as "don't cares" when they are programmed and should be masked off when read back.

D/A Mode Register (Base Address + 4) - not available
A/D Mode Register (Base Address + 6) - Bits 15 and 14
Control Register (Base Address + A Hex) - Bits 13, 12, 6 and 5
Interrupt Control (Base Address + C Hex) - Bits 3, 2, 1 and 0
Status Register (Base Address + C Hex) - Bits 4, 3, 2, 1 and 0
RAM Control Register (Base + 8 Hex and Extended Register = 0C Hex) - not available

For a complete listing of the register addresses and definitions please refer to Chapter Seven.

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9.7 The 82C54 Counter-Timers

The LSDAS-16-AC has one Intel 82C54 counter/timer. This counter/timer is the one that is referred to as Timer 1 in previous chapters of this manual. Only two of the three 82C54 channels are used on the LSDAS-16-AC. Channel 0 is dedicated to providing a 16-bit pacing clock source for the A/D subsystem. Channel 2 is available to the user through the J3 connector and can be used to perform those functions described in Chapter 8. Channels 0 and 2 can be strapped together for implementation of a 32-bit A/D pacing clock source (refer to Chapter 2). Channel 1 cannot be used.

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APPENDIX A: DAC Operation Examples

A.0 Overview

Appendix A contains a group of examples written in Assembly Language. These examples show simple D/A operation methods for the DAS boards. There is one example for each mode of operation for the D/A subsystem. (See Chapter Five for a discussion on D/A Conversion.)

A.1 D/A Mode 0

This program illustrates programed I/O for both DACs. This is D/A Mode 0, and the DACs are updated with data by the Assembly Language instruction "OUT". Each time data is transferred to the board, it is stored in a holding register and then transferred to the DAC. Macros are used to implement certain functions and make the program easier to read.

```
        .XLIST

        .LIST
        .SALL
        .CODE

START:      MOV         AX,@DATA
            MOV         DS,AX
            MOV         SS,AX
            MOV         SP,OFFSET STACK
START1:     BOARD_RESET

;Set to mode 0

            MOV         AX,DA_MODE_PIO_PIO
            SEND_DA_MODE

;Set CS to 0

            MOV         AX,DA_CH0_LO_PRI
            SEND_DA_CHSEL
```


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```
;Clear the mode reset bit

                CLR_DAMR

;Enable DAC updating

        EN_UREQ_DA_0
        EN_UREQ_DA_1

AGAIN:  MOV     CX, 0010H       ;Loop counter
3       MOV     AX, 0001H       ;Data for output
BACK:   MOV     DX, DA_0_DATA   ;Output to DAC 0
        OUT     DX, AX
        MOV     DX, DA_1_DATA   ;Output to DAC 1
        OUT     DX, AX
        SHL     AX, 1           ;Get next data
        PUSH    CX
        MOV     CX, 0010H
WATE:   LOOP    WATE
        POP     CX
        LOOP    BACK

;Output 0 - puts DACs at neg full scale

        MOV     AX, 0
        MOV     DX,DA_0_DATA
        OUT     DX,AX
        MOV     DX,DA_1_DATA
        OUT     DX,AX

;Output pos full scale

        MOV     AX, 0FFFH
        MOV     DX,DA_0_DATA
        OUT     DX,AX
        MOV     DX,DA_1_DATA
        OUT     DX,AX
        MP      AGAIN
        END     START
```


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A.2 D/A Mode 1

This program illustrates DAC1 being updated by programmed I/O and DAC0 being updated via DMA, Channel 6; this is D/A Mode 1.

```
        .LIST
        .SALL

        .DATA
        EVEN

DA_TEST_BUF     DW      0001H
                DW      0002H
                DW      0004H
                DW      0008H
                DW      0010H
                DW      0020H
                DW      0040H
                DW      0080H
                DW      0100H
                DW      0200H
                DW      0400H
                DW      0800H
                DW      1000H
                DW      2000H
                DW      4000H
                DW      8000H
DA_TEST_END   DW        ?

                .CODE

        START:  MOV     AX,@DATA
                MOV     DS,AX
                MOV     SS,AX
                MOV     SP,OFFSET STACK

;Mode 1, PIO_DMA
```


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```
START0:         BOARD_RESET
                MOV             AX,DA_MODE_DMA_PIO
                SEND_DA_MODE
                MOV             AX,DA_CH0_DMA
                SEND_DA_CHSEL
```

;Select the same timer for both channels; this update rate is set for 200kHz.

```
        DA_0_TIMER_PACE
        DA_1_TIMER_PACE
        MOV                     AX,DA_CH0_CT1_CH1
        SEND_DA_0_TMR
        MOV                     AX,DA_CH1_CT1_CH1
        SEND_DA_1_TMR
        CLR_DAMR
        MOV                     AX,CT_CTL_COMM +
                        CT_SEL_CH1 + CT_MODE2
        SEND_CT1_MODE
        MOV                     AX,6800/200
        SEND_CT1_CH1
```

;Send DAC1 data before DAC1 can be updated so the holding register has
;data before the DAC is updated.

```
        MOV             AX, 5555H
        MOV             DX,DA_1_DATA
        OUT             DX,AX
```


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```
;Set up DMA channel 6 for DAC0

DMA:    MOV                 AX,OFFSET
                            DA_TEST_BUF
        MOV                 BX,DS
        MOV                 CX,(DA_TEST_END -
                        DA_TEST_BUF)/2
        SETUP_CH6
        MOV                 AL,CH6_MODE_DA
        OUT                 DMA2_MODE,AL
        JMP                 $+2
        EN_DA_DMA_REQ
        MOV                 AL,CH6_ENABLE
        OUT                 DMA2_MASK_SR,AL
        JMP                 $+2

;Set the start da dma bit, enable tc, and enable the timer interrupt status bit

        START_DA_DMA
        EN_DA_TC_INT
        EN_DA_0_INT
;Wait for DAC0 timer to occur so can synchronize and start up properly.
;Data will not be transferred yet because the update enable bits are not set yet.

        MOV             DX,STATUS

        TRY_AGN_0:      IN              AX,DX
        TEST                            AX,DA_0_INT_TEST
        JZ                              TRY_AGN_0
        CLR_DA_0_INT

;Now enable the dacs so they can be updated

        EN_UREQ_DA_0
        EN_UREQ_DA_1
```


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```
;Wait for timer to set status bit so can synchronize DAC1 PIO out

        BACK:           MOV     DX,STATUS

        TRY_AGN_1:      IN      AX,DX
                TEST            AX,DA_0_INT_TEST
                JZ              TRY_AGN_1
                CLR_DA_0_INT

;Send DAC1 data

                MOV     AX,0AAAAH
                MOV     DX,DA_1_DATA
                OUT     DX,AX
                MOV     DX,STATUS
                MOV     BX, 0001

;Wait for timer int again so know when to output DAC1 data. Loop back to here until
;the DMA terminal count comes true indicating that all of the data has been transferred
;to DAC0.

TRY_AGN_2:      IN      AX,DX
                TEST    AX,DA_0_INT_TEST
                JZ      TRY_AGN_2
                CLR_DA_0_INT

                MOV     DX,STATUS

;Check TC int

                IN              AX,DX
                TEST            AX,DA_TC_INT_TEST
                JZ              CONTINUE
                CLR_DA_TC_INT
                STOP_DA_DMA
                JMP             DMA
CONTINUE:       SHL             BX,1
                MOV             DX,DA_1_DATA
                OUT             DX,AX
                JMP             TRY_AGN_2

                END             START
```


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A.3 D/A Mode 2

This program sets up the DACs to run in Mode 2 (DMA on both channels). The DAC data must be interleaved in the DMA buffer. It does not make sense to update the DACs at different rates, as the programmer could not determine which D/A converter is getting which data. Therefore, this mode should only be used when both DACs are updated by the same pacing source (timer).

```
                .LIST
                .SALL

                .DATA

DA_TEST_BUF     DW      0001H
                DW      8000H
                DW      0002H
                DW      4000H
                DW      0004H
                DW      2000H
                DW      0008H
                DW      1000H
                DW      0010H
                DW      0800H
                DW      0020H
                DW      0400H
                DW      0040H   ;This is a buffer containing
                DW      0200H   ;a periodic waveform
                DW      0080H   ;used for sending data to the
                DW      0100H   ;DACs via DMA.  For the sake
                DW      0100H   ;of conserving space in the
                DW      0080H   ;manual, we have chosen
                DW      0200H   ;to include only one period of
                DW      0040H   ;our waveform.  There can
                DW      0400H   ;of course, be more data.
                DW      0020H
                DW      0800H
                DW      0010H
                DW      1000H
                DW      0008H
                DW      2000H
                DW      0004H
                DW      4000H
                DW      0002H
                DW      8000H
                DW      0001H
```


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```
DA_TEST_END   DW      ?

TCM           DB      "TC OK $"
TMRM          DB      "TIMER INT DID NOT OCCUR $"
TCNOTOKM      DB      "TC DID NOT OCCUR $"

              .CODE

START:        MOV     AX,@DATA
              MOV     DS,AX
              MOV     SS,AX
              MOV     CX, 00FFH
              MOV     SP,OFFSET STACK

START0:       BOARD_RESET

;Send the mode - mode 2

              MOV             AX,DA_MODE_DMA_DMA
              SEND_DA_MODE

;Set CS to 0

              MOV             AX,DA_CH0_LO_PRI
              SEND_DA_CHSEL

;Set both dacs for timer operation

              DA_0_TIMER_PACE
              DA_1_TIMER_PACE

;Select the same timer for both dac update rates

              MOV             AX,DA_CH0_CT1_CH1
              SEND_DA_0_TMR
              MOV             AX,DA_CH1_CT1_CH1
              SEND_DA_1_TMR

;Set up Timer 1 Channel 1

        MOV                   AX,CT_CTL_COMM + CT_SEL_CH1 +
                              CT_MODE2
        SEND_CT1_MODE
        MOV                   AX,6800/100       ;100kHz update rate
        SEND_CT1_CH1
```


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```
;Set up DMA channel 6

DMA:    MOV                 AX,OFFSET DA_TEST_BUF
        MOV                 BX,DS
        MOV                 CX,(DA_TEST_END -
                        DA_TEST_BUF)/2
        SETUP_CH6
        MOV                 AL,CH6_MODE_DA
        OUT                 DMA2_MODE,AL
        JMP                 $+2
        EN_DA_DMA_REQ
        MOV                 AL,CH6_ENABLE
        OUT                 DMA2_MASK_SR,AL
        JMP                 $+2

;Allow DACs to start

        CLR_DAMR
        START_DA_DMA        ;Set D/A DMA start bit
        EN_DA_TC_INT        ;Enable D/A TC status bit
        EN_DA_0_INT         ;Enable DAC0 timer status bit

;Wait for timer to set status bit so can synchronize the setting of the update
;request bits

                MOV     DX,STATUS
                MOV     CX, 0FFFH       ;Timeout if wait too
                                        ;long
TRY_AGN_0:      IN      AX,DX
                TEST    AX,DA_0_INT_TEST
                JNZ     CONT
                LOOP    TRY_AGN_0
                JMP     HT1

;Set update requests

        CONT:   CLR_DA_0_INT
                EN_UREQ_DA_0
                EN_UREQ_DA_1

;Wait for D/A TC to occur - time out if not reasonable time

                MOV             CX, 0FFFH
TRY_AGN_1:      MOV             DX,STATUS
                IN               AX,DX
                TEST             AX,DA_TC_INT_TEST
```


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```
                JNZ             CONT1
                LOOP            TRY_AGN_1
                SET_DAMR
                CLR_DA_0_INT
                STOP_DA_DMA
                JMP             HT2

;Do some housekeeping

        CONT1:          CLR_DA_0_INT
                        STOP_DA_DMA
                        SET_DAMR
                        CLR_DA_0_INT
                        STOP_DA_DMA

;Output TC ok message

                MOV     DX, OFFSET TCM
                MOV     AH, 09H
                INT     21H
                MOV     DL, 0AH
                MOV     AH, 02H
                INT     21H
                MOV     DL, 0DH
                MOV     AH, 02H
                INT     21H
                JMP     DMA

;Output timer not ok message

HT1:            MOV     DX, OFFSET TMRM
                MOV     AH, 09H
                INT     21H
                MOV     DL, 0AH
                MOV     AH, 02H
                INT     21H
                MOV     DL, 0DH
                MOV     AH, 02H
                INT     21H
                JMP     DMA

;Output TC did not occur

HT2:            MOV             DX, OFFSET TCNOTOKM
                MOV             AH, 09H
                INT             21H
```


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```
                MOV             DL, 0AH
                MOV             AH, 02H
                INT             21H
                MOV             DL, 0DH
                MOV             AH, 02H
                INT             21H
                JMP             DMA
                SET_DAMR
                CLR_DA_0_INT
                STOP_DA_DMA
                MOV             DX,STATUS

TRY_AGN_2:      IN      AX,DX
                TEST    AX,DA_0_INT_TEST
                JZ      TRY_AGN_2
                DEC     CX
                JNZ     STARTE
                JMP     START0

START:          JMP     START0
                END     START
```

A.4 D/A Mode 4

This program sets DAC0 to be updated from the on-board RAM and DAC1 to be updated via programmed I/O. The data in the RAM has to have been written there already via D/A Mode 7.

```
                .LIST
                .SALL
                .CODE

START:          MOV             AX,@DATA
                MOV              DS,AX
                MOV             SS,AX
                MOV             SP,OFFSET STACK

START0:         BOARD_RESET
                MOV             CX, 20H

;Set the mode to 4

START1:         MOV                     AX,DA_MODE_RDR_PIO
                SEND_DA_MODE            ;mode 4
```


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```
;Set the CS bit to 0 to indicate that DAC0 is updated from RAM

        MOV                     AX,DA_CH0_RD_RAM  ;ch0 rd ram
        SEND_DA_CHSEL

;Set both DACs up for timer pacing

        DA_0_TIMER_PACE         ;set timer
        DA_1_ASYN_PACE          ;pio ch1

;Select counter timer 1 channel 1 for DAC0

        MOV                     AX,DA_CH0_CT1_CH1;Sel tmr for DAC0
        SEND_DA_0_TMR
        CLR_DAMR                ;Set D/A Mode Reset high

;Set up RAM address counter in counter timer 2 channel 0

        MOV     AX,CT_CTL_COMM + CT_SEL_CH0 + CT_MODE1
        SEND_CT2_MODE           ;D/A RAM address counter

;Sends 1 to the counter holding register

        MOV             AX,0001H
        SEND_CT2_CH0

;Transfers the count in the holding register to the counting element
;it also sets the counter output to its proper state

        TRANS_CT2_CH0

;Decrement to zero so data being transferred to DAC0 will start at
;location zero

        DEC_CT2_CH0

;Set the upper address of the RAM data area - in this case for
;illustration purposes it is set to the highest location 7FFF Hex

        MOV     AX,7FFFH
        SEND_CT2_CH0

;Disable the CPU control of the address counter and let the RAM
;control circuit have control

        DIS_CPU_CNTL_CT2
```


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```
;Clear the RAM control reset bit so updating from RAM can occur

        CLR_RAMMR

;Set up the pacing timer from timer 1 channel 1

        MOV     AX,CT_CTL_COMM + CT_SEL_CH1 + CT_MODE2
        SEND_CT1_MODE
        MOV     AX,6800/200         ;200kHz update rate
        SEND_CT1_CH1

;Enable DAC writes

        ENABLE_DAC_WR

;Enable the update request bits

        EN_UREQ_DA_0
        EN_UREQ_DA_1
        MOV         CX,  000FH

;Send PIO data to DAC1-this is not 100% correct because one should check
;the DAC ready bit before transferring data to the holding registers

BACK:   MOV         BX,0AAAAH
        MOV         AX,BX
        MOV         DX,DA_1_DATA
        OUT         DX,AX
        MOV         BX,0H
        MOV         AX,BX
        MOV         DX,DA_1_DATA
        OUT         DX,AX
        JMP         $+2
        LOOP        START
```


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A.5 D/A Mode 5

This program uses DAC Mode 5 to supply data to the DACs. DAC0 gets its data from the on-board RAM memory and DAC1 gets its data via DMA from a data buffer in the computer's memory.

```
                        .LIST
                        .SALL

                        .DATA
DA_TEST_BUF_1           DW          0FFFH
                        DW          0FFFH
                        DW          07FFH
                        DW          07FFH
                        DW          03FFH
                        DW          03FFH
                        DW          01FFH
                        DW          01FFH
                        DW          00FFH
                        DW          007FH
                        DW          003FH
                        DW          001FH
                        DW          000FH
                        DW          0007H
                        DW          0003H
                        DW          0001H
                        DW          0001H
                        DW          0003H
                        DW          0007H
                        DW          000FH
                        DW          001FH
                        DW          003FH
                        DW          007FH
                        DW          00FFH
                        DW          01FFH
                        DW          01FFH
                        DW          03FFH
                        DW          03FFH
                        DW          07FFH
                        DW          07FFH
                        DW          0FFFH
                        DW          0FFFH
DA_TEST_END_1 DW                    ?

                        .CODE
```


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```
START:      MOV         AX,@DATA
            MOV         DS,AX
            MOV         SS,AX
            MOV         SP,OFFSET STACK
START0:     BOARD_RESET

;Set the mode

            MOV         AX,DA_MODE_RDR_DMA
            SEND_DA_MODE

;Set CS bit to 0 to indicate that DAC0 is getting its data from
;the onboard RAM

            MOV         AX,DA_CH0_RD_RAM
            SEND_DA_CHSEL

;Select timer pacing for each DAC

            DA_0_TIMER_PACE
            DA_1_TIMER_PACE

;Set each DAC up for timer 1 channel 1

            MOV                 AX,DA_CH0_CT1_CH1
            SEND_DA_0_TMR
            MOV                 AX,DA_CH0_CT1_CH1
            SEND_DA_1_TMR
            CLR_DAMR

;Set up the on board RAM address counter

            MOV                 AX,CT_CTL_COMM + CT_SEL_CH0 +
                        CT_MODE1
            SEND_CT2_MODE

;Set 0001h into the address counter holding register

            MOV                 AX,0001H
            SEND_CT2_CH0

;Transfer the address to the counting element

            TRANS_CT2_CH0

;Decrement to zer0
```


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```
        DEC_CT2_CH0

;Set the on board RAM data starting address in the address counter
;holding register

        MOV             AX,01FFH
        SEND_CT2_CH0

;Disable CPU control of the address counter and let the RAM
;control circuit decrement the address

        DIS_CPU_CNTL_CT2
        CLR_RAMMR

;Set up timer 1 channel 1 for DAC pacing

        MOV             AX,CT_CTL_COMM + CT_SEL_CH1 + CT_MODE2
        SEND_CT1_MODE
        MOV             AX,6800/100     ;100kHz update rate
        SEND_CT1_CH1

;Enable writing into the DACs

        ENABLE_DAC_WR

;Enable DAC0 update request

        EN_UREQ_DA_0

;Set up DMA channel 6

        MOV             AX,OFFSET DA_TEST_BUF_1
        MOV             BX,DS
        MOV             CX,(DA_TEST_END_1 - DA_TEST_BUF_1) / 2
        SETUP_CH6
        MOV             AL,CH6_MODE_DA
        OUT             DMA2_MODE,AL
        JMP             $+2

;Enable the DAC DMA request circuitry

        EN_DA_DMA_REQ

;Finish setting up the DMA channel
```


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```
        MOV     AL,CH6_ENABLE
        OUT     DMA2_MASK_SR,AL
        JMP     $+2

;Start the DMA process so can load the holding register before

        START_DA_DMA

;Enable the D/A terminal count status bit

        EN_DA_TC_INT

;Enable the timer status bit

        EN_DA_1_INT

;Wait for the timer to set this bit before enabling the update request for DAC1

                MOV             DX,STATUS
TRY_AGN_0       IN              AX,DX
                TEST            AX,DA_1_INT_TEST
                JZ              TRY_AGN_0
                EN_UREQ_DA_1
BACK:           MOV             DX,STATUS

;Wait for terminal count to indicate done with the dma transfers

TRY_AGN_1:      IN              AX,DX
                TEST            AX,DA_TC_INT_TEST
                JZ              TRY_AGN_1

;Do some housekeeping when TC occurs

        STOP_DA_DMA
        CLR_DA_TC_INT
        CLR_DA_1_INT

;Set up DMA buffer again

        MOV             AX,OFFSET DA_TEST_BUF_1
        MOV             BX,DS
        MOV             CX,(DA_TEST_END_1 - DA_TEST_BUF_1)/2
        SETUP_CH6
        MOV             AL,CH6_MODE_DA
```


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```
        OUT     DMA2_MODE,AL
        JMP     $+2
        MOV     AL,CH6_ENABLE
        OUT     DMA2_MASK_SR,AL
        JMP     $+2

;Wait for timer

        MOV     DX,STATUS
TRY_AGN_2:  IN      AX,DX
        TEST    AX,DA_1_INT_TEST
        JZ      TRY_AGN_2

;Start DMA again

        START_DA_DMA
        JMP     BACK
        END     START
```

A.6 D/A Mode 6

This program allows both DACs to read data from the on-board RAM. A timer is used to pace the updating. Note that the data must already be in the memory by using mode 7 to write data into the RAM memory. There can only be one pacing source for updating both DACs.

```
        .LIST
        .SALL
        .CODE

START:  MOV     AX,@DATA
        MOV     DS,AX
        MOV     SS,AX
        MOV     SP,OFFSET STACK
START0: BOARD_RESET
```


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```
;Set up for Mode 6

        MOV                     AX,DA_MODE_RDR_RDR
        SEND_DA_MODE

;Set CS to 1 for DAC1

        MOV                     AX,DA_CH1_LO_PRI
        SEND_DA_CHSEL

;The CS bit chooses which DAC pacing info is used to update both DACs

        DA_1_TIMER_PACE


;Set up timer 1 channel 1 for pacing

        MOV                     AX,DA_CH1_CT1_CH1
        SEND_DA_1_TMR

;Enable the DAC circuitry

        CLR_DAMR

;Set up the RAM address counters for both DACs -
;timer 2 channel 0 for DAC0 and timer 2 channel 1 for DAC1
;Set the mode into timer 2 channels 0 and 1

        MOV             AX,CT_CTL_COMM + CT_SEL_CH0 + CT_MODE1
        SEND_CT2_MODE
        MOV             AX,CT_CTL_COMM + CT_SEL_CH1 + CT_MODE1
        SEND_CT2_MODE

;Set a 1 into each of the address counter holding registers

        MOV                     AX,0001H
        SEND_CT2_CH0
        MOV                     AX,0001H
        SEND_CT2_CH1

;Transfer the address into the counting element

        TRANS_CT2_CH0
        TRANS_CT2_CH1
```


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```
;Decrement both address counters to zero.  This sets the output of  the address
;counters to their correct states.

        DEC_CT2_CH0
        DEC_CT2_CH1

;Set the starting address of the on board RAM Into the address counter holding
;registers

        MOV                 AX,01ffH
        SEND_CT2_CH0
        MOV                 AX,01ffH
        SEND_CT2_CH1

;Enable RAM control of the timer

        DIS_CPU_CNTL_CT2
        CLR_RAMMR

;Set up the pacing timer

        MOV         AX,CT_CTL_COMM + CT_SEL_CH1 + CT_MODE2
        SEND_CT1_MODE
        MOV         AX,6800/150  ;PACE AT 150KHZ
        SEND_CT1_CH1

;enable DACs

        ENABLE_DAC_WR

;Enable DAC1 update requests

        EN_UREQ_DA_1

;Time out to allow DACs to be updated

        MOV         CX,1
        TIMEOUT
        JMP         START0
        INT         32
        END         START
```


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A.7 D/A Mode 7

This mode writes the data into the on-board RAM memory. Data can only be written into the RAM for one of the DACs at a time. DACs are updated from only one of the pacing setups. The CS Bit selects which DAC pacing information is to be used.

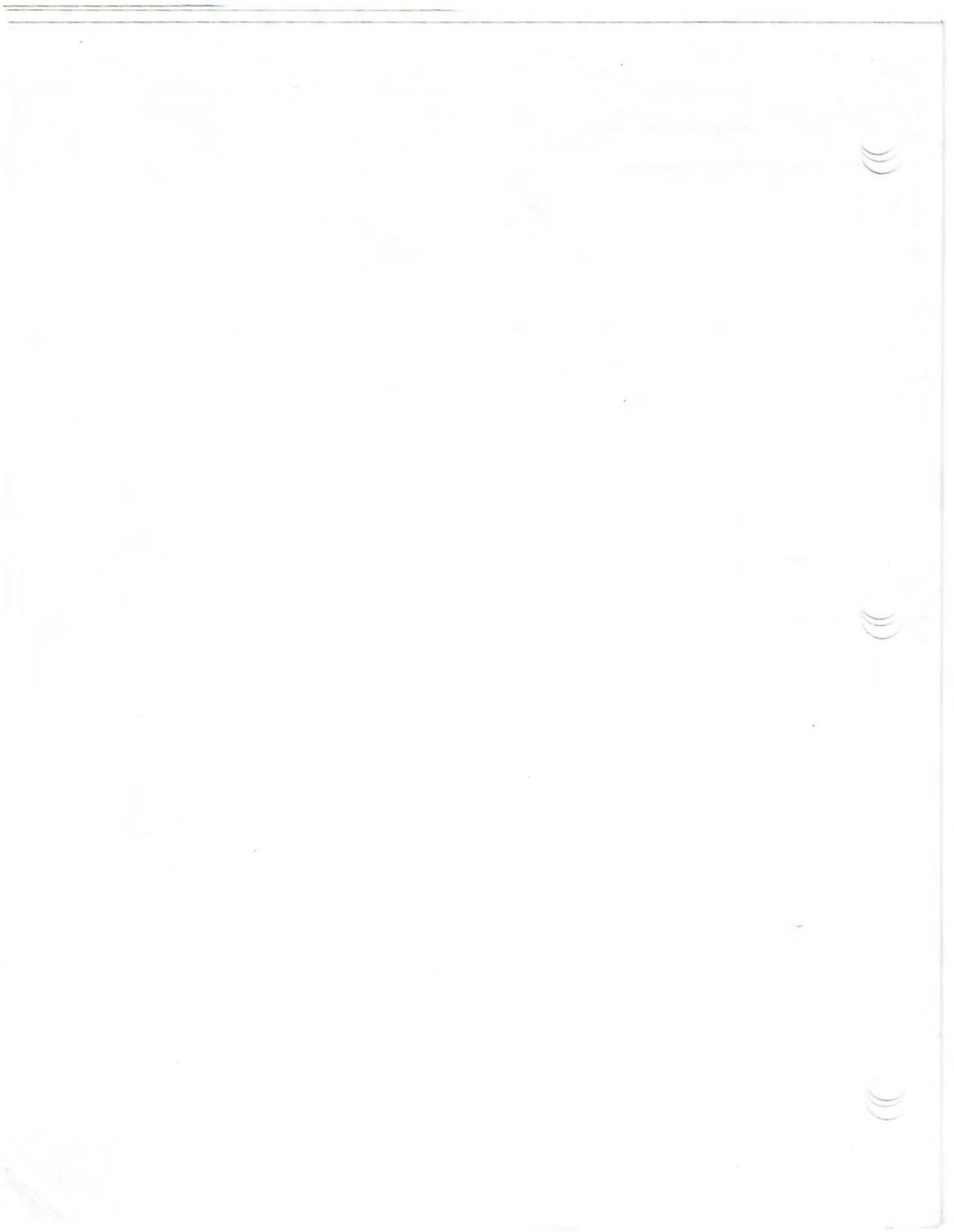
Note that the CS Bit also chooses which DAC channel is reading from the RAM memory. The other DAC is having its RAM memory loaded with data.

```
                        .LIST
                        .SALL

                        .DATA

DA_TEST_BUF_0           DW      0001H
                        DW      0002H
                        DW      0004H
                        DW      0008H
                        DW      0010H
                        DW      0020H
                        DW      0040H
                        DW      0080H
                        DW      0100H
                        DW      0200H
                        DW      0400H
                        DW      0800H
                        DW      0800H
                        DW      0400H
                        DW      0200H
                        DW      0100H
                        DW      0080H
                        DW      0040H
                        DW      0020H
                        DW      0010H
                        DW      0008H
                        DW      0004H
                        DW      0002H
                        DW      0001H
DA_TEST_END_0           DW      ?
DA_TEST_BUF_1           DW      0800H
                        DW      0400H
                        DW      0200H
                        DW      0100H
                        DW      0080H
```


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