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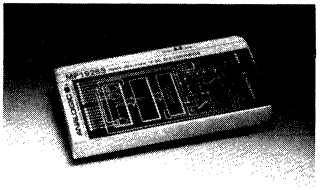
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ANALOGIC®

MP1926

Ultra-Linear, 200 kHz 16-Bit Sign/Magnitude D/A Converter

Description

The MP1926 is an ultra-linear, high speed, 16-bit digital-to-analog converter module designed specifically for reconstructing dynamic complex waveforms from digital data, particularly audio or acoustic signals, sonar, and other signals that have a substantial amount of the information content in the vicinity of "zero volts" (midrange). In such systems, power occasionally peaks well above the rms power level, as in speech or music. Thus, accurately recreating such information from digital data requires exceptional small signal performance to handle the information near zero level without crossover distortion, yet there must be a very large dynamic range to handle the bursts of higher amplitudes, together with the ability to handle the wide range of frequency interest.

The MP1926 meets these requirements with an internal sign/magnitude architecture that gives **18 bits of linearity for signals near zero volts and a 3 μs settling time** — at a price less than that of other, low speed, 16-bit DACs which typically offer, at best, 14-bit accuracy at midrange.

Accepting standard input binary codes, including offset binary and 2's complement. Analogic's proprietary (pat. pending) sign/magnitude internal architecture provides performance that actually improves as the signal approaches zero from either direction (error proportional to the signal's absolute value, or magnitude). With the commonly used "offset binary" architecture, which produces a bipolar output by offsetting an internal unipolar signal by one half full scale, even a small error in the

(continued)

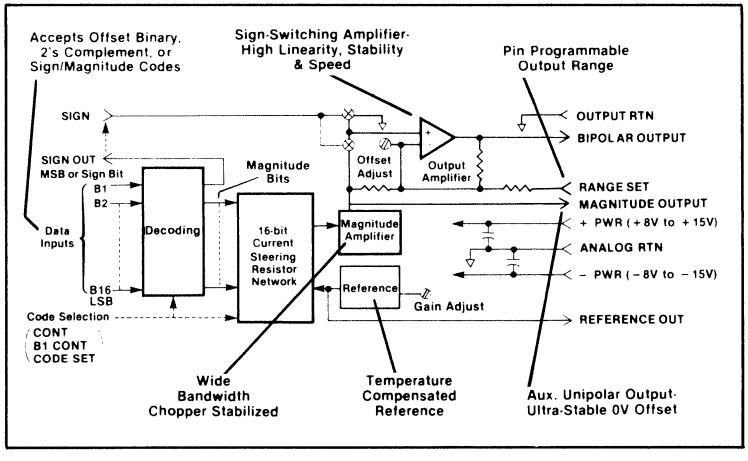


Figure 1. MP1926 Functional Block Diagram.

Features

- **Low Harmonic Distortion** 0.005% (0.0005 dB!)
- **Wide Dynamic Range 16 bits**
- **Ultra-High Linearity Over the Full Scale Range** ± ¼ LSB, max. mid-range non-linearity
- **High speed** settling time <3 μs (MP1926A)
- **Low Tempco's** total drift from all sources <1 ppm/°C (MP1926S)
- **Low Power** 250 mW
- **Built-In Code Conversion** uses standard codes
- **Low Cost**
- **Flexible**
  ± 8V to ± 15V power supply
  TTL or CMOS inputs
  Offset Binary, 2's Complement, or
  Sign/Magnitude codes
  Operates −25°C to +85°C

Applications

- **Professional Audio Systems — Low Total Harmonic Distortion**
- **Telecommunications Digitizing — High Noise Power Ratio**
- **High Resolution Information Translation Systems**
- **High Speed, High Precision, Automated Test Instrumentation**
- **Wide Dynamic Range, Computer Controlled, Industrial Processes**
- **Waveform Synthesis and Recovery**

SPECIFICATIONS

(All specifications guaranteed at 25°C unless otherwise noted)

BIPOLAR OUTPUT

Full Scale Voltage Ranges (FSR)[1]
±5V or ±10V

dc Output Impedance
0.1Ω max.

Load Current
5 mA max.

ACCURACY @ 25°C — TOTAL NONLINEARITY

For Mid-Range Outputs Centered about Zero Volts (¼ FSR)[2]
±4 ppm FSR max.

Over the Full Scale Range[3]
±15 ppm FSR max.

Absolute Range Accuracy[4]
MP1926A — ±0.1% FSR
MP1926S — ±0.01% FSR

Offset Voltage[4]
MP1926A — ±1 mV
MP1926S — ±0.1 mV

Zero Code, 0° to 70°C
Continuous and monotonic through zero

STABILITY

Tempco of Differential Nonlinearity for Mid-Range Outputs Centered about Zero Volt (¼ FSR)
±0.25 typ., ±1 max. ppm FSR/°C

Over the FSR
±0.5 typ., ±2 max. ppm FSR/°C

Tempco of Gain (Includes Reference)[5]
MP1926A — ±10 ppm of READING/°C typ., ±30 ppm of READING/°C max.
MP1926S — ±2 ppm of READING/°C typ., ±5 ppm of READING/°C max.

Tempco of Offset Voltage[6]
MP1926A — ±5 ppm FSR/°C max.
MP1926S — ±0.5 ppm FSR/°C max.

Power Supply Sensitivity
Gain
20 ppm FSR/V

Offset
20 μV/V

Recommended Recalibration Interval
MP1926A — N/A
MP1926S — See Note 4

Warm Up Time to Specified Accuracy
5 minutes max.

Settling Time for 5V step
to 0.01%
MP1926A — 3 μs max.
MP1926S — 40 μs max.

to 1 LSB
MP1926A — 5 μs max.
MP1926S — 50 μs max.

Slew Rate
MP1926A — 7.5V/μs min.
MP1926S — 0.15V/μs min.

Noise (10 Hz to 100 kHz)
35 μV rms

Output Fault Protection
Indefinite short to ground

MAGNITUDE OUTPUT (Auxiliary Output)

Voltage Range
0 to −5V

Offset Voltage
20 μV typ.

Tempco of Offset Voltage
1 μV/°C max.

Output Fault Protection
Indefinite short to ground

INTERNAL REFERENCE OUTPUT

Nominal Voltage
+5V (proportional to Range Control)

dc Output Impedance
0.1Ω max.

Load Current
1 mA max.

DIGITAL INPUTS

Resolution
16 bits

Format (Pin Programmable)
See Tables 1 & 2

Logic Compatibility[7]
CMOS, TTL

Low (FALSE) Level/High (TRUE) Level
0.4V ±0.6V/4.6V ±0.6V

Input Impedance
1 MΩ min.

POWER REQUIREMENTS[8]

Nominal Voltage[1]
±8V to ±15V

Absolute Max.
±16V

Current, Exclusive of Load ±16 mA

Dissipation @ ±8V, exclusive of load
250 mW max.

Dissipation @ ±15V, exclusive of load
500 mW max.

ENVIRONMENT

Rated Performance
0°C to 70°C

Operating Temperature Range
−25°C to +85°C

Storage Temperature Range
−55°C to +85°C

Relative Humidity
0 to 85%, non-condensing up to 40°C

PACKAGING

Dimensions, inches (mm rounded)
2 x 4 x 0.44 inches (50.8 x 101.6 x 11.2 mm)

Electromagnetic Shielding
5 sides

Electrostatic Shielding
6 sides

Notes
1. FSR is pin programmable. 20V FSR requires ± 15V power supply.
2. Deviation from best straight line.
3. Deviation from best straight line.
4. Range accuracy (gain) and offset voltage each adjustable via externally accessible potentiometers. Specifications given are factory setting, using ± 8V supplied. Recommended recalibration interval is three months in an instrumentation application (MP1926S).
5. For bipolar signals, X ppm of READING is less than or equal to X/2 ppm of FSR, e.g., 2 ppm of READING ≤1 ppm FSR.
6. Total at 0V, not affected by reference drift.
7. Unit does not include pull-up resistors, which may be required for TTL.
8. Analog Return, Output Return, and case are tied internally.

Description (cont.)

offsetting resistor can frequently cause large output errors near zero volts. Therefore, the MP1926 is the only high speed, 16-bit digital-to-analog converter to offer linearity near zero volts *better than ± ¼ LSB (4 ppm)* and total full range harmonic distortion (measured with an output deglitch amplifier) *better than 0.005% (0.0005 dB!).*

Moreover, this performance is preserved over a wide temperature range. The MP1926S, a version optimized for use in reference-type applications, offers voltage offset, linearity, and gain drifts so low that the worst-case total (algebraic sum) of their effects for signals near zero volts is typically **less than 1 ppm/°C from 0°C to 70°C.** Even the very fast MP1926A version offers better stability than provided by many higher-priced 16-bit DACs. Both versions have an auxiliary unipolar output that is proportional to the magnitude of the bipolar output and which offers zero voltage offset stability of 1 μV/°C!

Besides offering such linear and stable performance, the MP1926 offers versatility. It directly accepts offset binary and two's complement codes as well as sign/magnitude codes, without added circuitry, from CMOS or TTL logic, so that it can be interfaced easily with most computer-based systems. It operates from a single bipolar power supply (no separate +5V supply is required), and its low power consumption of 250 mW and metal case qualify it for use in a variety of environments. Thus the benefits of exceptionally good small-signal performance, high speed, and very wide dynamic range, coupled with low cost, make the MP1926 the ideal choice for a large variety of applications.

Performance Features

An internal sign/magnitude architecture provides optimum bipolar performance, particularly when compared to the commonly used offset binary architectures. Several key features of the MP1926 make this dramatic improvement in performance easy to use in many applications. Those features include low gain, linearity, offset errors: onboard decoding of several popular digital codes (converting to the sign/magnitude code used internally; and hard-wired range selection.

Bipolar Performance

An internal sign/magnitude architecture provides optimum bipolar performance because step size error decreases as the signal magnitude decreases, rather than being proportional to major bit weight contributions as in an offset binary architecture. The MP1926 employs a unique internal implementation of the sign/magnitude algorithm. Figure 1 shows that the 15 LSBs of a decoded (code converted) digital word control a resistor network that provides a scaled current to a chopper stabilized Magnitude Amplifier, which in turn converts this current to a unipolar (0V to −5V) voltage. The bipolar output is generated by using the MSB to configure the Output Amplifier as either an inverter or a follower.

Figure 2 shows the resulting performance for a typical MP1926 — note that the error decreases as the output approaches zero from either direction, that the performance is symmetric above and below 0V, and that the output crosses through zero continuously.

As shown, *for midrange outputs the nonlinearity is typically much less than 4 ppm FSR.* Thus the MP1926 provides a full 96 dB of *useable* dynamic range (2^{16} voltage steps). Most other 16-bit converters have a much smaller effective dynamic range because they exhibit relatively large errors

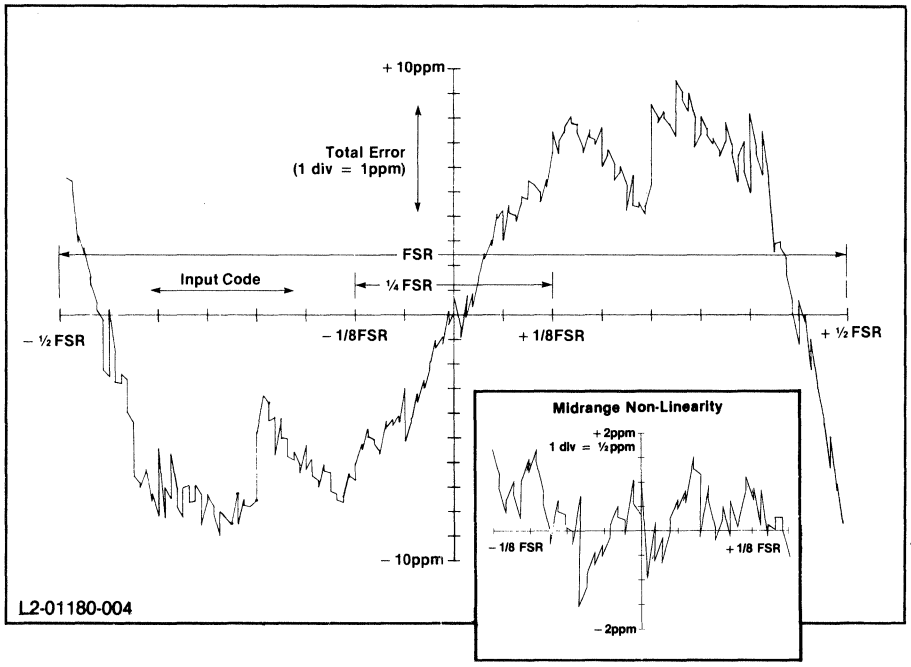


Figure 2. Error Plot of an MP1926. Error measured at zero volts and at 256 other points across the full scale range. These included the 128 most major bit transition points, plus a point 1 LSB away from each. Over the FSR the largest total error (non-linearity, gain and offset) is **less than 10 ppm.** Over the midrange centered around zero volts, the non-linearity error is **less than 2 ppm.**

for small output signals. The following paragraphs show why the MP1926 approach is superior to offset binary approaches and to earlier sign/magnitude approaches in most bipolar applications.

Figure 3 compares performance around zero of offset binary and sign/magnitude architectures, showing dramatically the lower gain error sensitivity of a sign/magnitude approach. Further, an offset binary converter requires a precise match (much better than ½ LSB) between the MSB resistor and the offsetting resistor. For outputs near 0V the MSB is switched on and all other bits are switched off (or MSB off, all other bits on), so small imbalances and drifts with time can easily cause a discontinuity at 0V which is proportional to the MSB weighting — i.e., an error proportional to one half of the full scale even for small signals.

On the other hand, in a converter using an internal sign/magnitude approach, the most significantly weighted resistors do not affect the current summing for outputs near 0V, so linearity is inherently superior when using the same quality resistors, both *initially* and *over time.* (Dynamic accuracy at zero is also superior because a zero crossing is not a major current switching point.)

Initial Linearity

For midrange outputs centered around 0V, the MP1926's linearity is better than ± ¼ LSB (4 ppm FSR). For outputs beyond midrange, the increment between codes equals the LSB step size of 15 ppm plus a differential nonlinearity of +13/–9 ppm FSR, *even at the major carries.* This ensures both monotonicity and no missing steps over the entire output range.

Long Term Stability

Most resistors, except for laboratory standard wire-wound types, exhibit tracking ratios worse than 15 ppm/year. In offset binary converters such resistor drift frequently results in significant linearity drift for signals near 0V; a converter using an internal sign/magnitude approach can be expected to be four or five times less sensitive to resistor drift. For signals centered around 0V (¼ FSR), *long-term linearity stability of the MP1926 is predicted to be much better than ½ LSB per year.*

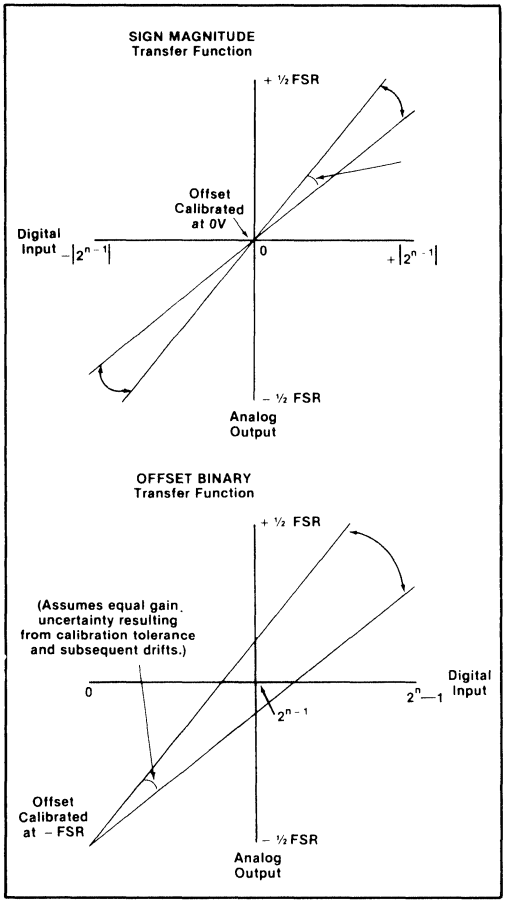


Figure 3. Comparison of Performance Near Zero. The transfer function of an offset binary converter originates at – FS (all current switches off). Thus 0V is usually ½ of FSR, and any gain drift will shift the 0V output as shown. With an internal sign/magnitude approach the transfer function originates at 0V (all current switches off), so the 0V output is not affected by gain drift.

The classical problem of attaining both low offset drift and high speed simultaneously when using a sign/magnitude approach has been solved by using the unique Magnitude Amplifier. (An offset error in the Magnitude signal would cause a discontinuity whenever the sign switches at a zero crossing, and would cause the output to be asymmetric about 0V). Earlier sign/magnitude approaches have met this low offset requirement by using slow amplifiers, limiting their applicability. The MP1926's Magnitude Amplifier is both chopper stabilized and fast. Its offset drift is an extremely low 1 μV/°C, yet the MP1926A settles to 1 LSB in only 5 μs. The converter has no offsetting resistor, so the only other contributor to offset drift is the output amplifier, resulting in less than 0.5 ppm/°C drift for the MP1926S. Therefore, the module's performance is symmetric about zero yet fast enough for a wide variety of applications.

In summary, the Analogic MP1926 sign/magnitude approach inherently provides better bipolar performance than would any offset binary approach using equal quality resistors and amplifiers. Furthermore, the precision chopper stabilized design of the MP1926 is the optimum internal implementation of the sign/magnitude approach. The resulting total improvement for a typical application (e.g., rms signal ±10% of the peak signal) can be on the order of 20 dB!

Input Decoding

The MP1926 may be connected to accept either of four input code types: offset binary, 2's complement, sign/magnitude, or modified sign/magnitude. Neither external decoding control nor an MSB input are required, because interconnecting the module per Table 1 automatically provides conversion to the sign/magnitude code used internally. Each code bit is supplied to one of 16 CMOS EXCLUSIVE OR gates. Each gate either follows or inverts the bit, depending on the state of the CONTrol signal connected to its second input.*

	MODULE CONNECTIONS			
CODE	SIGN to	CONT to	B1 CONT to	CODE SET to
Offset Binary	SIGN OUT	SIGN OUT	REF OUT	REF OUT
2's Complement	SIGN OUT	SIGN OUT	OUT RET	REF OUT
Sign/Magnitude*	SIGN OUT	OUT RTN	REF OUT	OUT RTN
Modified Sign/Magnitude*	SIGN OUT	OUT RTN	OUT RET	OUT RTN

*Sign Bit = B1

Table 1. Code Selection.

*For offset binary and two's complement operation, the CODE SET input connects a voltage available on the module to the 16th resistor in the network, offsetting the output by ½ LSB and thus avoiding the "+0V" and "–0V" codes implicit in sign/magnitude operation. The MP1926's offset control is factory adjusted to make this 17th bit offsetting transparent to the user who is supplying offset binary or 2's complement codes. To set up for sign/magnitude input coding, see the calibration procedure.

Output Range Selection

Outputs from the module have a low impedance and can drive up to 5 mA. The user may select the desired output voltage range by setting the gain of the Output Amplifier via the RANGE SET input. To select an output range of ±5V (10V FSR), connect RANGE SET to the bipolar OUTPUT. To select ±10V output range (20V FSR), connect RANGE SET to OUTPUT RETURN, and use ±15V power supplies.

Calibration

For audio and telecommunication applications, offset and range recalibration will rarely, if ever, be required. However, the module should be recalibrated whenever the full scale range is changed.

Comments

1. Interconnect the MP1926 per the application. Apply power and allow 5 minutes for warm-up.
2. Readjust the OFFSET control before readjusting the GAIN (range) control.
3. Refer to Table 2 for the corresponding codes and voltages.

Bipolar Zero Offset Adjustment Procedure

1. If supplying Offset Binary or 2's Complement input code, apply the code corresponding to zero while adjusting the OFFSET control so that the output is 0V ± the tolerance required for the application.
2. If supplying Sign/Magnitude or Modified Sign/Magnitude code:
a. Alternately apply the codes corresponding to +0V and −0V;
b. While so doing, adjust the OFFSET control so that the average value of these two outputs if 0V. (these two outputs will typically differ by less than 2 ppm.)

Range Adjustment Procedure

1. Apply a code corresponding to the largest voltage for which the absolute value is critical.
2. Adjust the GAIN control so that the output equals the corresponding voltage to within the application tolerance.

B1, B2, . . . , B15, B16	Bipolar Output
Offset Binary	
1 111 111 111 111 111	+4.999847V
1 000 000 000 000 000	0.000000V
0 000 000 000 000 000	−5.000000V
Two's Complement	
0 111 111 111 111 111	+4.999847V
0 000 000 000 000 000	0.000000V
1 000 000 000 000 000	−5.000000V
Sign/Magnitude	
1 111 111 111 111 111	+4.999847V
1 000 000 000 000 000	+0.000000V
0 000 000 000 000 000	−0.000000V
0 111 111 111 111 111	−4.999847V
Modified Sign/Magnitude	
0 111 111 111 111 111	+4.999847V
0 000 000 000 000 000	+0.000000V
1 000 000 000 000 000	−0.000000V
1 111 111 111 111 111	−4.999847V

Notes
For ±5V FSR, 1 LSB = 153μV
For ±10V FSR, multiply above voltages by 2.

Table 2. Input Coding.

TYPICAL APPLICATIONS

Professional Audio Systems

Figure 4 illustrates the highest performance, yet lowest cost solution available to the problem of simultaneously updating a stereo pair of analog outputs at rates up to 55 kHz from 16-bit resolution data. A conventional implementation would require two D/A converters, with digital double buffering for simultaneous update, feeding two output deglitch amplifiers. The MP1926A, with a voltage settling time of only 5 μs, allows two channels to be updated from a single D/A converter within the 18 μs available. The only buffering required for simultaneous updating can be provided by an AH201-1 Distortion Suppressor (Z1 in Figure 4.) The very low feedthrough (−100 dB) of the AH201-1 allows Channel 1 to be held while the MP1926A outputs Channel 2 data with negligible effect on Channel 1.

A deglitcher is always required at the output of D/A converter in audio aplications to minimize harmonic distortion. The AH201 is a deglitch amplifier designed specifically for use with the MP1926A in these applications. The Channel 2 AH201-2 deglitches by momentarily holding its output at ground during the time that the MP1926A is updating Channel 2. The Channel 1 AH201-2 holds its output at ground during the time that the AH201-1 is switching (see timing diagram). The response of the AH201 is time constant controlled (RC = 2 μs) to pass full power 20 kHz sine waves without output slew rate limiting (and subsequent distortion). The overall harmonic distortion of this configuration has been measured to be less than 0.005% (0.0005 dB!) over the frequency range of 20 Hz to 20 kHz.

For applications in which sequential updating of the outputs is acceptable, the AH201-1 shown in Figure 4 may be ommitted. Each half of the AH201-2 would be sequentially updated, coincident wih the D/A update of its channel data. Also, depending on the application, units may be driven from a single MP1926A.

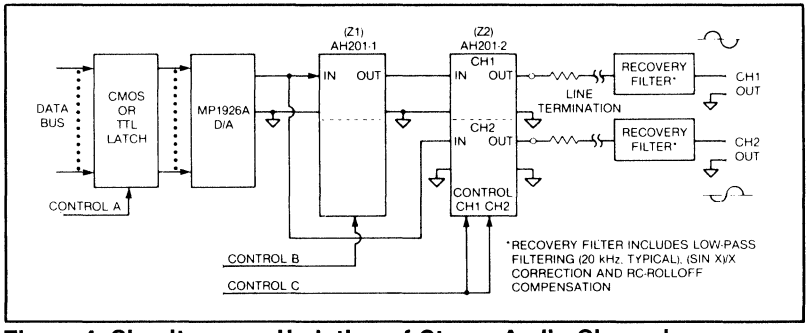


Figure 4. Simultaneous Updating of Stereo Audio Channels.

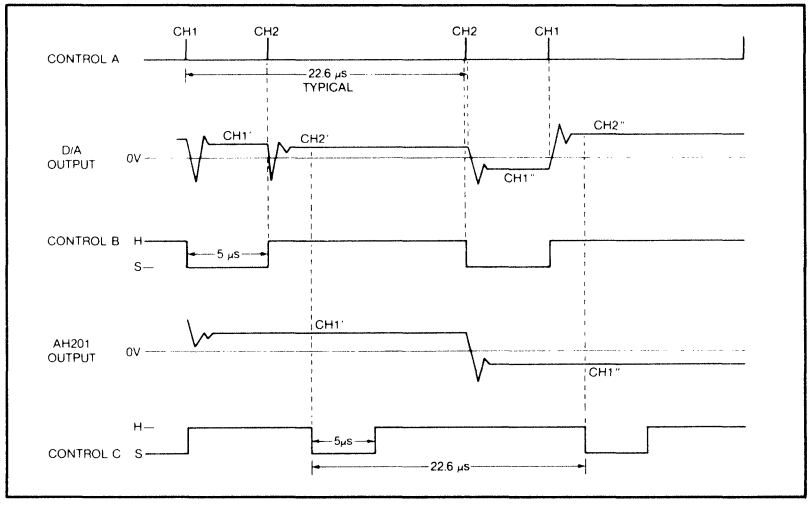
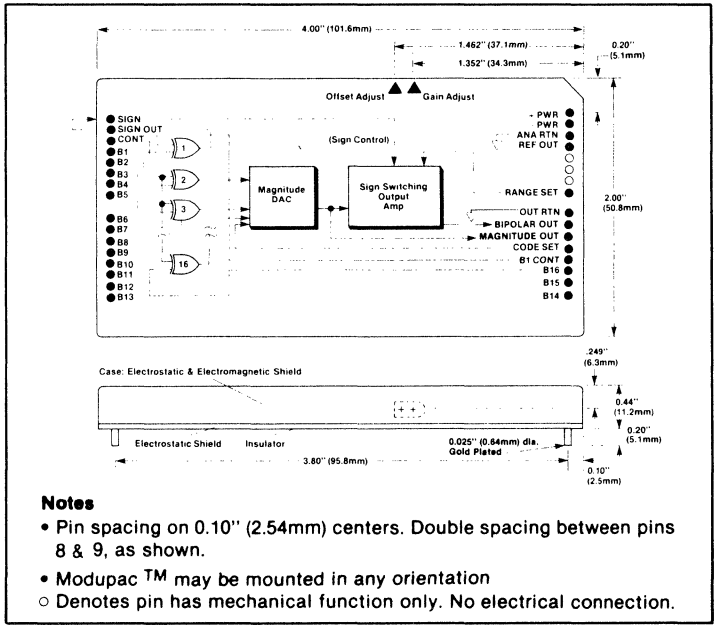


Figure 5. Typical Timing for Figure 4.



Notes

- Pin spacing on 0.10" (2.54mm) centers. Double spacing between pins 8 & 9, as shown.
- Modupac ™ may be mounted in any orientation

○ Denotes pin has mechanical function only. No electrical connection.

Figure 6. Mechanical & Pinout.

ORDERING GUIDE

For 3 μs settling time: Specify **MP1926A**

For 2 ppm of READING/°C gain stability: Specify **MP1926S**

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