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FOXFIRE™ II
Reference Manual
Rev. 1.3

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FOXFIRE™ II Reference Manual

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TABLE OF CONTENTS

1. ABOUT THIS MANUAL 1-1

1.1 INTRODUCTION 1-1
1.2 CONVENTIONS 1-1
1.3 ICONS 1-2
1.4 KEY WORDS AND DEFINITIONS 1-2

2. INTRODUCTION TO FOXFIRE™ II 2-1

2.1 PCI TECHNOLOGY 2-1
2.2 OVERVIEW OF FOXFIRE™ II 2-1
2.3 FOXFIRE™ II FEATURES 2-1

3. GETTING STARTED 3-1

3.1 UNPACKING 3-1
3.2 VISUAL INSPECTION 3-1
3.3 HANDLING THE FOXFIRE™ II CARD 3-1

4. INSTALLING FOXFIRE™ II 4-1

4.1 COMPARE SWITCHES 4-1
4.1.1 SW1 Definitions and Default Settings 4-1
4.1.2 SW2 Default Settings 4-2
4.1.3 Latency Monitor LEDs 4-2
4.1.4 Power Management LEDs 4-3

5. SALES AND TECHNICAL SUPPORT 5-1

6. HARDWARE REFERENCE 6-1

6.1 BOARD MODES 6-1
6.2 BOARD MODE CONTROL 6-3
6.2.1 0x40 Master Control Register 6-3
6.2.2 0x44 Status Register 6-5
6.3 BOARD MODE DESCRIPTION 6-6
6.3.1 Write and TRDY Latency Monitor (Latency Mode) 6-6
6.3.1.1 Write Latency Monitor Register Information 6-8
6.3.1.2 FRM to TRDY Latency Monitor Register Information 6-8
6.3.2 BIOS Test Card (BIOS Mode) 6-9
6.3.2.1 BIOS Test Card Register Information 6-10
6.3.2.2 Loading Configuration Data 6-12
6.3.2.3 Using BIOS Test Mode 6-14
6.3.2.4 Base Address Register Programming Examples 6-16
6.3.3 Power Management (Power Management Mode) 6-16
6.3.3.1 PCI Configuration Space Additions 6-16
6.3.3.2 Power Management Registers 6-17
6.4 TEST HARDWARE 6-20
6.5 FOXFIRE™ II REGISTER MAP 6-22

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1. About This Manual

1.1 Introduction

This guide, the FOXFIRE™ II Reference Manual, describes how to install, maintain and program the FOXFIRE™ II board. Topics covered in the manual include installation and board hardware.

1.2 Conventions

A variety of text styles are used throughout the manual to call attention to specific items.

Convention	Description
Text represented as `screen display`	This typeface is used to represent displays appearing on the screen, such as: at the "`A:\`" prompt
Text represented as `commands`	This typeface is used to represent commands that are to be entered, such as: type "`setup`"
Keys	When specific keys are referred to they are designated by their labels, such as "the Enter key" or "the Escape key", or they may be shown as [Enter] or[Esc]. When two or more keys are to be pressed simultaneously, the keys are linked with a plus sign (+). For example: [Ctrl] + [Alt] + [Del]
Text represented in ***bold italics***	This typeface is used to designate equations being used in the text.

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1.3 Icons

Throughout the manual, important information is highlighted with icons.

Icon	Type	Description
	Information Note	Information Notes call attention to important features or instructions.
	Caution	Cautions are directions that must be followed in order to avoid loss of system data and/or damage to hardware.
	Warning	Warnings are directions that must be followed to ensure personal safety.

1.4 Key Words and Definitions

Some of the terms used throughout the manual are defined below.

BIOS

Basic Input/Output System. Responsible for centralizing the task of allocating and deallocating system resources, which is crucial for achieving a resource conflict-free system.

Configuration Cycle

A special cycle used to access the configuration space of a function or device. The C/BE bits are 0xA for a read and 0xB for a write. IDSEL is also asserted during this cycle to inform the target board that AD[31:00] is in a specially encoded format. Bits [10:8] select the function number, bits[7:0] select the address in configuration space and bits [31:11] are reserved.

Configuration Space

Configuration space consists of 256 bytes that hold vital information about that particular board. The first 64 bytes make up the Predefined Header that holds information such as device and vendor IDs, board status and board control. The base address registers for the board are also stored here.

Expansion ROM Base Address Register

Located at offset 0x30 in configuration space, it is a base address register used by the system only at boot up. If it is enabled, then the system will shadow (copy) the entire contents

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into system RAM so it can be executed. Executing instructions off the board itself would be too slow to be practical. Once the system has come up, this base address register is shut down and not used.

Function

The PCI specification allows each device to have up to eight functions, or sets of configuration data. Different functions are selected by the special address cycle used during a configuration space access.

Mode

A feature of the FOXFIRE™ II board. The three modes are: Latency Mode, BIOS Mode, and Power Management Mode.

PCI

Peripheral Component Interconnect.

PCI Retry

A form of termination of a PCI cycle. It indicates that no data has been accessed during the cycle but the data can be accessed at a later time. A well designed card should always attempt to complete the current bus cycle without a retry.

PCI SIG

Peripheral Component Interconnect (PCI) Special Interest Group. See http://www.pcisig.com.

Soft Boot

Restarting the computer without cycling power.

Threshold

The value in PCI clocks before the FOXFIRE™ II board decides that a latency time violation has occurred.

Write-Lockable

When a bit is write-lockable, the corresponding mask bit must be a 1 for a write to occur. When the mask bit is a 0 then the data is left untouched.

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2. INTRODUCTION TO FOXFIRE™ II

2.1 PCI Technology

The Peripheral Component Interface (PCI) bus is a high-performance bus that provides a processor-independent data path between the host CPU in a PC and high-speed peripherals. This interconnect mechanism is designed specifically to accommodate multiple high-performance peripheral devices.

The PCI specification defines two types of PCI devices: initiator and target. The initiator, or bus master, is a more intelligent device that can conduct processing independently of the bus or other devices. A bus master device shares the bus with the main processor and targets. Bus mastering allows a peripheral device to take control of the system bus and not rely on the central processor. A target is a device that accepts commands and responds to the requests of a initiator.

The PCI specification supports automatic configuration. The PCI bus can run at a clock speed up to 33 MHz and employs a 32-bit data bus that supports multiple peripheral components and add-on cards at a peak bandwidth of 132 MBps, up to an order of magnitude greater than that of other PC buses (ISA, EISA, or MCA). A PCI adapter has configuration specifications set in on-board memory and provides installation information to the computer at start-up.

2.2 Overview of FOXFIRE™ II

2.3 FOXFIRE™ II Features

Features of the FOXFIRE™ II board include:

- Monitoring of write-latency
- Monitoring of TRDY latency
- BIOS test card
- Power Management compliance testing

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3. GETTING STARTED

3.1 Unpacking

The FOXFIRE™ II board is shipped in a static sensitive pack.



CAUTION

Before removing the board from the static pack, be sure to be grounded of any and all static electricity. Static discharge to the FOXFIRE™ II board could damage sensitive components.

3.2 Visual Inspection

Before installing the FOXFIRE™ II board in the computer, visually inspect it for damage that may have occurred during shipping.

3.3 Handling the FOXFIRE™ II Card

The FOXFIRE™ II Card should be held by the edges. Avoid touching any of the components on the board's surface, as they are sensitive and can be easily damaged.

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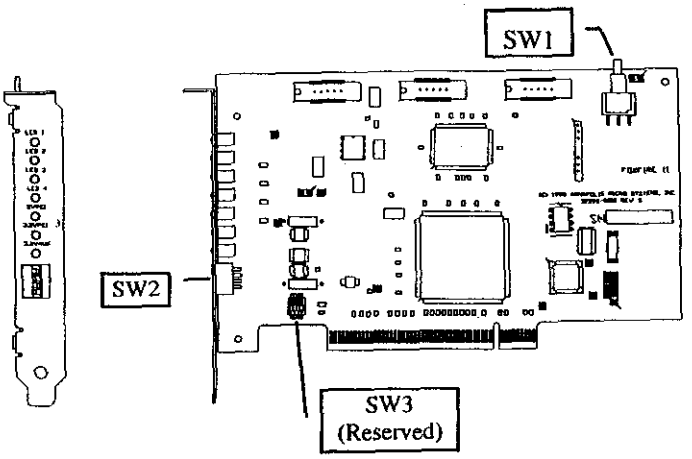


Figure 3-1: The FOXFIRE™ II Card

(Component Side)

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4. INSTALLING FOXFIRE™ II

The following section provides instructions on installing the FOXFIRE™ II board into the PCI host system.

4.1 Compare Switches

FOXFIRE™ II is delivered with all of its switches in their default settings. (See Figure 3-1 for the location of the switches on the FOXFIRE™ II board.) Carefully compare the switches on the FOXFIRE™ II board to the information below. Make sure that all of the switches are set accordingly.

4.1.1 SW1 - PME Momentary Push-Button

This push-button switch located on the top card edge is used to force assertion of PME#. See Section 6.4 for a detailed description of the PME Momentary Push-Button.

4.1.2 SW2 Definitions and Default Settings

SW2 Position #	ON	OFF
1	SRAM Base Address Register functional (will appear) on initial boot-up. Card will request 1 MB (default) of memory space.	Will not appear/disabled; will return all zeroes when read. Card will not request resources.
2	PME_En and PME_Status initialization will be "1b". When this switch is in the ON position the card's PME# output will be asserted immediately upon initially powering up the card. This feature is useful in determining whether the platform under test properly initializes the system's "sticky bits".	PME_En and PME_Status initialization will be "0b"
3	Vendor ID/Device ID stored in SRAM when BIOS test mode enabled	AMS Vendor ID/Device when BIOS test mode enabled
4	Write Latency monitor (Latency Mode) enables on power up.	Write Latency Monitor (Latency Mode) disabled on power up of system

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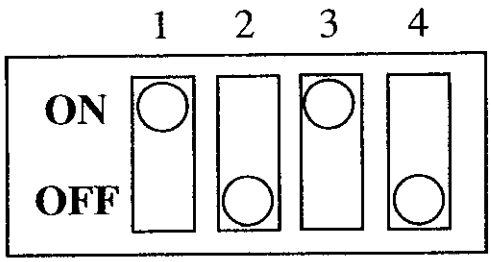


Figure 4-1: SW2 Default Settings

4.1.3 SW3 Default Settings

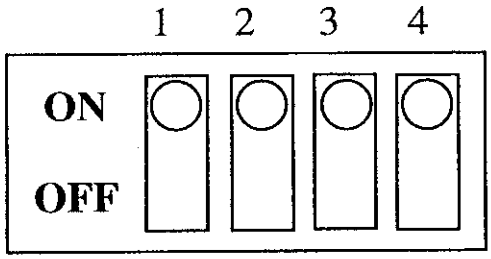


Figure 4-2: SW3 Default Settings

4.1.4 Latency Monitor LEDs

The following table shows the significance of each of the LEDs on the FOXFIRE™ II rear panel. See diagram 3-1 for location

LED #	Color	Purpose
1	Red	Write Latency Time-out
2	Green	Latency Mode in progress
3	Red	TRDY Time-out
4	Green	Board Power/Xilinx PCI Programmed

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4.1.5 Power Management LEDs

The LEDs in the following table illustrate which types of power the host machine supports. A lighted LED signifies that the corresponding power supply is currently supplying the proper voltage. *See diagram 3-1 for* location.

LED	Color	Purpose
3.3VPCI	GREEN	3.3VPCI Power
5VPCI	GREEN	5VPCI Power
3.3VAUX	GREEN	3.3Vaux Power

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5. SALES AND TECHNICAL SUPPORT

Please direct any questions or comments regarding the FOXFIRE™ II board to PCI SIG. as indicated below.



INFORMATION NOTE

If you have any questions about installing, programming, using, or maintaining your FOXFIRE™ II board, please contact PCI SIG at techsupp@pcisig.com, or fax to (503) 693-8344.

On-line sales and order information are available on the PCI SIG website: http://www.pcisig.com.

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6. HARDWARE REFERENCE

6.1 Board Modes

The FOXFIRE™ II board has one mode for determining the latencies of a PCI card, one mode for BIOS testing, and another for testing power management compliance. It is designed to be used with host software which controls the various modes that are available on the card.

The first mode (Latency Mode) monitors the PCI bus for unusually long retried write transactions and will light an LED as well as assert an interrupt request (if interrupt requesting is enabled) when one is observed. Software is able to program the threshold (measured in PCI clocks) where this error condition is triggered. Once an illegal transaction occurs, FOXFIRE™ II locally stores the address where the retried write had occurred to assist the user in determining which card was responsible for that particular transaction. This mode is useful in pinpointing PCI functions that violate the PCI Local Bus Specification's 10uS maximum completion rule. In addition to measuring retried write latency, Latency Mode can also simultaneously measure Target Ready (TRDY) latencies. FOXFIRE™ II will light a different LED and/or interrupt when TRDY does not become asserted within a programmable time after FRAME is asserted. By latching the address and control bits of the transaction where a FRAME# to TRDY# latency violation has occurred, it is possible to identify PCI functions that are not conforming to the PCI Local Bus Specification's 16 clock FRAME# to initial TRDY# rule.

The second mode (BIOS Mode) available on the FOXFIRE™ II board is designed for testing the BIOS. This mode is useful for seeing how a BIOS allocates resources during boot up. FOXFIRE™ II is capable of having up to eight functions implemented simultaneously, allowing for the testing of eight different scenarios at once. BIOS Mode also allows for a 224K byte ROM that is mapped off the expansion ROM base address register when enabled. Each function will share the same ROM, but will have unique interrupts (described later). The on-board SRAM allows storage of the ROM data and also the configuration information for all eight functions. The entire 256 byte configuration space for each function will be write-lockable (unless otherwise specified) and the corresponding mask registers will also be stored in the SRAM. It is possible to load the SRAM using an indirect address method or by enabling a base address register to access the SRAM directly.

The third mode (Power Management Mode) enables testing for compliance to the PCI Bus Power Management Interface Specification (Revision 1.1). FOXFIRE™ II is fully compliant and allows testing for Host compliancy. It is possible to wake a system out of the D3cold State manually by asserting PME# using the PME momentary push-button on

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the card. Host software can also cause an assertion of PME# in the D0-D3hot states. The FOXFIRE™ II card also automatically detects what variety of PCI power (3.3VPCI, 5VPCI, 3.3Vaux) is being supplied and will adjust accordingly. All three modes of operation are available if 5VPCI is available. To validate that the host system under test is capable of delivering the minimum required current for 3.3Vaux as defined for each state, FOXFIRE™ II can simulate a load on its 3.3Vaux pin of 20, 160, or 375 mA (+/- 5% for 160 and 375 mA loads and +0% /-25% for 20mA load). This programmable 3.3Vaux loading feature is also useful for validating that the system is properly budgeting available 3.3Vaux auxiliary power. The PME_Status and PME_En bits can also have their initial values set by a switch (SW1), which is useful for testing that the host system under test properly initializes these "sticky bits".

The different modes are described with more detail in section 6.3. Controlling the modes is described below in section 6.2.

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6.2 Board Mode Control

6.2.1 0x40 Master Control Register

The master control register is available in all three modes. Its primary function is to enable/disable modes and control board level functionality. When the FOXFIRE™ II card is in BIOS Mode it cannot run any other modes. Below is a brief description of how to run each mode:

Latency Mode Control: Setting bit 3 high will enable Latency Mode. Bits 1 and 2 control Latency Mode interrupts; setting bit 1 high will enable write latency interrupts and setting bit 2 high will enable TRDY latency interrupts. To clear an interrupt, write a zero to the respective enable bit. Once an interrupt is cleared, the enable bit may be set again and will not produce another interrupt until RESET is toggled. Although the write latency time-out LED is always enabled, the TRDY LED is enabled by setting bit 5 High. To reset Latency Mode, toggle bit 0 low-high-low. Since it is possible to set SW4 on the PCI panel to have Latency Mode enabled without software, bit 16 is a switch disable allowing software to override the switch setting.

BIOS Mode Control: Setting bit 7 high will enable BIOS Mode and setting bit 10 high will enable BIOS Mode interrupts. Bit 8 shows the status of the INT pin for the function being accessed. Functions 0, 3, 6 and 7 use INTA#; functions 1 and 2 use INTD#; function 4 uses INTB#; and function 5 uses INTC#. Writing a 1 to this bit will set the interrupt line, while writing a 0 will clear the interrupt. All modes can access this register. Setting bit 9 will enable interrupt mirroring where the FOXFIRE™ II board will also assert its interrupt on a line where another interrupt has been asserted. Bits 23:20 show the status of the interrupts that were asserted; bit 23 is INTD# ranging down to bit 20 which shows the status of the INTA# line. Writing a 0 to any of these bits will clear the interrupt on that line. Bit 11 will be high if a PCI reset was seen on boot and can be cleared by writing a zero to this bit. Bits 14:12 represent the current function being accessed.

Power Management Mode Control: There are no Power Management Mode control bits in this register. Refer to section 3.3.3.2 for control of this mode.

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Master Control Register

Bit	Name	Purpose	Type	Default
0	RESET	toggle 0-1-0 to reset Latency; Latency Mode is in reset when 1	R/W	0
1	TRDY_INT_EN	Latency Mode Interrupt enabled for FRM to TRDY latency time-out if 1	R/W	0
2	LM_INT_EN	Latency Mode Interrupt enabled for write latency time-out if 1	R/W	0
3	LM_EN	enables Latency Mode when 1; switch 4=ON can also enable Latency Mode unless disable bit is set (Bit 16)	R/W	0
4		RESERVED		0
5	TRDY_LED_EN	enables Latency Mode TRDY LED when 1	R/W	0
6		RESERVED		0
7	BM_EN	enables BIOS Mode when 1	R/W	0
8	BM_INT_PIN	shows status of selected functions interrupt for BIOS Mode. Writing a 1 to this bit will set that functions interrupt line; writing a 0 will clear it	R/W	
9	INT_MIR_ENB	PCI interrupts will be mirrored if 1	R/W	0
10	BM_INT_EN	enables BIOS Mode interrupt when 1	R/W	0
11	PCI_RST	PCI reset seen on soft boot when 1, clear by writing 0	R/W	0
12	BM_FUNCT0	BIOS Mode function bit 0	R	
13	BM_FUNCT1	BIOS Mode function bit 1	R	
14	BM_FUNCT2	BIOS Mode function bit 2	R	
15		RESERVED		
16	LM_SWTCH	Latency Mode enable switch (4); switch cannot enable Latency Mode when 1	R/W	0
17		RESERVED		0
18 19	BM_ROM_ALIAS0 BM_ROM_ALIAS1	00-Alias first 32K bytes of ROM 01-Alias first 64K bytes of ROM 10-Alias first 128K bytes of ROM 11-Alias all 224K bytes of ROM	R/W	00
20	BM_MIR_INTA#	interrupt line A set when 1 during interrupt mirroring; write 0 to clear	R/W	0
21	BM_MIR_INTB#	interrupt line B set when 1 during interrupt mirroring; write 0 to clear	R/W	0
22	BM_MIR_INTC#	interrupt line C set when 1 during interrupt mirroring; write 0 to clear	R/W	0
23	BM_MIR_INTD#	interrupt line D set when 1 during interrupt mirroring; write 0 to clear	R/W	0
24	BM_FUNCT0_EN	enables function 0 when 1	R	1
25	BM_FUNCT1_EN	enables function 1 when 1	R/W	0
26	BM_FUNCT2_EN	enables function 2 when 1	R/W	0
27	BM_FUNCT3_EN	enables function 3 when 1	R/W	0
28	BM_FUNCT4_EN	enables function 4 when 1	R/W	0
29	BM_FUNCT5_EN	enables function 5 when 1	R/W	0
30	BM_FUNCT6_EN	enables function 6 when 1	R/W	0
31	BM_FUNCT7_EN	enables function 7 when 1	R/W	0

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6.2.2 0x44 Status Register

The status register is available in Latency and Power Management Modes. It is generally Read Only except for a couple of read/write bits which are marked accordingly below. LEDs 1, 2 and 3 may be turned on by writing a 1 to their status register and turned off (unless a time-out has actually occurred) by writing a zero to the same bit.

Latency Mode Status: Bit 1 high shows that a Latency Mode write latency time-out interrupt is pending and bit 2 high shows that the Latency Mode write latency time-out LED is on. Bit 16 high signifies that an interrupt for the FRM to TRDY latency timer is pending. Latency Mode interrupts can be cleared by either resetting Latency Mode or clearing the appropriate interrupt enable bit located at bits 1 and 2 in the master control register. Bit 19 will be high if a FRM to TRDY time-out has occurred and will be cleared on a reset. If bit 18 is set then the FRM to TRDY latency time-out counter has reached its terminal count of 64 PCI clocks. Bit 0 shows the current status of the INT A pin. Bit 15 high represents that switch 4 on the PCI panel is on, enabling Latency Mode (unless disabled by setting bit 16 in the master control register high).

Power Management Mode Status: There are no Power Management Mode control bits in this register. Refer to section 3.3.3.2 for status of this mode.

Miscellaneous Status Bits: Bits 31:24 indicate current design version and revision. Bits 15:12 represent the current position of the back panel switches. If a bit it high that corresponds to the switch being set to the ON location. These bits are provided so that software can check their positions to determine different board modes. If bit 12 was high (switch 1) that would let the software know that the board has requested memory space through Base Address Register 0 (assuming BIOS Mode is disabled). If bit 14 was high (switch 3) then the device ID will be set to 0x003 and vendor ID will be set to 0x12DB for all 8 functions when BIOS Mode is enabled regardless of what is stored SRAM. If bit 15 (switch 4) is set that would indicate that Latency Mode is already enabled and the software could determine if this was correct. If not, the switch can be disabled by setting bit 16 high in the master control register.

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Status Register

Bit	Name	Purpose	Type
0	INTA	reflects PCI bus INT #A line	R
1	LM_INT	Latency Mode interrupt pending when 1; writing 0 to bit 2 in master control register will clear	R
2	LM_LED	shows status of Latency Mode write latency time-out LED (RED, LED1), writing a 1 will turn on	R/W
3		RESERVED	
4		RESERVED	
5		RESERVED	
6		RESERVED	
7		RESERVED	
8	LM_TRDY_LED	shows status of Latency Mode TRDY latency time-out LED (RED, LED 3), writing a 1 will turn on	R
9	IN_PROG_LED	shows state of LED 2 (Green) indicating Latency Mode is in progress	R/W
10		RESERVED	
11		RESERVED	
12	SW1-1	Panel Switch 1 setting; bit will be 1 when switch=ON	R
13	SW1-2	Panel Switch 2 setting; bit will be 1 when switch=ON	R
14	SW1-3	Panel Switch 3 setting; bit will be 1 when switch=ON	R
15	SW1-4	Panel Switch 4 setting; bit will be 1 when switch=ON	R
16	LM_TRDY_INT	FRM to TRDY latency time-out interrupt pending when 1; writing 0 to bit 1 in master control register will clear	R
17		RESERVED	
18	LM_TRDY_TC	FRM to TRDY latency time-out counter has reached terminal count when 1 (64 PCI clocks)	R
19	LM_TRDY_TMO	FRM to TRDY latency time-out when 1	R
20		RESERVED	
21		RESERVED	
22		RESERVED	
23		RESERVED	
24	REVISION_BIT1	Bit 1 of current design revision	R
25	REVISION_BIT2	Bit 2 of current design revision	R
26	REVISION_BIT3	Bit 3 of current design revision	R
27	REVISION_BIT4	Bit 4 of current design revision	R
28	VERSION_BIT1	Bit 1 of current design version	R
29	VERSION_BIT2	Bit 2 of current design version	R
30	VERSION_BIT3	Bit 3 of current design version	R
31	VERSION_BIT4	Bit 4 of current design version	R

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6.3 Board Mode Description

6.3.1 Write and TRDY Latency Monitor (Latency Mode)

A write transaction that is continually retried to the extent that the transaction takes more PCI clocks to successfully complete than the number of PCI clocks specified in the 16-bit time-out register (address 0x48) is said to be in violation of the maximum write latency rule. (The PCI Local Bus Specification dictates that write transactions must complete in less than or equal to 10uS). When a write latency violation is detected FOXFIRE™ II will light a red LED (LED 1) as well as signal an interrupt request on INTA# (if enabled). The default setting for this register is 10 microseconds (0x14A PCI clocks). When a retry transaction is sensed by the card, the address is latched into a 32 bit register (address 0x50) and the counter will be enabled, incrementing with every PCI clock. If the PCI master completes the retry before the time-out is reached, the card will go to an IDLE state and wait for another retry.

It is assumed that only one retry transaction will be followed at a time, and all other retries occurring between the currently tracked retry and completion by the Host will be ignored. It is also assumed that it is possible to miss an illegal transaction if a long legal transaction occurs just before an illegal transaction begins. Here the card would miss the illegal transaction because it would be "masked" by the long legal transaction. The illegal transaction would not be tracked since only one transaction is tracked at a time. This scenario is considered to be extremely rare and is ignored.

A TRDY latency violation is detected by FOXFIRE™ II within a PCI transaction if the target of that transaction holds off the assertion of its initial TRDY to the extent that the number of clocks between FRAME assertion and TRDY assertion is greater then the number of PCI clocks specified in the 6-bit time-out register (address 0x70). (The PCI Local Bus Specification dictates that a target's initial TRDY assertion shall not exceed 16 clocks following the assertion of FRAME for that transaction). When a TRDY violation is detected FOXFIRE™ II will light a red LED (LED 3) as well as signal an interrupt request on INTA# (if enabled). The default setting for this register is 0x0F. When FRAME is asserted, the address is latched into a 32 bit register (address 0x60) and the counter is enabled, incrementing with every PCI clock. If the target board asserts TRDY before the time-out is reached, FOXFIRE™ II will go into an IDLE state and wait for the next assertion of FRAME. The FRAME to TRDY latency timer will only respond to addresses greater than the address stored at 0x6C.

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Once a time-out is reached, either a power-on reset or software reset is required to restart this mode.

No software will be required to start this mode running since this mode can be enabled with SW1.4 in the ON position. Software will be required to change the latency time-out register value, enable the interrupt capability when a time-out is reached, read the address at which the latency time-out occurred, reset the board without resetting the system, and disable the LED when a latency time-out is encountered.

6.3.1.1 Write Latency Monitor Register Information

0x48 Write Retry Time-out Register-*Read/Write*-The time-out register holds the number of PCI clocks the mode will wait until it realizes a time-out. It will default to 0x14A or 10 microseconds if the PCI clock period is 30.3 nanoseconds.

0x4C Write Retry Count Register-*Read Only*-This 16 bit counter will begin counting when a retried transaction is sensed and no other retried transaction is being tracked. It will be incremented on every PCI clock after retry is sensed and the address is latched, and will count until a maximum count is reached or a board reset is given.

0x50 Write Retry Address Register-*Read Only*-This register holds upper 30 bits of the offending retried address. It is loaded every time a new test is started and not cleared until a completion is seen before latency time-out or a board reset.

6.3.1.2 FRM to TRDY Latency Monitor Register Information

0x60 TRDY Time-out Address Register-*Read-Only*-The 32 bit target address of the offending transaction will be written to this register when a FRAME to TRDY latency time-out is detected.

0x6C TRDY Address Compare Register-*Read/Write*-This register will compare its value to the PCI address and only allow monitoring of the FRM to TRDY latency timer if the PCI address is **greater**. Only bits [31:24] are implemented so bits [23:00] will always return zero. The current default value for this register is 0xF0000000. If this register is set to 0x0 then all PCI accesses will be monitored.

0x70 TRDY Latency Time-out Register-*Read/Write*-This time-out register will hold the number of PCI clocks allowed between when FRAME is first asserted to when TRDY is first asserted before a time-out is issued. The default value for this register is 0x0F.

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0x74 TRDY Latency Counter/Cycle Monitor-*Read Only*- Reading bits [29:24] of this counter/register after a time-out is issued will provide the number PCI clocks that were actually needed between when FRAME was first asserted to when TRDY was first asserted. This is a six bit counter so the maximum number of clocks that can be counted is 64. If more than 64 clocks are counted then bit 18 (LM_TRDY_TC) will go high in the status register until a reset is given. Bits [19:16] correspond to CBE bits [3:0] while FRAME is asserted. All other bits in this register will always return 0.

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6.3.2 BIOS Test Card (BIOS Mode)

BIOS Mode is used to test a computer BIOS's ability to handle the enumeration of detected PCI functions during the boot process, allowing the user to introduce up to eight functions, each one having unique characteristics. Since this board will be used to test functionality of the BIOS, FOXFIRE™ II retains its configuration over a soft boot (no power-cycling). This is important because the board can only be configured after the Host has gone through an initial boot-up and the board is Host accessible. Each function is mapped to a specific interrupt line and is capable of generating its own interrupt (if enabled). Although function 0 will always be active, it is possible to enable any combination of functions 1 through 7. All eight "functions" are stored in the SRAM at different offsets. There are eight register bits (bits [31:24] in the master control register) that select which of the eight available functions will appear in the next PCI bus scan. Since the configuration registers for each function will be stored in memory, the hardware collects register values from memory and loads them into a physical register in the PCI chip when a configuration register access is done. If a write is being performed, the PCI chip will perform a write-locked operation and then write the value back to memory.

FOXFIRE™ II will also support an expansion ROM that all functions will share. The ROM will be aliased throughout the space allotted to it by the system. The size that is aliased is selectable as the first 32Kb, 64Kb, 128Kb or 224 Kb of the ROM and is set using bits 18 and 19 in the master control register. While the BIOS test mode is active, the ROM is read-only.

The 256-byte configuration space will be divided as shown below where the predefined header will have special characteristics for each function. There is also a corresponding 256-byte space for mask registers starting at byte offset 0x100. Each register in configuration space has a corresponding mask register at its address plus a byte offset of 0x100.

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Configuration Space

Byte Offset	Name	Type	Size Bytes
0x000-0x03C	Predefined Header	Write-Locked	64
0x040	Device Specific Control	Read/Write	4
0x044	Address Register	Read/Write	4
0x048	Data Register	Read/Write	4
0x04C-0x050	Scratch Registers	Write-Locked	8
0x054	Expansion ROM Base Address Mask Register	Read/Write	4
0x058-0x0FC	Scratch Registers	Write-Locked	168
0x100-0x1FC	Mask Registers	Read/Write	256

6.3.2.1 BIOS Test Card Register Information

The predefined header space has two different kinds of read/write characteristics:

Read/Write- Bytes and fields have some bits that can be directly modified.

Write-Lockable- Bytes that are write-lockable can only be written to if their corresponding mask bit is a 1. If their corresponding mask bit is a 0, then data is unmodified during a write.

There are only two bits with special purposes that are implemented in the predefined header for BIOS Mode besides the Expansion BAR. The first is bit 1 of the Command register which is the memory decode enable bit and is unique to each function. This bit is always read/writeable. In addition, bit 0 of the Expansion BAR is unique to each function and is the ROM decode enable bit. The corresponding mask for the ROM decode enable bit is located at address 0x54 (bit 0). This mask bit is also unique to each function although the rest of the Expansion ROM mask register (bits 31:01) is the same across all functions.



INFORMATION NOTE

In order for the Expansion ROM to be decoded, both the memory enable bit and the ROM decode enable bit must be set in the same function.

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The predefined header space will be set up as follows:

Predefined Header Space

Byte Offset	Name	Type	Size Bytes
0x00-0x01	Vendor ID	Write-Lockable	2
0x02-0x03	Device ID	Write-Lockable	2
0x04-0x05	Command	Write-Lockable except bit 1 which is Read/Write	2
0x06-0x07	Status	Write-Lockable	2
0x08	Revision ID	Write-Lockable	1
0x09-0x0B	Class Code	Write-Lockable	3
0x0C	Cache Line Size	Write-Lockable	1
0x0D	Latency Timer	Write-Lockable	1
0x0E	Header Type	Write-Lockable	1
0x0F	BIST	Write-Lockable	1
0x10-0x27	Base Address 0-6	Write-Lockable	24
0x28-0x2F	Reserved	Write-Lockable	8
0x30-0x33	Expansion ROM Base Address reg.	Write-Lockable	4
0x34-0x3B	Reserved	Write-Lockable	8
0x3C	Interrupt Line	Write-Lockable	1
0x3D	Interrupt Pin	Write-Lockable	1
0x3E	Min_Gnt	Write-Lockable	1
0x3F	Max_Lat	Write-Lockable	1

To load the SRAM with both ROM data and configuration data, there is an indirect addressing scheme set up which is capable of accessing any data in the SRAM. This will be explained further in section 6.3.3.2 "Loading Configuration Data." The registers used for this are listed below along with the ROM mask register.

0x44 SRAM Address Register-*Read/Write*-This register is to be used along with the SRAM data register at 0x4C to access the SRAM using indirect addressing. By first writing the target address into this register, it is possible to access data stored in the SRAM by reading or writing from 0x48.

0x48 SRAM Data Register-*Read/Write*-This register is memory mapped into the SRAM at the address stored at 0x44.

0x54 Expansion ROM Base Address Mask Register-*Read/Write*- This register holds the mask value for the Expansion ROM Base Address Register located at 0x30. The Expansion ROM base address register is write-masked. Only the upper 16 bits of this register

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are implemented. Bit 0 is implemented differently than the rest of the register since it is unique to each functions. However, its functionality inside a particular function remains the same



INFORMATION NOTE

For BIOS Mode, the registers at addresses 0x40, 0x44, 0x48 and 0x54 (bits 31:01) are common to all functions. Therefore, any bit modified in any function will modify that bit in all functions.

6.3.2.2 Loading Configuration Data

For the BIOS test mode to boot up it is essential to load the SRAM with configuration data for all the functions that will be enabled. Methods 1 and 2 are also used to load the data for the Expansion ROM. For convenience there are three ways to load configuration data into the SRAM:

Method 1: Using Memory Base Address Register

The FOXFIRE™ II board is shipped with SW1.1 turned ON which will request 1 MB (default) of memory space for base address register 0. Since this base address register is essentially the same as the Expansion ROM base address register, they have the same mask register located at byte address 0x54 in configuration space. This mask register defaults to 0xFFF0000 to request the 1 Mb of memory space.

This method is the most straightforward and quickest to use. Since the entire SRAM is mapped onto this base address register it is easy to load PCI configuration data, the corresponding configuration mask information and the ROM data. The ROM starts at offset 0 and goes up to byte offset 0x37FFF. The configuration data starts at byte offset 0x38000. The offsets for individual functions can be found below in the "SRAM Offsets" table.

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INFORMATION NOTE

It only possible to use this method for loading if the BIOS test mode is disabled since this space will become read-only when the BIOS test mode is enabled.

Method 2: Indirect Addressing

This method is useful if it is impractical or impossible to use a base address register at power-up since it only involves configuration space read and writes. It is also a way to load or check data in the SRAM after the BIOS test mode is enabled. Unlike method 1, the BIOS test mode must be enabled for this method to work. To load (or read) the SRAM with this method first write the target address to the indirect address register located at byte address 0x44 in configuration space. Next, either read or write (depending on desired operation) to the indirect data register located at byte address 0x48 in configuration space. Addresses correspond to the offset into the SRAM and can be found below in the "SRAM Offsets" table.

Method 3: Direct Writes to Configuration Space

Although this is another method of loading the SRAM, it requires using one of the two above methods to be effective. This method involves direct writes or reads to configuration space once the BIOS test mode is enabled. This method is what the PCI bridge sees when it accesses configuration space so writes to the SRAM (configuration writes to the bridge) are susceptible to the mask settings. If a bit is write-locked then it is impossible to write through to the SRAM. Since the mask registers lie at addresses outside of configuration space, methods 1 or 2 must be used to modify the mask registers if a write is to be successful.

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SRAM Offsets

Partition Name		Byte offset	Dword offset	Size (Bytes)
Read Only Memory (ROM)	Alias Select bits	0x00000-	0x0000-	
	00	0x07FFF	0x1FFF	32K
	01	0x0FFFF	0x3FFF	64K
	10	0x1FFFF	0x7FFF	128K
	11	0x37FFF	0xDFFF	224K
Function 0		0x38000-0x380FF	0xE000-0xE03F	256
Function 0 Mask		0x38100-0x381FF	0xE040-0xE07F	256
Function 1		0x38200-0x382FF	0xE080-0xE0BF	256
Function 1 Mask		0x38300-0x383FF	0xE0C0-0xE0FF	256
Function 2		0x38400-0x384FF	0xE100-0xE13F	256
Function 2 Mask		0x38500-0x385FF	0xE140-0xE17F	256
Function 3		0x38600-0x386FF	0xE180-0xE1BF	256
Function 3 Mask		0x38700-0x387FF	0xE1C0-0xE1FF	256
Function 4		0x38800-0x388FF	0xE200-0xE23F	256
Function 4 Mask		0x38900-0x389FF	0xE240-0xE27F	256
Function 5		0x38A00-0x38AFF	0xE280-0xE2BF	256
Function 5 Mask		0x38B00-0x38BFF	0xE2C0-0xE2FF	256
Function 6		0x3C800-0x3C8FF	0xE300-0xE33F	256
Function 6 Mask		0x3D900-0x3D9FF	0xE340-0xE37F	256
Function 7		0x38E00-0x38EFF	0xE380-0xE3BF	256
Function 7 Mask		0x38F00-0x38FFF	0xE3C0-0xE3FF	256

6.3.2.3 Using BIOS Test Mode

When enabling the BIOS test mode, it is important to realize that function zero's configuration data becomes whatever is currently stored in the SRAM. Since the PCI specification has allowed for hot-swapping boards (although it is not supported mechanically) the PCI bridge will read and update each slot's configuration data from time to time to see if any boards have been added or removed from the PCI bus. Also, the currently started driver will be looking for a specific vendor and device

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ID when it does a configuration access. If a different vendor and/or device ID is loaded into SRAM for function zero, then the board may become inaccessible since the driver and PCI bridge think a different board is now in that slot. To avoid this scenario and having to cycle power to disable the BIOS mode (since it can no longer be disabled by the host software), there is an override switch on the back panel. This switch is only effective while in BIOS Mode. When this switch is set to OFF, the default device and vendor ID will always appear, regardless of whether the BIOS mode is enabled and which function is being accessed. For FOXFIRE™ II, the default values are 0x003 for device ID and 0x12DB for vendor ID. Setting the switch to ON will allow the device and vendor ID values stored in SRAM for each function to be read. The default position for this switch is ON.



INFORMATION NOTE

If in BIOS Mode and switch 3 on the back panel is set to OFF, the device and vendor IDs stored in SRAM will be overridden with 0x0003 and 0x12DB, respectively. To be able to read device and vendor ID values stored in the SRAM, turn switch 3 to the ON position.

To enable the Expansion ROM Base Address Register and be able to read ROM data at boot up, it is necessary to set bit zero high in the Expansion ROM Base Address Register located at byte address 0x30 in configuration space. If this bit is not set, then attempts to read from the ROM will produce a master abort since the board will not respond. This bit is the ROM Decode Enable bit. The Memory Space Control bit, located at bit 1 of the Command Register, has precedence over the ROM Decode Enable bit and must also be enabled for expansion ROM address decode.

When using multiple functions it is important to have bit 7 set in the Header Type Register located at 0x0E in the predefined header. When this bit is high it indicates the board is a multi-function device (has 2 to 8 functions). If this bit is zero then the PCI bridge will assume that the board only has one function. In the master control register there are 8 bits [31:24] used to enable different functions. Bit 24 corresponds to the enable for function zero and is always enabled, or high. The other seven bits are read/writeable and it is up to the user to determine which other functions (if any) are going to be enabled.

6.3.2.4 Base Address Register Programming Examples

One of the major uses for BIOS Mode is to see how the BIOS assigns resources to particular boards. Below are some examples of how to

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program a regular base address mask register so that on power-up the base address registers will request certain resources:

Programming Base Address Mask Registers for BIOS Mode

Base Address Behavior	Mask register programming
Request 128 bytes of I/O space	0x FF FF FF 81
Request 4 Meg of normal memory space	0x FF C0 00 00
Request 64K of prefetchable memory	0x FF FF 00 08
Request 8K of memory below 1 Meg	0x FF FF E0 02
Request 32 Meg in 64-bit Base Address register	0x FE 00 00 04 (in 1st one) 0x FF FF FF F0 (in 2nd)

Another feature of BIOS Mode is to see how the BIOS assigns resources to the Expansion ROM base address register. Below are some examples on how to program the Expansion ROM base address mask register so the Expansion ROM base address register will request certain resources on boot.

Programming Mask Register for Expansion ROM Base Register

Expansion ROM Address Behavior	BA_mod Programming
Request 16K bytes of memory space	0x FF FF C0 01
Request 1 Meg of normal memory space	0x FF F0 00 01

6.3.3 Power Management (Power Management Mode)

This mode is used to verify host system compliance with the PCI Bus Power Management Interface Revision 1.1 specification. During this mode only PCI function 0 will be visible to the system. FOXFIRE™ II meets all the required characteristics for proper power management as specified in Chapter 3 of the PCI Bus Power Management Interface Specification Revision 1.1. Any non-standard registers that vary from this specification are outlined below.

6.3.3.1 PCI Configuration Space Additions

There are some additions to the standard PCI configuration space needed to support power management. These were previously reserved spaces and will not affect systems that do not support power management.

In the Predefined Header, Status Register (offset 0x06) bit 4 is set to "1b" indicating that a Capabilities List exists. When the system looks at the

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Capabilities List it will see that the FOXFIRE™ II board support the PCI Bus Power Management Interface Revision 1.1 specification.

The 8-bit Cap_Ptr register is added at offset 0x34 that holds the address of the beginning of the PCI Power Management register block. For the FOXFIRE™ II card the beginning of this block is located at 0x80. Therefore, this register is hardwired to 0x80.

6.3.3.2 Power Management Registers

0x7c Misc_PMCTL Register- *Read/Write*-This 16 bit register provides software control over the assertion of PME# from bus powered PM states, as well as 3.3Vaux test loading. This register also provides control and status for monitoring 33Vaux and detecting the presence of other power sources.



INFORMATION NOTE

Bits [12:07] are only available with FOXFIRE™ II Rev. C and higher and prom version 2.0 or higher. In earlier versions these bits are hardwired to "0b."

- Bits [15:13] are Read Only and hardwired to "0b".
- Bit [12] is Read Only and represents the present state of the 33Vaux LED and whether or not 33Vaux is currently within spec. If this bit is "1b" then 33Vaux is within spec (3.0V-3.6V +/- 5%).
- Bit [11] is Read Only and will be set and held at "1b" if in any state other than S3, 33Vaux goes out of spec. This bit will remain set at "1b" until bit [07] in this register is set. There is a risk if only bit [12] is monitored that 33Vaux could go out of spec and come back in spec with out the host observing it. This bit along with bit [10] allow the host to detect if 33Vaux has ever gone out of spec.
- Bit [10] is Read Only and has the same functionality as bit [11] but it can be set in S3. Therefore, this bit is probably preferable to monitor. Bit [11] was included to obtain more information when 33Vaux goes out of spec. For example, if after coming out of S3 bit [10] is set to "1b" and [11] is set to "0b" then 33Vaux went out of spec only during S3. However, if both bits are set to "1b" then 33Vaux went out of spec after coming out of S3 and maybe also during S3.
- Bit [09] is Read Only and will be set to "1b" if the 33Vaux loading circuit is working. If this bit is "0b" it means that the FOXFIRE™ II board cannot draw enough current from the 33Vaux PCI pin. This bit allows monitoring to check if the system power supply is supplying enough current to 33Vaux.

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- Bit [08] is Read Only and indicates that the 33Vaux voltage is above about 2.7V if equal to "1b". When this bit is "0b" it means that 33Vaux is well below spec. This bit could be used to tell if 33VAUX is just barely out of spec (Bit [8] set to "1b" and bit [12] set to "0b") or severely below spec (Bit [8] set to "0b" and bit [12] set to "0b").
- Bit [07] is Read/Writeable and is used to clear bits [10] or [11] if they are set to "1b". Writing a "1b" to this bit holds bits [10] and [11] in reset and writing a "0b" to this bit takes them out of reset allowing their normal operation.
- Bit [06] indicates 5 VPCI present when "1b".
- Bit [05] indicates 3.3 VPCI is present when "1b".
- Bit [04] indicates 3.3 VAUX is present when "1b".
- Bit [03] is Read Only and hardwired to "0b".
- Bits [02:01] are the Read/Writeable **Load_Select** bits that determine how much 3.3Vaux current FOXFIRE™ II will draw. The default value for these bits is 10b (160 mA). The encoding of these bits is as follows:

Bit 02	Bit 01	Applied DC Load	Comments
0	0	20 mA +0/-25%	load for PME disabled card
0	1	375 mA +/- 5%	max. 3.3Vaux load
1	0	160 mA +/- 5%	~1/2 max. 3.3Vaux load
1	1	Reserved	

- Bit [00] is the **Assert_PME** bit which is used to provide the host with a method to force the assertion of PME#. Setting this bit to "1b" will assert PME# given that the **PME_En** bit (bit 8 in PMCSR) is also set (1b). If the **PME_En** bit is not set then this bit will have no effect on the PME# line. This bit is automatically cleared when the **PME_Status** bit (bit 15 in PMCSR) is cleared (0b).

0x80 Capability ID Register-*Read Only*-This 8-bit register is hardwired to 0x01. This signifies that the remainder of the capability register block represents the PCI Power Management programming interface.

0x81 Next Item Pointer Register-*Read Only*-This 8-bit register is hardwired to 0x00 which indicates that there are no other extended features other than PCI power management.

0x82 Power Management Capabilities Register (PMC)-*Read Only*-This is a 16-bit register that is will return 0xFFC2 if 3.3Vaux is detected and FOXFIRE™ II is configured to draw 375 mA from

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3.3Vaux. This setting indicates that function 0 of FOXFIRE™ II has the following power management capabilities:

- Bits [15:11] represent the level of **PME_Support**. When 3.3Vaux is present FOXFIRE™ II will return 0xF for these bits signifying that the card can generate a PME from D0, D1, D2, D3hot and D3cold states. If 3.3Vaux is not present then FOXFIRE™ II will return 0x7 since PME# cannot be asserted in D3cold.
- Bits [10] is the **D2_Support** bit. This bit is hardwired to a "1b" since FOXFIRE™ II supports the optional D2 PM state.
- Bits [09] is the **D1_Support** bit. This bit is hardwired to a "1b" since FOXFIRE™ II supports the optional D1 PM state.
- Bits [08:06] are the **Aux_Current** bits that indicate the 3.3Vaux auxiliary current requirements of FOXFIRE™ II. The value of these bits will depend on how the Load_Select bits are set in the Misc_PMCTL register. If FOXFIRE™ II is configured to consume 375 mA @ 3.3Vaux and PME# assertion during D3cold is possible then this register will return "111b". If configured for 160 mA and PME# assertion during D3cold is possible then this register will return "011b." If PME# assertion during D3cold is not possible this register will return "000b."
- Bit [05] is the **DSI** (Device Specific Initialization) bit. This bit is hardwired to "0b" on FOXFIRE™ II since the card does not require any form of device specific initialization (can use a generic device-class appropriate device driver).
- Bit [04] is reserved and hardwired to "0b."
- Bit [03] is the **PME_Clock** bit and is hardwired to a "0b" since FOXFIRE™ II does not require a PCI free-running clock to generate PME# from any PCI bus PM state.
- Bits [02:00] are the **PCI-PM Version** bits. FOXFIRE™ II is PCI-PM Specification Revision 1.1 compliant so these bits are hardwired to "010b."

0x84 Power Management Control/ Status Register (PMCSR) - *Read/Write-* This 16 bit register is used to control and monitor the FOXFIRE™ II's power management state.

- Bit [15] is the **PME_Status** bit. It is a read/writeable_clear bit that is set to "1b" whenever the FOXFIRE™ II card asserts PME#. As long as this bit is set the card is asserting the PME# line. Writing a "1b" to this bit will clear the bit, deassert PME#, and clear the **Assert_PME** bit (bit 0 in Misc_PMCTL) if it is set.
- Bits [14:13] are the read only **Data_Scale** bits. These two bits are hardwired to "00b".
- Bits [12:09] are the read only **Data_Select** bits. These four bits are hardwired to "0000b".
- Bit [8] is the **PME_En** bit. This read/writeable bit is used to enable FOXFIRE™ II to generate a PME (power management event) wake

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request. PME# assertion is enabled when this bit is set to "1b". When this bit is set to "0b" then FOXFIRE™ II cannot assert PME#.

- Bits [07:02] are read only reserved bits that are hardwired to "000000b."
- Bits [01:00] are the read/writeable **PowerState** bits. They are used to control/report the current PM state of the FOXFIRE™ II card. They are encoded as follows:

Bit 01	Bit 00	Power State
0	0	D0
0	1	D1
1	0	D2
1	1	D3hot

6.4 Test Hardware

3.3Vaux Voltmeter Test Stake Pins- There are two test stakes provided for measuring the 3.3Vaux voltage. These stakes consist of a ground stake and a 3.3Vaux stake. These will be used while FOXFIRE™ II is drawing a known current from 3.3Vaux to determine how much current the system is actually supplying.

On FOXFIRE™ II Rev. C and higher there is also a test stake called 3.3Vaux Out which is the voltage after a 0.01 ohm resistor. If external 33Vaux is being supplied to the board it should be applied to PCI 3.3Vaux which is the connected to the 33Vaux PCI pin and the other side of the sense resistor.

PME Momentary Push-Button- This push-button located on the top card edge is used to force assertion of PME#. It is specifically designed to assert PME# during D3cold but can assert PME# during any PM state provided that the PME_En bit is set to "1b". The push-button and all related logic draws its power from 3.3Vaux. If the PME_En bit is set and the push-button is depressed then PME# will be asserted until FOXFIRE™ II's PME_Status bit is cleared by system software.

PME Momentary Push-Button Test Stake Pins- These two test stakes will be in parallel with the PME Momentary Push-Button and allow for an external push-button to be used. They are located to the right of the push-button.

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Power Detection LEDs-There are three LEDs on the PCI back panel bracket that signify which types of power the host system is supplying. If the LED is lit then its corresponding power is present on the PCI bus. The labels, color and PCB reference designators of these LEDs are as follows:

Power Detecting	Label	Color	Reference Designator
5 Volt PCI	5VPCI	Green	D5
3.3 Volt PCI	3.3PCI	Green	D6
3.3Volt Auxiliary	3.3AUX	Green	D8 (Rev A, B) D7 (Rev C, D)

Note that presence detection for each of these voltages is also visible to software via Misc_PMCTL register (offset 0x7c) bits[6:4].

PME_En and PME_Status Initialization Switch- This switch sets the default value for the PME_En and PME_Status bits. When the switch is set to "ON" both bits will be initialized to "1b." Setting the switch to "OFF" will initialize both bits to "0b." The switch is located on the PCI back panel bracket at position 2 of SW1. These bits are initialized the first time 3.3Vaux is detected or if 3.3Vaux is not available they will be initialized by every PCI reset. Note that if the switch is set to "ON", FOXFIRE™ II will also immediately assert its PME# output pin, which will remain asserted until it's PME_Status bit is cleared by the system.

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6.5 FOXFIRE™ II Register Map

Address	Name	Mode Used	Modes Visible	Size in Bytes
0x40-0x43	Master Control Register	L,B	L,B,P	4
0x44-0x47*	Status Register SRAM Address register	L B	L,P B	4
0x48-0x4B*	Write Retry Time-out Register SRAM data register	L B	L,P B	4
0x4C-0x4F	Write Retry Count Register	L	L,P	4
0x50-0x53	Write Retry Address Register	L	L,P	4
0x54-0x57	Expansion ROM Base Address Mask Register	B	L,B,P	4
0x58-0x5B	RESERVED			4
0x5C-0x5F	RESERVED			4
0x60-0x63	TRDY Time-out Address Register	L	L,P	4
0x64-0x67	RESERVED			4
0x68-0x6B	RESERVED			4
0x6C-0x6F	TRDY Address Compare Register	L	L,P	4
0x70-0x73	TRDY Latency Time-out Register	L	L,P	4
0x74-0x7B	TRDY Latency Counter/Cycle Monitor Register	L	L,P	4
0x7C-0x7D	Misc_PMCTL	P	L,P	2
0x7E-0x7F	Reserved			2
0x80	Capability ID Register	P	L,P	1
0x81	Next Item Pointer Register	P	L,P	1
0x82-0x83	Power Management Capabilities Register (PMC)	P	L,P	2
0x84-0x85	Power Management Control/ Status Register (PMCSR)	P	L,P	2

L-Latency Mode B-BIOS mode P-Power Management Mode

* These addresses have distinct registers associated with them depending on which mode is enabled. Modifying one distinct register in a given mode will not affect the contents of the other distinct register.

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INDEX

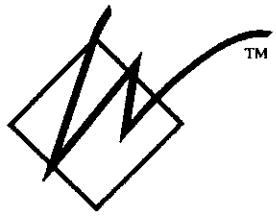
3.3Vaux, 4-3, 6-2, 6-18, 6-19, 6-20, 6-21, 6-22
Assert_PME, 6-19, 6-21
Aux_Current, 6-20
BIOS, 1-2
BIOS Test Card, 6-10
  Register Information, 6-11
board mode control, 6-3
board modes, 6-1
Board parts, 3-2
Cap_Ptr, 6-18
Configuration Cycle, 1-2
Configuration Space, 1-2, 6-11, 6-14, 6-17
Conventions, 1-1
D1_Support, 6-20
D2_Support, 6-20
D3cold, 6-1, 6-20, 6-22
Data_Scale, 6-21
device ID, 6-5, 6-16
DSI, 6-20
Expansion ROM Base Address Register, 1-2, 6-13, 6-17
FOXFIRE™ II Features, 2-1
Function, 1-3
Handling, 3-1
Header Type Register, 6-16
Icons, 1-2
Indirect Addressing, 6-14
installation, 4-1
LEDs, 4-2, 4-3, 6-5, 6-22
Load_Select bits, 6-19
Memory Base Address Register, 6-13
Memory Space Control bit, 6-16
Misc_PMCTL Register, 6-18
Mode, 1-3
Ordering Information, 5-1
PCI, 1-3
PCI Retry, 1-3
PCI SIG, 1-3
PCI specification, 2-1
PCI Technology, 2-1
PCI-PM Version, 6-20

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PMC, 6-18, 6-19, 6-20, 6-21, 6-24
PMCSR, 6-19, 6-21, 6-24
PME momentary push-button, 6-2, 6-22
PME_Clock, 6-20
PME_En, 4-1, 6-19, 6-21, 6-22
***PME_En and PME_Status Initialization Switch*, 6-22**
PME_Status, 4-1, 6-19, 6-21, 6-22
PME_Support, 6-20
Power Detection, 6-22
PowerState, 6-21
Read/Write, 6-11
ROM Decode Enable bit, 6-16
Sales Support, 5-1
Soft Boot, 1-3
SW1, 6-22
SW2, 4-1
switches, 4-1
Technical Support, 5-1
Test Stake, 6-21, 6-22
Threshold, 1-3
vendor ID, 1-2, 6-5, 6-16
Write-Lockable, 1-3, 6-11

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