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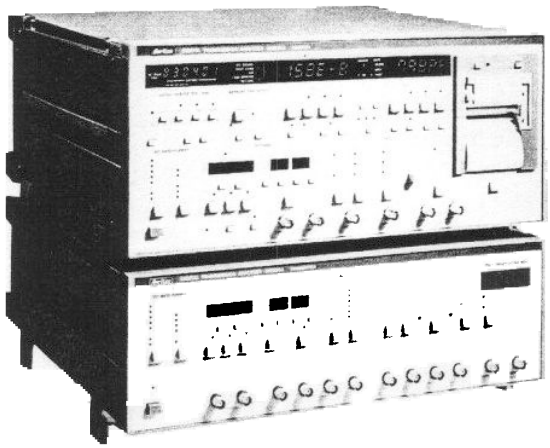
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PCM MEASURING EQUIPMENT

DIGITAL TRANSMISSION ANALYZER

ME520A

1 kHz to 150MHz (1 kHz to 170MHz with Option 02)



《GP-IB》

The Digital Transmission Analyzer ME520A measures digital errors of bit rates from 1kbit to 150Mbit/s (maximum 170Mbit/s with Option 02), and digital timing jitter of clock frequencies from 700kHz to 150MHz (maximum 170MHz with Option 02).

This analyzer is ideal for development and maintenance of 1st to 4th order digital line transmission systems, digital radio transmission systems, and digital optical transmission systems, including the 10CH system of the PCM 30CH system (CEPT).

The input/output interface conforms to CCITT Rec. G.703, the pseudo-random pattern conforms to CCITT Rec. O.151, and jitter measurement conforms to CCITT Rec. O.171.

The ME520A consists of a transmitter and a receiver. End-to-end and loop-back tests can be performed with one ME520A.

The transmitter can output pseudo-random (PRBS $2^{10}-1$, $2^{15}-1$, $2^{23}-1$), 1 to 16 bit variable length programmable words, and 2 × 8 bit alternate word patterns as NRZ and RZ unipolar signals, AMI and HDB3 bipolar signals, and in CMI signal formats. Bit and code error addition, internal clock frequency offset, and jitter modulation by external signals are possible by adding functions.

The receiver can measure digital errors of unipolar, AMI, HDB3, and CMI signals. Jitter measurement is also possible with clock signals or code signals (clock regenerated internally). Digital error and jitter are simultaneously measured and analyzed and the results are displayed digitally. The measured results can be printed out with a built-in thermal printer (option 01) and the results can be stored.

The GP-IB interface is standard with both the transmitter and the receiver unit. It is convenient for taking measurements automatically.

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Transmitter specifications

Bit rate	Internal clock	Bit rate	704, 2048, 8448, 34368, 68736, 139264kbit/s
		Accuracy	±2ppm, ±5ppm/0 to 50°C
	External clock	Frequency	1kHz to 150MHz, (Option 02: up to 170MHz)
		Amplitude	0.3 to 3Vp-p, 1kHz to 1MHz (rectangular), >1MHz (Sine or rectangular)
		Impedance	Nominal 75Ω, unbalanced
		Duty cycle	50%
	Burst gate input	Amplitude	ECL level, high disables clock
		Impedance	Nominal 75Ω, unbalanced
		Termination	Nominal -2V
Clock output	Numbers		2 separate buffered outputs, common phase
	Polarity		CLOCK or $\overline{\text{CLOCK}}$, selectable
	Level	TTL	High state = 2.5V, low state = 0.5V
		ECL	ECL level
		SET	Amplitude 1 to 2V, offset 0 to ±2V
	Format		Square wave, 50 ±10% duty cycle on internal clock
	Impedance		75Ω, unbalanced
Pattern	PRBS (Pseudo-random binary sequence)		2^{10}-1, 2^{15}-1, 2^{23}-1
	Word		Freely programmable digital word, adjustable length 1 to 16 bits. Two 8-bit words, any possible setting. (Can be changed over by an external control signal)
	Zero substitution		Sequence can be disabled for 8 to 120 of clock periods, in multiples of 8 clock periods.
Error pulse	Error addition	Error rate	10^{-3}, 10^{-4}, 10^{-5} and 10^{-6}, selectable
		Single error	1 error is produced for each depression of key
	External error input	Impedance	Nominal 680Ω, unbalanced to -5.2V
		Frequency	DC to one-half the clock frequency
Output data	CMI	Bit rate	1kbit/s to 150Mbit/s
		Amplitude	1 ±0.1Vp-p
		Numbers	4 separate buffered outputs, common phase
	Unipolar (RZ, NRZ)	Bit rate	1kbit/s to 150Mbit/s, (Option 02: up to 170MHz)
		Level	TTL, ECL, SET, selectable (TTL: high state = 2.5V, low state = 0.5V) (SET: amplitude 1 to 2V, offset 0 to ±2V)
		RZ duty cycle	50 ±10% on internal clock
		NRZ width	100 ±5%
		Numbers	4 separate buffered outputs, each delayed 4 bits
	Bipolar (RZ)	Bit rate	1kbit/s to 50Mbit/s
		Format	AMI, HDB3
		Amplitude	2.37 ±0.237V/0 ±0.237V or 1.0 ±0.1V/0 ±0.1V, selectable
		Numbers	4 separate buffered outputs, each delayed 4 bits
Jitter modulation	Function		Timing jitter can be added to the clock and data output signals by applying an external modulation source.
	Input	Frequency	DC to 5% or 2.5% of bit rate (see Fig. 1 and Table 1)
		Sensitivity	10UIp-p/V (5Hz)
		Impedance	Nominal 75Ω, unbalanced to ground
	Output	Display	10.10UIp-p, max.
	Jitter reference clock output	Level	ECL
		Impedance	Nominal low, unbalanced to ground

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Pattern sync output	Pattern	PRBS	1 pulse/1 sequence
		2 to 16 bits word length	1 pulse/2 sequences
		1 bit word length	1 pulse/4 bits
		2 x 8-bit word length	1 pulse/1 sequence
GP-IB interface			Meets IEEE Standard 488-1978
Ambient temperature, rated range of use			0 to 50°C
Power			180 to 275V, 50/60Hz, approx. 200VA
Dimensions and weight			132.5H, 426W, 351D mm, approx. 11kg
Accessories supplied			Two coaxial cords (BNC-3C-2V-BNC) 2m One power cord One set of fuses One operation manual (per transmitter-receiver combination)

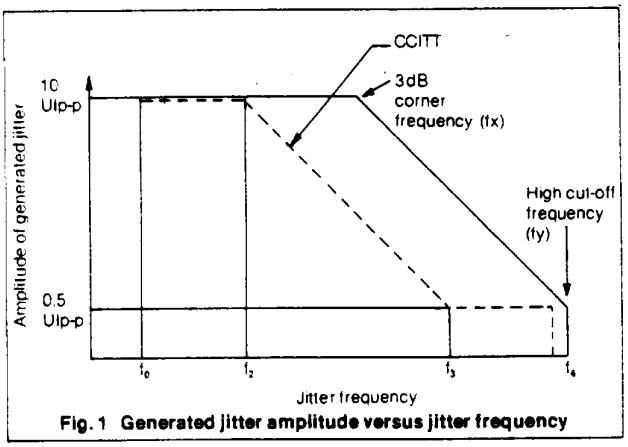


Fig. 1 Generated jitter amplitude versus jitter frequency

Table 1 Jitter frequency

	CCITT Rec. 0.171				ME520A	
Bit rate (kb/s)	f_0 (Hz)	f_2 (kHz)	f_3 (kHz)	f_4 (kHz)	fx* (kHz)	fy* (kHz)
704					4.5	35
2,048	2	2.4	45	100	13	102
8,448	2	10.7	200	400	50	422
34,368	2	1.0	20	800	210	1,000
68,736					300	2,000
139,264	2	0.5	10	3,500	600	4,000
EXT	Can be modulated at internal rates ±10%					

* Typical figures

Receiver specifications

Bit rate	Clock recovery	Receiving rate	704, 2048, 8448, 34368, 68736, 139264kbit/s
		Pulling range	±100ppm (AMI), ±3% (HDB3), ±1% (68736kbit/s CMI), ±3% (139264kbit/s CMI)
		Format	AMI, HDB3 (RZ, 704, 2048, 8448, 34368kbit/s) CMI (68736, 139264kbit/s)
	Clock input	Polarity	CLOCK or $\overline{\text{CLOCK}}$, selectable
		Frequency	1kHz to 150MHz (Option 02: up to 170MHz)
		Amplitude	0.3 to 3Vp-p
		Impedance	75Ω, unbalanced
		Termination	Ground or nominal -2V (via switch)
Pattern	PRBS (Pseudo-random binary sequence)		2^{10}-1, 2^{15}-1, 2^{23}-1
	Word		Freely programmable digital word, ajustable length 1 to 16 bits
	Zero substitution		Sequence can be disabled for 8 to 120 of clock periods, in multiples of 8 clock periods.
Input data	RZ, NRZ input	Bit rate	1kbit/s to 150Mbit/s, (Option 02: up to 170MHz)
		Threshold	-3V to +3V, ground or ECL, selectable
		Impedance	75Ω, unbalanced
		Amplitude	0.3 to 3Vp-p
		Polarity	DATA or $\overline{\text{DATA}}$, internally switched at the binary level

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Input data	CMI input	Threshold	Ground
		Impedance	75Ω, unbalanced
		Amplitude	1Vp-p automatic $\sqrt{f}$ equalization
		Monitor mode	Additional gain 26dB
		Polarity	DATA or $\overline{\text{DATA}}$, internally switched at the binary level
	AMI, HDB3 input	Impedance	75Ω, unbalanced
		Amplitude	2.37V/0V (704, 2048, 8448kb/s), 1V/0V (34368kb/s), Automatic $\sqrt{f}$ equalization
		Monitor mode	Additional gain at 30dB: 704, 2048, 8448kbit/s Additional gain at 26dB: 34368kbit/s
		Polarity	DATA or $\overline{\text{DATA}}$, internally switched at the binary level
Error measurement	Bit error		Closed loop bit-by-bit detection at the binary level
	Code error	AMI	Bipolar violations are code errors
		HDB3	"Violation of violations" rule, i.e., two consecutive bipolar violations with same polarity.
		CMI	"Violation of CMI coding rules," i.e., two consecutive bits, whose intervals are one full unit time, with same polarity.
	Block error		For PRBS only, the block length coincides with the length of the PRBS. Error is detected if a block contains one or more bit errors.
	Pattern synchronization	Mode	Automatic or manual
		Sync gain	PRBS: No errors in 32 clock periods WORD: No errors in 32 to 512 clock periods
		Sync loss	PRBS: Approx. 10,000 errors in 30,000 clock periods WORD: Approx. 1,000 errors in 30,000 clock periods
Error display	Error rate	Display	0.00E-MN (0.00 x 10^{MN}), MN=1 to 15 with automatic scaling
		Accuracy	Indication given if measurement result is based on <100 errors
	Error count	Method	Totalizes errors over selected gating period
		Display	6-digit LED display with leading zero blanking When count exceeds 999999, display automatically changes to 0.00E00, with automatic round-up to a maximum count of 9.99E15 (9.99 x 10^{15}).
	Error intervals	Method	Totalizes the number of intervals (1, 0.1, 0.01 sec.) which contain one or more errors (intervals can be selected by the switch on rear panel.)
		Display	Same as error count
	Error-free intervals %	Method	Totalizes the number of intervals (1, 0.1, 0.01 sec.) during which no errors occur over selected gating period.
		Display	6-digit LED display with leading zero blanking up to 100.000%.
Status display	Display		Live and last record of No signal, sync loss, AIS, <100 errors
Jitter measurement	Range, accuracy	1UI	0.000 to 1.010UIp-p,
		10UI	0.00 to 10.10UIp-p, ±4% ± additional error as shown in Table 2 (with HP1, LP)
	Jitter amplitude versus jitter frequency		Refer to Fig. 2 and Table 3
	Hit count	Display	When count exceeds 999999, display automatically changes to 0.00E00, with automatic round-up to a maximum count of 9.99E15 (9.99 x 10^{15}).
		Sensitivity	Typically ≧100ns pulse width counted
		Hit threshold	Range 1: 0.05 to 0.5UIp-p Range 10: 0.5 to 5.0UIp-p
		Accuracy	Typically ±5%
	Hit intervals	Method	Totalizes the number of hit intervals (1, 0.1, 0.01 sec.) (intervals can be selected by the switch).
			Other specifications are same as hit count.
	Hit-free intervals %	Method	Totalizes the number of intervals (1, 0.1, 0.01 sec.) during which no hits occur.
		Display	6-digit LED display with leading zero blanking up to 100.000%

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Gating period and real-time clock	Gating period	Setting		Manual, clock, time, external
		Display	Last data	Displayed data and status record is data in last gating period
			Current data	Displayed data and status record is data in current gating period
	Real-time clock			Year, month, day or day, hour, minute
GP-IB interface				Meets IEEE Standard 488-1978
Ambient temperature, rated range of use				0 to 50°C
Power				180 to 275V, 50/60Hz, approx. 230VA
Dimensions and weight				177H, 426W, 351D mm, approx. 15kg
Accessories supplied				Two coaxial cords (BNC-3C-2V-BNC) 2m One power cord One set of fuses One operation manual

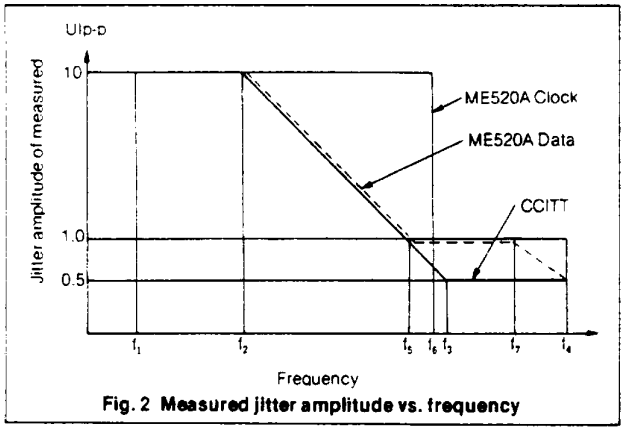


Fig. 2 Measured jitter amplitude vs. frequency

Table 2 Additional error

Range	Additional error in UIp-p				
	HDB3, CMI		Clock		
	F<139M	F≧139M	F≦70M	70M<F≦150M	F>150M (OPT 02)
Range 1	≦0.035	≦0.08	≦0.01	≦0.02	≦0.03
Range 10	≦0.12	≦0.24	≦0.1	≦0.2	≦0.3

Table 3 Jitter frequency

	CCITT Rec. O.171				ME520A (typical)		
Bit rate (kb/s)	f_1 (Hz)	f_2 (Hz)	f_3 (Hz)	f_4 (Hz)	f_5 (Hz)	f_6 (Hz)	f_7 (Hz)
704	(20)	(1k)		(35k)	7k	8k	10k
2,048	20	2.4k	4.5k	100k	24k	27k	30k
8,448	20	10.7k	200k	400k	107k	110k	120k
34,368	100	1k	20k	800k	10k	344k	320k
68,736	(100)	(40k)		(1M)	400k	400k	500k
139,264	200	500	10k	3.5M	100k	500k	1.4M

Options

01: Built-in printer: Supplied with six rolls of thermal paper

02: Operation up to 170MHz: With NRZ, RZ format

Note: Several kinds of internal clock frequencies, (different from those of the standard model) are available as options. Refer to the ME520A data sheet.

Optional accessories

Item	Order No.	Remarks
Coaxial cord BNC-3C-2V-BNC, 2m	J0081	
GP-IB cable, 2m	J0008	
Roll paper for printer	Z0031	Two rolls/One set
Portable Test Rack MB23A	–	
Portable Test Rack MB24A	–	
Soft carrying case for transmitter section of ME520A	B0064	Protective covers for front and rear panel of transmitter (B0019) are required
Soft carrying case for receiver section of ME520A	B0065	Protective covers for front and rear panel of receiver (B0020) are required
Protective case for transmitter section of ME520A	B0066	Soft carrying case (B0064) and protective covers (B0019) are required
Protective case for receiver section of ME520A	B0067	Soft carrying case (B0065) and protective covers (B0020) are required
Protective cover for transmitter section of ME520A	B0019	Two (front and rear) covers required
Protective cover for receiver section of ME520A	B0020	Two (front and rear) covers required
Rack mount kit 3U	B0042	
Rack mount kit 4U	B0043	
Matching transformer MP35A	–	75Ω unbalanced/120Ω balanced (for 2048kb/s)

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