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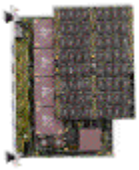
HydraPlus™

Quad TMS320C40 DSPs for VMEbus in a Single 6U Slot



200 MFLOPS Harvard Architecture
Up to 32 Mbytes private zero wait-state SRAM
Shared memory up to 16 Mbytes DRAM or 12 Mbytes SRAM
VMEbus master/slave capability
Optional VSB master interface
Flexible communication port configuration
On-board JTAG controller ASIC
Comprehensive software support

The Hydra Architecture



All Ariel Hydra products employ a true Harvard architecture. Unlike other multi-C40 designs which employ shared memory in lieu of distributed memory, each of Hydra's C40s can concurrently access two separate banks of private memory without incurring wait states. This provides deterministic system behavior and optimized performance. A four processor Hydra is equipped with nine independent banks of memory; two distributed banks private to each DSP and a common bank of memory shared by all DSPs. Buffered transceivers isolate each C40's private Global Bus to

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prevent shared memory bus accesses from interfering with private memory accesses. This performance-optimized memory architecture, coupled with a comm port interconnection scheme designed for interprocessor communications and I/O defines the Hydra architecture.

System Specifications

processor
Four Texas Instruments TMS320C40 DSPs; 50 MHz.

private memory
Local bus: 1 or 4 Mbytes zero wait-state SRAM. Global bus: 1 or 4 Mbytes zero wait-state SRAM.

shared memory
4or 16 Mbytes of shared DRAM. Alternately, 4, 8 or 12 Mbytes of one-wait-state shared SRAM. The shared bus is isolated from the DSPs' private bus to ensure zero-wait-state access of private SRAM.

non-volatile memory
DSP1 has a 512-Kbyte boot EPROM and a 2048-bit nonvolatile EEPROM.

communication ports
Six 20-Mbytes/sec bidirectional ports per DSP. Three of each DSP's comm ports are connected to the other on-board DSPs with the remainder (12 total) available externally on the front panel.

VSB bus
Optional master-only industry-standard VSB interface on VME P2 connector supports 32-bit parallel I/O. Requires VSB backplane.

ADbus
A high-speed 24-bit parallel bus. ADbus boards can interrupt DSP2 and up to six ADbus modules can be connected to the HydraPlus ADbus port.

debug port
JTAG P1149.1 boundary scan with extensions for in-circuit emulation. Accessible over VMEbus or via on-board 14-pin header for direct connection to Texas Instruments XDS-510 or Ariel UXDS debuggers.

serial ports
Two RS-232 ports accessible on front panel, 150 baud to 19.2 Kbaud.

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host interface

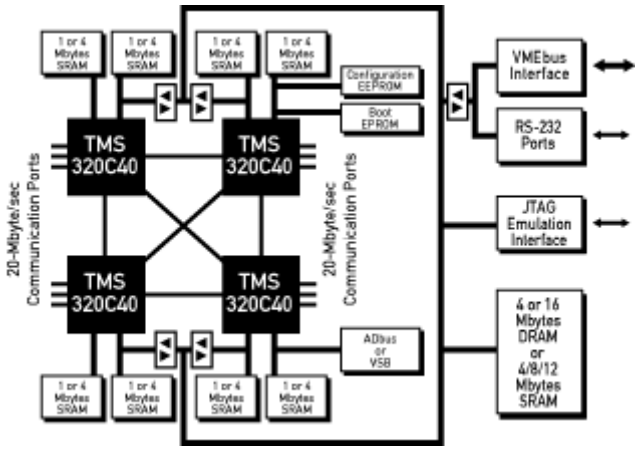
6U VMEbus master/slave interface. Memory-mapped in VMEbus memory space. Host interrupts and DMA are supported.

power

3.5 A at 5V typical.

size and weight

262 x 187 x 21 mm overall, 855 grams; 10.3 x 7.4 x 0.8 in. overall, 1.88 lbs.



TMS320C4x Processor Specifications

processing rate

50 MHz, 40 nsec basic instruction rate, 50 MFLOPS, 25 MIPS.

on-chip memory

2 x 1K x 32 bits.

off-chip memory

Up to 16 Gbytes, long-word addressable.

arithmetic

32/40-bit floating point, 32-bit integer.

other features

Dual 32-bit memory buses; six high-speed communication ports; six channel DMA coprocessor; JTAG interface; 512-byte program cache.

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Software Specifications

system interface

Host platform interfaces for HydraPlus include device drivers for SunOS, Solaris, VxWorks, pSOS and MS-DOS. Debugging HydraPlus is accomplished via the onboard JTAG interface and Ariel's AXDS, or UXDS, or Texas Instruments' XDS-510.

base software

SunOS device drivers, MS-DOS interface library, VME bus-mastering library, diagnostics, utility and example programs with source code.

optional software

Ariel AXDS or UXDS source-level symbolic debuggers, VxWorks device drivers, pSOS device drivers, DSP Expert Library; TI C compiler, assembler, simulator, XDS-510 debugger; Spectron Microsystems SPOX; Eonic Systems Virtuoso; 3L Parallel C; Tartan compilers and libraries.

distribution media

3.5" floppy disk or 1/4" tape.

documentation

User's Guide, Software Installation Guide, Hardware Reference Manual, Software Reference Manual.

ORDERING INFORMATION for HydraPlus

HydraPlus Series: Ultra-high performance floating-point signal and array processing boards based on the Texas Instruments TMS320C40 dual-bus processor. HydraPlus is a 6U VME board with four 50 MHz processors for peak performance of up to 1100 MOPS and 200 MFLOPS. Each DSP has two banks of private, zero wait-state SRAM, with up to 4 Mbytes per bank for each DSP. In addition to the private SRAM, a shared memory bank is accessible from all DSPs and the VMEbus via a multimaster Internal Shared Bus. The standard shared memory configuration is a 4-Mbyte bank of DRAM; optional shared memory configurations include a larger DRAM bank or a bank of 1 wait-state SRAM instead of DRAM. HydraPlus can operate as a VME bus master or slave and has slot 1 controller capability. Three high-speed parallel communication ports from each DSP are brought out to front-panel connectors. DSP#2 of HydraPlus supports a parallel I/O interface, either ADbus (a straightforward 24-bit interface) or a VSB master-only interface on the VME P2 connector. Documentation and software sets include HydraPlus hardware and software manuals, VMEbus interface chipset manual, device driver software for SunOS hosts, and interface libraries for popular DOS-based embedded PC hosts.

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HYV354M32B0
Four-processor 50 MHz HydraPlus with 8 3 1 Mbyte SRAM, 4 Mbytes shared DRAM, and ADbus

HYV354M32B1
Four-processor 50 MHz HydraPlus with 8 3 1 Mbyte SRAM, 4 Mbytes shared DRAM, and VSB interface

HYV354M35B0
Four-processor 50 MHz HydraPlus with 8 3 1 Mbyte SRAM, 4 Mbytes shared SRAM, and ADbus

HYV354M35B1
Four-processor 50 MHz HydraPlus with 8 3 1 Mbyte SRAM, 4 Mbytes shared SRAM, and VSB interface

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Shared Memory Options

***-D3**
16 Mbyte shared DRAM option for HydraPlus

***-SS4**
4 Mbyte shared SRAM option for HydraPlus

***-SS5**
8 Mbyte shared SRAM option for HydraPlus

***-SS6**
12 Mbyte shared SRAM option for HydraPlus

Accessories

DOCSET-HYP
Documentation and base software set for HydraPlus boards

DOCSET-HYPB
Documentation and base software set for HydraPlus boards with optional VSB interface

CBL-COM-VP6
Hydra-series comm port cable, 6" (15 cm)

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CBL-COM-VP12
Hydra-series comm port cable, 12" (30 cm)

Development Tools and Software The following tools and libraries for SunOS development platforms represent only a fraction of the software that is available for HydraPlus and other Hydra-series products. Please contact an Ariel sales engineer for more information on additional development environments, operating systems, and PC-hosted tools.

C40-CC-SUN
Texas Instruments TMS320C4x C compiler with assembler/linker; SunOS

TAR-C-SUN
Tartan high-performance TMS320C4x C compilation system with FasTar library; SunOS

AXDS-SUN
Ariel Sun-resident debugger for Hydra-series debugging via VMEbus interface; SunOS

RAXDS-VXW
Ariel Sun-resident remote debugger for Hydra-series debugging via VxWorks VME host; SunOS

UXDS-SPARC
Ariel SPARC-resident C4x emulator/debugger with SBus JTAG interface; SunOS/Solaris

XDS510-WS
Texas Instruments Sun-resident C4x emulator/debugger with SCSI JTAG interface; SunOS

UXDS-VISTA
Ariel PC-resident parallel-processor C4x emulator/debugger with ISA JTAG interface; Windows 3.x

UXDS-PC-MP
Ariel PC-resident parallel-processor C4x emulator/debugger with ISA JTAG interface; OS/2

XDS510-XL
Texas Instruments PC-resident parallel-processor emulator/debugger with ISA JTAG interface; OS/2

VXDRV-HY-68K
VxWorks driver for Hydra-series boards; for Motorola 680x0 VxWorks host

VXDRV-HY-SPARC
VxWorks driver for Hydra-series boards; for SPARC-based VxWorks host

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AXL-C40-SUN

Ariel DSP Expert Library, optimized vector math and signal processing library for TMS320C4x; SunOS

FASTAR-SUN

Tartan FasTar optimized run-time C library for TMS320C4x; SunOS

FLOTAR-SUN

Tartan FloTar double-precision math library for TMS320C4x; SunOS

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