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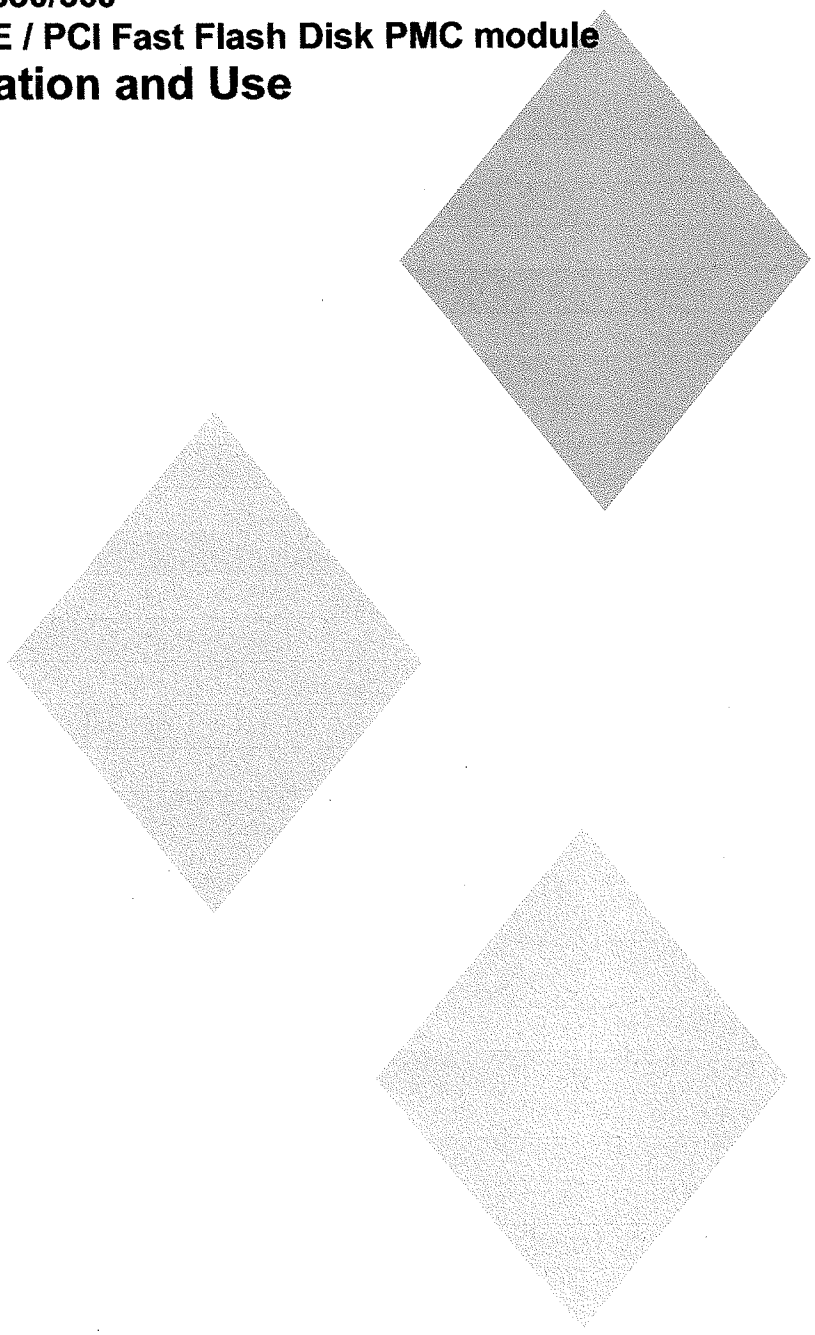
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M-Systems
Flash Disk Pioneers

ASPMC630/660
Ultra-IDE / PCI Fast Flash Disk PMC module
Installation and Use



V660D
March 2004 Edition

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Safety Summary

The following general safety precautions must be observed during all phases of operation, service and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.
The safety precautions listed below represent warnings of certain dangers of which Asine is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Asine representative for service and repair to ensure that all safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing and adjusting this equipment and its components.

Flammability

All Asine PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by recognized manufacturers.

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EMI Caution

This equipment generates uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

Lithium Battery Caution (when applicable)

Upon existence, *your attention of installed lithium* battery.

Caution

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec *une batterie du m¬me type ou d'un type 'quivalent recommand'* par le constructeur.Mettre au rebut les batteries usag'es conform'ment aux instructions du fabricant.

Vorsicht

Explosionsgefahr bei unsachgem¬□em Austausch der Batterie.Ersatz nur durch denselben oder einen vom Hersteller empfohlenen Typ.Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

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Flash Disk Pioneers

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About This Manual

The ASPMC630/660 **Ultra-IDE/PCI Fast Flash Disk Module** *Installation and Use* manual provides the information you will need to install and configure your ASCPMC630/660 board Flash Disk. It provides specific preparation and installation information and data applicable to the module.

The ASPMC630/660 is a high-performance Fast Flash Disk Module plug into a PMC slot via IDE/PCI interface, featuring the Asine Group & M-systems architecture with your choice of capacity, IDE or PCI interfaces, temperature range, conformal coating and conduction cool.

As of the printing date of this manual, the ASPMC630/660 are available in the configurations shown below.

Model Number Description

ASPMC630 Ultra-IDE Fast Flash Disk Models*

Model	Commercial 0°C to70°C	Enhanced –25°C to +75°C	Extended –40°C to +85°C
2GB	ASPMC630-0020-C	ASPMC630-0020-E	ASPMC630-0020-Z
3GB	ASPMC630-0030-C	ASPMC630-0030-E	ASPMC630-0030-Z
4GB	ASPMC630-0040-C	ASPMC630-0040-E	ASPMC630-0040-Z
6GB	ASPMC630-0060-C	ASPMC630-0060-E	ASPMC630-0060-Z
8GB	ASPMC630-0080-C	ASPMC630-0080-E	ASPMC630-0080-Z
10GB	NA	NA	NA
14GB	NA	NA	NA
16GB	NA	NA	NA

ASPMC660 PCI Fast Flash Disk Models*

Model	Commercial 0°C to70°C	Enhanced –25°C to +75°C	Extended –40°C to +85°C
2GB	ASPMC660-0020-C	ASPMC660-0020-E	ASPMC660-0020-Z
3GB	ASPMC660-0030-C	ASPMC660-0030-E	ASPMC660-0030-Z
4GB	ASPMC660-0040-C	ASPMC660-0040-E	ASPMC660-0040-Z
6GB	ASPMC660-0060-C	ASPMC660-0060-E	ASPMC660-0060-Z
8GB	ASPMC660-0080-C	ASPMC660-0080-E	ASPMC660-0080-Z
10GB	NA	NA	NA
14GB	NA	NA	NA
16GB	NA	NA	NA

***Two optional suffixes:**

C – Conduction cool

F – Conformal coating

For example: ASPMC630-0040-EF is an Ultra-IDE, 4GB capacity running at –25°C to +75°C, conformal coated.

For example: ASPMC660-0160-ZCF is an Ultra-IDE PCI interfaced, 16GB capacity running at –40°C to +85°C, conduction cooled and conformal coated.

Other special capacities, pinout and performance products available per specific request.

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Summary of Changes

This is the first edition of the *Installation and Use* manual.

Date	Doc. Rev	Changes
10/Nov/2002	V660A	Proto definition EL00A
02/Aug/2003	V660B	Final first manual release
04/10/2003	V660C	Unification of 630 and 660 into one release manual
21/3/2004	V660D	Adaptation of Ultra ATA Flash Disk, release1.10
16/7/2004	V660D4.22	Production edition from B30 and B60 assemblies

Overview of Contents

The following paragraphs briefly describe the contents of each chapter.

Chapter 1, *Hardware Preparation and Installation* - provides a description of the ASPMC630/660 and its main integrated Fast Flash Disk blocks. The remainder of the chapter includes an explanation of the installation procedure, including preparation and jumper setting information.

Chapter 2, *Operation* - provides a description of the operational functions of the ASPMC630/660 including tips on power, a description of the jumper settings, the status indicators and I/O connectors.

Chapter 3, *Functional Description* - provides a summary of the ASPMC630/660 features, a block diagram, and a description of the major functional areas.

Appendix A, *Data Sheet* - provides the Data Sheet for the ASPMC630/660.

Appendix B, *Related Documentation* - provides a listing of related documentation for the ASPMC630/660, including vendor documentation and industry related specifications.

Comments and Suggestions

Asine welcomes and appreciates your comments on its documentation.

We want to know what you think about our manuals and how we can improve the contents. Please mail comments to:

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You can also submit comments to the following e-mail address:

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In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

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Conventions Used in This Manual

The following typographical conventions are used in this document:

Bold is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

Italic is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

Courier is used for system output (for example, screen displays, reports), examples and system prompts.

<Enter>,<Return>or **<C**R> represents the carriage return or Enter key.

CTRL represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-**d.

Terminology

A character precedes a data or address parameter to specify the numeric format, as follows (if not specified, the format is hexadecimal):

An asterisk (*) following a signal name for signals that are *level significant* denotes that the signal is *true* or valid when the signal is low.

0x Specifies a hexadecimal number
% Specifies a binary number
& Specifies a decimal number

An asterisk (*) following a signal name for signals that are *edge significant* denotes that the actions initiated by that signal occur on high to low transition.

In this manual, *assertion* and *negation* are used to specify forcing a signal to a particular state. In particular, *assertion* and *assert* refer to a signal that is active or true; *negation* and *negate* indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:
Byte 8 bits, numbered 0 through 7,with bit 0 being the least significant.
Half word 16 bits, numbered 0 through 15, with bit 0 being the least significant.
Word 32 bits, numbered 0 through 31, with bit 0 being the least significant.
Double word 64 bits, numbered 0 through 63, with bit 0 being the least significant.

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1

Hardware Preparation and Installation

Introduction

This chapter provides information on hardware preparation and installation for the ASPMC630/660 single board Flash Disk / FFD.

Note Unless otherwise specified, the designation "ASPMC630/660" refers to all models of the ASPMC630 and ASPMC660 Series Ultra-IDE/PCI Flash Disk Modules.

Getting Started

Overview and Equipment Requirements

The **ASPMC630/660** plugs into a single PMC slot via Jn1, Jn2, Jn4, P1 and optional associated cables. Additionally, the ASPMC630/660 is user-configurable by setting on-board jumpers. IDE I/O connectivity is possible through the front panel IDE 40pin connector as well as through the backplane J3 or J5 (for CompactPCI) and P2 or P0 (for VME) utilizing its Jn4 interface. In addition, the following is required:

- System enclosure (e.g. CompactPCI or VME, other)
- CPU with IDE controller for the ASPMC630 (no need for onboard CPU IDE controller for the ASPMC660) with PCI compatible BIOS or PMC carrier
- System console terminal
- CPU monitor/debugger or operating system (and/or application software)

Unpacking Instructions

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

Note If the shipping carton(s) is/are damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Use ESD

Wrist Strap

Asine strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system.

Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD).

After removing the component from its protective wrapper or from the system, place the component on a grounded, static-free and adequately protected working surface. Do not slide the component over any surface.

In the case of a printed circuit board (PCB), place the board with the component side facing up.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available locally) that is attached to an active electrical ground.

Note A system chassis may not be a suitable grounding source if it is unplugged.

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Preparation

Hardware Configuration

To produce the desired board configuration and to ensure proper operation of the ASPMC630/660, it may be necessary to perform certain modifications before and after installation. The following paragraphs discuss the preparation of the ASPMC630/660 hardware components prior to installing them into a chassis and connecting them.
The following table lists the manually configured Jumper Header JP1 on the ASPMC630/660 and their default settings.

Table 1-1. Master/Slave/Cable-Select Configured Jumper Header JP1 Default*

Option	Description	select	Default
No-Jumper	Master/Slave IDE Select	Master	**Default***
1-2	Master/Slave IDE Select	Slave	
2-4	Master/Slave IDE Select	Cable Select	
5-6	Secure Erase all Flash Disk	Carry Secure erase operation	**Standard R/W operation***
7-8	Flash Disk write protect	Write Protect	**Write Enabled***

JP1 Jumper Header Settings

Prior to performing the installation instructions, you must ensure that the ASPMC630/660 jumper header JP1 is set properly for your particular configuration. For example, if you are using the ASPMC630 with external IDE cable to the CPU IDE controller, selecting master/cable-select or slave behavior must be in conjunction of existing additional IDE devices on this same cable. As a general rule and according to IDE specifications, each IDE bus cable should include no more than two IDE devices from one is master and the other is configured as a slave. If only one device exist, than CS (Cable Select) is allowed.
For more Flash Disk details refer to M-Systems **FFD 2.5" Ultra IDE Flash Disk Manual**.

Note Your attention to ASPMC630 Conduction Cool version signal integrity for the IDE connectivity utilizing the Jn4 signals. Jn4 signals, routed by the carrier, should be adequate for high speed data transfer of the IDE bus running at up to Ultra DMA5 speeds.

System Considerations

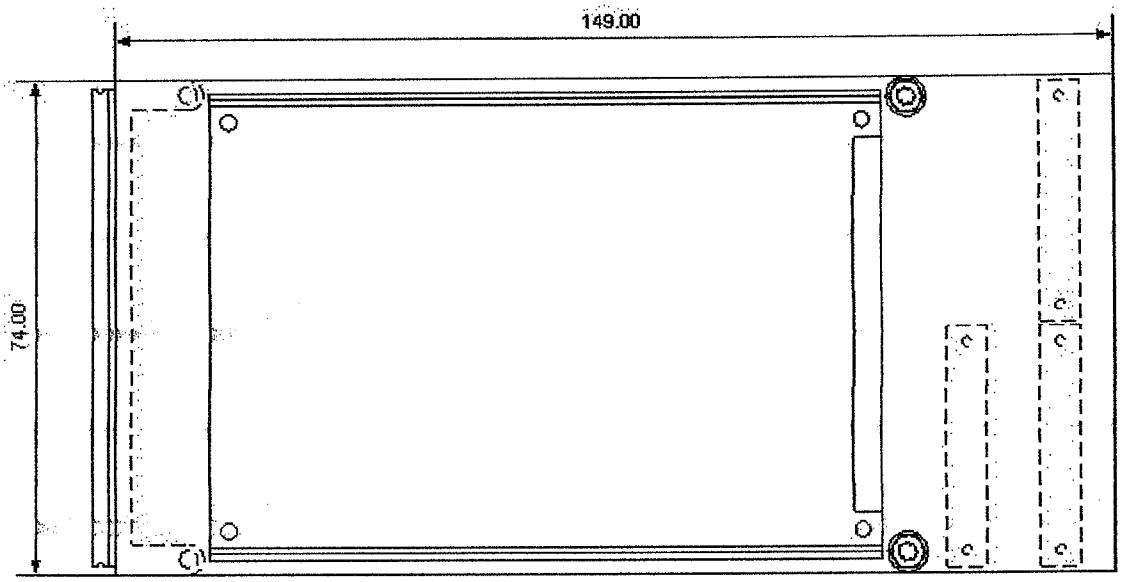
The ASPMC630 only draws power through the Jn1/Jn2 connectors and ensure not to exceed the permitted power consumption and current, while the ASPMC660 interface also to the PCI bus through these connectors. The ASPMC630/660 will not function properly if not installed on a PMC slot.
Flash Disk Secure Erase and Write Protect features are supported through logical (active low) levels through backplan and ASPMC630/660 headers connectivity.

Note

Multiple ASPMC630/660 boards may be installed on a single PMC carrier. However, no more than two IDE devices can be connected on a single IDE bus, while one will be configured as MASTER and the other will be configured as SLAVE.
JP2 is for factory usage only.

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Figure 1-1. ASPMC630/660 Convection Model Layout



ASPMC630/660 Installation

Before installing the ASPMC630/660 into the PMC slot, ensure that the jumper JP1 is configured properly.

Perform the following steps to install the ASPMC630/660 on your carrier board:

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing and adjusting.

Caution

Inserting or removing modules with power applied may result in damage to module components. Avoid touching areas of integrated circuitry, static discharge can damage these circuits.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground. Note that the system chassis may not be grounded if it is unplugged. The ESD strap must be secured to your wrist and to ground throughout the procedure

2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the carrier board.

3. Remove the filler panel from the carrier board where you are going to install the ASPMC630/660.

4. Verify onboard IDE mastership selected per Table 1-1 for the ASPMC630.
No need to setup ASPMC mastership header JP1 if no other IDE device is added.
Default ASPMC660 header JP1 is configured to enable host IDE controller to access the ASPMC flash disk.
Slide the ASPMC630/660 into the selected carrier PMC slot. Verify that the module seated properly in the Jn1, Jn2 and Jn4 connectors on the carrier board. Do not damage or bend connector pins.

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5. Secure the ASPMC630/660 (convection cool versions) on the carrier board with four screws on top. *See Figure 1-2.*
The ASPMC630/660 Conduction Cool versions must be installed and use all screws' locations available on the carrier.

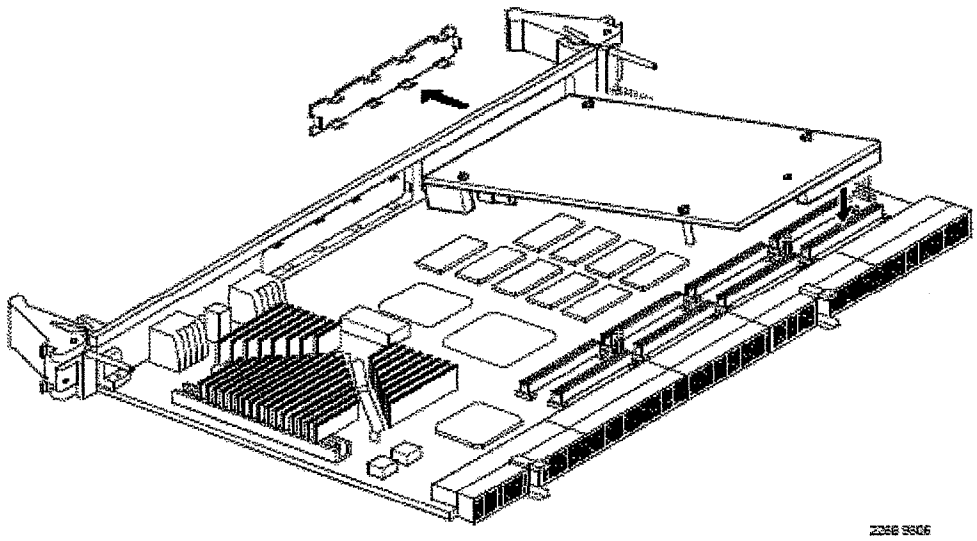


Figure 1-2. ASPMC630/660 Convection Model Installation on carrier board

6. For ASPMC630 select the desired connectivity options:
A. For the Conduction Cool version - Backplane IDE signal routing – go to paragraph #7.
B. For the Convection Cool version - Front IDE P1 connector – go to paragraph #7.1.
Or for ASPMC660 – go to paragraph #8.

7. For backplane IDE connectivity: Slide the selected J3/J5 (for CompactPCI, or P2/P0 for VME) adapter into the corresponding rear selected carrier board slot and properly secure the adapter. Verify that the adapter seated properly connector on the chassis backplane. Connect an IDE cable to your IDE controller.
Note In case of additional IDE devices on same bus, complainant bus architecture should be considered. Adding an IDE device to the above configured setup, must follow IDE master/slave rules.
Go to paragraph #9.

7.1 For front P1 IDE connectivity: Connect an IDE cable from ASPMC630 front P1 connector to your IDE controller.
Note In case of additional IDE devices on same bus, complainant bus architecture should be considered. Adding an IDE device to the above configured setup, must follow IDE master/slave rules.
Go to paragraph #9.

8. For ASPMC660 setup – no cabling is needed.

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9. Backplan connectivity support special Flash Disk Secure Erase and Write Protect (**"WP*"**). Low logical level on **"ERASE*"** signal will initiate **all** media data secure erase operation and Low logical level on (**"WP*"**) will disable any attempt for data write to media. Utilizing Write Protect feature shows Operating System dependency in regard. Each Operating System will show different behavior. Signals could be accessed through backplan (J3/J5 for CompactPCI, or P2/P0 for VME).

10. If you intend to use Debug/PPCbug/CPU-Monitor-F/W interactively, connect the terminal that is to be used as the Debugging system console to the DEBUG port on the front panel of your CPU board.

11. Replace the chassis or system cover(s) and cable peripherals to the panel connectors as required.

12. Reconnect the system to the AC or DC power source and turn the system power on.

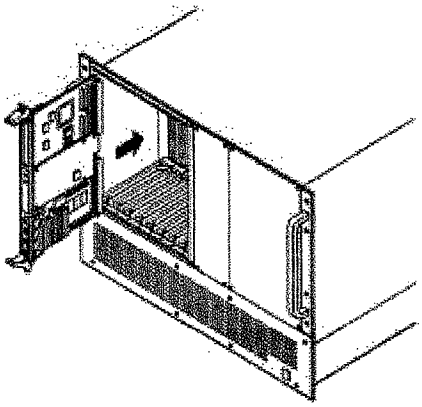


Figure 1-3. ASPMC630/660 (*on-carrier*) Installation and Removal

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2
Operation

Introduction

This chapter provides operating instructions for the ASPMC630/660 **Ultra IDE Fast Flash Disk Module.** It includes necessary information about powering up along with the functionality of the jumpers, status indicators and I/O IDE port.

Indicators

The visible side of the ASPMC630/660 referred as side #2 (Up) and the other (none visible) referred as side #1 (Down).

LED Activity During the Sanitize Procedure

During the Format and Sanitize procedures, the front panel (or side #2) green LED provides the following indications:

a. Remains lit during the Erase phase (for the Sanitize procedure, during each erase phase)

b. Blinks during the Media Fill phase (for the Sanitize procedure, during each fill phase)

c. Remains lit for a short period while the disk achieves ready status after completing the Format or Sanitize procedures

LED Activity During Read/Write/Format

During the Read or Write, the green LED blinks and provides evidence of Flash Disk being accessed. Remains lit for a short period while the disk achieves ready status after completing the Format or Sanitize procedures

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Connectors Pinout

There are four connectors on the ASPMC630/660 – P1 (on the front panel) and Jn4 (PMC I/O) connecting the flash disk to the IDE bus and permitting external IDE controller or devices to be added. The ASPMC630 only draws power through the Jn1/Jn2 while the ASPMC660 interface also to the PCI bus signals through these connectors. Pin assignment is shown in Table 2-1 and Table 2-2.

Notes

ASPMC630 Conduction Cool version IDE Interface is through PMC Jn4 - see table 2-3

ASPMC660 Conduction Cool version interface the flash disk via its PCI interface. No IDE connectivity exist.

Table 2-1. ASPMC660 Jn1, Jn2 pin assignment

Note The ASPMC630 connects only to the power and ground pins of Jn1/Jn2.

Pin #	Jn1				Jn2		Pin #
1	TCK	–12V	2	1	+12V	TRST*	2
3	GND	INTA*	4	3	TMS	TDO	4
5	INTB*	INTC*	6	5	TDI	GND	6
7	BUSMODE1#	+5V	8	7	GND	Not Used	8
9	INTD*	Not Used	10	9	Not Used	Not Used	10
11	BUSMODE2#	Not Used	12	11	Pull-up	+3.3V	12
13	CLK	GND	14	13	RST*	BUSMODE3#	14
15	GND	PMCGNT*	16	15	+3.3V	BUSMODE4#	16
17	PMCREQ*	+5V	18	17	Not Used	GND	18
19	V (I/O)	AD31	20	19	AD30	AD29	20
21	AD28	AD27	22	21	GND	AD26	22
23	AD25	GND	24	23	AD24	+3.3V	24
25	GND	C/BE3*	26	25	IDSEL	AD23	26
27	AD22	AD21	28	27	+3.3V	AD20	28
29	AD19	+5V	30	29	AD18	GND	30
31	V (I/O)	AD17	32	31	AD16	C/BE2*	32
33	FRAME*	GND	34	33	GND	Not Used	34
35	GND	IRDY*	36	35	TDRY*	+3.3V	36
37	DEVSEL*	+5V	38	37	GND	STOP*	38
39	GND	LOCK*	40	39	PERR*	GND	40
41	SDONE*	SBO*	42	41	+3.3V	SERR*	42
43	PAR	GND	44	43	C/BE1*	GND	44
45	V (I/O)	AD15	46	45	AD14	AD13	46
47	AD12	AD11	48	47	M66EN	AD10	48
49	AD09	+5V	50	49	AD08	+3.3V	50
51	GND	C/BE0*	52	51	AD07	Not Used	52
53	AD06	AD05	54	53	+3.3V	Not Used	54
55	AD04	GND	56	55	Not Used	GND	56
57	V (I/O)	AD03	58	57	Not Used	Not Used	58
59	AD02	AD01	60	59	GND	Not Used	60
61	AD00	+5V	62	61	ACK64*	+3.3V	62
63	GND	REQ64*	64	63	GND	Not Used	64

Note All unassigned pins are N.C. (not connected).

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Table 2-2. *ASPMC630/660 Convection Cool versions P1 Front Panel (40 pin Connector) pin assignment*

Note
ASPMC630 Conduction Cool version IDE Interface is through PMC Jn4 see table 2-3
ASPMC660 Conduction Cool version interface the flash disk via its PCI interface. No IDE connectivity exist.

Pin #			Pin #
1	RESET*	GND	**2**
3	HD7	HD8	**4**
5	HD6	HD9	**6**
7	HD5	HD10	**8**
9	HD4	HD11	**10**
11	HD3	HD12	**12**
13	HD2	HD13	**14**
15	HD1	HD14	**16**
17	HD0	HD15	**18**
19	GND	KEY	**20**
21	DMARQ	GND	**22**
23	HIOW*	GND	**24**
25	HIOR*	GND	**26**
27	IORDY	CSEL	**28**
29	DMACK*	GND	**30**
31	INTRQ	IOCS16*	**32**
33	HA1	PDIAG	**34**
35	HA0	HA2	**36**
37	CS0*	CS1*	**38**
39	DASP*	GND	**40**

Note
All unassigned pins are N.C. (not connected).

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Table 2-3. ASPMC630-nnnn-C (Conduction Cool version only) Jn4 Connector pin Assignment

Note: The ASPMC660 connects only to the ERASE* (pin #51) and WP* (Write Protect pin#52) of Jn4. Jn4 Pin #54 is reserved for future use.

Pin #			Pin #
1	RESET*	GND	2
3	HD7	HD8	4
5	HD6	HD9	6
7	HD5	HD10	8
9	HD4	HD11	10
11	HD3	HD12	12
13	HD2	HD13	14
15	HD1	HD14	16
17	HD0	HD15	18
19	GND	KEY	20
21	DMARQ	GND	22
23	HIOW*	GND	24
25	HIOR*	GND	26
27	IORDY	CSEL	28
29	DMACK*	GND	30
31	INTRQ	IOCS16*	32
33	HA1	PDIAG	34
35	HA0	HA2	36
37	CS0*	CS1*	38
39	DASP*	GND	40
41	N.C.	N.C.	42
43	N.C.	N.C.	44
45	N.C.	N.C.	46
47	N.C.	N.C.	48
49	N.C.	N.C.	50
51	ERASE*	WP*	52
53	GND	RESERVED	54
55	N.C.	N.C.	56
57	N.C.	N.C.	58
59	N.C.	N.C.	60
61	N.C.	N.C.	62
63	N.C.	N.C.	64

Note

All unassigned pins are N.C. (not connected).

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3

Functional Description

Introduction

This chapter provides a functional description for the ASPMC630/660 **IDE Fast Flash Disk Module**. The ASPMC630/660 is a high-performance product featuring M-Systems FFD technology. M-Systems UltraATA Fast Flash Disk (FFD) disk is a state-of-the-art, solid-state disk based on NAND flash technology, containing no moving parts.

The outstanding performance of the UltraATA FFD is based on M-Systems' TrueFFS® technology that provides full disk emulation, enhanced endurance with dynamic wear-leveling and bad-block mapping-out flash management.
Due to its unique design, the UltraATA FFD eliminates seek time, latency and other electro-mechanical delays inherent in conventional disk drives.

The FFD UltraATA IDE provides superior performance up to 100 MBytes/sec burst rate, up to 40 MBytes/sec sustained read/write rate. The UltraATA FFD IDE is fully compatible with the IDE-2 IDE-3 and IDE-5 (ATA-5) interface.
UltraATA FFD top reliability, 5,000,000 Write/Erase cycles, unlimited Read and high MTBF, MIL-STD 810F compliant NEBS Level 3 compliant, 1500G operating shock, 16.3G RMS operating random vibration -40°C to +85°C operating temperature, -55°C to +95°C storage temperature and up to 70,000 feet operating altitude enables solutions to extreme demanding applications.

UltraATA FFD provides an ideal storage solution for mission-critical applications that must operate under harsh environmental conditions. Mass storage solutions for data recorders, automotive, moving maps, sonar, radar, fire control systems, black boxes, data acquisition systems and rugged laptops and servers in air force, navy and army installations worldwide featuring a maintenance-free solution.

Features Summary

The table below lists the general features for the ASPMC630/660. Refer *to Appendix A, General Specifications*, for additional product specifications and information.

Table 3-1. ASPMC630/660 General Features

Feature	Specification
	• 1 GB – 16 Bytes of non-volatile Flash memory in a single PMC slot • Burst Read/Write rates (Synchronous) 100 Mbytes/sec • Sustained Read/Write up to 40 Mbytes/sec • Less than 20 µsec access time • Fast security erase and Sanitize : 5-35 sec entire media typical • FFD MTBF - 952,925 hours for 2.0GB (Telcordia SR-332, GB, 25°C) • Embedded EDC/ECC, based on 48-bit Reed Solomon Algorithm • Built-in power-up self test

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- Automatic self-diagnostics
- TrueFFS® dynamic wear-leveling and bad block mapping out algorithms
- Very low power – max 910mA / 4.7 W @ 16 GB max power dissipation (depending on capacity). Max 620 mA / 3.8 W for the ASPMC630
- >5,000,000 Write/Erase cycles; Read unlimited
- Operating temperatures : Commercial 0°C +70°C , Enhanced -25°C +75°C, Extended -405°C +85°C
- Humidity 5 to 95% relative, non-condensing
- Altitude (operating & non-operating) up to 70,000 feet
- ANSI IDE-2, IDE-3 and IDE-5/ATA-5 Standard Protocol (Industry Standard IDE-2, CCS, ANSI IDE Standard X3.131-1994)
- No special OS drivers required - uses existing Windows, VxWorks® , other OS's IDE drivers
- Supported by Integrity® OS.
- Long term product lifecycle support
- Air convection or conduction cool for harsh and rugged applications
- Conformal coating – optional
- MIL-STD 810F Compliant FFD

Features Descriptions

General

As stated earlier, the ASPMC630/660 is a high-performance PMC based single slot module featuring M-Systems' TrueFFS® technology.
Designed to meet the needs of OEM's servicing the extreme automotive, military and aerospace, industrial automation and semiconductor process equipment market segments, the ASPMC630/660 is available in commercial grade (0°C to 70°C), industrial/enhanced grade (–25°C to 75°C) and extended (–40°C to 85°C) temperatures.

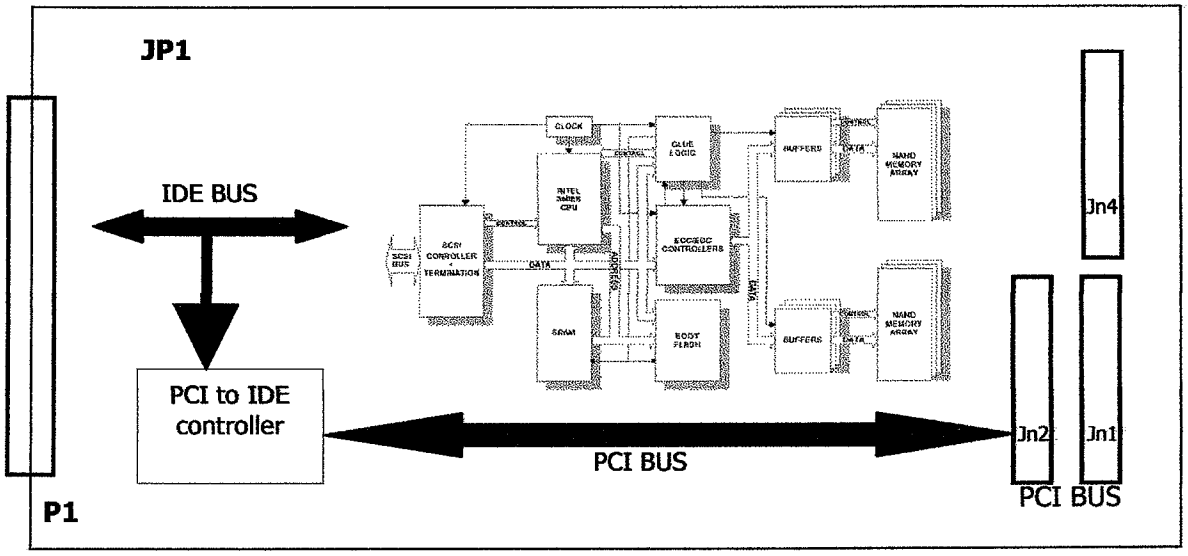


Figure 3-1. ASPMC630/660 Block Diagram

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Memory

Flash Memory

The ASPMC630/660 contains several banks of Flash memory FFD devices having capacities up to 16GB of FFD Flash Disk.

ASPMC660 PCI Interface F/W

The ASPMC660 contains a PCI to IDE controller with dedicated F/W (Firmware). Thus, enabling the Flash Disk IDE to be accessed as a global PCI disk device. Upon system startup, computer's PCI BIOS scan the PCI (or CompactPCI) bus for added functions. The ASPMC660 and the rest of functions are found, registered by the BIOS as active functions and presented to the OS (Operating System) once booted. The ASPMC660 dedicated F/W offers Flash Disk initialization & configuration management on system power-on startup.

Input/Output Interfaces

P1, Jn4 IDE Interface

The ASPMC630/660 has standard P1 (40pin) IDE interconnect mechanism used to route the IDE signals to the external controller. The ASPMC630 front P1 (only at the Convection Cool version) and Jn4 (at the Conduction Cool version) enables the user to connect an IDE controller to the Flash Disk IDE interface while the ASPMC660 (P1) can be connected to eternal IDE device (e.g. – second disk). IDE pin assignment is shown in Tables 2-2 and 2-3. The Jumper header JP1 sets IDE MASTER/SLAVE mode for the on-board Flash Disk and applicable for the ASPMC630.

Routing the ASPMC630/660 IDE interface to the CompactPCI backplan J3 or J5 is managed by the carrier. Each PMC modules carrier routes it's hosted PMC I/O signals to the CompactPCI, VME (or other bus) backplan interconnect connectors. As a general rule, the PMC I/O signals are routed to J3 or J5 for CompactPCI and to P1 or P0 for VME carriers. (Figure 3-2). A carrier is defined to be either a CPU board, active (bridged) PCI carrier or passive one.

Jn4 Secure Erase and Write Protect

Backplan connectivity and front panel P1 support special Flash Disk Secure Erase and Write Protect (**"WP*"**). Low logical level on **"ERASE*"** signal will initiate **all** media data secure erase operation and Low logical level on (**"WP*"**) will disable **any** attempt for data write to media.

Signals could be accessed through backplan (J3/J5 for CompactPCI, or P2/P0 for VME). Refer to Jn4 at Table 2-3.

PCI Jn1/Jn2 Interface

The PCI/CompactPCI bus (address/data/control) is not connected at the ASPMC630. The ASPMC630 only draws power through the Jn1/Jn2 pins while the ASPMC660 interface also to the PCI bus through these connectors. The ASPMC660 is 3.3V I/O signals tolerant.

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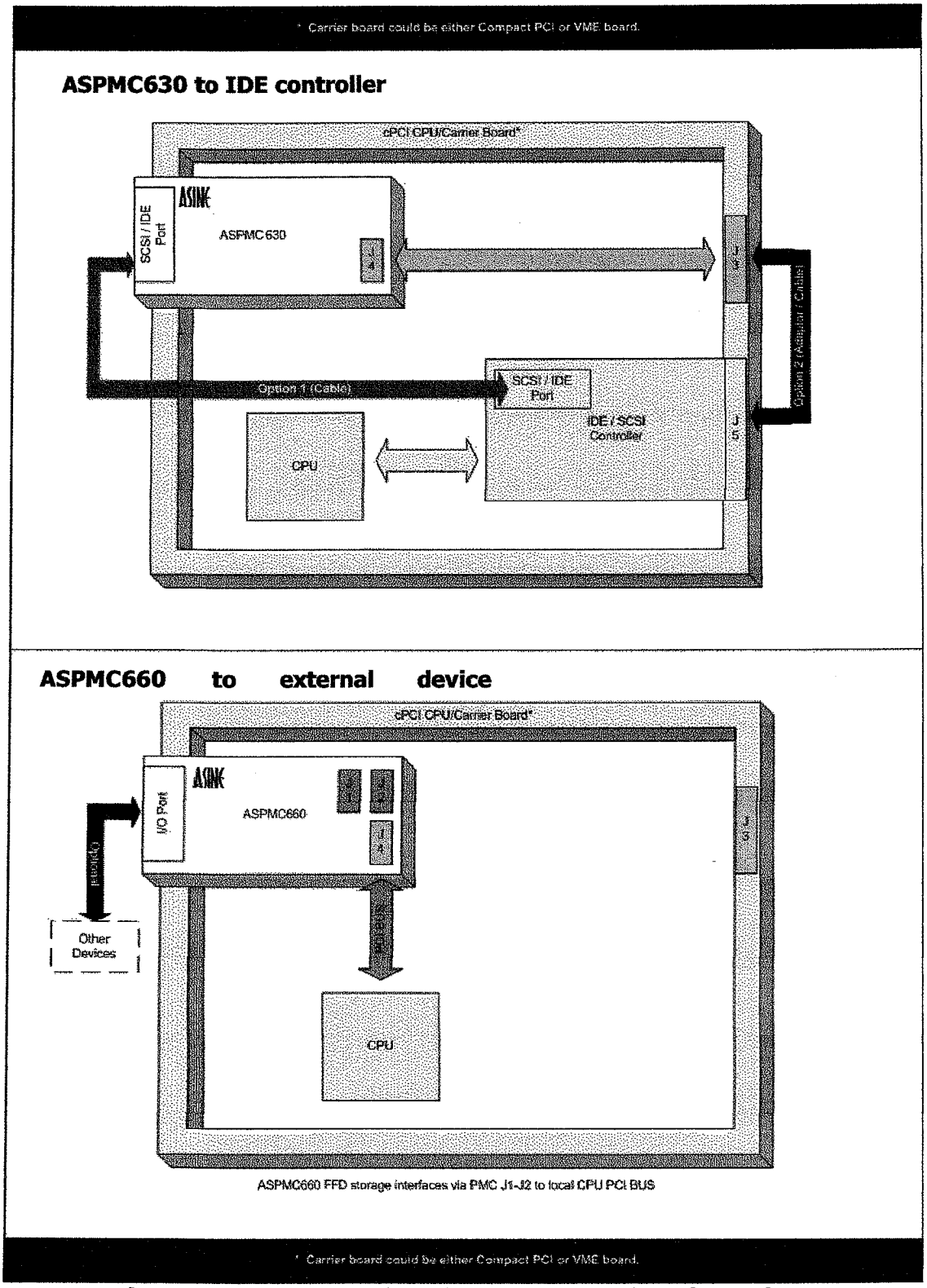


Figure 3-2. ASPMC630/660 interconnect and carrier options

Power supply

The ASPMC630/660 utilizes +5V supply from Jn1/Jn2.

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Appendix A

Introduction

This appendix lists general specifications and power characteristics for the **ASPMC630/660 Series IDE/PCI Flash Disk Modules.**

Specifications

Table A-1. ASPMC630/660 Specifications

General and Reliability

Parameter	Unit	Value	Min	Typ.	Max
Form Factor	NA	PMC IEEE1386.1			
Bus type	NA	PCI 3.3V/5V for ASPMC660			
Connectors Type	male 2.54mm	40 pin			
Optional coating	IPC610C Standard	1B31			
FFD Case	NA				
Weight – Convection Cool Model	Gr.				240 @ up to 6GB
Cooling No suffix		Force air or surface temperature not to exceed operating temperature range			
Cooling and Mechanical 'C' suffix		IEEE 1101.2-1992 and IEEE 1386.1 standards, 10mm height			
Reliability Read cycles Write cycles EDC/ECC Bad Block File System Diagnostics Dynamic Wear leveling		 Unlimited 48bit Reed Solomon Auto Mapout TrueFFS® Self test Yes			 5,000,000
ASPMC630 - Operating System support		No specific drivers needed for any IDE drive supported OS. Embedded support through Windows, Solaris, VxWorks using existing SCSI drivers Integrity OS supported			
ASPMC660 - Operating System support		Linux - No specific drivers needed for kernels 2.4 and later. Drivers support through Windows 9X/ME/ 2K/XP, VxWorks embedded drivers BSP			

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Max. Ratings

Parameter	Unit	Value	Min	Typ.	Max
Voltage	V		4.75	5	5.25
Current	mA		220 @ 256MB Standby mode		800 @ 4GB
Power dissipation -630 -660	Watt			 2.6 @ 8 GB 3.9 @ 8 GB	 3.3 @ 8GB 4.2 @ 8GB
Operating Temperature 'C' suffix 'E' suffix 'Z' suffix	Celsius		 0 -25 -40		 +70 +75 +85
Shock and Vibration	G RMS		(analyzed per MIL810F) FFD 16.3G-rms, random, 20-2000Hz, 3 vibration axes		
Altitude	Feet		0		60,000
Relative Humidity	% Relative		5		95
Storage	Celsius		-55		+95

Operating Environment

Parameter	Unit	Value	Min	Typ.	Max
Voltage	V		4.75	5	5.25
Current	mA		220 @ 256MB Standby mode		800 @ 4 GB
Power dissipation -630 -660	Watt			 2.6 @ 8 GB 3.9 @ 8 GB	 3.3 @ 8GB 4.2 @ 8GB
Operating Temperature 'C' suffix 'E' suffix 'Z' suffix	Celsius		 0 -25 -40		 +70 +75 +85
Voltage	V		4.75	5	5.25
Altitude	Feet		0		60,000
Relative Humidity	% Relative		5		95

Power Consumption @ 5V supply

Parameter	Unit	Value	Min	Typ.	Max
Current	mA		220 @ 256MB Standby mode		800 @ 4 GB
Power dissipation -630 -660	Watt			 2.6 @ 8 GB 3.9 @ 8 GB	 3.3 @ 8GB 4.2 @ 8GB

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Electrical Interface and Capacity*

Parameter	Unit	Value	Min	Typ.	Max
PCI bus	NA	Rev. 2.2 32bit/33MHz 3.3V and 5V signaling			
Transfer rate – Burst Read/Write Read, Sustained @ 32KB blocks Write, Sustained @ 32KB blocks	MB/Sec.				 100 40 40
Access time	uSec.				20
Seek time		No seek time			
IDE level					DMA0-2, Ultra-DMA 0-5, PIO 0-4
IDE ID		Supported, CS0/CS1			
IDE I/F		40 pin			
IDE mastership		*Cable, Master, Slave* selectable			
Status Green LED		Activity			
Flash Media Erase	Sec.			5 @ 256MB 35 @ 4GB	
Flash Media Erase + Fill NSA 130-2 and USA-AF AFSSI 5020	Sec.			24 @ 256MB 400 @ 4GB	

* Flash disk parameters represent media overall performance.

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Appendix B
Related Documentation & Specifications

Document	Description
P1386.1	IEEE - Common Mezzanine Card Specification (CMC)
1101.2-1992	IEEE Conduction Cooled PCI Mezzanine Card
PCI Local Bus Specification	Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1
X3.131.1990	ANSI Small Computer System Interface-2 (IDE-2),Draft Document Global Engineering Documents – Web Site:http://global.ihs.com/index.cfm
ANSI/VITA 1-1994	VME64 Specification VITA (VMEbus International Trade Association) Web Site:http://www.vita.com/
PICMG 2.0 R3.0	CompactPCI Core Specification
PICMG 2.3 R1.0	PMC on CompactPCI
	M-Systems FFD 2.5" Ultra Narrow IDE product specification Web Site:http://www.m-sys.com/

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