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U S E R ' S M A N U A L

SLEWABLE FUNCTION GENERATOR INDUSTRY PACK

MODEL IP202S

Document Part No: 11027724D

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INTRODUCTION

This manual describes the operation and use of the C&H Model IP202S Industry Pack Module (Part Number 11027720 Rev. A of higher). This mezzanine module is designed to interface within any Industry Pack carrier adhering to the ANSI/VITA 4-1995 IndustryPack® standard. These carriers are available in many formats such as VME, VXI, PXI, PC-AT, PCI, and cPCI. C&H provides two carriers (Models VX403B and VX403C) that allows up to four standard Industry Pack modules to be installed in a single VXI slot.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

The part numbers covered by this manual are:

Part Number	Description
11027720-0001	Direct Output only
11027720-0002	Direct and Transformer Output

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1.0 GENERAL DESCRIPTION

The IP202S is a single wide industry pack (IP) function generator that provides a signal output that can sweep through a frequency range at a programmable slew rate. The output signal can be a sine, square, triangle, or sawtooth waveform up to 1 MHz. Signal amplitude and offset level can also vary with the frequency. The IP202S can be used with any conforming industry pack carrier module, such as VME/VXI, PXI, PC-AT, PCI, or cPCI.

1.1 PURPOSE OF EQUIPMENT

This IP is well suited for typical signal function generation and situations requiring frequency sweeping operations, such as the simulation of wheel sensor and tachometer outputs. The IP is particularly useful for testing automotive electronics, such as those used in anti-lock braking systems.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

- Slewable frequency with selectable frequency ranges
- Programmable slew (sweep) times, start/stop frequencies, amplitude, offset level, and dwell (delay) times
- Selectable waveform output -- sine, square, triangle, and sawtooth (sawtooth obtained by adjusting duty cycle of triangle waveform)
- Separately programmable output amplitude (10Vpp) and offset level (±5V) for both the start and stop frequencies
- Programmable and Externally Modulated Duty Cycle
- Fixed, Single Ramp, Single Cycle and Continuous Cycle modes
- External slew start synchronization using IP Strobe input or external strobe signal
- Software control to pause, then continue ramping or cycling
- Optional isolated transformer coupled output (-0002 option)

1.2.2 Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		+0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V from IP interface	150	mA
	+12V from IP interface	60	mA
	-12V from IP interface	60	mA

AC CHARACTERISTICS

		Limit			
Parameter	**Conditions**	**Min**	**Typ.**	**Max**	**Units**
Frequency					
- Range	Four sweep ranges[1]	0		1.023	MHz
- Programming Resolution	Range: 0 to 1.023KHz		1		Hz
	0 to 10.23KHz		10		Hz
	0 to 102.3KHz		100		Hz
	0 to 1.023MHz		1000		Hz
- Accuracy	For frequencies > 1% of range full-scale			1.0	%
Direct Output Characteristics (OUT)					
Output Impedance	Output enabled	0.5		1.0	Ω
	Output disabled		180		KΩ
Output Current		-50		+50	mA
Amplitude Range	No load	0		10	Vpp
Amplitude Resolution	8 bits		0.039		V
Amplitude Accuarcy	or 100mV, which ever is greater			±7	%
DC Offset Range	No load	-5		+5	V
DC Offset Resolution	8 bits		0.039		V
DC Offset Accuracy	or 100mV, which ever is greater			±7	%
Total Harmonic Distortion	Sine wave	-30			dB
Rise/Fall Time	Square wave (10% to 90% at full output)			40	ns
Overshoot	No load, p-p amplitude at full output			2	%
Transformer Output Characteristics (TOUTH/L) (-0002 only)					
Impedance	10K:10K Transformer		1		KΩ
Response	300Hz – 50KHz		±2		dB
Frequency Sweep					
Modes	Fixed, single ramp, single cycle, and continuous				
Type	Exponential				
Sweep Rate	Range: 0 to 1.023KHz	.020		6^2	KHz/sec
	0 to 10.23KHz	.2		60^2	KHz/sec
	0 to 102.3KHz	2		600^2	KHz/sec
	0 to 1.023MHz	20		6000^2	KHz/sec
Resolution	Incremental percentage change (7 bits)		5		%

AC CHARACTERISTICS (continued)

Parameter	Conditions	Limit Min	Typ.	Max	Units
Amplitude Sweep					
Type	Linear				
Time	Proportional to frequency sweep rate[3]				
Span		0		10	Vpp
DC Offset Sweep					
Type	Linear				
Time	Proportional to frequency sweep rate[3]				
Span		-5		+5	V
Dwell Time					
Resolution	Programmable: 1ms, 10ms, 100ms, or 1 sec.				
Accuracy	Percentage + 500µs		±1		%
Duty Cycle					
Resolution	5 bits		2.3		%
Range		15		85	%
Accuracy	In absolute percentage points		±3		%
EXTSTB Input					
Level	Selectable: Zero Crossing TTL CMOS		0 0.8 2.5		V V V
Input Impedance	Selectable: Low High	 10	50		Ω KΩ
EXTDC Input					
Level	Varies duty cycle from 85% down to 15%	-2.3		+2.3	V
Resolution			15		%/V
Modulation				2	MHz

Notes:
1. All ranges start at 0Hz. Frequency ramping and cycling operations can not cross from one range to the next.
2. Although the values can be programmed higher than this, the practical limit is shown.
3. Point A to Point B in the same time frequency sweeps from Point A to Point B.

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 4-1995 for single-wide IP modules. The nominal dimensions are 3.900" (990.6 mm) long × 1.800"(4.572 mm) wide.

1.2.4 Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +50°C
Storage Temperature:	-40°C to +70°C
Humidity:	<95% without condensation

Carrier modules may differ in environmental specification. Refer to the carrier's documentation for information.

1.2.5 Bus Compliance

The module complies with the Industry Pack Specification ANSI/VITA 4-1995 for single-wide IPs.

Manufacturer ID:	25_{16}
Model Number:	02_{16}
Clock Rate:	8 MHz
Data Transfer:	16 bit
Strobe:	supported
Interrupts:	not supported
DMA:	not supported
ID Space:	Twelve (12) bytes, including CRC (read-only)
IO Space:	Four (4) 16-bit locations
Memory Space:	none

1.2.6 Applicable Documents

ANSI/VITA 4-1995 Industry Pack Specification, VITA, 1995

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

In most cases the IP202S is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the carrier immediately as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The IP202S contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF IP MODULES

All IP modules must be installed into the carrier before the carrier is installed into the host system. IPs are installed by firmly pressing the connector on the IP together with the connector on the carrier. The connectors are keyed to prevent wrong insertion. Secure the IP with mounting hardware provided as shown in Figure 1.

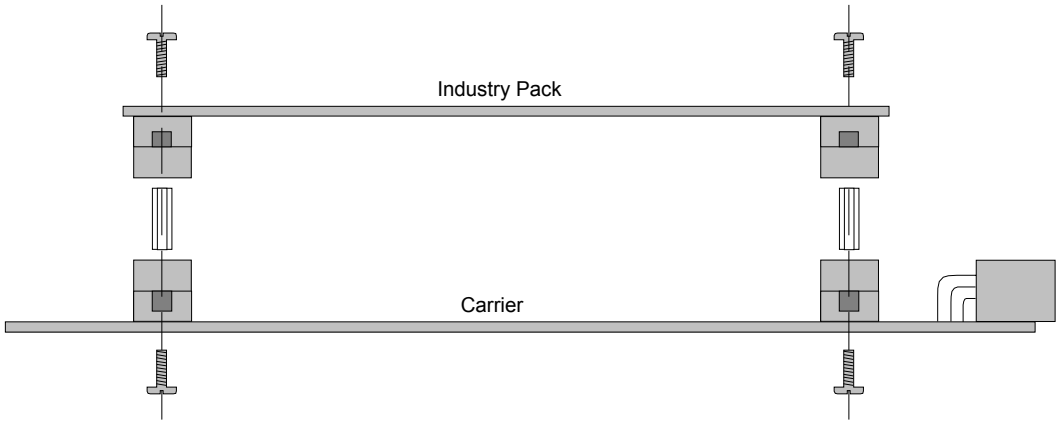


Figure 1. IP Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

The IP202S provides a signal output that can sweep through a frequency range at a programmable slew rate. The output signal can be a sine, square, triangle, or sawtooth waveform up to 1 MHz. A simplified block diagram of the module is shown in Figure 2.

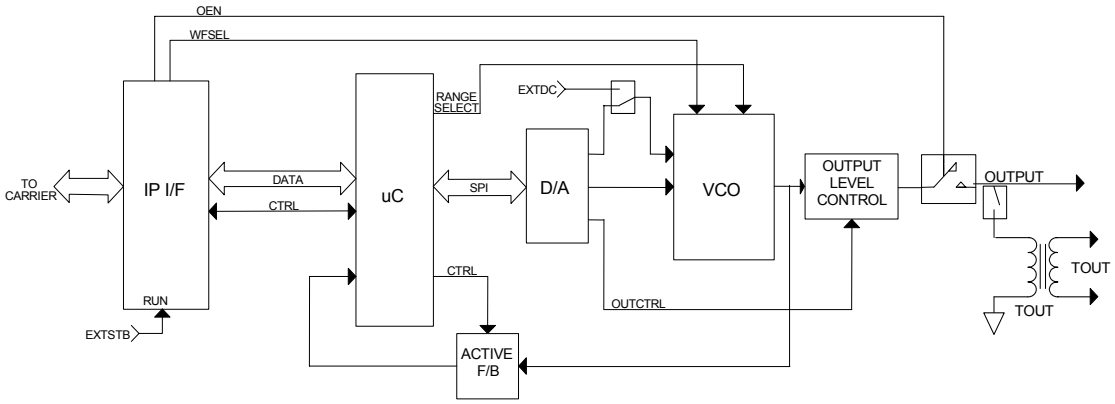


Figure 2. Functional Block Diagram

3.1.1 IP Interface

The IP interface provides the electrical connection, buffering, and control between the carrier board and the frequency generation and slewing logic.

3.1.2 Microcontroller

The microcontroller provides timing of all functions for slew rate control of the output frequency. Serial data is continuously output to the digital/analog converters to set the VCO at the desired frequency and duty cycle.

3.1.3 Digital/Analog Converters (DACs)

These serial DACs convert the serial data from the microcontroller into a voltage level signal to control the VCO.

3.1.4 Voltage Controlled Oscillator (VCO)

The VCO converts the voltage input from the DACs into a output signal of the desired frequency, duty cycle, and waveform.

3.1.5 Output Control

The output control provides output amplitude control and signal conditioning.

3.1.6 Active Feedback

The active feedback logic provides continuous output frequency monitoring and input to the microcontroller for frequency adjustment due to temperature and component variations.

3.1.7 Transformer

The optional transformer coupled output provides an magnetically isolated signal source for loads requiring isolation from the module ground. The frequency response is 300Hz - 50KHz (±2dB). The reflected source impedance is 1000 ohms. The DC Offset capability is lost due to the transformer coupling.

3.2 OPERATION

3.2.1 Operational Modes

Four modes of operation are available: Fixed, Single Ramp, Single Cycle, and Continuous Cycle. The mode of operation is controlled by configuration bits in the Status/Control Register. In all modes, the RUN bit must be set to allow frequency sweeping. The STB (Strobe Enable) bit, allows external hardware synchronization of the beginning of the cycle. With Strobe enabled, in Single Ramp and Single Cycle modes, the strobe signal acts as a trigger. The ramp or cycle begins when the strobe signal goes active and will complete the ramp or cycle regardless of the level of the strobe signal. In Fixed or Continuous Cycle mode, the output frequency will follow or start cycling when the strobe signal goes active. When the strobe signal goes inactive, it will hold at the current frequency. However, if it becomes active again, the output will change to and start from Frequency A.

Fixed Mode In Fixed mode, the output frequency slews to the programmed Frequency A at the rate specified by Slew Rate A. If the programmed Frequency A is changed, the output frequency slews toward the new programmed value at the specified slew rate. If the programmed frequency is changed before the frequency is reached, the output frequency slews from the current frequency towards the new programmed frequency at the specified slew rate. Dwell Times A and B are ignored in this mode.

Single Ramp In Single Ramp mode, the output frequency always begins at Frequency A. The cycle begins when the RUN bit is set. If the current frequency is not equal to Frequency A, the output frequency immediately changes (ignoring the slew rate) to the programmed Frequency A. The output then slews toward Frequency B at the rate specified by Slew Rate A. When Frequency B is reached, the RUN bit is automatically cleared and the output frequency holds at Frequency B. The output amplitude and offset level also changes according to the programmed values for Amplitude A and B and Offset A and B (see 3.2.2). Dwell Times A and B are ignored in this mode.

Single Cycle In Single Cycle mode, the output frequency always begins at Frequency A. The cycle begins when the RUN bit is set. If the current frequency is not equal to Frequency A, the output frequency immediately changes (ignoring the slew rate) to the programmed Frequency A. The output then slews toward Frequency B at the rate specified by Slew Rate A. When Frequency B is reached, the output remains at Frequency B until Dwell Time B has expired. It then slews toward Frequency A at the rate specified by Slew Rate B. When Frequency A is reached, the RUN bit is automatically cleared and the output frequency holds at Frequency A. The output amplitude and offset level also changes according to the programmed values for Amplitude A and B and Offset A and B (see 3.2.2). Dwell Time A is ignored in this mode.

Continuous Cycle Continuous Cycle mode operates the same as Single Cycle mode, except operation does not stop after one cycle and the RUN bit is not cleared. The output frequency continuously sweeps between Frequency A and Frequency B. When Frequency B is reached, the output remains at Frequency B until Dwell Time B has expired. It then slew towards Frequency A at the rate specified by Slew Rate B. When Frequency A is reached, the output remains at Frequency A until Dwell Time A has expired and then the cycle repeats. The

output amplitude and offset level also change according to the programmed values for Amplitude A and B and Offset A and B (see 3.2.2).

3.2.2 Output Level Control

The output level is controlled by setting the Amplitude and Offset in the Output Level Control Register. The amplitude and offset for Frequency A can be different than the Frequency B amplitude and offset. During frequency slewing, the amplitude and offset will proportionally change as the frequency changes. The peak-to-peak amplitude can be varied from 0Vpp to 10Vpp and the DC offset can be varied from -5V to +5V. To output a waveform with a low level of 0V and a high level of 4V, set the amplitude to 4Vpp and the offset to +2V.

3.2.3 Duty Cycle

The waveform duty cycle (defined as the percentage of time that the output waveform is above the DC offset) can be software programmed or controlled by an external signal to facilitate pulse-width modulation and the generation of sawtooth waveforms. The duty cycle can also be used to reduce sine-wave distortion. The Duty Cycle jumper as described in section 3.3 defines the method of control. The duty cycle can vary from 15% to 85%. To software program the duty cycle, place the Duty Cycle jumper in the SW position and program the desired duty cycle in the Status/Control Register. To control the duty cycle externally, place the Duty Cycle jumper in the EXT position and apply a -2.3V to +2.3V signal to the EXTDC control pin on the IP I/O connector. The duty cycle can be modulated up to 2MHz.

3.3 HARDWARE CONFIGURATION

Jumper selectable options are shown in Figure 3.

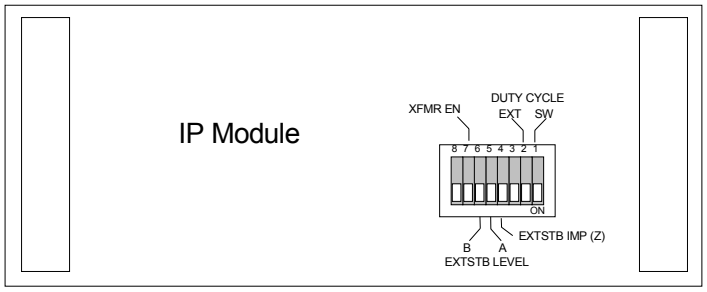


Figure 3. Hardware Configurable Controls

XFMR EN This switch enables the optional transformer coupled output.

Duty Cycle These switches select either software or external duty cycle control to allow generation of sawtooth waveforms or pulse-width modulation of the output signal. Do not select both.

EXTSTB Impedance (Z) This switch selects the input impedance of the EXTSTB front connector signal. With the switch ON the input impedance is 50Ω. With the switch OFF (default), the impedance is >10KΩ.

EXTSTB Level These switches control the threshold level of the EXTSTB front connector signal. The level can be set to 0V (zero crossing), TTL (0.8V), or CMOS (2.5V).

Threshold	Switch A	Switch B
0V	OFF	OFF
TTL	ON	ON
CMOS	ON	OFF

3.4 CONNECTORS

3.4.1 IP Logic Bus Connector

The IP logic bus connector contains signal and voltage connections for the standard IP interface logic. (See Appendix A for pin assignments)

3.4.2 I/O Connector

The IP I/O connector provides the output signal and various status/control signals. (See Appendix A for pin assignments)

OUT	Sine, triangle, or square wave signal out *(Variable Level Output and Offset)*
TOUTH	Isolated transformer coupled output, high side *(1000Ω, 300Hz-50KHz response)*
TOUTL	Isolated transformer coupled signal output, low side *(1000Ω, 300Hz-50KHz response)*
EXTSTB*	The External Strobe is logically ORed (either strobe active produces an internal Strobe signal) with the IP interface STROBE* signal to produce the internal Strobe signal. A 10K pull-up is provided on the EXTSTB*. *(TTL/CMOS Active Low Input)*
EXTDC	The External Duty Cycle adjust input controls the waveform duty cycle (defined as a percentage of time the waveform is positive) if the Duty Cycle jumper is configured for external duty cycle control. Varying the voltage from +2.3V to -2.3V causes the output duty cycle to vary from 15% to 85%, about 15% per volt. The duty cycle can be modulated up to 2MHz. *(Input)*
+5V	+5V supply. Can used for external buffer, amplifier, or other logic. *(Do not exceed 500mA)*
+12V	+12V supply. Can used for external buffer, amplifier, or other logic. *(Do not exceed 100mA)*
-12V	-12V supply. Can used for external buffer, amplifier, or other logic. *(Do not exceed 100mA)*

3.5 CONFIGURATION REGISTERS

3.5.1 ID PROM Registers

The ID PROM registers provide manufacturer and module number as shown in Table I.

Table I. ID PROM Contents

IP Address, hex	Register Description	Value, hex
01	ASCII "I"	49
03	ASCII "P"	50
05	ASCII "A"	41
07	ASCII "C"	43
09	Manufacturer ID	25
0B	Model Number	02
0D	Revision Level	10*
0F	Reserved	00
11	Low Byte Driver ID (Firmware Rev)	30*
13	High Byte Driver ID	00
15	Number of Bytes Used	0C
17	CRC	84*

* These values may differ, depending on the revision levels.

3.5.2 I/O Registers

There are a variety of registers used to configure and control the IP202S module. The registers are addressable within the I/O Space. An address map of the registers is shown in Table II. Details of the registers is provided in Figure 4.

Table II. I/O Address Map

IO Address, hex	Register Description
00	Status/Control
02	Waveform Control
04	Output Amplitude Control
06	Output Offset Control
08	Frequency A Control
0A	Dwell/Slew A Control
0C	Frequency B Control
0E	Dwell/Slew B Control

Status/Control Register (00_{16}) This read/write register provides the main control and status of the module operation Bits are provided for controlling the operational mode, strobe (run) configuration, output enable, and self-test initiation.

Waveform Control Register (02_{16}) This read/write register provides control of the waveform (square, triangle, or sine), duty cycle, and frequency range.

Output Amplitude Control Register (04_{16}) This read/write register provides control of the peak-to-peak signal level of the output at Frequency A and at Frequency B.

Output Offset Control Register (06_{16}) This read/write register provides control of the voltage offset of the output at Frequency A and at Frequency B.

Frequency A/B Control ($08_{16}/0C_{16}$) These read/write registers provides control of Frequency A and B. A special read-back mode on the Frequency A Register allows the current output frequency to be monitored. The output frequency and resolution depends on the Range selected in the Waveform Control Register as shown in Table III.

Dwell/Slew A/B Control ($0A_{16}/0E_{16}$) These read/write registers provides control of the dwell time and slew rate for Frequency A and B. Dwell A sets the amount of time the output stays (dwells) at Frequency A after either Run is enabled or Frequency A is reached when in Continuous Cycle mode. Slew A sets the rate at which the output frequency will sweep from Frequency A to Frequency B. Dwell B sets the amount of time the output stays (dwells) at Frequency B after Frequency B is reached when in Single Cycle or Continuous Cycle mode. Slew B sets the rate at which the output frequency will sweep from Frequency B to Frequency A. Table III shows the slew rate range for each frequency range. Each increment in slew rate is 5% faster than the previous slew rate. The following formulas apply:

if SlewValue = $7F_{16}$,
then
SlewRate = ∞ (frequency change is immediate),
else

$$\text{SlewRate} = 20 \times \text{RangeFactor} \times 1.05^{\text{SlewValue}}$$

$$\text{SlewValue} = \frac{\log\left(\frac{\text{SlewRate}}{20 \times \text{RangeFactor}}\right)}{\log(1.05)}$$

where SlewRate = the desired slew rate in Hz/second
SlewValue = the 7-bit binary register value for the slew
RangeFactor = the multiply factor for the selected range:

Selected Range	Factor
0 - 1.020KHz	1
0 - 10.20KHz	10
0 - 102.0KHz	100
0 - 1.020MHz	1000

Table III. Frequency and Slew Rates

Selected Range	Frequency Bit Resolution	Slew Rate Range	Slew Rate Resolution
0 - 1.023KHz	1Hz	20 - ~10K Hz/sec.	5% increments
0 - 10.23KHz	10Hz	200 - ~100K Hz/sec.	5% increments
0 - 102.3KHz	100Hz	2K - ~1M Hz/sec.	5% increments
0 - 1.023MHz	1000Hz	20K - ~10M Hz/sec.	5% increments

Status/Control Register

00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(read-only)				-	*RBI*	*FCO*	RS	PAU	Mode			INV	STB	RUN	OEN
Read	Selftest Result				-	*RBI*	*FCO*	RS	PAU	Mode			INV	STB	RUN	OEN

RBI ⇨ Read-back Information Select (0 = default, 1 = factory use only)
FCO ⇨ Frequency Correction Off (0 = default, 1 = factory use only)
RS[1] ⇨ Run Selftest (1 = run selftest, cleared when selftest is completed)
PAU ⇨ Pause (0 = normal, 1 = pause sweeping)
Mode ⇨ Slew Mode
- 0 0 0 Fixed (follows Freq. A)
- 0 0 1 Single Ramp (from Freq. A to Freq. B and hold)
- 0 1 0 Single Cycle (from Freq. A to Freq. B then back to Freq. A and hold)
- 0 1 1 Continuous Cycle (cycle between Frequency A and B)
- 1 X X (reserved)

INV ⇨ Invert External Strobe (0 = active low, 1 = active high)
STB[2] ⇨ Strobe Enable (0 = ignore strobe, 1 = use strobe signal to control sweeping)
RUN ⇨ Run/Stop (1 = run, 0 = hold a current frequency[3])
OEN ⇨ Output Enable (0 = disabled, 1 = enabled)
Selftest Result ⇨ Selftest Result (0 = successful, 1 = failure, Bit 12=1KHz range, Bit 13=10KHz range, Bit 14=100KHz range, Bit 15=1MHz range, reset on register read)

Notes:
1) Output is temporarily disabled during selftest.
2) When STB is set to 1, in Single Ramp and Single Cycle modes, the strobe signal acts as a trigger. The ramp or cycle begins when the strobe signal goes active and will complete the ramp or cycle regardless of the level of the strobe signal. In Fixed or Continuous Cycle mode, the output frequency will follow or start cycling when the strobe signal goes active. When the strobe signal goes inactive, it will hold at the current frequency. However, if it becomes active again, the output will change to and start from Frequency A. In either case, the RUN bit must also be set for STB to control operation.
3) When RUN is set to 0, the output holds at the current frequency, but will change to and start from Frequency A when the RUN bit is set back to a 1.

Waveform Control Register

02

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	Duty Cycle					-	-	Range		-	-	WFS	
Read	-	-	-	Duty Cycle					-	-	Range		-	-	WFS	

Duty Cycle ⇨ Waveform Duty Cycle (00_{16} = 85%, $1F_{16}$ = 15%, resolution is ~2.3% per bit, default = $0F_{16}$ = ~50%)
Range ⇨ Frequency Range Select
- 0 0 0 - 1.023KHz
- 0 1 0 - 10.23KHz
- 1 0 0 - 102.3Khz
- 1 1 0 - 1.023MHz

WFS ⇨ Waveform Select
- 0 0 Square wave
- 0 1 Triangle wave
- 1 X Sine wave

Figure 4. I/O Registers

Output Amplitude Control Register

04

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Amplitude B								Amplitude A							
Read	Amplitude B								Amplitude A							

Amplitude A/B ⇨ Output Peak-to-Peak Amplitude for Frequency A or B (00_{16} = 0V, FF_{16} = +10V, ~0.04V per bit (default = 00_{16}))

Output Offset Control Register

06

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Offset B								Offset A							
Read	Offset B								Offset A							

Offset A/B ⇨ Output Offset Voltage for Frequency A or B (00_{16} = -5V, 80_{16} = 0V, FF_{16} = +5V, ~0.04V per bit (default = 80_{16}))

Figure 4. I/O Registers (continued)

Frequency A Control Register

08

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	RBM	(not used)					Frequency A									
Read	0	(not used)					Programmed Frequency A									
Read	1	(not used)					Current Frequency									

RBM ⇨ Read-Back Mode (0 = read programmed value, 1 = read current frequency)
Frequency A ⇨ Desired Frequency A. See 3.2.1 for details.

Note: The data read in the Frequency A bits depends on the read-back mode (RBM) selected.

Dwell/Slew Rate A Control Register

0A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	DR A		Dwell Time A						-	Slew Value A						
Read	DR A		Dwell Time A						-	Slew Value A						

DR A ⇨ Dwell Time Range
- 0 0 Milliseconds
- 0 1 Tens of milliseconds
- 1 0 Hundreds of milliseconds
- 1 1 Seconds

Dwell Time A ⇨ Amount of time (value × Dwell Time Range) the output stays (dwells) at Frequency A before sweeping to Frequency B. See 3.5.2 for details.
Slew Value A ⇨ Rate of change for ramping from Frequency A to Frequency B. See 3.5.2 for details.

Figure 4. I/O Registers (continued)

Frequency B Control Register

0C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	RBM	(not used)					Frequency B									
Read	0	(not used)					Programmed Frequency B									
Read	1	(not used)					(factory use only)									

RBM ⇨ Read-Back Mode (0 = read programmed value, 1 = factory use only)
Frequency B ⇨ Desired Frequency B. See 3.2.1 for details.

Note: The data read in the Frequency B bits depends on the read-back mode (RBM) selected.

Dwell/Slew Rate B Control Register

0E

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	DR B		Dwell Time B						-	Slew Value B						
Read	DR B		Dwell Time B						-	Slew Value B						

DR B ⇨ Dwell Time Range
- 0 0 Milliseconds
- 0 1 Tens of milliseconds
- 1 0 Hundreds of milliseconds
- 1 1 Seconds

Dwell Time B ⇨ Amount of time (value × Dwell Time Range) the output stays (dwells) at Frequency B before sweeping to Frequency A. See 3.5.2 for details.
Slew Value B ⇨ Rate of change for ramping from Frequency B to Frequency A. See 3.5.2 for details.

Figure 4. I/O Registers (continued)

APPENDIX A - CONNECTORS

I/O Pin	Signal	I/O Pin	Signal
1	GND	26	GND
2	CLK	27	+5V
3	RESET-	28	R/W-
4	D0	29	IDSEL-
5	D1	30	DMAREQ0-
6	D2	31	MEMSEL-
7	D3	32	DMAREQ1-
8	D4	33	INTSEL-
9	D5	34	DMACK0-
10	D6	35	IOSEL-
11	D7	36	reserved
12	D8	37	A1
13	D9	38	DMAEND-
14	D10	39	A2
15	D11	40	ERROR-
16	D12	41	A3
17	D13	42	INTREQ0-
18	D14	43	A4
19	D15	44	INTREQ1-
20	BS0-	45	A5
21	BS1-	46	STROBE-
22	-12V	47	A6
23	+12V	48	ACK-
24	+5V	49	reserved
25	GND	50	GND

Figure A-1. IP/Carrier Interface Connector Configuration

I/O Pin	Signal	I/O Pin	Signal
1	GND	26	GND
2		27	
3	GND	28	
4	OUT	29	GND
5	GND	30	
6		31	GND
7	GND	32	
8	TOUTH	33	
9	GND	34	
10	TOUTL	35	
11	GND	36	
12	EXTSTB-	37	GND
13	GND	38	
14	EXTDC	39	GND
15		40	
16		41	
17		42	
18		43	
19		44	
20		45	
21		46	
22	-12V	47	
23	+12V	48	
24	+5V	49	
25	GND	50	GND

Figure A-2. IP I/O Connector Configuration

N O T E S :

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