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RACAL INSTRUMENTS
7064M
MESSAGE BASED
PROTOTYPE MODULE

PUBLICATION NO. 980820 Rev. A

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Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.



This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until, performance is checked by qualified personnel.

EC Declaration of Conformity

We

Astronics Test Systems
4 Goodyear
Irvine, CA 92618

declare under sole responsibility that the

7064M 1S Msg Based Prototype Module, P/N 407620-100
7064M 2S Msg Based Prototype Module, P/N 407620-200
7064M 3S Msg Based Prototype Module, P/N 407620-300
7064M 1S Msg Based Prototype No Intf., P/N 407620-101
7064M 2S Msg Based Prototype No Intf., P/N 407620-201
7064M 3S Msg Based Prototype No Intf., P/N 407620-301
OPT05 Msg Based Interface Module P/N 407620-OPT05

conform to the following Product Specifications:

Safety: EN 61010-1:1993+A2:1995

EMC: EN 61326:1997+A1:1998,CLASS A

Supplementary Information:

The above specifications are met when the product is installed in an Astronics Test Systems certified mainframe with faceplates installed over all unused slots, as applicable.

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.

Irvine, CA, March 5, 2002 Karen L. Evensen

Karen Evensen
Director of Engineering

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Chapter 1

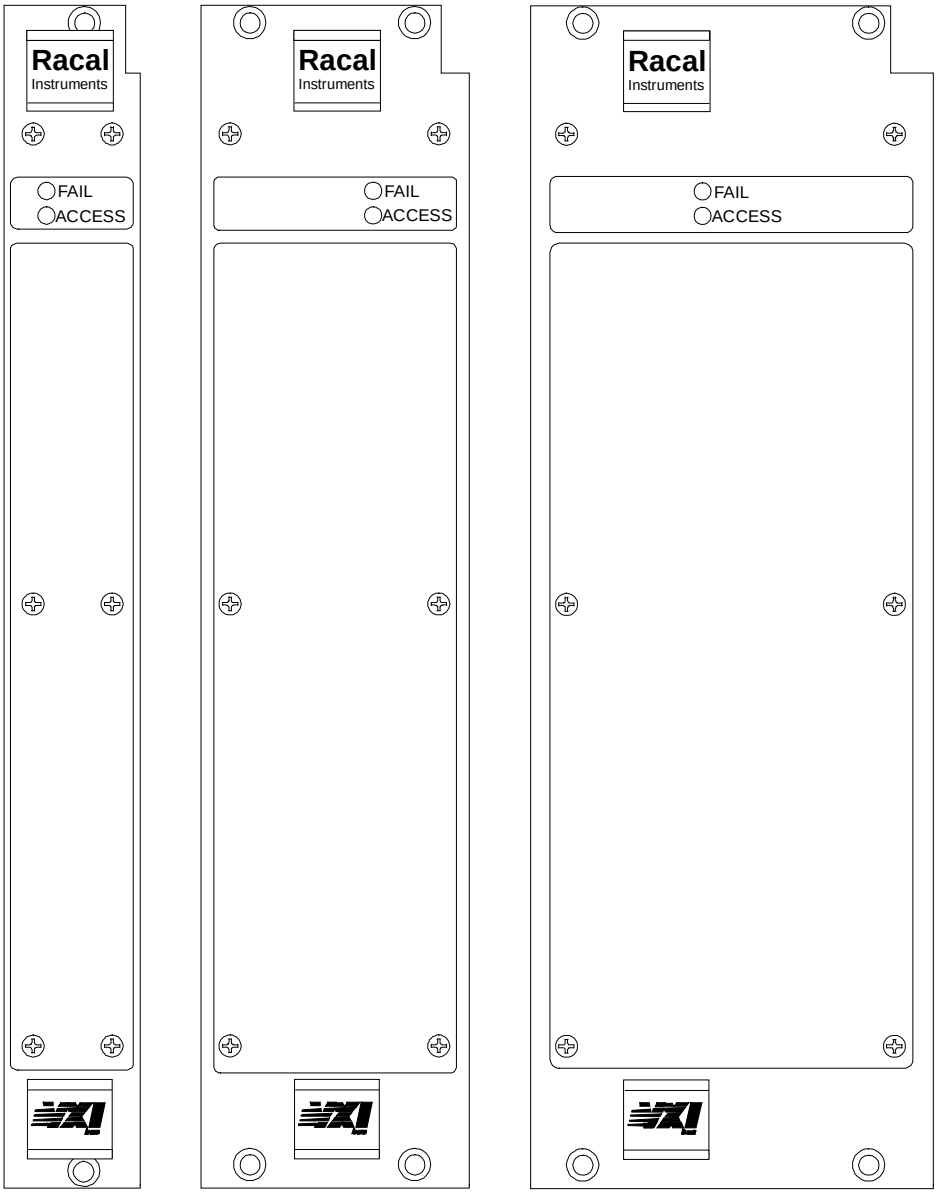
GENERAL DESCRIPTION

What's In This Chapter

- Introduction
- General Description of the 7064M
- 7064M Specifications
- 7064M Options Table

Introduction

This manual contains information on how to install and operate the 7064M in a VXIbus environment. It describes the functions and applications of the 7064M Message Based Prototype.



7064M-10X **7064M-20X** **7064M-30X**

Figure 1-1, 7064M Message Based Front Panel

General Description

The 7064M-100, -200, and -300 are “master” message-based VXIbus development cards made up of a removable message-based interface and a breadboard card for prototyping and developing of digital and analog circuits. The 7064M-101, -201, and -301 “slave” VXIbus development cards consist of the breadboard card only (omitting the removable message-based interface card).

Eighty-two square inches of breadboard real estate are available to

the user, along with all the appropriate VXIbus backplane signals. The user circuitry in the breadboard area is controlled through twelve 8-bit individually configurable ports located on the breadboard card. The user circuitry can also be controlled through the message-based module's 68000 micro controller directly if Option 95, Source Code is purchased (P/N 407620-Opt95) The upper half of the 68000 address space is available for this purpose.

The development area consists of five separate areas to provide maximum flexibility and utilization. Refer to **Figure 1-2** and the description on the following page:

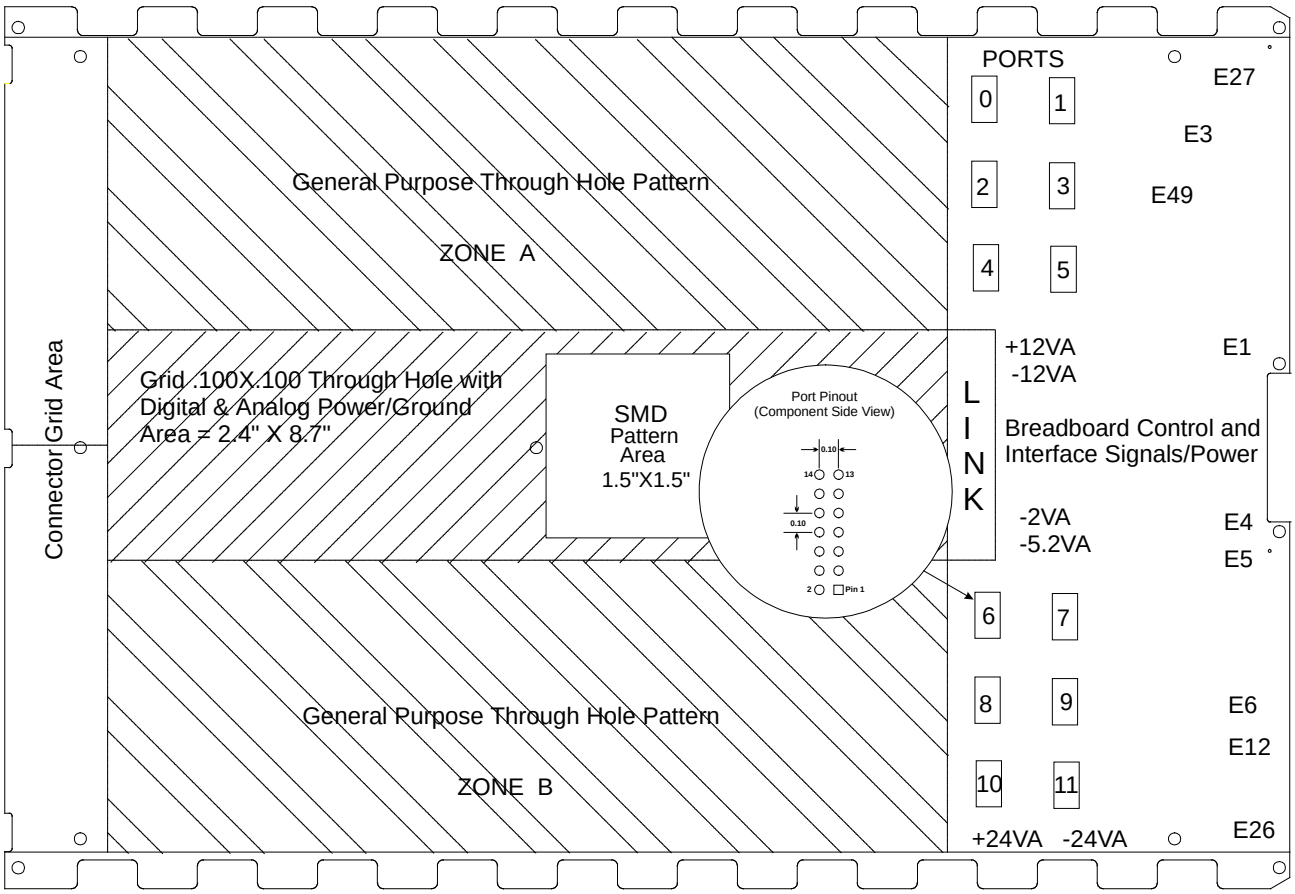


Figure 1-2, 7064M Message-Based Breadboard

- **Universal grid area** - Universal array with 0.1 inch center hole pattern allows placement of large grid arrays.
- **General-purpose through-hole pattern area** - Rows of holes based on 0.1 grid allow placement of the standard DIP packages and de-coupling capacitors. There are two uncommitted power distribution planes in each zone (A and B) available to the user. These uncommitted planes (referred to as “Top” and “Bottom”) may be connected to various power supplies provided by the VXI backplane. Connections to the +5V Power, Ground, and “Top” and “Bottom” planes are placed along the DIP rows for convenient connection.
- **SMD pattern area** - Multipurpose pattern can accommodate the following combination of Plastic Leaded Chip Carrier (PLCC) and Small Outline (SO) Surface Mount Devices:

  a) PLCC-68 (1 each)

  b) PLCC-44 (1 each)

  c) PLCC-32 (1 each) + PLCC-20 (1 each) + SO-20L (2 each)

  d) PLCC-28 (1 each) + PLCC-20 (1 each) + SO-20L (2 each)
- **Connector grid area** - A universal array with 0.1 inch center hole pattern is provided for the easy placement of interface connectors, and has enough mounting holes to accommodate high-density connectors.

All seven VXIbus supply lines are available to the user and are fused, reducing the risk of damage to the backplane. The 7064M module also provides the EMI power filtering required by the VXIbus specifications, removing the need for the user to design this circuitry.

The 7064M is available in single, double, or triple slot versions (-10X, -20X, -30X).

7064M
Specifications

Table 1-1, VXI Interface

Characteristics	Description
VXI Interface Capabilities	VXIbus Specification Rev 1.4 compliant Message-Based Device A16, A16/24 Servant only Static or Dynamic Configuration Instrument Protocol (I) IEEE-488.2 Instrument Protocol (I4) Programmable Interrupter Event Generator Response Generator Trigger input interrupts CPU Trigger output under CPU control
VXI *Plug&Play* Support	Fully Compliant
Software Protocols supported by VXI Interface	IEEE 488.2 common commands (for I4 instrument)
Device Dependent Registers/ Shared Memory	Shared RAM configured as A24 Shared Memory
Annunciators (Front Panel) FAIL ACCESS	 Failed LED, Refer to VXIbus Spec 1.4 for definition. Indicates VXI A16/A24 access.
CPU	16 MHz 68000
Memory RAM ROM Non-vol RAM Shared RAM	 32K X 16 64K X 16 8K X 16 32K X 16 (see Device Dependent Registers/ Shared Memory above)
Interface Connection CPU Port Shared Memory Port	 Full access to CPU address (A23-A1), data (D15-D0) and control lines at P100. Full access to VXI ASIC Shared Memory address (SA23-SA1), data (SD15-SD0), and control lines at P103 connector.

Table 1-2, 7064M Module Power

Characteristic	Description	
DC Current (I_{PM})	**Voltage**	**I_{PM} (Steady-State Current)**
	+5V	1.25A
Dynamic Current (I_{dM})	**Voltage**	**I_{dM} (mAmps $_{pp}$)**
	+5V	10.0

Table 1-3, Breadboard Area Specification

Characteristics	Description
Maximum User Current +5V -5.2V -2V +12V -12V +24V -24V	Specification 5 Amps Max 5 Amps Max 2 Amps Max 1 Amp Max 1 Amp Max 1 Amp Max 1 Amp Max
User Breadboard Area	82 square inches
I/O Port Configuration	12 X 8-bit
I/O Port Drive Current (TTL Logic Levels) Sink Source	 64 mAmp @ 0.55V max 15 mAmp @ 2.4V min
I/O Port Reset Polarity	Logic 1 or logic 0, jumper selectable (JP1)
I/O Port Operating Modes Clocked Input Buffered Input Latched Output w/Read back	 User supplied clock stores data in port. Port data sampled during VXIbus read. Data written during VXIbus write is latched (until subsequent write).
I/O Port Control Signals (x=port number 0 - 11) O/Ix LAT/BUFFx CLKINx	 Input/Output selection: O/Ix = 0 selects output, O/Ix =1 selects input Clocked/Buffered selection: LAT/BUFFx=0 selects buffered input, LAT/BUFFx=1 selects clocked input Clock input strobes input data on the rising edge Note: all control lines are TTL logic level signals

Table 1-4, Cooling Requirements

Parameter	Specification
Maximum Module Power	6.25 Watts (Does not include user circuits in prototyping area)
Minimum Airflow	0.5 Liters/sec at .04mm H_2O for a 10°C Rise (See "Module Cooling Considerations" in Section 3)
Minimum Airflow, Typical 20-Watt Application	2.1 Liters/sec at .20mm H_2O for a 10°C Rise

Table 1-5, 7064M Mechanical Parameters

Parameter	Specification		
Enclosure Style	VXI "C" SIZE - Prototype Enclosure		
Enclosure Dimensions (in.)	7064M-10X: 14Lx 10.3W x l.2D 7064M-20X: 14Lx 10.3W x 2.4D 7064M-30X: 14Lx 10.3W x 3.6D		
Enclosure weight	7064M-100: 2.2 Lbs. 7064M-200: 2.5 Lbs. 7064M-300: 2.8 Lbs. Note: Subtract 0.65lbs if no Message-Based interface installed (models -101, -201, -301)		
Prototype Area Maximum Clearance For Components	**Module**	**Circuit Side**	**Component Side**
	7064M-10X	0.13 in.	0.75 in.
	7064M-20X	1.30 in.	0.75 in.
	7064M-30X	1.30 in.	1.95 in.

Table 1-6, 7064M Environmental Specifications

Parameter	Specification
Temperature, operating	0°C to +55°C
Temperature, non-operating	-40°C to +71°C
Relative Humidity	95 +/-5% RH non-condensing; 75+/-5 %RH above 30°C; 45+/-5 %RH above 40°C
Altitude, operating	10,000 ft
Altitude, non-operating	15,000 ft
Vibration	0.013" double amplitude, 5-55Hz
Fungus resistance	Yes, fungus inert materials used.

Table 1-7, Reliability and Safety Specifications

Parameter	Specification
MTBF	>200,000 Hours, calculated per MIL-HBK217, ground-benign, 30°C
MTTR	< 30 minutes

Table 1-8, EMC Specifications

Council Directive 89/336/EEC
EN55011, Group, Class A
EN50082-1, IEC801-2,3,4

DEFINITIONS

EMC	Electro-Magnetic Compatibility
MTBF	Mean Time Between Failure
MTTR	Mean Time To Repair
RH	Relative Humidity
PLCC-XX	Plastic Leaded Chip Carrier Package, XX=Pin Count
SO-20L	Small Outline Package, 20-pin low profile

Table1-9, Option Table

Model/Option	Part No.	Description
7064M-100	407620-100	Single slot master message based prototype module.
7064M-101	407620-101	Single slot slave message based prototype module without interface installed.
7064M-200	407620-200	Double slot master message based prototype module.
7064M-201	407620-201	Double slot slave message based prototype module without interface installed.
7064M-300	407620-300	Triple slot slave master message based prototype module.
7064M-301	407620-301	Triple slot slave message based prototype module without interface installed.
7064M-Opt 05	407620-Opt 05	Message based interface card only.
7064M-001	407620-001	Single slot sheet metal enclosure only.
7064M-002	407620-002	Double slot sheet metal enclosure only.
7064M-003	407620-003	Triple slot sheet metal enclosure only.
7064M-Opt 95	407620-Opt 95	Source code for message based interface. Includes manual and source code disks (See Appendix A for Details).

Chapter 2

INSTALLATION INSTRUCTIONS

What's In This Chapter

- Unpacking and Inspection
- VXIbus Logical Address Switch
- VXIbus Interrupt Handler Setting
- Installation into Mainframe
- Self Test Description
- Local Bus Usage
- VXIbus *Plug&Play* Software Installation

Unpacking and Inspection

1. Remove the 7064M module and inspect it for damage. If any damage is apparent, inform the carrier immediately. Retain shipping carton and packing material for the carrier's inspection.

2. Verify that the pieces in the package you received contain the correct 7064M module option and the 7064M Users Manual. Notify Customer Support if the module appears damaged in any way. Do not attempt to install a damaged module into a VXI chassis.

3. The7064M module is shipped in an anti-static bag to prevent electrostatic damage to the module. Do not remove the module from the anti-static bag unless it is in a static-controlled area.

CAUTION:

ALWAYS PERFORM DISASSEMBLY, REPAIR AND CLEANING AT A STATIC SAFE WORKSTATION.

VXIbus Logical Address Switch

The 7064M Message Based Prototype Module has an internal 8-position address DIP switch used to determine the base address of the VXIbus configuration registers. It is located on the top of the module, accessible through the case. Any setting other than 255 indicates static configuration. Refer to VXIbus Specification Revision 1.4 for details.

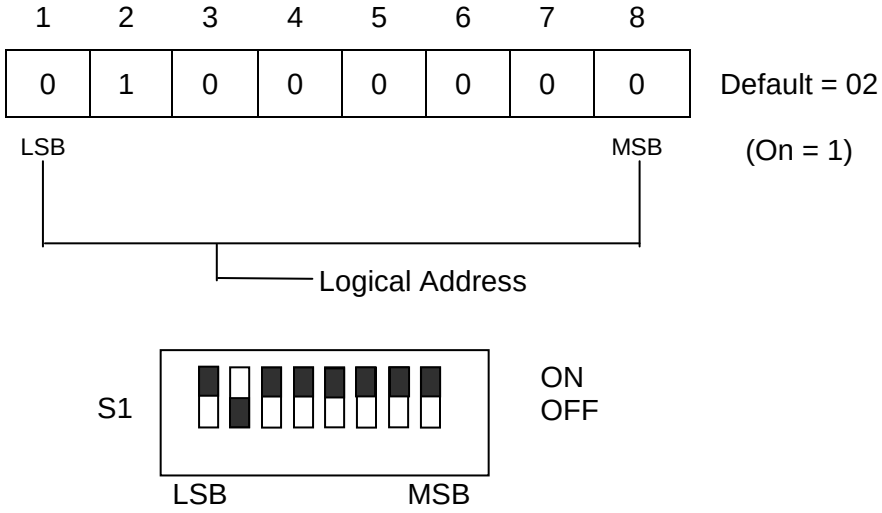


Figure 2-1, VXIbus Logical Address Switch

Dynamic configuration is an optional alternative method of assigning logical addresses to VXIbus devices, and is defined in detail in Section F of the VXIbus System Specification Revision 1.4. In the ON position, the switch is set to logical 1, and in the OFF position to a logical 0. The user can select any logical address from 1 to 254 for static configuration.

NOTE:

Logical address 0 is not allowed. Set logical address to 255 for dynamic configuration.

NOTE:

The 7064M Message Based Breadboard Module is shipped with the logical address set for 2. Refer to the Resource Manager's manual for details about addressing methods.

VXIbus Interrupt Handler Setting

One programmable interrupt line is provided on the 7064M module. This line is assigned by using the *assign interrupter line* word serial protocol command (See Page 182 of Section E, Revision 1.4 of the VXIbus Specifications). The *Int_ID* is set to 1.

7064M to VXIbus Mainframe Installation

The 7064M module is ready for operation when shipped. The address switch is set to 2.

To install the 7064M in a C-size VXI chassis, use the following instructions:

1. Ensure power is OFF.
2. Configure the interrupt daisy chain on the backplane to bypass empty slots, per VXIbus specifications.
3. Remove the front cover of the VXI chassis, and slide the 7064M into the appropriate slot with the LED's towards the top (or to the left when using a horizontal chassis).

To ensure reliable VXIbus communications when using 7064M “slave” modules without a VXIbus communications interface (i.e., 7064M-101, 7064M-201, and 7064M-301 series), the user must note the following. The VME Specification requires that the Interrupt Acknowledge (IACK) and BUSGRANT (BG) signal lines be daisy-chained from slot-to-slot across the backplane. This means that for each slot the BUSGRANT and IACK signals are input on Row A of the P1 connector and output on Row C of the P1 connector. When there is no VXIbus interface installed in the 7064M module, the user must ensure that these signals are passed onto the next slot. There are three ways this can be done, depending on the backplane installed in your VXIbus chassis. You will need to consult the chassis manual to verify the type of backplane you have.

1. **VXIbus Backplanes with Bus Grant and Interrupt Acknowledge DIP Switches.** - The user must close the switches in the slot where the 7064M will be installed. (Example: 1264A, 1261).

2. **VXIbus Backplanes with Active Automatic Daisy-Chain.** - The Bus Grant and Interrupt Acknowledge signals will be automatically passed to the next slot. (Example: 1261B, 1269 chassis).

3. **VXIbus Backplanes with Auto-Configuration P1 Connectors.** - With this style of connector, the BUSGRANT and IACK daisy-chains are broken as soon as the module is installed in a slot. The user must reconnect the daisy-chain in the 7064M module. This is done by shorting the pins on the P3 or J101 connector as shown in **Table 2-1** below (Example: 1261AH, 1261A+, 1261AM chassis).

Table 2-1, Signal Shorts For Chassis With Auto-Configuration P1 Connectors

SIGNAL	P3 or P101 SHORT
BG0IN* and BG0OUT*	Pin 4 Row B to Pin 5 Row B
BG1IN* and BG1OUT*	Pin 6 Row B to Pin 7 Row B
BG2IN* and BG2OUT*	Pin 8 Row B to Pin 9 Row B
BG3IN* and BG3OUT*	Pin 10 Row B to Pin 11 Row B
IACKIN* and IACKOUT*	Pin 21 Row A to Pin 22 Row A

Power-Up Self-Test Initialization

Before turning on the VXIbus mainframe, make sure a Slot 0 with a Resource Manager is present. Upon power-up of the system, the 7064M goes through the following power-up sequence:

- The 7064M breadboard module has two LED's on the front panel - FAIL and ACCESS. The LED functions are:

  FAIL On during a self-test

  Off when the self-test has successfully completed

  ACCESS Blinks on when the VXIbus is accessing the module's logical address

At power-up, the 7064M goes through a series of operations to ensure proper initialization and establish the proper start-up state. A brief description of this power-up sequence follows.

Self-Test

Tests are performed on ROM, RAM, Non-Vol and the timer to ensure they are operating correctly.

Board ID Check

Each breadboard may have one or more board ID bytes selected by the user. The user selects a port, a value and a mask if necessary. This information is stored into Non-vol by the user and verified during the power-up sequence.

Port Initialization

All I/O ports configured as outputs are initialized to either all 0's or all 1's during system reset (jumper selectable on each breadboard). The user can also specify initial values for ports and have them stored in Non-vol. If any of these values have been specified, they are set at this point in the power-up sequence. The operation of the board ID is described in more detail in Section 3.

VXIbus Interface Initialization

At times, it may be desirable for the user to specify an initial value for one or more of the VXIbus registers. For example, the user specifies a model code. This requires the new model code to be placed in the "device-type" VXIbus register. The user can specify these values and have them stored in Non-Vol. If any of these values have been specified, they are set up at this point in the power-up sequence.

Local Bus Usage with 7064M Breadboard

The VXIbus has a provision for interconnecting adjacent cards through a local bus. The bus consists of 12 lines which jumper cards together. A card on the left of another will have connections on the “C” side of P2 tied to the “A” side of P2 for the card to its right.

Slave Module with 7064M Master Module

NOTE:

Master module has an option 5 control card mounted. Slave module does NOT have an option 5 control card mounted and must be installed in the chassis to the right side of the Master module.

The Master and Slave module should always have the following pads jumpered with 22 gage jumper wire:

	J3	J4
LB0		
LB1		
LB2		
LB3		
LB4		
LB5		
LB6		
LB7		
LB8		
LB9		

The Slave module must be the next card on the right of the Master module. When a Slave module is used with a Master module the following jumpers must be installed on the Master module. Use 22 gage jumper wire.

	J5	J6
LB0		
LB1		
LB2		
LB3		
LB4		
LB5		
LB6		
LB7		
LB8		
LB9		

The same jumpers should be installed on the Slave module if multiple Slave modules are installed with the exception of the last Slave module.

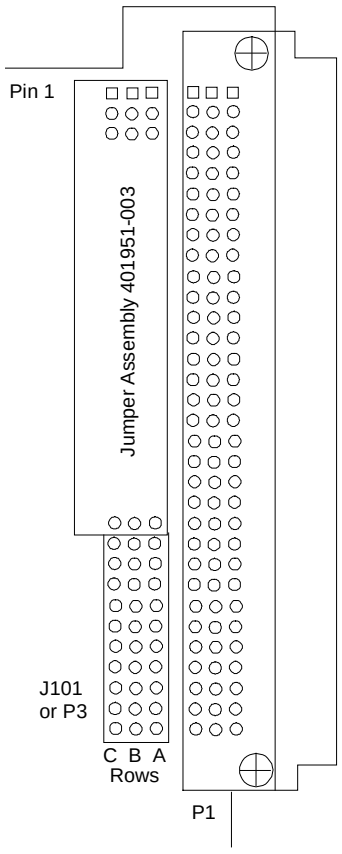
Bus Grant and Local Bus Jumpers

The Slave module must always have the Bus Grant and Local Bus jumper boards plugged into J3 and J4.

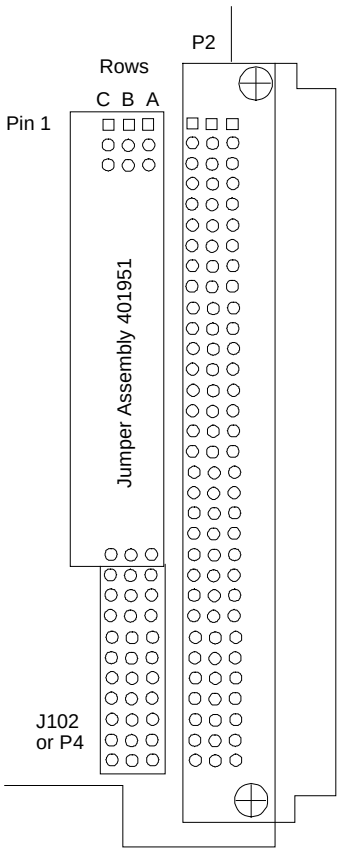
Bus Grant (Part Number 401951-003) has been designed to perform this task and may be ordered from the Astronics Test Systems Sales Department. The jumper should be located in P3 or J101, pins 1 through 22 as shown in **Figure 2-1**. For Slave module operation 401951-003 must be plugged into the P3 connector.

Local Bus Jumper (401951) should be plugged into J102 or P4 connector.

Figure 2-2, Installation of Bus Grant Jumper and Local Bus Jumper



Bus Grant Jumper



Local Bus Jumper

Installing the VXI*plug&play* Software

After the 7064M been installed into the VXI mainframe, the VXI*plug&play* software may be used to communicate with the 7064M. To install the software, first power on the mainframe, then perform the following operations:

1. Start Windows (3.1, 95, or NT) on your computer if it is not already running.

2. Insert the appropriate (Windows 3.1 or 95/NT) VXI*plug&play* installation disk #1 into the 3-1/2" floppy disk drive.

3. Run the SETUP program on the installation disk.

4. Follow the instructions presented by the SETUP program.

   After the SETUP program has completed, the executable Soft Front Panel program may be run. To run the soft Front Panel, ensure that the following conditions are met:

1. The computer is connected to the VXI mainframe via a MXI/VXI interface, a GPIB/VXI interface, or the computer is an embedded VXI computer.

2. VISA is loaded onto your system. VISA is a library of functions which provide communication between a computer and instruments (GPIB and VXI). VISA may be obtained from the manufacturer of the MXI/VXI, GPIB/VXI, or embedded computer.

3. The VXI mainframe has power applied and the power switch has been turned ON.

4. For the MXI/VXI and embedded computers, the resource manager program has been run since the VXI mainframe power was last turned ON.

   To run the Soft Front Panel, "double-click" on the 7064M Front Panel" icon in the "VXIPNP" Windows Group.

If the four conditions above are met, the Soft Front Panel program will automatically locate the 7064M in the Mainframe. The Soft Front Panel program will display the VXI logical address of the 7064M and the "Active" LED on the Soft Front Panel will be green.

Chapter 3
USING THE BREADBOARD

What's In This Chapter

This chapter provides information as follows:

- Module cooling considerations and operating point calculations.
- Connection points for signals and power used to interface to the user development area.
- Card address switch settings.
- Software commands to allow user control of circuits in the user development area.

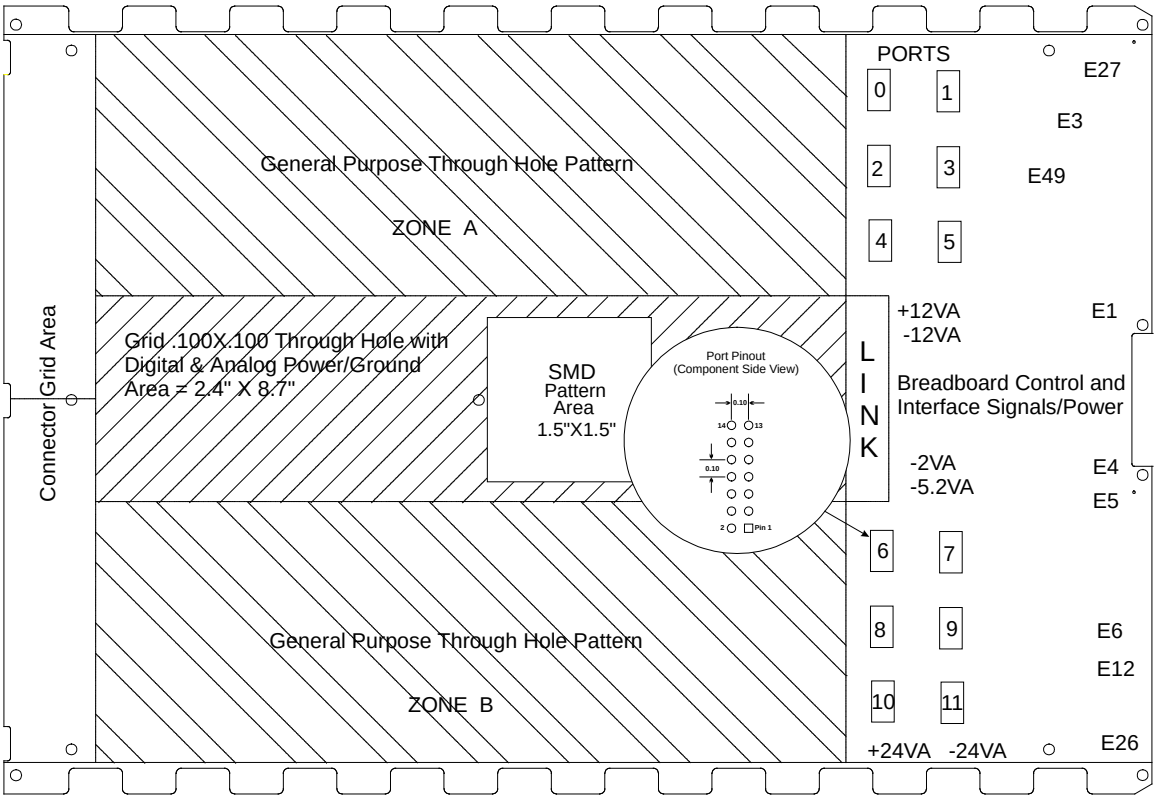


Figure 3-1, 7064M Message-Based Breadboard

Module Cooling Considerations

VXI modules are specified to require a particular airflow to maintain a specific temperature rise, which is typically 10° Celsius. The airflow and back-pressure (pressure change across the module) values determine a single operating point that may be plotted on a VXI mainframe cooling curve. If the operating point lies under the mainframe cooling curve, there is a high probability that the module will remain within its specified temperature rise. If the operating point is above the mainframe cooling curve, the temperature rise of the module may exceed the specified value.

Calculated Module Operating Point

A calculation of the operating point or cooling requirements for the 7064M (and user circuitry) can be determined if the total power dissipation is known. This is detailed below.

CAUTION:

A module with hot spots or airflow restrictions may require increased airflow. Refer to the VXIbus Specification Revision 1.4 for details.

To calculate the module operating point:

1. Determine the desired maximum temperature rise allowed across the module. It is typically 10°C, but may be higher or lower depending on the specified operating environment, function of the module, part sensitivities, etc.
2. Determine the maximum power in watts dissipated inside the module ($P_{6.25\ WATTS} + P_{USER\ CIRCUITRY}$).
3. Determine the airflow required by the module to maintain the desired temperature rise. In most cases, this is calculated from the power dissipated, desired temperature rise, and the specific heat of air. (For a 10°C rise, airflow in L/S=0.08 * power in watts.) The required airflow may be increased or decreased depending on hot spots, airflow blockages, etc.
4. Determine the pressure drop across the module when the specified airflow (in L/S) is forced through the module. A reasonable estimate may be calculated from the equation for a typically dense VXI module: $P=0.02G^2 + 0.05G$. (P is pressure in mmH_2O and G is airflow in liters per second.)
5. Plot the module operating point (P, L/S) on the mainframe curve. If the module operating point lies under the mainframe cooling curve, the module should remain within its specified temperature rise.

DC Voltages Available to Prototyping Area

The 7064M Message Based Prototype module provides filtered and fused VXI supply voltages on the board. The user can access these voltages for his prototyping circuitry. The VXI voltages available are listed below in **Table 3-1**.

Table 3-1, DC Voltages Available to Prototyping Area

Voltage	Max Current	Fuse	User Access Point
+5V	5Amps Max	10A	+5VA
+12V	1Amp Max	2A	+12VA
+24V	1Amp Max	2A	+24VA
-5.2V	5Amps Max	10A	-5.2VA
-2V	2Amps Max	5A	-2VA
-12V	1Amp Max	2A	-12VA
-24V	1Amp Max	2A	-24VA

Note: All fuses are Littlefuse 255 Series or equivalent.

+5V and Ground are distributed throughout the prototyping area. Refer to **Figure 3-1** for connection points for other VXI voltages. There are 77 +5V/Ground power pads throughout the prototype area. A connection to the VXI Chassis is provided the center standoff located in the development area. Connect the feed-through at the center standoff to the adjacent “GND” feed-through to make the “Chassis” to “Logic” ground connection.

Local Bus Interface

Direct access to the VXI Local Bus is provided on the 7064M Message Based Prototype Module. The VXI Local Bus allows communication between modules in adjacent slots of a VXI chassis. Local Bus “A” is connected to the module on the left, while Local Bus “C” is connected to the module to the right. The user should exercise caution when using the Local Bus to ensure module to module compatibility. Refer to VXI Rev. 1.4 Section B6.2.6 and B7.3.7 for further explanation of the VXI Local Bus. Connections are provided as follows on the 7064M:

Table 3-2, VXI Signals

7064M Signal	VXI Local bus Signal
J5 pin LB0	Local Bus C0
J5 pin LB1	Local Bus C1
J5 pin LB2	Local Bus C2
J5 pin LB3	Local Bus C3
J5 pin LB4	Local Bus C4
J5 pin LB5	Local Bus C5
J5 pin LB6	Local Bus C6
J5 pin LB7	Local Bus C7
J5 pin LB8	Local Bus C8
J5 pin LB9	Local Bus C9
J5 pin LB10	Local Bus C10
J5 pin LB11	Local Bus C11

J101 pin 5	Local Bus A0
J101 pin 6	Local Bus A1
J101 pin 8	Local Bus A2
J101 pin 9	Local Bus A3
J101 pin 11	Local Bus A4
J101 pin 12	Local Bus A5
J101 pin 14	Local Bus A6
J101 pin 15	Local Bus A7
J101 pin 17	Local Bus A8
J101 pin 18	Local Bus A9
J101 pin 20	Local Bus A10
J101 pin 21	Local Bus A11

TTL Trigger Lines

The 7064M Message Based Prototype Module provides direct access to the VXI TTL Trigger lines. These lines are typically used for intermodule communication applications such as trigger, handshake, clock, or logic state transmission. They are open collector active low signals and are pulled high (inactive) by the VXI backplane. Several standard communication protocols are defined by VXI Rev. 1.4. Refer to section B6.2.3 of the VXI Rev. 1.4 specification for further details. The TTL Trigger connections are defined below.

Table 3-3, VXI TTL Trigger Lines

E-Point	Signal Name
E6	TTLTRG0-
E7	TTLTRG1-
E8	TTLTRG2-
E9	TTLTRG3-
E10	TTLTRG4-
E11	TTLTRG5-
E12	TTLTRG6-
E13	TTLTRG7-

Miscellaneous VXI Signals

The 7064M provides direct access to various VXI defined signals. Details of each of these signals can be found in the VXI Rev. 1.4 specifications. Connections to these signals are as follows.

Table 3-4, Miscellaneous Signals

Signal Name	E-Point
ACFAIL-	E27
SERCLK	E4
SERDAT-	E5
CLK10+	E4
CLK10-	E5
SUMBUS	E26
BERR-	E41
+5VSTDBY	E1
SYSRESET-	E3
SYSCLK(buffered)	E49

I/O Port Write Strobes

The 7064M provides direct access to the I/O port “write” strobes. These signals are used by the message-based interface to clock data into ports when configured as outputs. The signals are driven by HCT00 nand gates.

Table 3-5, I/O Port Write Strobes

Port #	E-Point
0	14
1	15
2	16
3	17
4	18
5	19
6	20
7	21
8	22
9	23
10	24
11	25

Input/Output Ports

The 7064M breadboard has twelve 8-bit ports (refer to **Figure 3-1**). Each Port can be individually configured for input or output. Three lines are supplied for the user to control the type of port and its operation. The port outputs are designed to accept a 14-pin dual row (0.10 inch spacing) connector for the user to easily wire into the breadboard area.

Table 3-6, I/O Port Description for Port 0 to Port 11

Signal X = 0 to 11	Port x Pin X = 0 to 11	Type	Description
O/Ix!	1	Control	Along with LAT/BUFFx! controls the operational mode of the port.
+5VA	2,6	Power	Fused +5V Power
CLKINx	3	Control	Used to clock data into the port when the port is configured as a clocked input. A rising edge on this line clocks data into the port. Once clocked in, the data can be read over the VXIbus. If the port is configured as a buffered input, this line has no effect on the port operation.
GND	4	Power	Logic Ground

Signal X = 0 to 11	Port x Pin X = 0 to 11	Type	Description
LAT/BUFFx!	5	Control	Used to configure an input port as either a clocked input or a buffered input. When the LAT/BUFFx! line is held low, the input port functions as a buffered input. When the LAT/BUFFx! line is held high, the input port functions as a clocked input.
I/Ox(0..7)	(7 to 14)	IN/OUT	The I/Ox (0..7) Signals comprise an 8-bit data/control port used to interface to the breadboard area. Note that "x" refers to ports 0 to 11. The twelve I/O ports can be configured in three ways: Clocked Inputs – The user supplies a clock signal that stores data in the port. Buffered Input – Data on the input lines are read when the port is read from the VXIbus. Latched Output with Readback – Data written to an output port through the VXIbus is held on the I/O lines until a subsequent write changes the data.

Controlling the I/O Ports

Control of user-defined circuitry in the breadboard area is accomplished through the use of the 96 buffered I/O lines available on the breadboard card.

A set of local commands is available to the user to allow for the control of the user-defined circuitry through the twelve I/O ports available.

When a command is sent to the 7064M using word serial protocol, it is received and parsed by the command parser. If the command matches a command from the local command set (See Page 3-11), the appropriate routine is called. If no matching command is found, bit 3 in the standard Event Status Register is set to indicate an error.

Output Port Reset Polarity

All outputs are set to a known level during reset. The user can select whether all the outputs will be set to a logic 1, or all outputs will be set to a logic 0 by simply doing the following:

- To cause all outputs to be set to a logic 1 during reset, connect pin 1 to pin 2 on JP1 of the breadboard card (See Drawing No. 405124 for the location of JP1).
- To cause all outputs to be set to a logic 0 during reset, connect pin 2 to pin 3 on JP1.

NOTE:

The 7064M breadboard module is shipped with connections on JP1 set to clear all ports to a logic 0 during reset. JP1 has no effect on ports configured *for input.*

I/O Port Configuration

The 7064M I/O ports can be configured in three ways:

- Clocked Inputs - The user supplies a clock signal that stores data in the port. At a later time, the port can be read from the VXIbus.
- Buffered Inputs - Data on the input lines is read when the port is read from the VXIbus. No clock signal is required.
- Latched Output with Readback - Data written to an output port through the VXIbus is held on the data lines until another write changes the data.

I/O Port Control

There are two lines that control the configuration of an I/O - O/Ix! and LAT/BUFFx!, where x is the associated port number (0 to 11):

- The O/Ix! line: Used to configure the port as an input or an output. When the O/Ix! line is held low, the port functions as an input. When the O/Ix! line is held high, the port functions as an output.
- LAT/BUFFx! line: Used to configure an input port as either a clocked input or a buffered input. When the LAT/Buffx! line is held low, the input port functions as a buffered input. When the LAT/Buffx! line is held high, the input port functions as an clocked input. If the port is configured as an output, this line should be held low (configured as a buffer). The data latched on the output can then be read back with a read from the VXIbus. This allows bit operations which modify a single bit, leaving the other bits in a port unchanged.

Table 3-7, I/O Port Control

O/Ix!	LAT/BUFFx!	OPERATION
0	0	Buffered Input
0	1	Clocked Input
1	0	LatchedOutput With Read Back
1	1	Not Recommended

NOTE:

These two control lines do not have to be static. They can be connected to data pins on an output port, or they can be connected to some user control lines. This allows ports to be used for bi-directional communication, or other more complex functions.

There is one line that is used as a clock line, where x is the associated port number (0 to 11):

- CLKINx line: Used to clock data into the port when the port is configured as a clocked input. A rising edge on this line clocks data into the port. Once clocked in, the data can be read over the VXIbus. If the port is configured as a buffered input, this line has no affect on the port operation.

NOTE:

The 7064M breadboard is shipped with the I/O ports configured for Latched Output with Readback as the default mode.

Module Address Switch

The card addresses can be offset from the default (zero) by setting the card address switch found on the left side (viewed from the front) of the module. This four pin DIP switch modifies the card address to be used with the local command set. Refer to **Table 3-8** for a description of the switch.

Table 3-8, Card Address Switch

SWITCH				Card Address	Port Address	
1	2	3	4			
0	0	0	0	0	0	2047
0	0	0	1	1	2048	4095
0	0	1	0	2	4096	6140
0	0	1	1	3	6141	8191
0	1	0	0	4	8192	10239
0	1	0	1	5	10240	12287
0	1	1	0	6	12288	14335
0	1	1	1	7	14336	16383
1	0	0	0	8	16384	18431
1	0	0	1	9	18432	20479
1	0	1	0	10	20480	22527
1	0	1	1	11	22528	24575
1	1	0	0	12	24576	26623
1	1	0	1	13	26624	28671
1	1	1	0	14	28672	30719
1	1	1	1	15	30720	32767

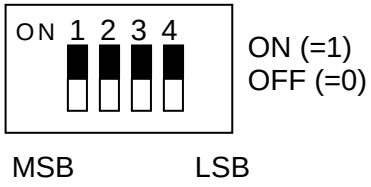


Figure 3-2, Card Address Switch

Port Addressing Schemes

There are two types of addressing used in port commands:

- port addressing
- card-relative port addressing

The port I/O commands in the local command set that do not begin with a ‘c’ use port addressing. Port addresses range from 0 to 32767 (Refer to **Table 3-8**). Ports are divided among 16 cards. Each card potentially has 2048 ports. This means a card with its address set to 0 has ports 0 to 2047. With its address set to 1, it has ports 2048 to 4095, etc. The lower twelve port addresses on each card are reserved for the twelve I/O ports used to control the breadboard area. The user may use the remaining addresses.

Another group of commands is available to perform the same functions, with an offset for each group of ports on a card. These port-relative I/O commands are the commands that start with a ‘c’. This may be more convenient for a system with a large number of breadboard modules. These commands use a ‘card’ (0 to 15) and a ‘cport’ (0 to 2047) to locate the actual address.

When using one breadboard only, the card address can be set to 0, and the first set of commands can be used. This has the advantage of shorter commands. Again, the lower twelve port addresses are reserved for the twelve I/O ports used to control the breadboard area.

Example:

The command "setbit(4096,0);" and "csetbit(2,0,0);" both set port 0, bit 0 on card number 2 to 1.

Base Numbers

Numbers used to reference cards, ports, values, etc. can be represented in any of the standard bases. The default base is decimal. Hex numbers are represented by a leading ‘#H’ in the number. For example, 255 is represented by #HFF. Upper case and lower case are the same and can be mixed freely. Binary numbers are represented by a leading ‘#B’. For example, 255 in binary is #B11111111. Octal numbers are represented by a leading ‘#Q’. For example, 255 in octal is #Q377. All base indicators can be either upper or lower case. C-style hex and octal numbers are also accepted.

Commands that return values can have the values returned in binary, octal, decimal or hex. The format of the returned value is determined by the *base* command (affects returned values only).

Local Command Set

Command Syntactic Style

The syntactic style of the 7064M command set is similar to the C-language function calls. All built-in and user-supplied commands are invoked by name, as if calling C functions. The commands are terminated with a semicolon. This section lists the command set required for control of the breadboard.

Command Overview

Below is a brief overview of commands grouped by function. Command syntax follows later in this section.

Output Format Command

base(base-value);

Used to set the output number format for return values:

Valid values of base-value are:

1	Binary
8	Octal
10	Decimal
16	Hex

The default value is decimal. When a base-value other than decimal is used, the numbers are formatted as described above.

Example:

1. The number *255* could be returned in any of these formats:

255	Decimal
#HFF	Hex
#Q377	Octal
#B11111111	Binary

2. The command "base(1);" sets the base to binary.

Port I/O Bit Commands

setbit(port,bit-number);
rstbit(port,bit-number);
outbit(port,bit-number,value);
pulsehi(port,bit-number);
pulselo(port,bit-number);
inbit(port,bit-number);
csetbit(card,cport,bit-number);
crstbit(card,cport,bit-number);
coutbit(card,cport,bit-number,value);
cpulsehi(card,cport,bit-number);
cpulselo(card,cport,bit-number);
cinbit(card,cport,bit-number);

These commands are provided for bit level manipulation. These commands use a bit-number to identify which bit is to be operated on. Bit-numbers range from 0 to 7. 0 is the least significant bit while 7 is the most significant bit.

In order to modify bits in a port without changing others, it is necessary to have the ports configured so the current state can be read. This is done on an output port by leaving the port configured for readback. For this operation, the LAT/BUFFx! is held low (default state).

setbit and csetbit - bit is set to 1
rstbit and crstbit - bit is set to 0 outbit and coutbit - bit is set to value
pulsehi and cpulsehi - the bit is set to 1 and then to 0
pulselo and cpulselo - the bit is set to 0 and then to 1
inbit and cinbit - reads and returns the value of the bit (i.e. 0 or 1)

Port I/O Byte Commands

outportb(port,byte);
inportb(port);
coutportb(card,cport,byte);
cinportb(card,cport);

These commands are provided for operations on bytes of data.

outportb and coutportb - port is set to the value
inportb and cinportb - reads and returns the value read from the port

Example:

"outportb(2,10);" followed by "inportb(2)" writes to port 2 with a decimal value of 10, and reads this value back.

Port I/O Word Commands – Two Consecutive Ports

outport(port,value);
inport(port);
coutport(card,cport,value);
cinport(card,cport);

Commands are provided for operations on 16-bit words. In this case, two consecutive ports are used as a 16-bit word. The port with the lower address is the least significant byte, and the port with the higher address is the most significant byte. The port specified in these commands is the lower address, which may be even or odd. The lower address port will be written first.

outport and coutport - ports are set to 16 bit value
inport and cinport - return the 16 bit value read from the ports.

Example:

"coutport(0,0,#B0000000011111111);" followed by "cinport(0,0)," writes *255* in binary to port 0 of card 0, and reads back the port value in decimal.

Trigger Commands

triggin(trig_line);
trigout(trig_line);
triggen( );

These commands allow the 7064M to utilize any one of the eight(8) VXIbus TTL trigger lines.

triggin - defines which TTL trigger line the 7064M will respond to.
trigout - defines which TTL trigger line the 7064M will generate a trigger on.
triggen - generates a trigger by the 7064M on the defined "trigout" line.

Example:

"triggin(1);" followed by "trigout(1);" sets up the 7064M to respond to and generate triggers on VXIbus TTL trigger line 1. Every time the command "triggen();" is sent, the 7064M triggers itself.

NOTE:

"triggin(8)" disables triggin. The default value is set to 8.

Scanlist Commands

delay(time_usec);
scan(value);
scanbreak(port)
scanclear(port)
scanlist(port,io,data,io,data,…)
scanread(port);
scansize(port);
scansrc(src);

delay – sets the scanlist delay time in microseconds (range 500 to 10,000,000. The interrupt uses this scan delay value to dynamically configure the interrupt interval.

scan – start/continue/stop the scan function.

scanbreak – inserts a breakpoint into the scanlist for the specified port

scanclear – removes the scanlist and deallocates the memory for the specified port

scanlist – sets up scan data for the specified port

scanread – reads from memory the ;list of scan data for the specified port

scansize – returns the datasize for the specified port

scansrc – defines whether the scanning source is internal or external

Examples:

scansrc(1);	sets the scan source to External.
memalloc(2, 10);	allocates 10 words for port 2 in Share RAM.
scanlist (2, 1, 100, 1, 113, 0, 55);	defines scanlist for port 2 with the values 100 and 113 to be output data, and 55 to be mask data.
memsize(2);	returns “10” (total allocated memory for port 2).
scansize(2);	return “3” (total data size of scanlist for port 2).
scanbreak(2);	inserts a breakpoint after scandata 55 for port 2.
scanlist (2, 0, 120, 1, 99);	appends 120 as input data and 99

	as output data to current scanlist for port 2.
scansize(2);	now returns “5” as total scan data for port 2
scan(1);	starts scanning.
*TRG	port 2 now has the value of 100
*TRG	port 2 now has the value of 113.
*TRG	data is read from port 2 and masked with the 55
*TRG	port 2 still has 113 because of the breakpoint at 55
scanread(2);	returns “49" (only one value in scanread at this time)
scan(2);	continues scanning passing breakpoint.
*TRG (2 times)	port 2 now has the value of 99.
scanread(2);	return “49, 112” as scanread data for port 2
scan(0);	stops scanning for port 2
*TRG (3 times)	port 2 value remains the same which is 99.
scanclear(2);	clears out scanlist for port 2 and deallocates memory
scansize(2);	returns “Specified port does not exist.”

Non-Vol Management Commands

initnv();	This command intializes the Non-Vol memory to Zero. The states are “0” (passed) and”1” (failed).
nvcheckport(port, mask, value);	Puts a record in Non-Vol Memory that tells the system (at the time the command is given, at power on, or after a *RST) to read a particular port, AND it with the mask, and compare it with value. If they don't compare, report the mismatch. This could be used to make a system "NOTE" if all required boards were not present.
nvnocheck0;	Remove all the check records (see nvcheckport above) from Non-Vol Memory.
nvsetport(port, value);	Put a record in Non-Vol Memory that tells the firmware to initialize a particular port. At the end of the power-up sequence, value is stored in port.
nvnoset0;	Remove all set port records (set nvsetport above) from Non-Vol Memory.
nvsetvxireg(register_num, reg_value);	Allows the user to SET the response of a VXI register (reg_value is a WORD).
nvnovxireg ();	This command removes all saved records from Non-Vol memory for saved registers.
Storeopt (“string”);	Store an Option Identification string into Non-Vol. Maximum string length is 80. Example: “RI 7064M, OPT XX,XX,….” Where XX is a ASCII byte in range 00-99.

Timer Management Commands

delay(time_usec);	Delay between Scan Steps for time_usec (time in microsec.).
gettimel();	Return the elapsed time from Power On in usec. (Max time=2^{32}) This elapsed time is incremented at each interrupt interval which is depending upon the user defined scan delay time. If the new scan delay time is entered before the next interrupt comes in, the elapsed time value returned will be off by the maximum of previous scan delay frame. The resolution is depending upon the value of the scan delay.
rsettime();	Set the elapsed time to 0.

Memory Management Commands

peek(address);	Gets a WORD from the memory location “int *address”
peekb(address);	Gets a BYTE from the memory location “char *address”
poke(address, value);	Puts a WORD “int value” at the memory location “int *address”
pokeb(address, value);	Puts a BYTE “char value” at the memory location “char *address”

Output Format Commands

base(value); Set the output format to one of these formats: For value = 1 Binary, = 8 Octal, = 10 Decimal, and =16 Hex.

Range Notes:

card	::=	0-15
port	::=	0-32767 (each module has ports numbered 0-2047)
bit_number	::=	0-7
mask	::=	0-7
value	::=	0-65535
register_num	::=	0-31
register_value	::=	0-65535
address	::=	0-1048560

IEEE-488.2 Commands

*IDN? Identification Query
RESPONSE: “RACAL INSTRUMENTS, 7064M, 0, 1.1”

*RST Resets the hardware to its initial states as follows:

1. Clear out all defined scanlists and deallocate memory
2. Disable input and output triggers
3. Initialize ports to the values in Non-Vol (if any).

*TST? Internal Self-Test Query --- Execute a RAM, ROM, CPU, NON-VOL

	and timer test.
*CLS	Clear Status Command --- Clear the status data structures and force the 7064M into the Operation Complete Idle State and the Operation Complete Query Idle State. See **Figure 3-3**.
*ESE <Nrf>	Programs the IEEE-488.2 Standard Event Status Enable Register. Value ranges from 0-255. These bits provide the mechanism whereby bits in the Standard Event Status Register (ESR) are used to set bit 5 of IEEE-488.2 defined Status Byte. See **Figure 3-3**.
*ESE?	Reads the present value programmed for the IEEE-488.2 ESE Register. The ESE register is the “Standard Event Status Enable Register”. This register value determines which of the bits in the Standard Event Status Register may set bit 5 in the IEEE-488.2 defined Status Byte.
*ESR?	Reads the present value from the IEEE-488.2 ESR register. This is the “Standard Event Status Register”.
*SRE <Nrf>	Programs the IEEE-488.2 Service Request Enable Register. Value ranges from 0-255. The 7064M generates a VXI Request True Event when it detects that one of the bits in the Status Byte is set and the corresponding bit the SRE register is set. The bit value of bit 6 shall be ignored.
*SRE?	Service Request Enable Register Query --- Allows the user to find out current state of the Service Request Enable Register. The data is NR1 format in the range 0-255. The value for bit 6 is always sent as 0.
*STB?	Read Status Byte Query --- Allows the user to read the status byte and Master Summary Status Bit. The data is NR1 format in the range 0-255.
*OPC	Operation Complete Command --- This command causes the 7064M to generate the operation complete message in the Standard Event Status Register when all pending selected device operations have been finished.

*OPC?	Operation Complete Query --- Place an ASCII character 1 into 7064M's Output Queue when all pending device operations have completed. See 12.5.3 IEEE-488.2 for more detail. The response syntax is a single ASCII byte “1”.
*WAI	Wait-to-Continue Command --- This command will prevent the 7064M from executing any further commands or queries until the execution of this command is completed.
*TRG	This command triggers the 7064M to advance to its next state or perform its next pre-programmed operation. For instance, if scanlist has been defined for some particular ports, then the data from the scanlist will output/input to/from port when Trigger command is executed.
*OPT?	Option Identification --- Responds with the string. "RI 7064M, OPT XX[,XX,…..]” where XX is a ASCII byte in the range 00-99.
*SAV <Nrf>	Save the current state of the 7064M --- Store state of the 12 PORTs on all installed MODULEs to Non-Vol location 00 to 9.
*RCL <Nrf>	Recall port values from Non-Vol location 00 to 9.

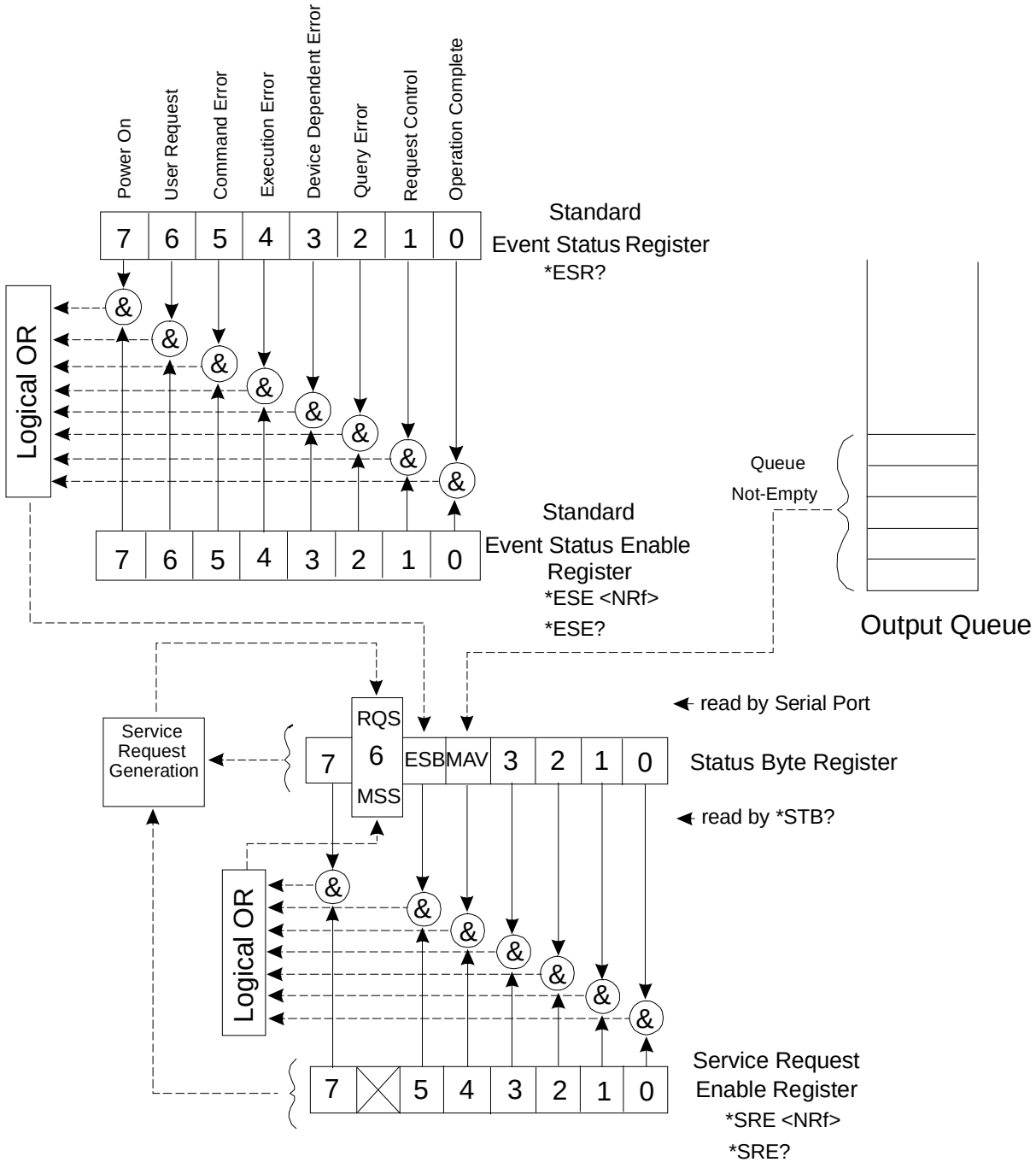


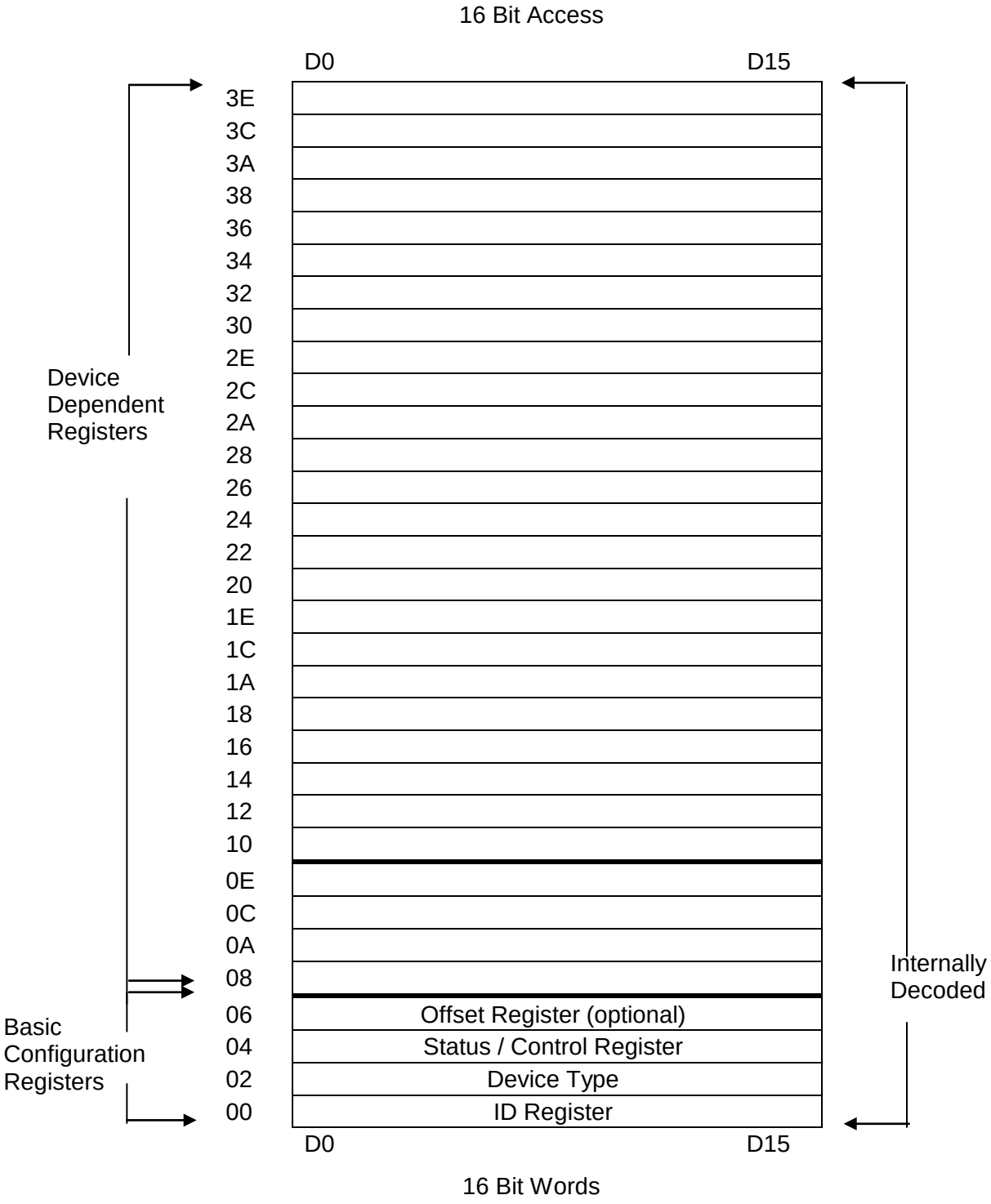
Figure 3-3, Standard Status Data Structure Overview

Command Reference		
Command	**Description**	**Page Ref**
base(value);	Set the output format to one of these formats: For value = 1 Binary, = 8 Octal, = 10 Decimal, and =16 Hex.	3-12, 18
cinbit (card, port, bit_number);	Get as input a BIT from "card#, port#, bit#"	3-13
cinport (card, port);	Get as input a WORD from "card#, port#"	3-14
cinportb (card, port);	Get as input a BYTE from "card#,port	3-13
*CLS	Clear Status Command --- Clear the status data structures and force the 7064M into the Operation Complete Idle State and the Operation Complete Query Idle State. See **Figure 3-1**.	3-19
coutbit (card, port, bit_number, value);	Output a BIT to "card#, port# bit#, value"	3-13
coutport (card, port, value);	Output a WORD to "card#, port#"	3-14
coutportb (card, port, value);	Output a BYTE to "card#, port#"	3-13
cpulsehi (card, port, bit_number);	Pulse HI the BIT at "card#, port#, bit#"	3-13
cpulselo (card, port, bit_number);	Pulse LOW the BIT at "card#, port#, bit#"	3-13
crstbit (card, port, bit_number);	Set to 0 the BIT at "card#, port#, bit#"	3-13
csetbit (card, port, bit_number);	Set to 1 the BIT at "card#, port#, bit#"	3-13
delay(time_usec);	Delay between Scan Steps for time_usec (time in microsec.) Range is 500 to 10,000,000.	3-15
*ESE <Nrf>	Programs the IEEE-488.2 Standard Event Status Enable Register. Value ranges from 0-255. These bits provide the mechanism whereby bits in the Standard Event Status Register (ESR) are used to set bit 5 of IEEE-488.2 defined Status Byte. See **Figure 3-1**.	3-19
*ESE?	Reads the present value programmed for the IEEE-488.2 ESE Register. The ESE register is the “Standard Event Status Enable Register”. This register value determines which of the bits in the Standard Event Status Register may set bit 5 in the IEEE-488.2 defined Status Byte.	3-19
*ESR?	Reads the present value from the IEEE-488.2 ESR register. This is the “Standard Event Status Register”.	3-19
gettimel();	Return the elapsed time from Power On in usec. (Max time=2^{32})	3-17
*IDN?	Identification Query RESPONSE: “RACAL INSTRUMENTS, 7064M, 0, 1.1”	3-18
inbit (port, bit_number);	Read and return the value of the BIT at “port#, bit#"	3-13
initnv();	Initializes Non-Vol memory to Zero. The states are “0” (passed) and “1” (failed).	3-17, 20
inport (port);	Read and return the value of the WORD at "port#"	3-14
inportb(port)	Read and return the value of the BYTE at "port#"	3-13
memalloc(port, size);	This command allocates the specified memory size for specified physical port.	3-15
memsize (port);	This command returns the size in words of the current total allocated memory for the specified physical port.	3-15

Command	Description	Page Ref
nvcheckport(port, mask, value);	Puts a record in Non-Vol Memory that tells the system (at the time the command is given, at power on, or after a *RST) to read a particular port, AND it with the mask, and compare it with value. If they don't compare, report the mismatch. This could be used to make a system "NOTE" if all required boards were not present.	3-17
nvnocheck0;	Remove all the check records (see nvcheckport above) from Non-Vol Memory.	3-17
nvnoset0;	Remove all set port records (set nvsetport above) from Non-Vol Memory.	3-17
nvnovxireg ();	This command removes all saved records from Non-Vol memory for saved registers.	3-17
nvsetport(port, value);	Put a record in Non-Vol Memory that tells the firmware to initialize a particular port. At the end of the power-up sequence, value is stored in port.	3-17
nvsetvxireg(register_num, reg_value);	Allows the user to SET the response of a VXI register (reg_value is a WORD).	3-17
*OPC	Operation Complete Command --- This command causes the 7064M to generate the operation complete message in the Standard Event Status Register when all pending selected device operations have been finished.	3-19
*OPC?	Operation Complete Query --- Place an ASCII character 1 into 7064M's Output Queue when all pending device operations have completed. See 12.5.3 IEEE-488.2 for more detail. The response syntax is a single ASCII byte “1”.	3-20
*OPT?	Option Identification--- Responds with the string. "RI 7064M, OPT XX[,XX,…..]” where XX is a ASCII byte in the range 00-99.	3-20
outbit (port, bit_number, value);	Set the BIT of the PORT to VALUE at "port#, bit#, value#"	3-13
outport (port, value);	Set the WORD of the PORT to VALUE at "port#, value#"	3-14
outportb (port, value);	Set the BYTE of the PORT to VALUE at "port#, value#"	3-13
peek(address);	Gets a WORD from the memory location "int *address"	3-18
peekb(address);	Gets a BYTE from the memory location "char *address"	3-18
poke(address, value);	Puts a WORD "int value" at the memory location "int *address"	3-18
pokeb(address, value);	Puts a BYTE "char value" at the memory location "char *address"	3-18
pulsehi (port, bit_number);	Pulse a BIT of the PORT to 1 then 0 at "port#, bit#"	3-13
pulselo (port, bit_number);	Pulse a BIT of the PORT to 0 then 1 at "port#, bit#"	3-13
*RCL <Nrf>'	Recall port values from Non-Vol location 00 to 9.	3-20
rsettime();	Set the elapsed time to 0	3-17
*RST	• Resets the hardware to its initial states as follows: • Clear out all defined scanlists and deallocate memory • Disable input and output triggers • Initialize ports to the values in Non-Vol (if any)	3-18
rstbit (port, bit_number);	Set the BIT of the PORT to 0 at "port#, bit#"	3-13

Command	Description	Page Ref
*SAV <Nrf>	Save the current state of the 7064M------ Store state of the 12 PORTs on all installed MODULEs to Non-Vol location 00 to 9.	3-20
scan (value);	Start/Continue/Stop the Scan function. Default is disabled. Start scanning if value = 1, set for Continous scan if value = 2, or Stop scanning if value = 0.	3-15, 16
scanbreak(port);	This command inserts a break point into scanlist for the specified physical port. When break point is reached, scanning for this particular port is stopped until scan continue is executed.	3-15
scanclear(port);	This command removes the scanlist and deallocates the memory for the specified physical port.	3-15, 16
scanlist(port,io,data,io,data,...);	This command sets up scan data for the specified physical port. The io value defines whether the data is output or mask. If io = 1, then the data in the scanlist is output to the port. If io = 0, data read from the port is ANDed with the data which now serves as a mask. The result is then written into the memory which can be read from the scanread command. Note: Subsequent scanlist commands on the same port will append to the I/O data in the previous list.	3-15
scanread(port);	This command reads from the memory the list of scan data for the specified physical port.	3-15, 16
scansize(port);	This command returns the datasize for the specified port.	3-15, 16
scansrc (src);	This command defines whether the scanning source is EXTERNAL or INTERNAL. For INTERNAL scanning source, a certain delay has to be specified using the delay command in order for other commands to be executed. SRC=0 for Internal and SRC=1 for External.	3-15
setbit (port, bit_number);	Set the BIT of the PORT to 1 at "port#, bit#"	3-13
*SRE <Nrf>	Programs the IEEE-488.2 Service Request Enable Register. Value ranges from 0-255. The 7064M generates a VXI Request True Event when it detects that one of the bits in the Status Byte is set and the corresponding bit the SRE register is set. The bit value of bit 6 shall be ignored.	3-19
*SRE?	Service Request Enable Register Query--- Allows the user to find out current state of the Service Request Enable Register. The data is NR1 format in the range 0-255. The value for bit 6 is always sent as 0.	3-19
*STB?	Read Status Byte Query --- Allows the user to read the status byte and Master Sunnary Status Bit. The data is NR1 format in the range 0-255.	3-19
Storeopt (“string”);	Store an Option Identification string into Non-Vol. Maximum string length is 80. Example: “RI 7064M, OPT XX,XX,….” Where XX is a ASCII byte in range 00-99.	3-20
*TRG	This command triggers the 7064M to advance to its next state or perform its next pre-programmed operation. For instance, if scanlist has been defined for some particular ports, then the data from the scanlist will output/input to/from port when Trigger command is executed.	3-15, 20
triggen ();	Enable VXI Trigger Output line	3-14
triggin(line);	0-7 Is the VXI Trigger Input Line, 8 is used to disable	3-14
trigout(line);	0-7 Is the YXI Trigger Output Line, 8 is used to disable	3-14
*TST?	Internal Self-Test Query--- Execute a RAM, ROM, CPU, NON-VOL and timer test.	3-19
*WAI	Wait-to-Continue Command --- This command will prevent the 7064M from executing any further commands or queries until the execution of this command is completed.	3-20

7064M A16 Register Map



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Appendix A
68000 INTERFACE

Introduction

This section contains information that applies to user who have purchased Option-95 (P/N 407620-OPT95), Source Code for Message-Based Interface.

The Message-Based Interface has a simple and flexible software architecture that allows users to load and execute their own application code in a variety of ways. Additionally, the Message Based Interface provides several system services at the level of C-language function calls. Many Message-Based Interface system configuration parameters are programmable, giving the user the ability to custom-tailor the Message-Based Interface for a particular application.

Consult the OPT-095 manual for further information about implementing user-developed firmware.

VXIbus Interface

The VXI interface is implemented with dual-port RAMs. The RAMs and interface I/O support circuitry are located in this area.

User space is the upper half of memory. The user may use this space in conjunction with any user-supplied code and circuitry to implement special functions and handle special needs.

All of the I/O ports are located in the local bus space. Reads and writes to this area cause transfers across the local bus. These cause reads or writes to the I/O ports.

Timer

A timer is used to maintain a real time clock with the time since power-up initialization. A set of routines is provided to allow the user access to the timer.

Memory Space

The memory space of the 68000 is divided into two major areas. The upper half of memory is available for the user. This 8 Mbyte space has no breadboard circuitry or memory located in it. The lower half of memory contains all of the breadboard's I/O ports, the onboard memory and circuitry.

The address space is decoded as follows:

000000 - 1FFFFF	ROM
200000 - 3FFFFF	Reserved
400000 - 5FFFFF	RAM
600000 - 6FFFFF	Non-Vol
700000 - 73FFFF	Timer
740000 - 77FFFF	Not Supported
780000 - 7BFFFF	I/O ports on local bus
7C0000 - 7FFFFF	VXI interface
800000 - FFFFFF	User area

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