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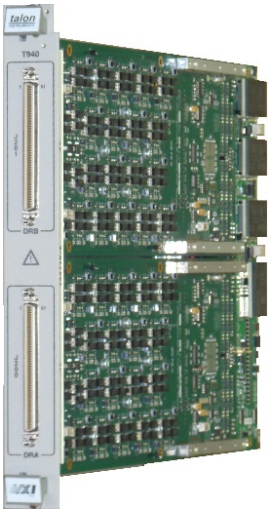
Model T940

64-Channel

Digital Resource Module

User Manual

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FOR YOUR SAFETY

Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.



This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.
2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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DOCUMENT CHANGE HISTORY

Revision	Date	Description of Change
A	10/6/2009	Document Control release
B	1/18/2012	EO: Added T940 variant and DR3e & DR7 boards. Updated software screens and specifications.
C	4/17/2012	ECN00132: Added information regarding DR9 option.
D	9/11/2012	ECN00901. Updated manual to add driver updates and functionality impacts.
E	2/6/2013	ECN02110. Updated specifications and added additional board clarifications as well as the procedure to install a DR9 board. Updated soft front panel operation to reflect changes in software. Also added UR14 board and probe features
F	7/23/2013	ECN03095: Added information regarding DR8 option.
G	5/7/2014	ECN04897: Added additional content including attributes and static state control, statis mode, comparator delay, pass/fail clear, and static data. Revised MTBF hours for boards. Rebranded manual to Astronics.
H	6/13/2014	ECN05018: Added information regarding new DR4 option including Appendix E, DR4 Driver/Receiver Board.
J	5/19/2015	ECN06159: General update of manual to latest software and sequencer revision, addition of calibration and advanced topics chapters, specification updates.
K	10/28/2015	ECN06542: Updated text and soft-front panel screen shots to include new reference ADC and load calibration, DR4 calibration validation support, current alarm high/low, -4 power converter control, support for Sequencer 0.23, and updated slew rate specs.

Chapter 1
Introduction

This manual provides information necessary to set up and operate the T940 64-Channel Digital Resource Modules (DRM). Throughout this manual, “DRM” is used to refer to the T940.

Separate chapters and appendices include:

- Overview and features of the DRM
- Installation
- Front panel and connector descriptions
- Functional descriptions
- Detailed soft front panel software operation
- Specifications
- Acronyms and glossary of terms
- Driver/Receiver boards technical information
- Timing characteristics

Overview and Features

The Talon Instruments™ Digital Resource Module (DRM) provides two high speed data sequencers and up to 64 high-performance digital I/O channels in a space-saving single-wide VXI module. The DRM operates at data rates up to 50 MHz with 1 ns edge placement and less than 3 ns channel-to-channel skew.

Designed for High Reliability

The comprehensive thermal design ensures reliability with excellent cooling, monitoring, and protection. Each high-power module is equipped with a custom-designed heat sink to provide optimal cooling. An on-board temperature monitor protects the pin electronics devices from overheating and provides over-temperature shutdown.

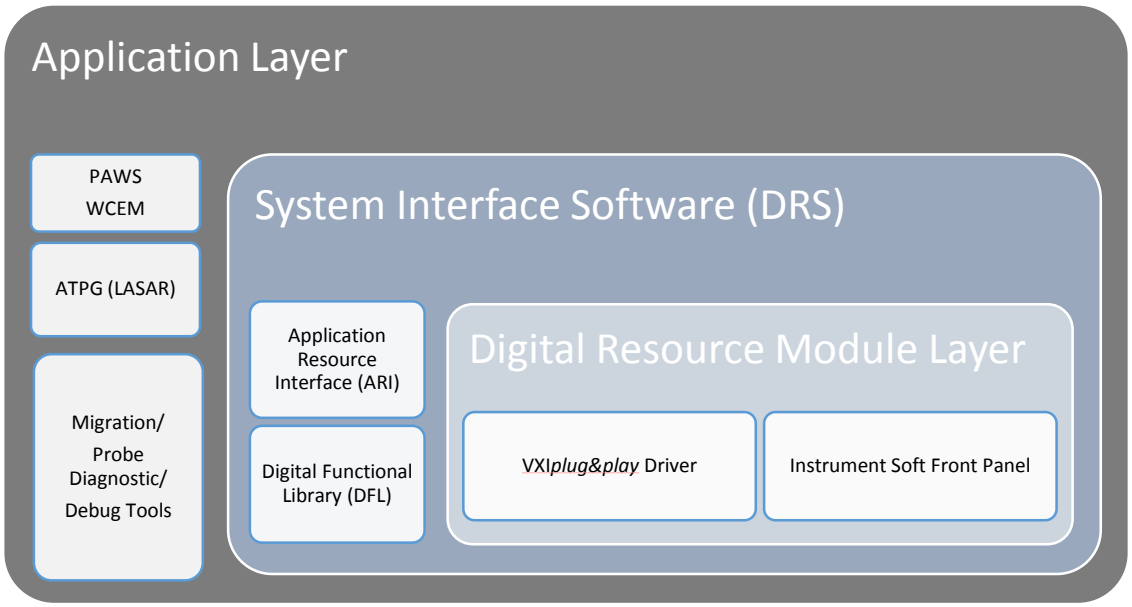
An optional Racal Instruments™ 1263HP series high-power VXI chassis provides an integrated power supply for DRM front panel power and additional cooling for large digital test systems. (See an illustration of the chassis in **Chapter 2, Installation**). For additional information on this chassis, contact your sales representative.

Advanced Features for Modern Digital Test Development

The DRM is designed for today's challenging digital test system applications through innovative design. The flexible Field Programmable Gate Array (FPGA) design enables the DRM to meet special user and legacy requirements. The high-speed Data Sequencer provides control over test patterns, timing, and format.

Innovative Software Tools Speed Test Development

The VXI*plug&play* driver and Digital Resource Module Layer support third-party test development tools to ease development and integration into popular test environments. The optional Microsoft Windows® CIIL Emulation Module (WCEM), for the Astronics Test Systems PAWS™ Runtime System (RTS), provides an interface to the DRM from the IEEE standard ATLAS test language for modern test development.



Ideal for Legacy Replacement and Preserving TPS Investments

The DRM is ideal for replacing less reliable, obsolete instruments. With the innovative software tools, the investments in digital technology can be preserved and sustained going forward on a modern platform. Legacy TPS performance has been demonstrated on ARGCS, RTCASS, NGATS, ESTS, B-1B ARTS and used to replace L300 legacy systems.

Scalable Design

Built-in scalability and modular design enable configurations from 24 to 768 channels in 24 or 32 channel increments. DRMs and Digital Resource Suites (DRSs) can operate as independent digital instruments or as a single digital subsystem. Driver/Receiver module types can also be intermixed to match the signal requirements of the test system.

High-Speed Data Sequencer

The high-speed data sequencer provides state-of-the-art control over digital test patterns. Each DRM contains two data sequencers that can operate

independently or linked for timing, memory, and control of the two Driver/Receiver boards. Sequencer logic supports full unit under test (UUT) handshaking and controls timing, format, pattern data, looping, and conditional testing. The sequencer includes definable standby and idle sequences.

Triggering and Synchronization

The DRM features extensive control over digital testing to synchronize the DRM with other test instruments and control digital test sequencing. The DRM accepts triggers from the VXI TTL Trigger Bus, VXI ECL Trigger Bus, front panel Auxiliary inputs, or from any channel, and provides two sync outputs per DRM. Triggers can be used to synchronize the T940 with other instruments and as a test input for test sequence control. Sync outputs can be offset to the start of a test sequence or step.

Instrument Soft Front Panel

The soft front panel software provides interactive control of the DRM. The intuitive graphical interface enables setup and configuration, calibration, and sequencer control. Channels may be set up either individually or in user-defined groups.

WCEM for Astronics Test Systems PAWS

The optional WCEM for the PAWS Runtime system provides an interface to the DRM from the IEEE standard ATLAS test language. This interface provides the capability for the DRM to support both legacy and modern system implementations that take advantage of the higher-order, signal-oriented features of IEEE ATLAS.

The interface utilizes the PAWS system, the popular independent implementation of the ATLAS language. The user does not need to know the nuances of the DRM as the ATLAS language provides the higher-order interface to the hardware.

Application Resource Interface (ARI)

The optional Application Resource Interface (ARI) provides C-callable functions and services to the standard DRM driver, providing the capability for users to configure and execute multiple DRMs as a DRS. This interface provides the capability to emulate the legacy system characteristics without changes to the underlying C program that executes the digital test.

Digital Function Library (DFL)

The optional Digital Function Library (DFL) provides an interface to Legacy Applications that can be adapted as needed to implementations to seamlessly support legacy investments. This interface provides the capability for the system to emulate the legacy software characteristics without changes to the underlying C program that executes the digital test.

Automatic Test Program Generation (ATPG)

The optional ATPG provides an interface to IEEE-Std-1445 formatted files that can be generated from automatic test program generators such as LASAR to seamlessly integrate with the DRM. This interface provides the capability for the system to utilize the various features of IEEE-Std-1445 to support guided probe,

fault dictionary and complex patterns and timing set(s).

Migration Tools and Translators

The optional Migration Tools and Translators support many legacy test systems from a variety of manufacturers. Test programs from supported systems are easily translated without extensive code rewriting.

Driver/Receiver Board Options

The DRM currently has the following Driver/Receiver board types available:

DR1: Driver/Receiver

The DR1 features:

- Channels: 32 single-ended LVTTL
- Relay Isolation on all I/O and AUX channels.
- Selectable resistive input load to VCC (+3.3 V), ground or both.
- Direct or 100 ohm selectable output impedance
- Auxiliary channels
  - Four LVTTL with selectable output impedance and resistive input load.
  - Four LVTTL
  - Four ECL (single ended or differential)

DR2: Driver/Receiver

The DR2 features:

- Channels: 32 differential LVDS
- Auxiliary channels:
  – Four LVDS
  – Four LVTTL
  – Four ECL (single ended or differential)

DR3e: Driver/Receiver

The DR3e features:

- Channels: 32 single-ended variable voltage or 16 differential channels
- Voltage range: -15 V to +24 V with an output swing of up to 24 V
- Relay Isolation on all I/O and AUX channels.
- Full drive current on all channels simultaneously
- Programmable current load with dual commutating voltages
- Selectable resistive input load (8 choices) to a programmed voltage
- Selectable output slew rate (0.25 V/ns to 1.3 V/ns)
- 12/50 Ohm selectable output impedance
- Over-current detection

- Over-voltage detection/protection
- Auxiliary channels:
  - Four variable voltage
  - Four LVTTL
  - Four ECL (single-ended or differential)

DR4: Driver/Receiver

The DR4 features:

- Channels: 48 single-ended variable voltage or 24 differential channels
- Voltage range: -31 V to +31 V with an output swing of up to 31 V
- Relay Isolation on all channel I/O
- Selectable current drive
- 5 Ω, 50 Ω selectable output impedance
- Over-current detection
- Temperature monitoring
- 16 TTL auxiliary channels

DR7: Driver/Receiver

The DR7 features:

- Channels: 32 differential RS-422/485
- Auxiliary channels:
  – Four RS-422/485
  – Four LVTTL
  – Four ECL (single ended or differential)

DR8: Driver/Receiver

The DR8 features:

- Channels: 32 single-ended TTL
- Relay Isolation on all I/O and AUX channels.
- Selectable resistive input load to VCC (+5.0 V), ground or both.
- Direct or 100 ohm selectable output impedance
- Auxiliary channels
  - Four TTL with selectable output impedance and resistive input load.
  - Four TTL
  - Four ECL (single ended or differential)

DR9: Driver/Receiver

The DR9 features:

- Channels: 24 single-ended variable voltage or 12 differential channels and 24 analog test channels

- Voltage range: -15 V to +24 V with an output swing of up to 24 V
- Relay Isolation on all I/O channels.
- Provides full drive current on all channels simultaneously
- Programmable current load with dual commutating voltages
- Selectable resistive input load (8 choices) to a programmed voltage
- Selectable slew rate (0.25 V/ns to 1.3 V/ns)
- 12/50 Ohm selectable output impedance
- Over-current detection
- Over-voltage detection/protection
- Auxiliary channels:
  – Four LVTTL (no relay isolation)

Utility Resource (UR) Option

The DRM currently has the following utility resource module type available:

UR14: Utility Resource

The UR14 features:

- Channels: 32 Low Speed single-ended, open-collector utility pins
- Voltage range: 0 to +30 V
- Suitable for Inductive loads, internal clamping to ~42 V
- +5 V Pull-up allowing each channel to operate as low speed TTL.
- Programmable input level detection (per byte) 0-20 V
- Programmable over-current detection (per byte) 0-1 A
- External probe support
- Auxiliary channels:
  - Six variable voltage (Two are used with the external probe)
  - Four LVTTL
  - Four ECL (single ended or differential)
  - Four LVTTL or SE ECL I/O
  - Four LVTTL or ECL (single-ended or differential) I/O
  - Three ECL (single-ended or differential) I/O
  - Two LVTTL I/O

Basic Elements of the DRM System

As illustrated in Figure 1-1, the DRM module is comprised of the following major components; front panel, a Digital Board (DB), and selected Driver/Receiver

Boards (named DRA and DRB for their mounted location). (A T940 module is shown in the photo as an example.)

The block diagram in Figure 1-2 shows how the various components work together. DRA and DRB could be any of the DR boards (such as DR1, DR2, DR3e, etc.) offered for the DRM system.

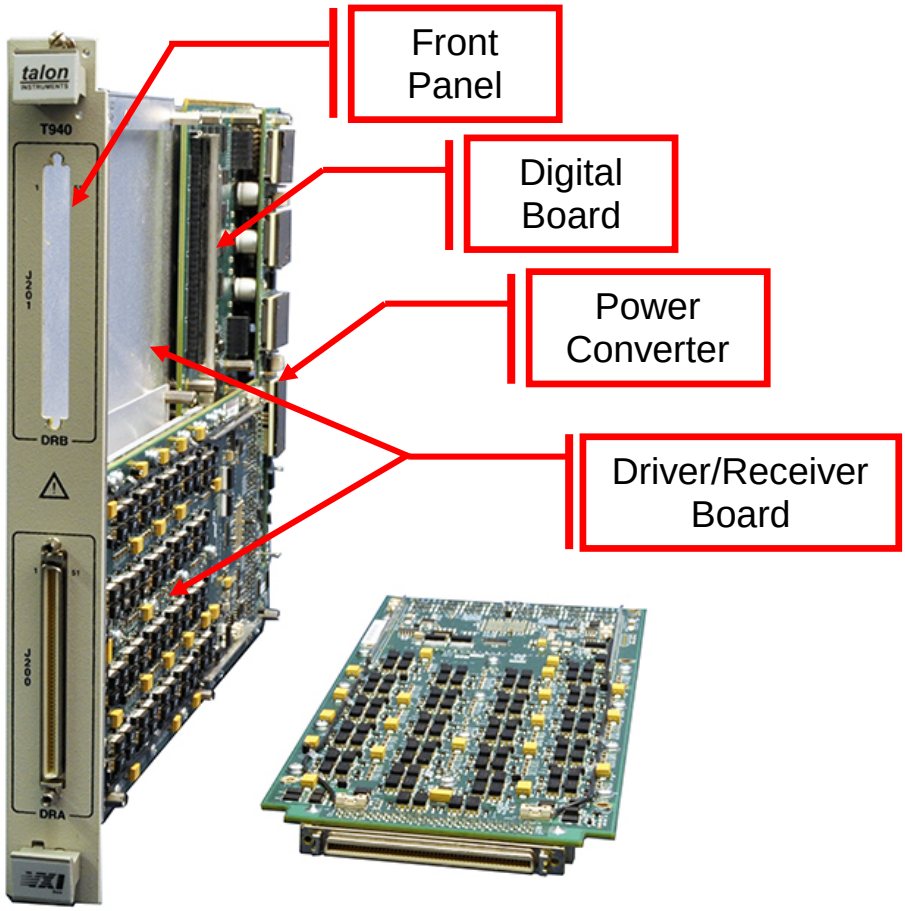


Figure 1-1: Example DRM with Two Driver/Receiver Boards (DRA and DRB)

If the DRM has only one Driver/Receiver board, the front panel will have a blank cover panel where the front connector would have been located.

Note: *The DR9 board has a different front connector panel than the others. Refer to Appendix H for more information about and an illustration of the DR9.*

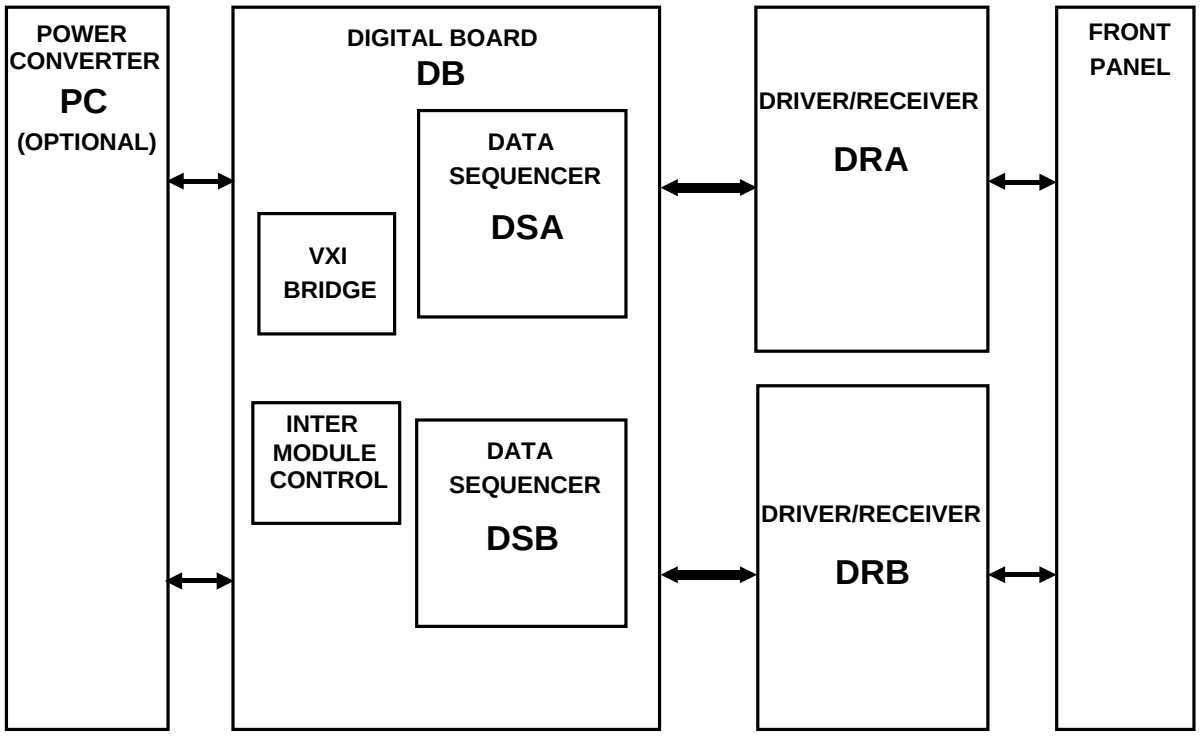


Figure 1-2: DRM Digital Resource Module Block Diagram

Front Panel

The DRM front panel provides the interface to the device being tested. There is a Driver/Receiver board connector for input and output of signals. As an option, the T940 can be equipped with an external power connector to power the DR3e.



Figure 1-3: T940 Optional Front Panel PWR Connector

Power Converter (PC)

The PC may be optionally installed on the Digital Board when variable voltage DR boards such as the DR3e, DR9, or UR14 are used. The PC converts backplane voltages into digital bias voltages. Its protection circuitry can detect faults in any of the four on-board power supplies, status of the input fuses, or a high input current or overcurrent condition. There are three types of power converters, each of which has seven voltage ranges.

Digital Board (DB)

The DB contains the connectors and headers required for routing signals to/from the VXI backplane as well as the DRA/DRB logic. The DB logic is comprised of the following major components.

VXI Bridge

The VXI Bridge maintains the VXI interface with the backplane. The bridge includes the communication registers for the VXI protocol requirements. The DRM functions are programmed through VXI A16/A32/A24 register access.

Inter-Module Control

In a multi-module system, the VXI Local Bus is used to synchronize the modules. The Inter-Module Control logic is used to route and terminate these signals.

Data Sequencer A and B

Each DB contains two Data Sequencers, DSA and DSB. Each data sequencer can be run independently or synchronized. Data Sequencer A provides the timing, memory and control for the DRA board (Channels 1 through 32). Data Sequencer B provides the timing, memory and control for the DRB board (Channels 33 through 64).

The Data Sequencer logic consists of the following:

- Timing Data (Phase Assert, Phase Return, Window Open, Window Close)
- Stimulus Format Code (Non Return, Return to Zero, etc.)
- Pattern Data (Output Levels, Input Compare, CRC Enable)
- Sequence Data (Pattern Period, Pattern Order, Looping, Conditional Testing)
- Result Data (Error Flags, Error Count, CRC per Channel, Record Memory)

Driver/Receiver (DR) Board

Driver/Receiver Board A (DRA)

The DRA board contains all the driver/receiver logic, relays, sensors and termination circuitry for channels 1 through 32.

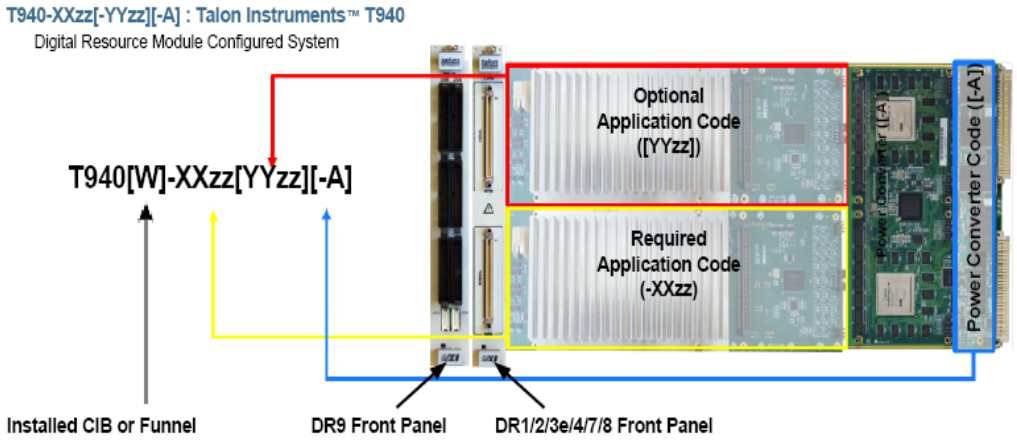
Driver/Receiver Board B (DRB)

The DRB board contains all the driver/receiver logic, relays, sensors and termination circuitry for channels 33 through 64.

Model and Part Number Information

Model #	Description	Ordering Part #
DR1	LVTTL, 32 channels, 100 Ω source termination	405349-001
	LVTTL, 32 channels, 50 Ω source termination	405349-002
DR2	LVDS, 32 channels, 100 Ω source termination	405350
DR3e	Variable voltage, -15 V to +24 V, 32 Channels	408002
DR4	Variable voltage, -31 V to +31 V, 48 Channels	408558
DR7	RS422/RS485, 32 channels, 100 Ω source termination	408242-101
DR8	TTL, 32 channels, 100 Ω source termination	408241-101
	TTL, 32 channels, 50 Ω source termination	408241-102
DR9	Variable voltage, -15V to +24V, 24 Direct/Analog Test Channels	408254
UR14	Utility resource, 32 HV Open Collector channels, probe interface, auxiliary interface	408290

To understand a configured module part number for a T940 DRM, use the T940 model number configurator shown in the next figure.



To create the 2nd, 3rd, and 4th sections of the part # for a configured T940, substitute the [W], "-XXzz," "-YYzz," and [-A] in the part # with the correct CIB/Funnel, Application and Power Converter Code from the table below. Note that the rightmost front panel is representative of the DR1/2/3e/7/8 modules and the leftmost is for the DR9 and is similar in style to the T940-UR14 front panel.

Model	**Code (-XXzz) (-[YYzz])**	**Application Code Description**	**Spares Part #**
DR1	150	LVTTL, 32 Channels, 50 Ω source termination	405349-002
DR1	110	LVTTL, 32 Channels, 100 Ω source termination	405349-001
DR2	210	LVDS, 32 Channels, 100 Ω source termination	405350
DR3e	3e50	Variable Voltage, -15 V to +24 V, 32 Channels, Over-voltage	408002
DR7	710	RS-422, 32 Channels, 100 Ω source termination	405350-101
DR8	850	TTL, 32 Channels, 50 Ω source termination	405349-102
DR8	810	TTL, 32 Channels, 100 Ω source termination	405349-101
DR9	950	Variable Voltage, -15 V to +24 V, 24 Direct/Analog Test Channels	408248
UR14	1450	Utility Resource, 32 HV Open Collector channels, probe interface, auxiliary interface	408291
Model	**Code ([-A])**	**Power Converter Code Description (Specify for DR3e or DR9)**	**Spares Part #**
Type 1	1	VXI 3.0 power converter, 24V	405404-001
Type 3	3	VXI 4.0 power converter, 24V	405404-003
Type 4	4	VXI 3.0 or 4.0 power converter, 16V	405404-004
Model	**Code ([W])**	**Installed CIB or Funnel Code Description**	**Spares Part #**
Type F	F	VP90 Style Coaxial Funnel (available for DR9 and UR14)	DR9: 408257 UR14: 408258
Type F1	F1	Mini VP90 Style Signal Contact Funnel (available for DR3e and UR14)	DR3e: 408257-S-2986 UR14: 408258-S-2987
Type C	C	Legacy Compatible Connector CIB Module (available for DR1, DR3e, DR4, DR8)	405489

Accessories

Model #	Description	Ordering Part #
T940/300-XXX	Front Panel Signal Flat Ribbon Cable (1 per Driver/Receiver Board)	408123-XXX
T940/302-XXX	Front Panel Signal Flat Shielded Cable (1 per Driver/Receiver Board)	408122-XXX
T940/303-001	Coaxial Cable, 22 positions, Auxiliary I/O from T940 master to CRB slot	408124-001
T940/304-XXX	Front Panel Power Cable (1 per Digital Resource Module with F/P power option)	408091-XXX
T940/305-XXX	Single-Ended Coaxial Cable, 44 positions, 3', unterminated	408125-XXX
NA	T940 Coaxial IDC Cable, 17 positions, both ends IDC terminated (4 per 64 channel module, used with DR9 and DR3e modules)	602715-XXX
N/A	A/C-type LBUS Lockout Key	455540
N/A	C-type LBUS Lockout Key	455541
N/A	T940 Inter-Module Mode Jumper	408382
N/A	External Probe Module Right Angle	405389-001
N/A	External Probe Module Flush	405389-002
N/A	External Probe Module Handheld Probe Kit	PM6139
N/A	External Probe Module Cable 3 feet	408378-036
N/A	External Probe Module Cable 10 feet	408378-YYY

Note:

1. *In the above table,* XXX *is the length in feet.*
2. *In the above table,* YYY *is the length in inches from 36 to 120 in 12-inch increments.*
3. *For more information about Lockout Keys, refer to the* **Front Panel LBUS Lockout Keys** *section in* **Chapter 3.**

Chapter 2
Installation

The following sections discuss the installation procedure for the DRM module into a VXI chassis.

Before installing the DRM module, ensure that the digital board (DB) DIP switches are set to correct settings for your setup – either in the factory default mode or with specific address and mode settings to your test situation. Refer to the next several sections for this setup information.

If you have received a small packet of extra screws with the module, place these in a secure location for future use should you add a Driver/Receiver board at a later date.

WARNING

The DRM is NOT hot-swappable. The power to the VXI chassis must be turned off before installing a DRM. Plugging the module in before the power is off may result in damage to the electronics.

Note: *The following pictures show the DRM with the cover panel removed.*



Figure 2-1: T940 with Two DR7 Boards Installed

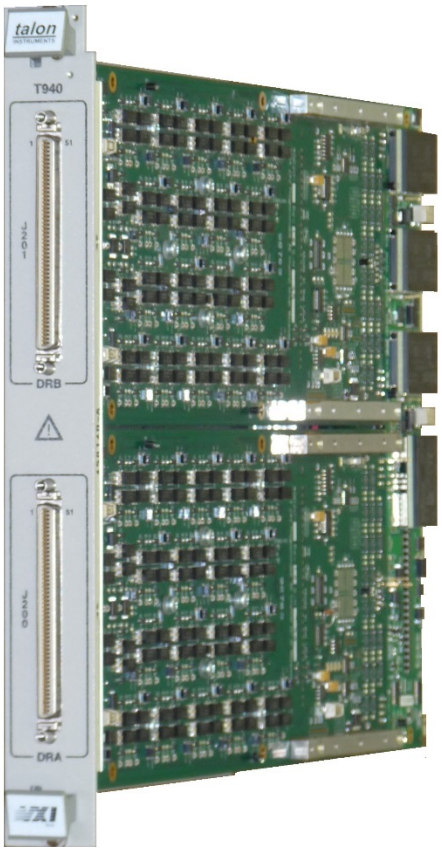


Figure 2-2: T940 with Two DR3e Boards Installed

Initial Digital Board (DB) Switch Setting

WARNING

Use standard ESD procedures including ground straps and static-safe work surfaces whenever handling the DRM or any of its Driver/Receiver boards.

There are three DIP switches on the Digital Board located between the VXI connectors P1 and P2 at the rear end of the board. When shipped, they are set to current factory default settings.

However, SW1 and SW2 can be set to modify several selections including:

- Logical Address Selection
- VXI Interrupt Level Selection
- A24/A32 Map Selection

If you are using two or more T940 boards in a system, there is also a jumper that needs to be set depending how it is configured (for instance, Primary, Secondary, or Terminator).

See the following sections for more information.

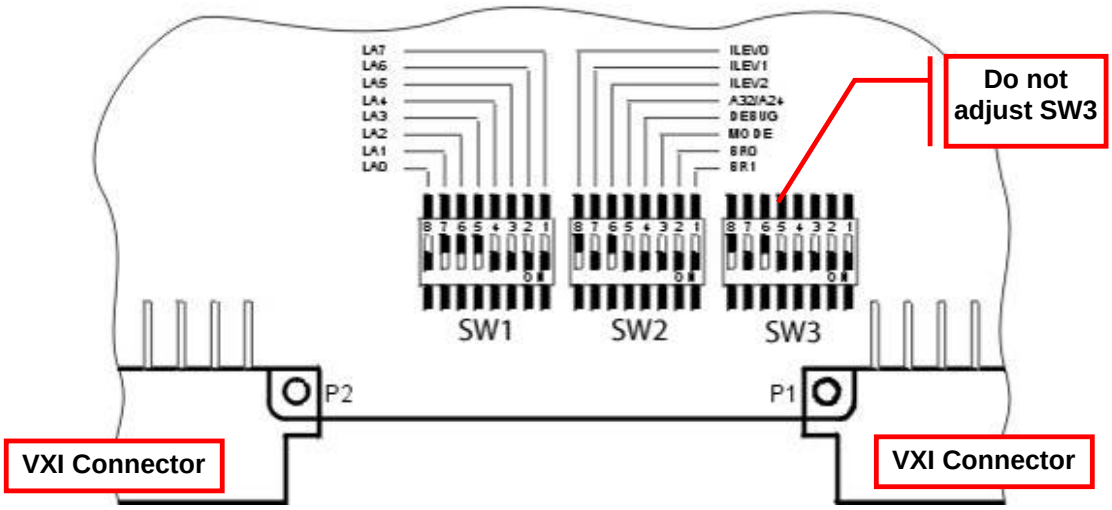


Figure 2-3: Digital Board (DB) Switch Locations

CAUTION

Switch settings shown in Figure 2-2 are for example only and are not particularly what your board should be set to. Refer to the text for proper switch settings.

Logical Address Selection

The VXI chassis Resource Manager identifies units in the system by the unit's logical address. The VXI logical address can range from 0 to 255. The exceptions are addresses 0 and 255. Address 0 is reserved for the Resource Manager. Address 255 is used for dynamic configuration.

The logical address of the DRM can be statically or dynamically configured. **SW1**, an eight position DIP switch located on the DB (Figure 2-3) is used to assign the logical address. Refer to Table 2-1.

A switch setting between 1 and 254 will establish a static logical address of the binary encoded value. A switch setting of 255 will place the DRM in a dynamic logical address mode where the final logical address is assigned by the resource manager. A switch setting of 0, while normally invalid as a selection, also will place the DRM in a dynamic mode avoiding configuration conflicts with Logical Address 0.

The DRM is shipped in the dynamic configuration with a switch setting of 255.

Table 2-1: Logical Address Selection

SW1								
Position	8	7	6	5	4	3	2	1
Signal	LA0	LA1	LA2	LA3	LA4	LA5	LA6	LA7

Switch position 8 through 1 corresponds to bits 0 through 7 of the logical

address. The “ON” setting sets the corresponding bit of the logical address to a one (1).

VXI Interrupt Selection

The VXI backplane supports 7 levels of interrupts. Using the Slot 0 API functions, interrupt handlers can be installed and enabled for each interrupt level.

Switch positions 8, 7, and 6 of SW2 are used to assign the DRM interrupt level. A value of zero disables interrupt generation by the DRM. Values between one and seven select the interrupt of the same value. For example; if SW2 position 7 and 6 are ON and position 1 is OFF then VXI interrupt level 6 will be used by the DRM.

VXI level one is set at the factory prior to shipment.

Table 2-2: VXI Interrupt Selection

SW2			
Position	8	7	6
Signal	ILEV0	ILEV1	ILEV2

ILEV2	ILEV1	ILEV0	VXI Interrupt Level
OFF	OFF	OFF	Disabled (none)
OFF	OFF	ON	Level 1 Selected (factory default)
OFF	ON	OFF	Level 2 Selected
OFF	ON	ON	Level 3 Selected
ON	OFF	OFF	Level 4 Selected
ON	OFF	ON	Level 5 Selected
ON	ON	OFF	Level 6 Selected
ON	ON	ON	Level 7 Selected

A24/A32 Map Selection

In addition to the standard configuration registers assigned to the DRM in the A16 memory space, 1M of extended memory space is required by the DRM. The VXI resource manager assigns extended memory in either the A32 or A24 memory space.

Switch position 5 of SW2 is used to select A32/A24 register mapping.

Table 2-3: A24/A32 Map Selection

SW2	
Position	5
Signal	A32/A24

A32/A24	Register Mapping
OFF	A32 (factory default)
ON	A24

ATTENTION

GPIB-VXI slot zero controllers do not support A32 register transfers. A24 register mapping must be selected for DRM operation with these controllers.

Other Settings

There are a few switch settings that are used for development or debug which, under normal operation, should not be changed. The factory-set default setting for normal operation is noted in each case.

Debug Selection

This is a factory setting and must be set OFF for normal operation.

Switch position 4 of SW2 is used to select debug operation.

Table 2-4: Debug Selection

SW2	
Position	4
Signal	DEBUG

DEBUG	Debug Operation
OFF	Debug off (Default)
ON	Debug on

Mode Selection

Switch position 3 of SW2 is used to select the VXI bus protocol mode.

Table 2-5: Mode Selection

SW2	
Position	3
Signal	MODE

MODE	Message Based Enabled
OFF	VXI Message Based
ON	VXI Register Based (Default)

Bus Request Selection

The VXI backplane supports 4 levels of bus request.

Switch positions 2 and 1 of SW2 are used to select the VXI bus request level.

Table 2-6: Bus Request Selection

SW2		
Position	2	1
Signal	BRO	BR1

BR1	BR0	Bus Request Level
OFF	OFF	0
OFF	ON	1
ON	OFF	2
ON	ON	3 (Default)

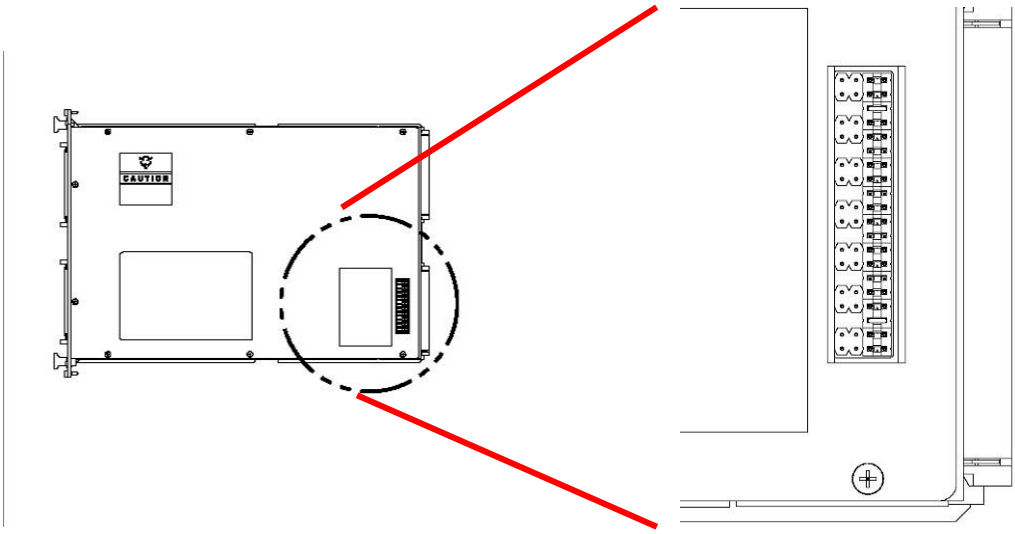
DRS Inter-Module Mode Control

Note: *This is used when setting up a Digital Resource Suite (DRS) with two or more DRMs.*

The T940 uses a jumper bar (PN 408382) to define whether the DRM is the Primary, Secondary, or Terminator. **A T940 DRS is configured right to left**. The Primary must be installed to the **right** of the Terminator. Secondary DRMs, if any, are placed between the Primary and Terminator.

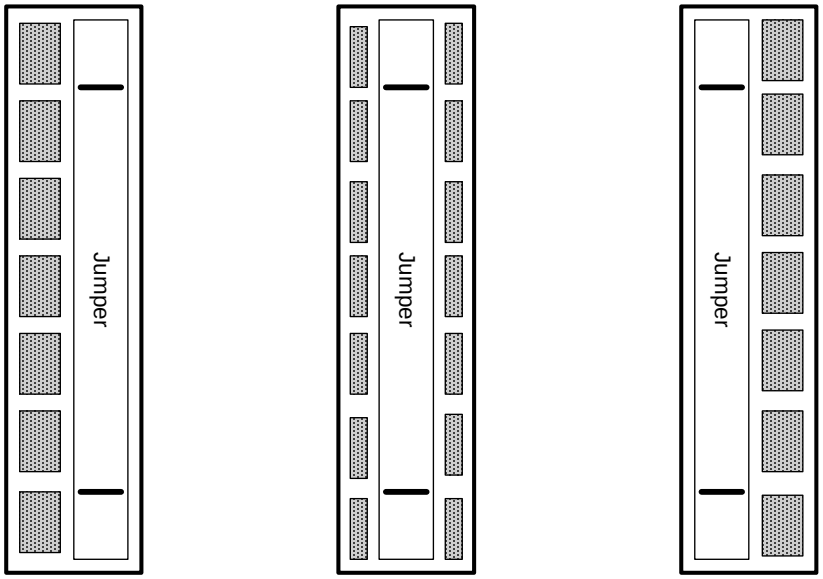
The **Inter-Module Control** section in **Chapter 4**, **Functional Description**, describes this feature in detail. The **Inter-Module Mode** section in **Chapter 5, Soft Front Panel Operation**, discusses the configuration of the DRMs.

Three settings are available based on the position of the jumper.. Figure 2-4 shows the location of the T940 jumper. The jumper is accessible through a cutout in the T940 cover. To remove the jumper, use the paper tab of the jumper bar to lift it off the connector. Figure 2-5 shows the jumper positions for the desired setting: Primary, Secondary, or Terminator.



Note: *Jumper above is shown in the "Terminator" position.*

Figure 2-4: T940 Inter-Module Mode Jumper Connector Location



Terminator Position **Secondary Position** **Primary Position**

Note: *The gray areas in the figure indicate the open portions of the connector.*

Figure 2-5: T940 Inter-Module Mode Jumper Positions and Settings

Installing the Module into a VXI Chassis

WARNING

The DRM is NOT hot-swappable. The power to the VXI chassis must be turned off before installing a DRM. Plugging the module in before the power is off may result in damage to the electronics.

ATTENTION

Be sure that the VXI chassis has sufficient power and cooling capability – particularly if multiple DR3e, DR4, or DR9 modules are installed into the same chassis.

The DRM may be installed in any VXI chassis slot except slot 0 (zero), which is reserved for the Resource Manager. (See Figure 2-6.)

Always check VXI connectors P1 and P2 for bent pins prior to installation.

When inserting the DRM into the chassis, it should be gently rocked back and forth to seat the connectors into the backplane receptacles.



Figure 2-6: Installing the DRM into a Chassis

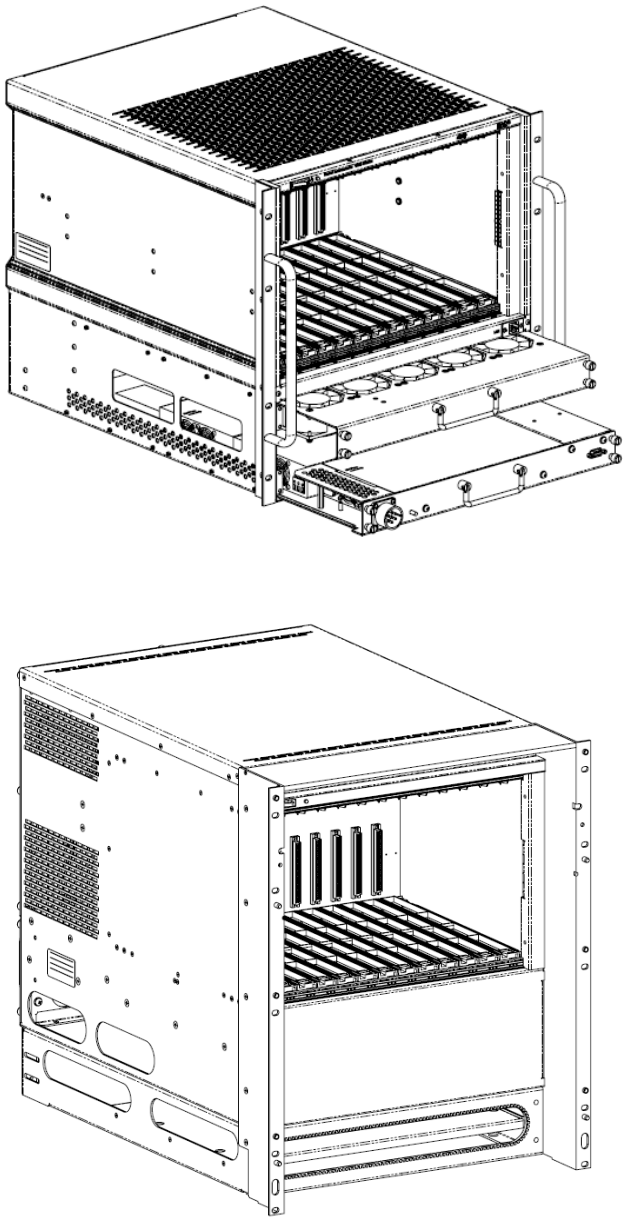


Figure 2-7: 1263 Series VXI Chassis (1263HPf top, 1263HPr bottom)

The optional Racal Instruments 1263 High Power 13-slot VXI chassis series (Figure 2-7) is recommended for multiple DRMs which are populated with multiple DR3e, DR4 or DR9 modules. These chassis have an integrated power supply and enhanced cooling that will support such DRMs.

For information on these products, contact your Astronics Test Systems sales representatives.

Any VXI chassis will support a DRM that is populated with DR1s, DR2s, DR7s, DR8s, or UR14s.

Initial Power-On

The DRM is normally a register-based VXI module with an embedded processor to manage standard VXI communications.

1. **Turn off** the chassis power before installing the DRM.
2. Once the DRM is properly installed in a VXI chassis, turn on the chassis power.

   The SYSFAIL- line will be immediately driven. The DRM embedded processor will verify the processor core and VXI communication registers.
3. **After about five seconds**, if the DRM passes its internal self-test, the SYSFAIL- line will no longer be driven by the DRM and the **Ready** and **Passed** bits in the VXI Status Register are set.

If the DRM fails the self-test (for instance, the Sys Fail indicator light glows red on the Controller or the Res Man software does not see the module), the SYSFAIL- line will continue to be driven. Should this happen, turn the chassis power off, make certain the DRM is properly installed in the chassis, and turn the chassis power back on.

Should the DRM continue to fail, perform the following or contact Customer Support for assistance.

1. Install the instrument driver (see next section).
2. Run the Soft Front Panel program and select **Instrument** > **Self Test**

Should the Soft Front Panel self-test continue to fail, contact Customer Support for assistance. Customer Support contact information is included in the front section of this manual before the Table of Contents.

Software Installation

The DRM is shipped with a VXI*plug&play* Instrument Driver.

VXI*plug&play* Instrument Driver

The DRM instrument driver links the communication interface and an application development environment (ADE). It provides a higher level, more abstract view of the instrument. It also provides ADE-specific information that supports the capabilities of the ADE, such as a graphical representation.

Some of the ADEs that this driver supports are listed below:

- Agilent Technologies Agilent VEE
- Astronics Test Systems PAWS
- Microsoft Visual Studio (Visual Basic, C, Visual C++, Visual C#)
- National Instruments LabVIEW
- National Instruments LabWindows/CVI

Included with the instrument driver is the Soft Front Panel (SFP) software. The soft front panel is a graphical user interface for the DRM. It can be used to verify communications and to debug applications during development and integration.

The DRM VXI*plug&play* Instrument Driver uses the VISA communication library to operate the instrument. The VISA library is typically provided by the manufacturer of the VXI Slot 0 device. Contact your Slot 0 device manufacturer if you do not have the VISA library installed on your system.

Installing the Instrument Driver

1. Insert the included documentation CD into your computer's CD/DVD drive.
2. There are two versions of the driver installer on the CD, one with the Run-Time Engine (RTE) and one without.
   - The installer with the RTE is in the **Driver with RTE** folder.
   - The installer without the RTE is in the **Driver without RTE** folder.
3. Double-click the **setup.exe** file.
4. Follow the setup directions.

After the instrument driver is installed, the DRM soft front panel will be launched.

The following files are installed from the CD:

- ANSI C source code for the Instrument Driver and Soft Front Panel, i.e., .c and .h files.
- MS Windows 32 bit DLL library, i.e., tat964_32.dll and tat964.def files.
- Microsoft 32 bit DLL import library, i.e., tat964.lib file.
- Function panel file, i.e., tat964.fp file.
- MS Visual Basic Function Declaration text file, i.e., tat964.bas file.
- Windows help file, i.e., tat964.chm file.

Visit the Astronics Test Systems website at **http://www.astronicstestsystems.com/support/downloads** to check for updated DRM driver or firmware updates.

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Chapter 3
DRM Front Panel

The DRM front panel provides the hardware interface to the unit under test (UUT). Figures 3-1 and 3-2 illustrate the front panel and its connectors.

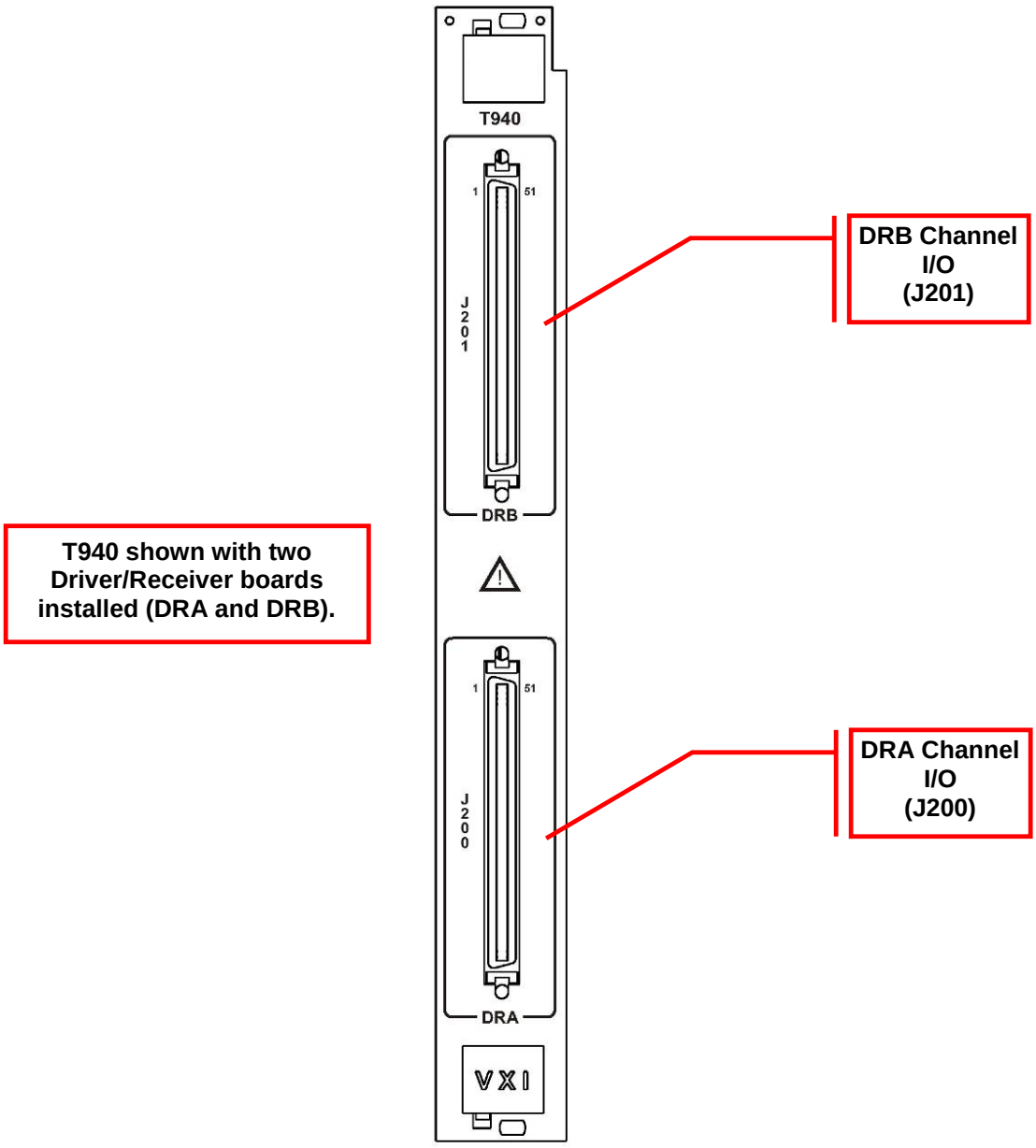


Figure 3-1: T940 Front Panel (Appearance Typical)

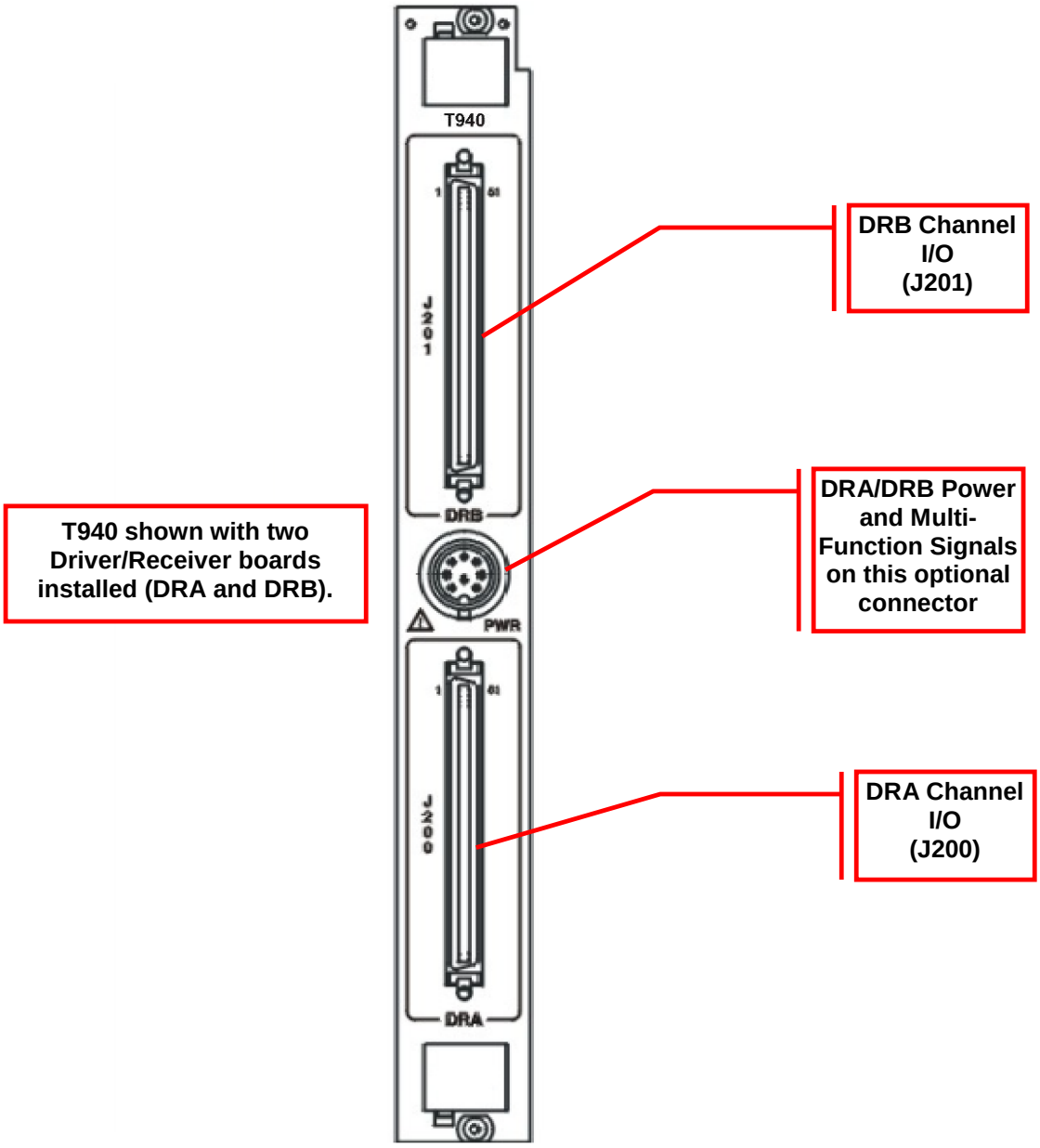


Figure 3-2: T940 Front Panel (Showing Optional Front Power Connector)

J200 and J201 DRA Channel I/O

The J200 and J201 connectors' pinouts depend on the Driver/Receiver (DR) boards that are installed. Refer to the Appendix of the specific DR board for connector interface information.

PWR Connector – DRA/DRB Power and Signals

The PWR connector is an option on the T940 which is used to supply external power to DR3e Driver/Receiver boards and can be used to supply

multi-function signals (MFSIG) and grounds to all boards.



Figure 3-3: PWR Connector

Table 3-1: PWR Connector Pinout

Connector	Name	Connector	Name
1	DRB V+	5	DRB V-
2	DRB MFSIG	6	DRA MFSIG
3	DRA V+	7	DRA GND
4	DRB GND	8	DRA V-

Front Panel Connectors

Table 3-2 lists the manufacturer's part numbers and the Astronics Test Systems ordering numbers for the DRM mating connectors. Table 3-3 lists the part and ordering numbers for the DRM cable assemblies.

Table 3-2: Mating Connector Part Numbers

Connector	Manufacturer & Part Number	ATS Order Number
J200-J201 (mate)	3M 101A0-6000EC	40892
J200-J201 (flat cable backshell for the above)	3M 103A0-12R1-00	Included with 40892
PWR	Amphenol T3505 001	408091

Table 3-3: Cable Assembly Part Numbers

Description	ATS Order Number
T940 coaxial cable, 17 positions, both ends IDC-terminated.	602715-XXX
Front Panel Signal Flat Shielded Cable (1 per DRA or DRB)	408122-XXX
Front Panel Signal Flat Ribbon Cable (1 per DRA or DRB)	408123-XXX
Front Panel Power Cable (1 per DRM)	408091-XXX

Note:

1. *XXX denotes the length in feet (i.e., 408123-006 would indicate a six-foot*

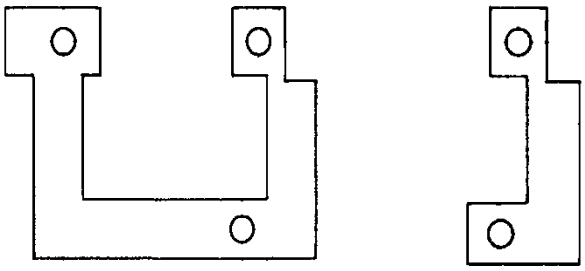
J200/J201 flat ribbon mating cable.

2. *DRM cable assemblies are open at one end.*

Front Panel LBUS Lockout Keys

The VXIbus-defined LBUS Lockout Keys are designed to prevent adjacent VXI Modules with incompatible logic families from connecting to the Local Bus. They are attached to the exterior of the module at the top of the front panel.

Figure 3-4 illustrates the two types of LBUS Lockout Keys used for this product. Figure 3-5 shows the application of Lockout Keys for the T964.



A/C-type **C-type**

Figure 3-4: LBUS Lockout Keys

The LBUS Lockout Key is fitted to all modules. The T964 requires the use of the A/C-type LBUS Lockout Key (PN 455540) on all modules. The T940 may use the C-type key (PN 455541) for the leftmost module as long as the jumper block for the module is **NOT** in the Primary position (and it shouldn't be if it's the leftmost T940 DRM).

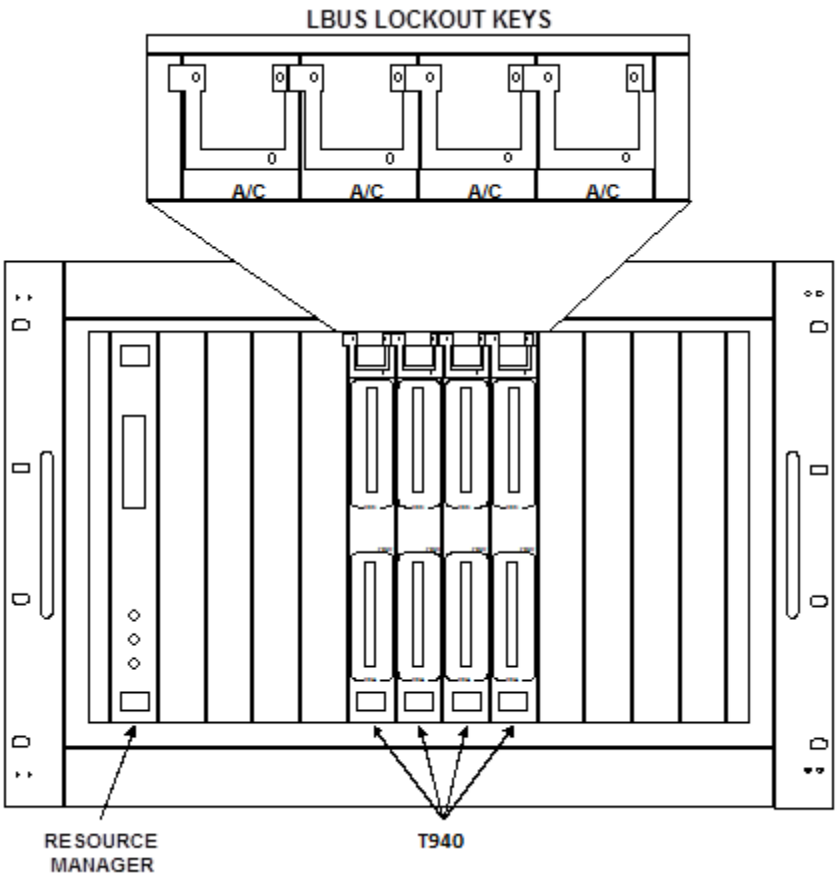


Figure 3-5: LBUS Lockout Configuration

LBUS Lockout Key Installation

In order to accommodate the VXIbus specification's defined minimum thickness of the lockout key and the clearance provided around the module ejector handle, two LBUS lockout keys must be fitted on top of each other for each module.

To install lockout keys to the module:

1. Set the module ejector handle to the un-ejected position.
2. The first key may be pushed around the ejector handle and aligned with the front panel screw holes. This takes up most of the clearance under the ejector handle, preventing the second lockout key from being installed.

   To provide the necessary clearance, move the first lockout key away from the module body, and slide the second key underneath the first key and around the ejector handle.

To secure the lockout keys to the module:

1. Align the lockout keys screw holes with the holes in the module front panel.

2. Install two screws in the holes at the top of the module front panel and tighten the screws.
3. Move the ejector handle to the ejected position, and install a third screw in the hole now made accessible.

Chapter 4
Functional Description

This section describes the DRM hardware block diagrams.

For information about DRM address maps and register descriptions, contact your local sales representative or contact Sales Support at atsinfo@astronics.com.

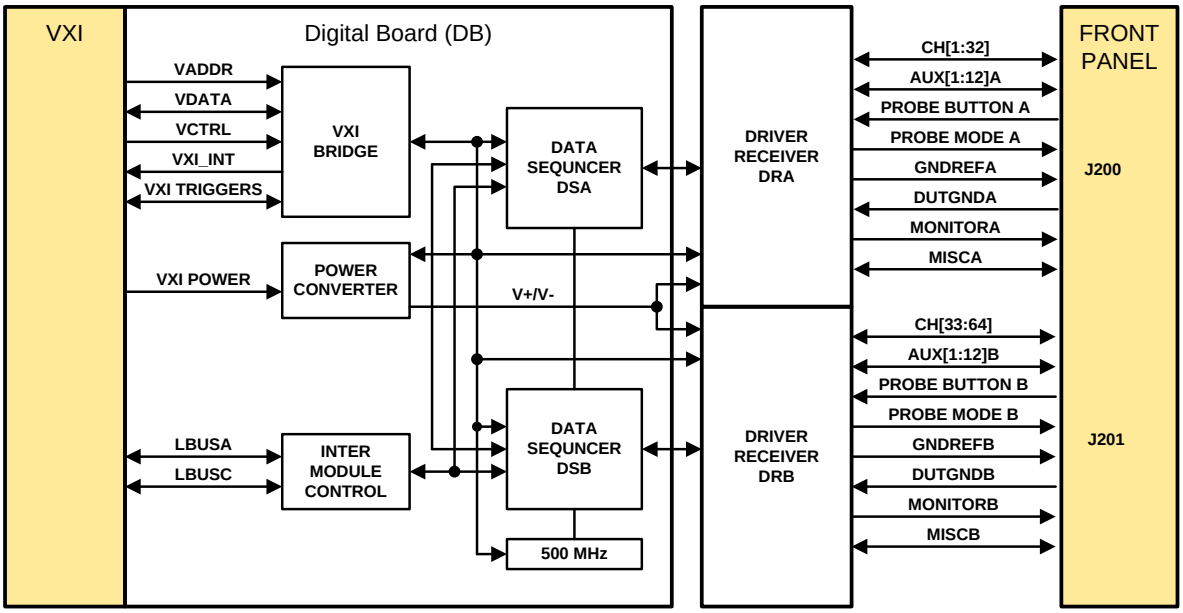


Figure 4-1: T940 DRM Block Diagram

The following sections describe each component in detail.

Digital Board (DB)

The digital board contains the digital engine of the DRM and the logic to program and group two or more as a digital subsystem.

VXI Bridge

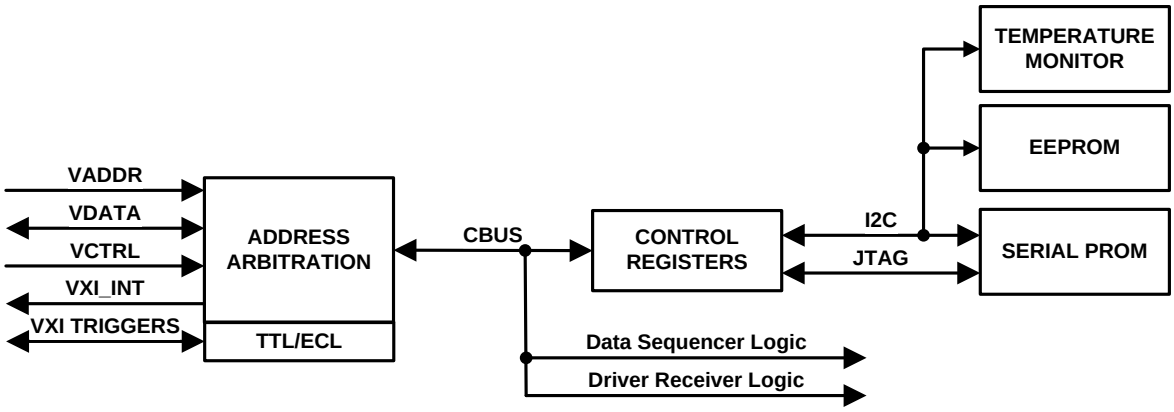


Figure 4-2: T940 VXI Bridge Block Diagram

Terms Used in this Section

VADDR	(VXI Address Bus) The 32 bit backplane address bus
VDATA	(VXI Data Bus) The 32 bit backplane data bus
VCTRL	(VXI Control Bus) The backplane control bus
VXI_INT	(VXI Interrupt Signals) The backplane interrupt signals
VXI TRIGGERS	(TTLTRG[0:7], ECLTRG[0,1]) The backplane trigger signals.
CBUS	An internal control bus connecting the arbitration logic to the Data Sequencers and the Driver/Receiver board's Control Logic
JTAG	(Joint Test Action Group, IEEE 1149.1) Serial interface that allows the serial PROM to be reloaded for in-field system upgrades
I2C	(Inter-Integrated Circuit) Multi master serial interface that allows communication to the temperature monitor and EEPROM

Description

The main purpose of the VXI Bridge is to provide a communication interface between the VXI backplane and the hardware resources.

Power Converter

The PC converts backplane voltages into digital bias voltages V+ and V- for front end types DR3E, DR9 and UR14. Its protection circuitry can detect faults in any of the four on-board power supplies, status of the input fuses, or a high input current or overcurrent condition. There are three types of power converters, each of which has seven voltage ranges.

Front end features of the DR3E, DR9 and UR14 have headroom requirements to the V+ and V- bias voltages. Refer to the specific front end appendix for

headroom requirements and specifications for each power converter range.

Type 1 and Type 3

The type 1 power converter is designed for use in a VXI 3.0 chassis and the type 3 power converter is designed for a VXI 4.0 chassis and utilizes the additional power pins and can supply more current. Installing a type 3 power converter in a VXI 3.0 chassis is allowed but it is up to the user to limit the number of active channels to prevent damage to the chassis.

Table 4-1: Power Converter Type 1 and Type 3 Ranges

Range	V+ Nominal Voltage	V- Nominal Voltage
-12 to +12	+16V	-15.6V
-15 to +5	+9.6V	-19.2V
-10 to +10	+16V	-14.1V
-5 to +7	+12V	-9.6V
-5 to +15	+19.2V	-9.6V
0 to +22	+28.8V	-4.5V
-2 to +20	+26.4V	-6V

Type 4

The type 4 power converter has a reduced voltage range and better power distribution of the VXI backplane supplies.

Table 4-2: Power Converter Type 004 Ranges

Range	V+ Nominal Voltage	V- Nominal Voltage
-7 to +7	+14.4V	-11.7V
-15 to +2	+9.6V	-18.9V
-10 to +9	+16.8V	-14.1V
-3 to +7	+14.4V	-7.2V
-5 to +5	+14.4V	-9.6V
0 to +16	+24V	-4.5V
-2 to +14	+21.6V	-6V

Inter-Module Control

The T940 inter-module configuration is determined by jumpers and the primary to terminator order is right to left. The following sections describe the T940 inter-module implementation.

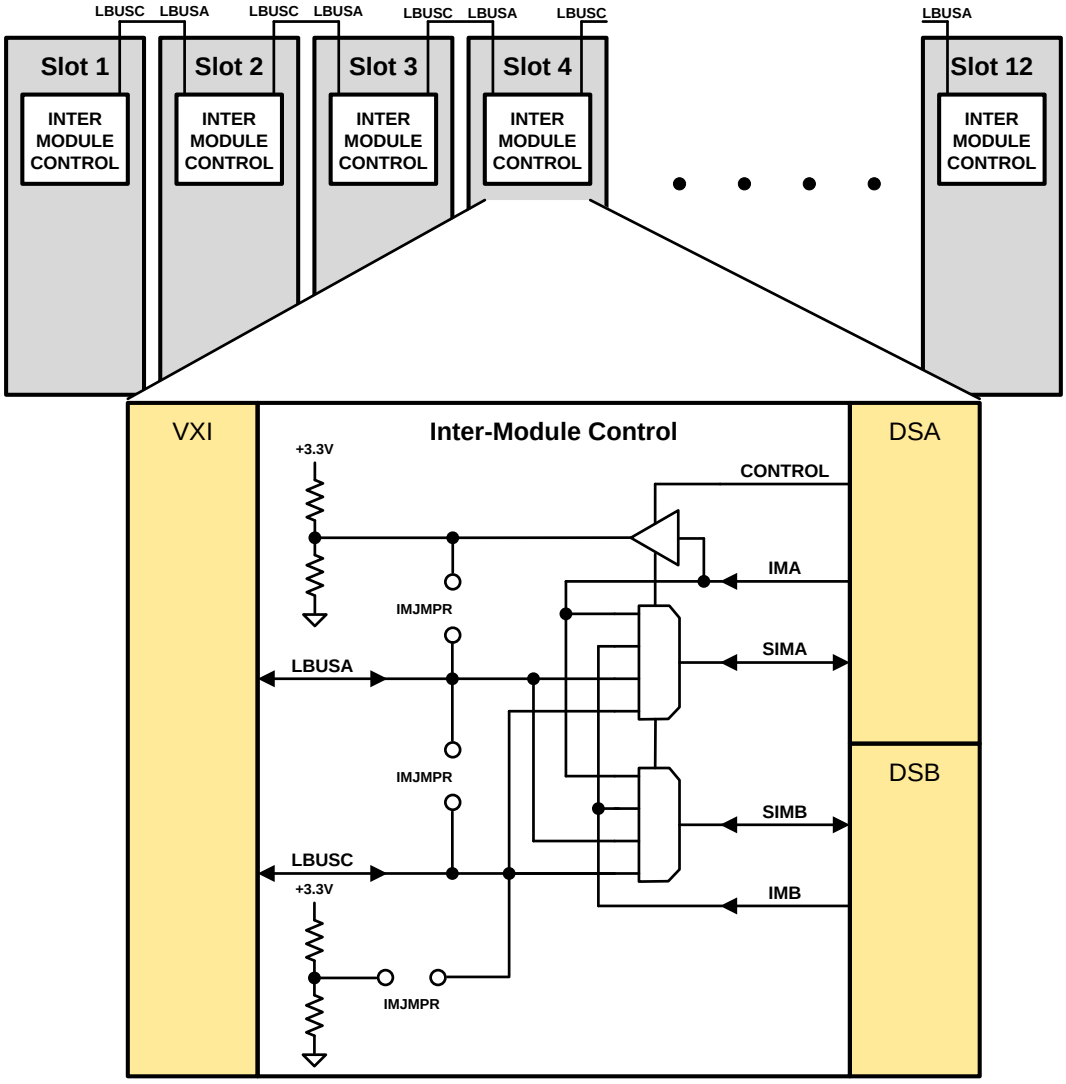


Figure 4-3: T940 Inter-Module Control Block Diagram

Terms Used in this Section

DRM	(Digital Resource Module) A DRM is a single T940 module. A DRM is comprised of a Digital Board (DB) and one or two Driver/Receiver boards (DRA and DRB)
DRS	(Digital Resource Suite) A DRS is two or more adjacent DRMs synchronized together to form a digital test system with more than 64 channels.
DRA	Driver/Receiver A
DRB	Driver/Receiver B
DSA	Data Sequencer A
DSB	Data Sequencer B
Coupled	Used to describe a DRM sequencer that is included in a DRS chain.

Linked	Used to describe two sequencers (DSA and DSB) on the same DRM that are synchronized together.
Primary	Used to describe the DRM that provides all the timing for the sequencers that are part of the DRS chain. DSA is always coupled to the DRS chain and is the source of the timing and control. DSB can be coupled to the new chain or run independently from the chain. The primary module must be located in the right most slot position in the VXI chassis relative to the DRMs that will be coupled.
Secondary	Used to describe the DRMs located between the primary and terminator module that pass the timing signals to the DRM in the next lower slot position. Individual sequencers can be coupled to the DRS or run independently from the primary module as linked or not linked.
Terminator	Used to describe the DRM in the left most position of the DRS chain. Individual sequencers can be coupled to the DRS or run independently from the primary module as linked or not linked.
LBUSA	VXI Local Bus A, used to connect adjacent modules.
LBUSC	VXI Local Bus C, used to connect adjacent modules.
CONTROL	Control signals used to set relay, driver and mux settings.
IMA	Inter-Module signals from DSA.
SIMA	Selected Inter-Module signal used by DSA.
IMB	Inter-Module signals from DSB.
SIMB	Selected Inter-Module signal used by DSB.
IMJMPR	T940 inter-module jumper. This jumper sets the DRS mode as primary, secondary or terminator.

Note: *Refer to* **DRS Inter-Module Mode Control** *in* **Chapter 2, Installation** *for information on the Inter-Module Control jumper settings.*

Description

The DRM utilizes the following VXI backplane resources to enable adjacent DRMs to be synchronized together to form a DRS:

- VXI Local Bus A/C (LBUSA/LBUSC) – Sequencer A on the primary module drives all twelve LBUSA signals (Phases, Windows, Clocks and Jump Flag). Both Sequencers can receive LBUSA and LBUSC signals.
- VXI Triggers – Used for passing information between the DRS modules (e.g. error flag, synchronization flag, reset signal, driver disable signal, channel handshake)

T940 Inter-Module Mode Settings

The VXI*plug&play* API function that sets the inter-module mode is “tat964_setModuleInterconnect”. The valid settings with reference to figure 4-3 are:

Primary DRM Inter-Module Modes: These modes apply to a DRM that is jumpered as a Primary.

- Independent Not Linked – SIMA set to IMA and SIMB set to IMB. IMJMPR position is a don't care. Primary driver disabled. The DRM is not coupled to a DRS. DSA and DSB are not linked.
- Independent Linked – SIMA and SIMB set to IMA. IMJMPR position is a don't care. Primary driver disabled. The DRM is not coupled to a DRS. DSA and DSB are linked.
- Primary DSA Coupled – SIMA set to LBUSA, SIMB set to IMB. IMJMPR position set to primary (LBUSA connected to termination). Primary driver enabled. The DRM is coupled to a DRS. DSA is coupled to a DRS. DSB is independent.
- Primary DSA and DSB Coupled – SIMA and SIMB set to LBUSA. . IMJMPR position set to primary (LBUSA connected to termination). Primary driver enabled. The DRM is coupled to a DRS. DSA and DSB are coupled to a DRS.

Secondary DRM Inter-Module Modes: These modes apply to a DRM that is jumpered as a Secondary.

- Independent Not Linked – SIMA set to IMA and SIMB set to IMB. IMJMPR position is a don't care. Primary driver disabled. The DRM is not coupled to a DRS. DSA and DSB are not linked.
- Independent Linked – SIMA and SIMB set to IMA. IMJMPR position is a don't care. Primary driver disabled. The DRM is not coupled to a DRS. DSA and DSB are linked.
- Secondary Not Linked – SIMA set to IMA and SIMB set to IMB. IMJMPR position set to secondary (LBUSA connected to LBUSC). Primary driver disabled. The DRM is coupled to a DRS. DSA and DSB are not linked and independent.
- Secondary Linked – SIMA and SIMB set to IMA. IMJMPR position set to secondary (LBUSA connected to LBUSC). Primary driver disabled. The DRM is coupled to a DRS. DSA and DSB are linked and independent.
- Secondary DSA Coupled – SIMA set to LBUSC and SIMB set to IMB. IMJMPR position set to secondary (LBUSA connected to LBUSC). Primary driver disabled. DSA is coupled to a DRS. DSB is independent.
- Secondary DSB Coupled – SIMA set to IMA and SIMB set to LBUSC. IMJMPR position set to secondary (LBUSA connected to LBUSC). Primary driver disabled. DSB is coupled to a DRS. DSA is independent.
- Secondary DSA and DSB Coupled – SIMA and SIMB set to LBUSC. IMJMPR position set to secondary (LBUSA connected to LBUSC). Primary driver disabled. DSA and DSB are coupled to a DRS.

Terminator DRM Inter-Module Modes: The following modes apply to a DRM that is jumpered as a Terminator.

- Independent Not Linked – SIMA set to IMA and SIMB set to IMB. IMJMPR

position is a don't care. Primary driver disabled. The DRM is not coupled to a DRS. DSA and DSB are not linked.

- Independent Linked – SIMA and SIMB set to IMA. IMJMPR position is a don't care. Primary driver disabled. The DRM is not coupled to a DRS. DSA and DSB are linked and independent.
- Terminator Not Linked – SIMA set to IMA and SIMB set to IMB. IMJMPR position set to terminator (LBUSC connected to termination). Primary driver disabled. The DRM is coupled to a DRS. DSA and DSB are not linked and independent.
- Terminator Linked – SIMA and SIMB set to IMA. IMJMPR position set to terminator (LBUSC connected to termination). Primary driver disabled. The DRM is coupled to a DRS. DSA and DSB are linked.
- Terminator DSA Coupled – SIMA set to LBUSC and SIMB set to IMB. IMJMPR position set to terminator (LBUSC connected to termination). Primary driver disabled. DSA is coupled to a DRS. DSB is independent.
- Terminator DSB Coupled – SIMA set to IMA and SIMB set to LBUSC. IMJMPR position set to terminator (LBUSC connected to termination). Primary driver disabled. DSB is coupled to a DRS. DSA is independent.
- Terminator DSA and DSB Coupled – SIMA and SIMB set to LBUSC. IMJMPR position set to terminator (LBUSC connected to termination). Primary driver disabled. DSA and DSB are coupled to a DRS.

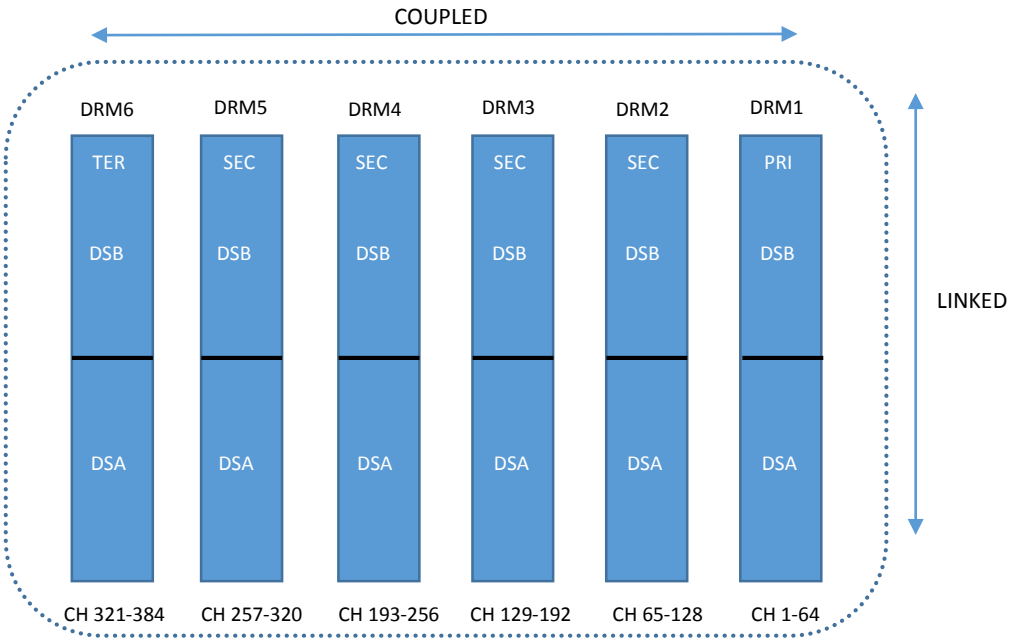
Examples

Each DRM in the following examples have 32 channels on DRA and 32 channels on DRB (e.g. DR3E).

Individual sequencers can be run independently even if they are intermixed within a module chain.

One Group of 384 Channels,

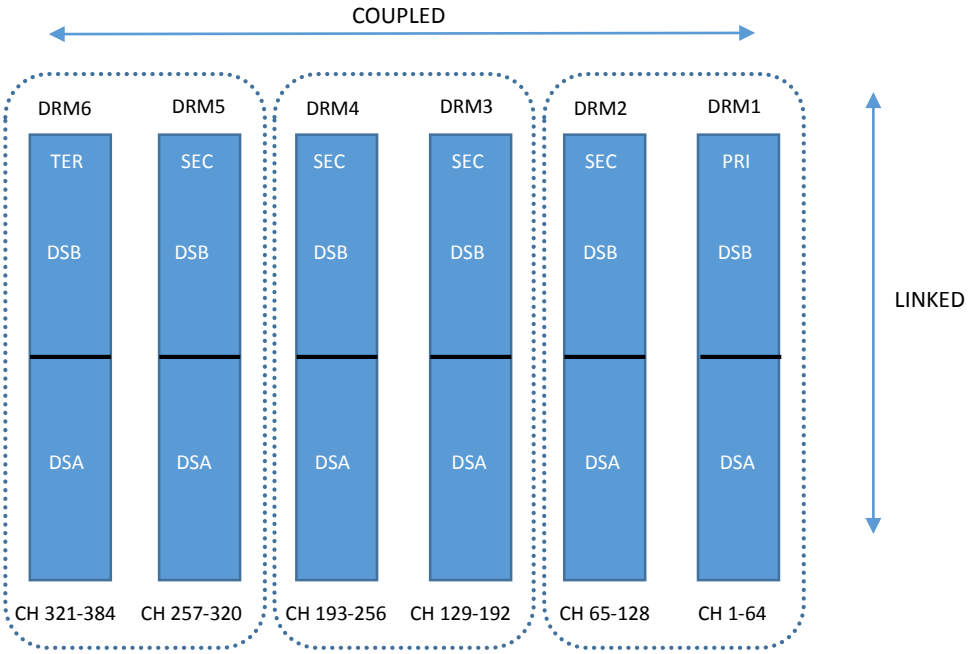
Module	T940 Inter-Module Mode
DRM1	Primary Linked
DRM2	Secondary DSA and DSB Coupled
DRM3	Secondary DSA and DSB Coupled
DRM4	Secondary DSA and DSB Coupled
DRM5	Secondary DSA and DSB Coupled
DRM6	Terminator Linked



In this example, all 12 sequencers, DSA and DSB on DRM1 through DRM6 are coupled to a single DRS (368 channels).

Three Groups of 128 Channels

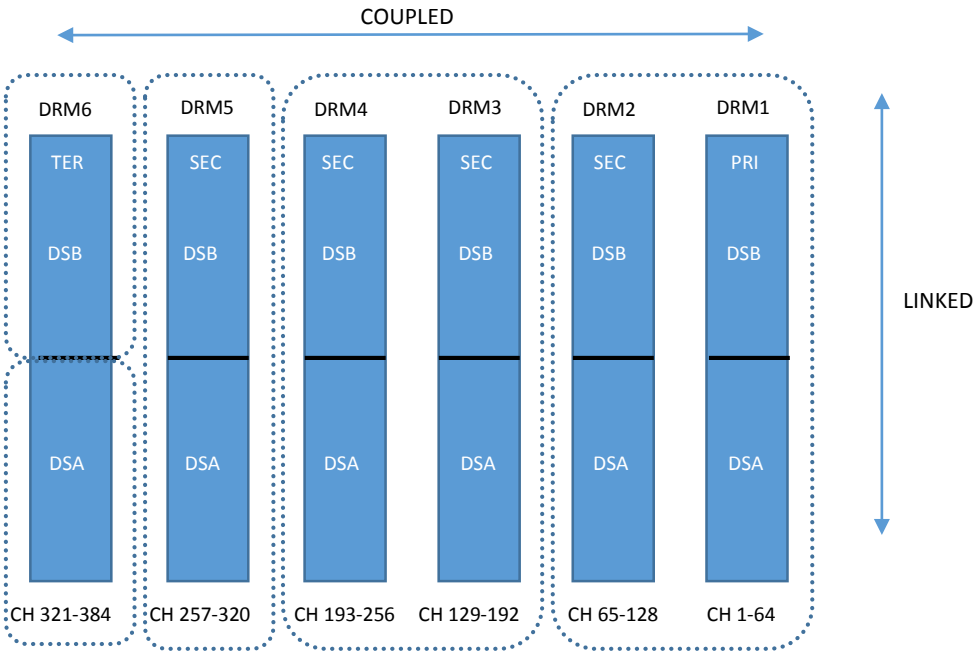
Module	T940 Configuration
M1	Primary Linked
M2	Terminator DSA and DSB Coupled
M3	Primary Linked
M4	Terminator DSA and DSB Coupled
M5	Primary Linked
M6	Terminator DSA and DSB Coupled



In this example, DSA and DSB on DRM1 and DRM2 are coupled to a DRS (128 channels). DSA and DSB on DRM3 and DRM4 are coupled to a second DRS (128 channels). DSA and DSB on DRM5 and DRM6 are coupled to a third DRS (128 channels).

Two Groups of 128 Channels, One Group of 64 Channels, and Two Groups of 32 Channels

Module	T940 Configuration
M1	Primary Linked
M2	Terminator DSA and DSB Coupled
M3	Primary Linked
M4	Terminator DSA and DSB Coupled
M5	Secondary Linked
M6	Terminator Not Linked



In this example, DSA and DSB on DRM1 and DRM2 are coupled to a DRS (128 channels), DSA and DSB on DRM3 and DRM4 are coupled to a second DRS (128 channels), DSA and DSB on DRM5 are linked and running independent of a DRS (64 channels). DSA and DSB on DRM6 are not linked and running independent of a DRS (two groups of 32 channels each).

Data Sequencer

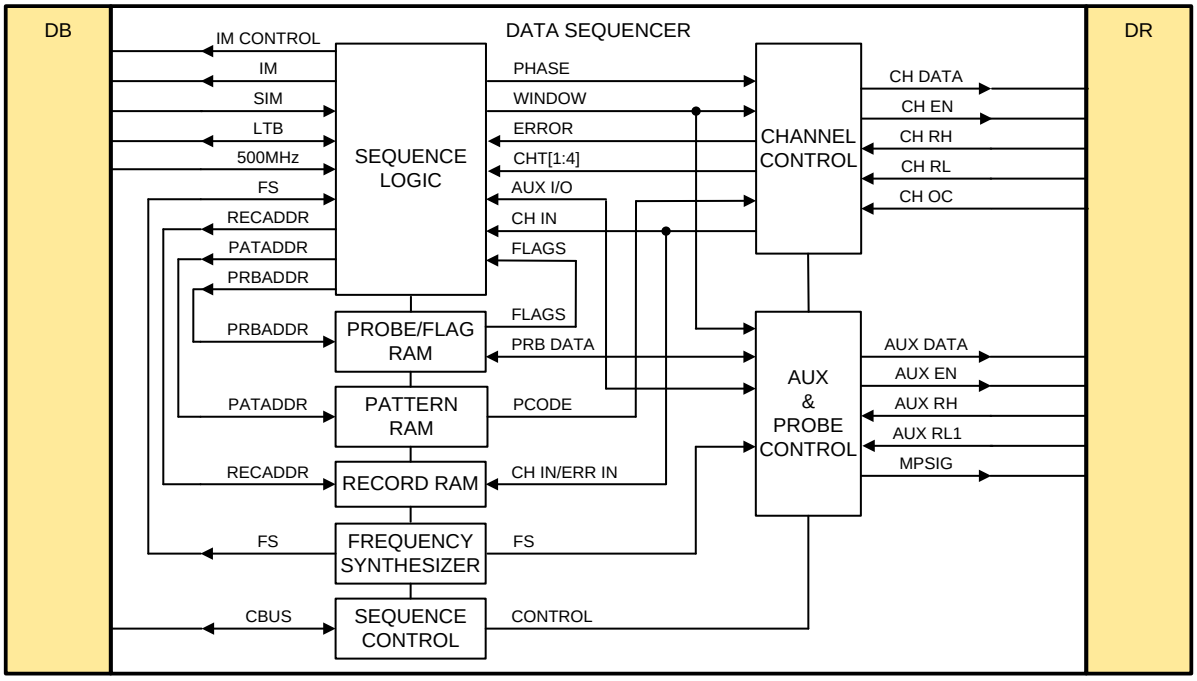


Figure 4-4: Data Sequencer Block Diagram

Terms Used in this Section

250 MHz	250 MHz clock derived from the 500 MHz clock.
500 MHz	500 MHz oscillator clock.
AUX DATA	AUX output data value.
AUX EN	AUX output enable value.
AUX I/O	AUX output and enable signals as well as the AUX input and probe data.
AUX RH	AUX input response high comparator result.
AUX RL1	AUX input response low comparator result.
BERREN	(Burst Error Enable). This flag allows the user to designate which patterns will be examined for Burst Error, Burst Error counting and the logging of errors in the Error Address Memory BERREN is a qualifier for the burst error and burst error count.
CBUS	An internal control bus connecting the arbitration and trigger logic on the VXI Bridge to the Data Sequencer.
CH DATA	Channel output data value.
CH EN	Channel output enable value.
CH IN	Channel input data which is the response data.
CH IN/ERR IN	Channel input data which is either the response data or the input pattern code test result.
CH OC	Channel output over current flag.
CH RH	Channel input response high comparator result.
CH RH	Channel input response low comparator result.
CONDEN	(Condition Enable) A qualifier for conditional jumping on error.
CONTROL	Control signals and registers to program the data sequence settings/memory.
ERROR	Signal that indicates an input pattern code failed.
FLAGS	BERREN and CONDEN flags.
FS	Frequency Synthesizer Clock.
HALT	Sequence trigger used to stop the sequence controller for single stepping applications.
IM CONTROL	Signals used to set relay, driver and mux settings.
IM	Inter-Module signals.
IMSEQ	Inter-module sequence Controller signals that can be assigned to the VXI or LTB for DRS coupling. Error Pass Valid Sequence Reset DRS Sync Driver Disable Master Reset
JUMP	Sequence trigger used conditional jumping.

LTB	Linked Trigger Bus signals connecting DSA to DSB.
MCLK	Master Clock
MPSIG	Multipurpose signal output.
PAT DEL[1:2]	Pattern delay timers.
PAT TO	Pattern timeout timer.
PATADDR	Pattern address used by the external pattern RAM.
PAUSE	Sequence trigger used to stop the timing generator for handshaking applications.
PCODE	Pattern code contains the input and output instructions.
PG	Pulse Generator output.
PHASE	Four output timing signals.
PRB DATA	The probe expect and probe result data.
PRBADDR	Probe/flag address used by the external RAM.
RECADDR	Record address used by the external record RAM.
RESUME	Sequence trigger used to resume a paused timing generator for handshaking applications.
SEQ	Sequence Controller signals that can be assigned to the VXI or LTB. Probe Button Sequence Flag 1 Sequence Flag 2 Idle Active Sequence Active
SEQ CLK	Sequence Clock.
SEQ JUMP	Signal that a valid jump event is true.
SET TO	Sequence timeout timer.
SEQ REC	Signals from the sequence controller that programs the record control logic.
SEQ TRIG	Sequence trigger signals consisting of the following: Pause Trigger 1 Pause Trigger 1 Resume Pause Trigger 2 Pause Trigger 2 Resume Phase 1 Resume Phase 2 Resume Phase 3 Resume Phase 4 Resume Execute Start Execute Stop Jump 1 Jump 2 Jump 3

	Jump 4
SIM	Selected Inter-Module signals.
START	Sequence trigger used to start the pattern controller.
STOP	Sequence trigger used to stop the pattern controller.
SYNC[1:2]	Programmable sync pulse signals.
TEST CODE	Selects the jump test event.
T0 CLK	Internal SEQ CLK generated by the sequence controller.
VA[0:3]	Vector address bits for vectored jumps.
VXI TRIGGERS	(TTLTRG[0:7], ECLTRG[0,1]) The backplane trigger signals.
VXICLK10	10 MHz VXI backplane clock.
WATCHDOG	Watchdog timer.
WINDOW	Four input timing signals. WINDOW4 is used by the probe logic.

Sequence Logic

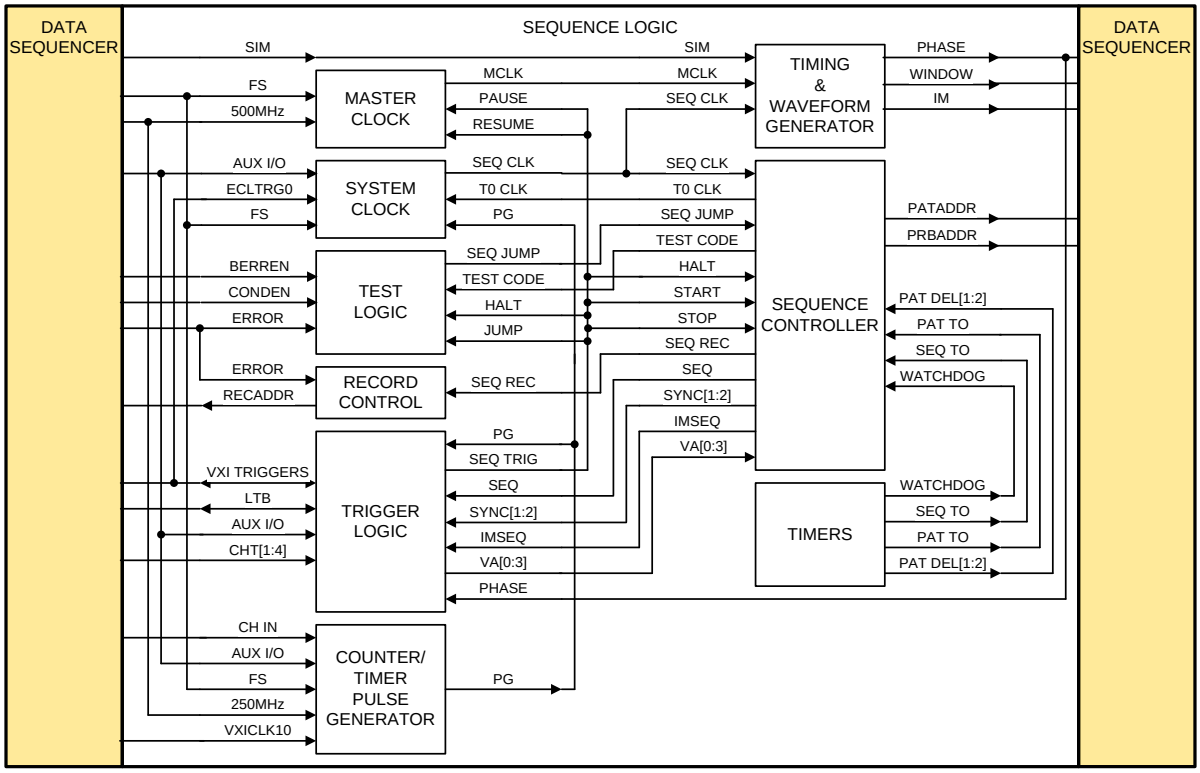


Figure 4-5: Sequencer Logic Block Diagram

Master Clock

This block selects the master clock signal used by the timing and waveform generator.

System Clock

This block selects the sequence clock signal used by the sequence controller.

Test Logic

This block determines if a valid conditional jump is enabled or not.

Record Control

This block generates the address for the Record RAM based on the Recording Mode. This block also contains the error address memory, record index memory and burst error counter.

Trigger Logic

This block takes in Channel Test signals, AUX inputs and VXI triggers and Linked Trigger bus inputs and uses them to enable jumps, start/stop the sequencer, pause the Master Clock or halt the sequence controller. Edge capture conditions that are to be cleared are also handled by this block.

Counter/Timer & Pulse Generator

The pulse generator can be used to generate triggers, system clock or as a AUX output signal.

The counter/timer can be used to measure frequency or time interval data from any channel or AUX input.

Sequence Controller

This block contains the Sequence RAM which defines the order in which Patterns will be output/input. As such, this block provides the addressing to the Pattern RAM and the Record RAM. The Sequence RAM also contains the T0CLK period, Jump Type, Jump Addresses, looping controls/loop counts, Jump codes, CPP and other control bits for: Pause Code/Pause Resume Options, Record Capture type, Waveform control and Phase Trigger Type along with 2 Sequence Flags that can be output. The **T940 Sequencer Operation Details** section of Chapter 8 provides detailed information on sequence operation.

Timers

This block contains the Watchdog, Sequence Timeout, Pattern Delay (2) and the Pattern Timeout Timers.

Probe/Flag RAM

The probe input code, probe results and CONDEN/BERREN data for each pattern is stored in this RAM.

Pattern RAM

The output code as well as the input code for every channel of each pattern is stored in the Pattern RAM.

Record RAM

This is where the individual channel results are stored. The channel results are either the pattern input compare result or raw response data based on RH or RL. The results can be stored in normal or indexed starting from address zero and expanded.

Frequency Synthesizer

The Frequency Synthesizer (FS) may be used in lieu of the 500 MHz oscillator as the master clock. The reference clock for the FS may be a built-in 20 MHz oscillator, VXICLK10, LCLK100/2 or any of the AUX inputs in the range of 5 to 80 MHz.

Sequence Control

This block contains the registers and logic used to program the data sequencer.

Channel Control

This block takes the output code from the pattern RAM, formats it and outputs it according to the phase timing (PHASE). The resultant drive (CH DATA) and enable (CH EN) signals go to the Driver/Receiver logic.

The response high (CH RH) and response low (CH RL) signals from the Receivers are examined, and then, based on the window timing (WINDOW), the response is analyzed with respect to the input code. The channel results are routed to the Record RAM. The cumulative Error signal goes to the Sequence Logic block so it can be used for Jumping, Halting and the Counting of Errors. Individual over-current (OC) signals from the Channel Drivers can also be processed by this block to disable the channel drivers if desired.

AUX & Probe Control

AUX control allows user and diagnostic signals to be input or output the AUX pins. The inputs go to the Sequence Logic block described above. There is also a Multi-purpose signal (MPSIG) which can be combined with other signals on the Driver/Receiver board and provided to the user on the power connector.

Probe expect data is received from the Probe/Flag RAM and result data is generated that is stored back into the Probe/Flag RAM.

Driver/Receiver

The DRM can accommodate two Driver/Receiver boards (named DRA or DRB for their mounted location). Each Driver/Receiver board contains unique driver/receiver circuitry and front panel connector pinouts that are described in an appendix dedicated to each specific Driver/Receiver type.

Chapter 5
Soft Front Panel Operation

The Soft Front Panel (SFP) is a stand-alone executable that can be used to program, query and run the DRM digital resource.

Regardless of the user's choice of programming path (VXI*plug&play* instrument driver, A24/A32 register-based access, or a combination of these) the following basic 7-step process is required to implement a DRM test program:

1. Open a communication link to the DRM module called a session.
2. Configure global hardware parameters.
3. Configure the available I/O channels.
4. Edit the Data Sequencers
    a. Program the timing sets to govern the I/O data transfers.
    b. Create the pattern sets and populate them as appropriate.
    c. Create the Waveforms and define
    d. Set sequence parameters
    e. Edit sequence steps
5. Execute the sequence.
6. Utilize status and post process functions to evaluate/analyze results.
7. Close the VXI DRM session.

The following sections describe the SFP operation as it pertains to the previous seven steps. Additionally, sections are included covering the instrument functions, self-test, calibration, and utility functions.

The relevant VXI*plug&play* instrument driver function(s) for each step are also listed. The program has a help menu for additional assistance.

SFP Basics

A single T940 is referred to as a Digital Resource Module (**DRM**). A single DRM can be programmed as two separate 32 channel instruments (Not Linked) or as a single 64 channel instrument (Linked).

Multiple DRMs can be coupled and synchronized as a Digital Resource Suite (**DRS**). Each 32 channel group in the DRM can be included in the DRS or it can be independent. Up to eight DRMs can be coupled.

The SFP is a DRM utility that can be used to debug or check out user configurations and programming.

When started, the SFP searches for all the installed DRMs in the VXI system. If more than one DRM is detected, a dialog box prompts the user to select the DRM to initialize. Each instance of the SFP opens a VXI session with a single DRM in the system. Once a single DRM is selected, a dialog box prompts the user if the DRM should be reset.

Resetting the DRM clears any previously programmed settings. Selecting **No** retains all the DRM structures and settings previously programmed.

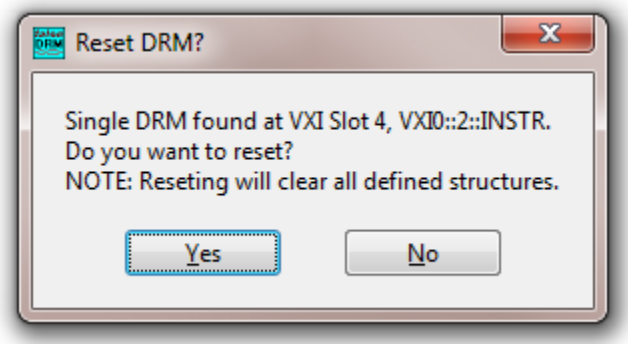


Figure 5-1: Reset Screen

The following warning will display if a DRM module with a type 3 power converter is installed in a VXI 3.0 chassis.

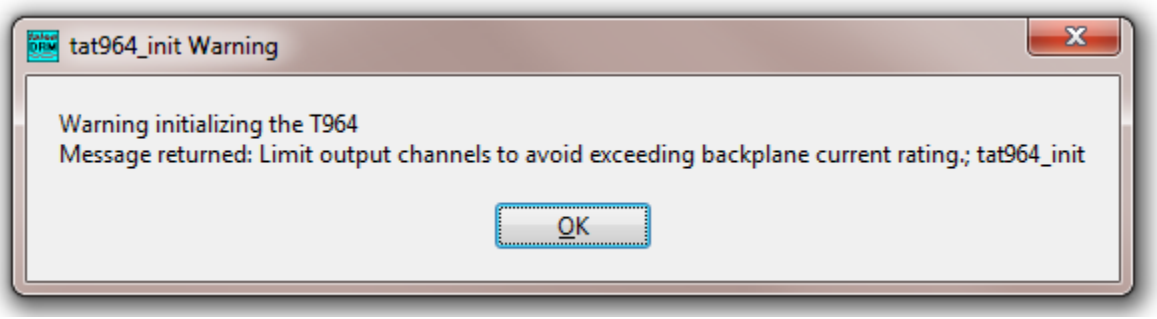


Figure 5-2: Initialize Warning

SFP Main Panel

After a VXI session has opened and the reset option selected, the main panel is displayed.

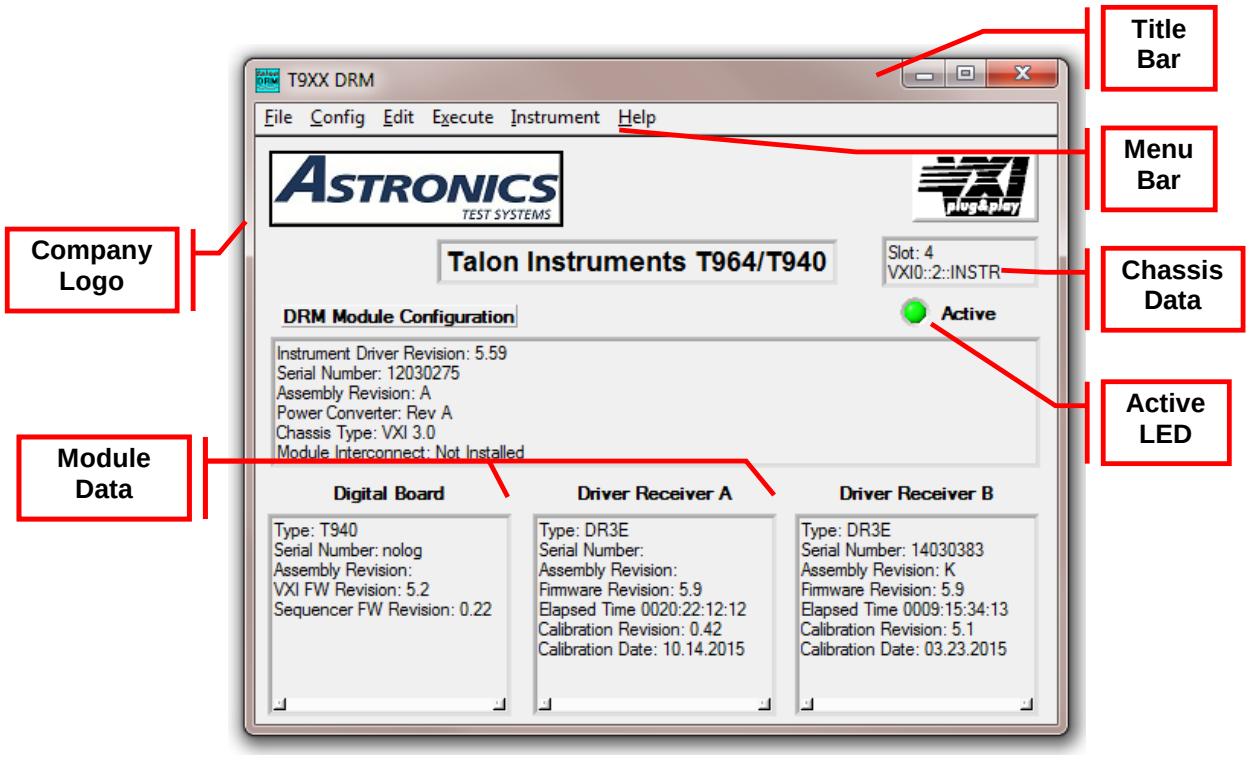


Figure 5-3: Main Panel

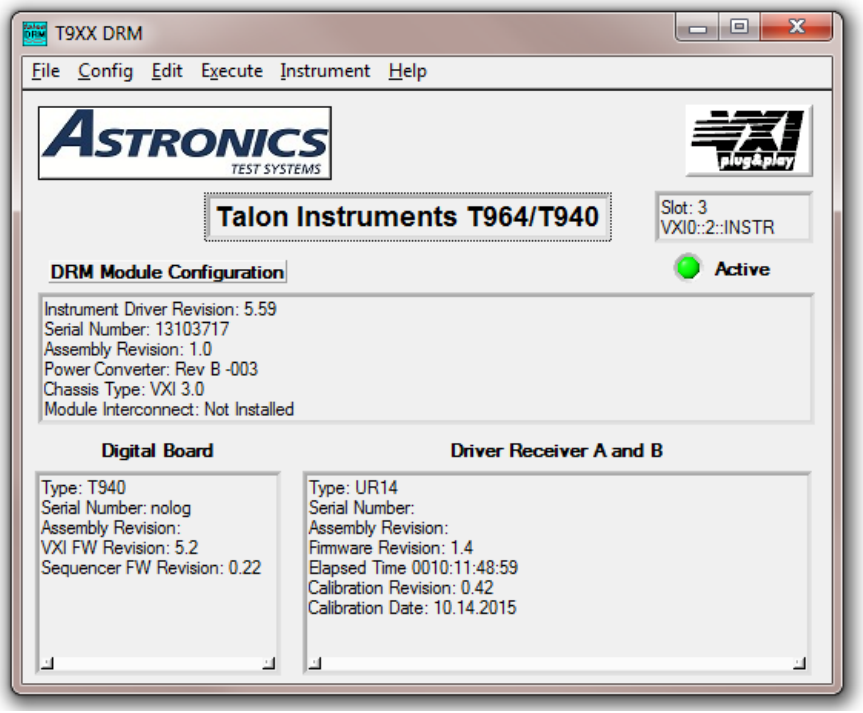


Figure 5-4: Main Panel UR14

The following sections describe the main panel controls and indicators.

Company Logo

Pressing this control displays the information panel.



Figure 5-5: Company Information Panel

Active LED

The Active LED indicates whether a VXI session has been established successfully.

Chassis Data

The chassis data control indicates the slot position and logical address of the DRM that the SFP is connected to.

Module Data

The module data is displayed in four separate controls. The module data is stored in non-volatile memory.

Title Bar

The title bar will display the current project file.

SFP Main Panel Menu Bar

The SFP main panel menu bar provides access to select, program and save the DRM hardware. Relevant VXI*plug&play* API functions are included with the menu options.

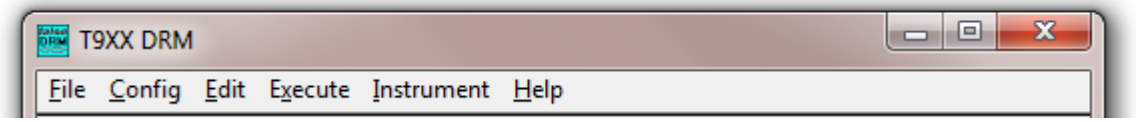


Figure 5-6: Menu Bar

File Menu

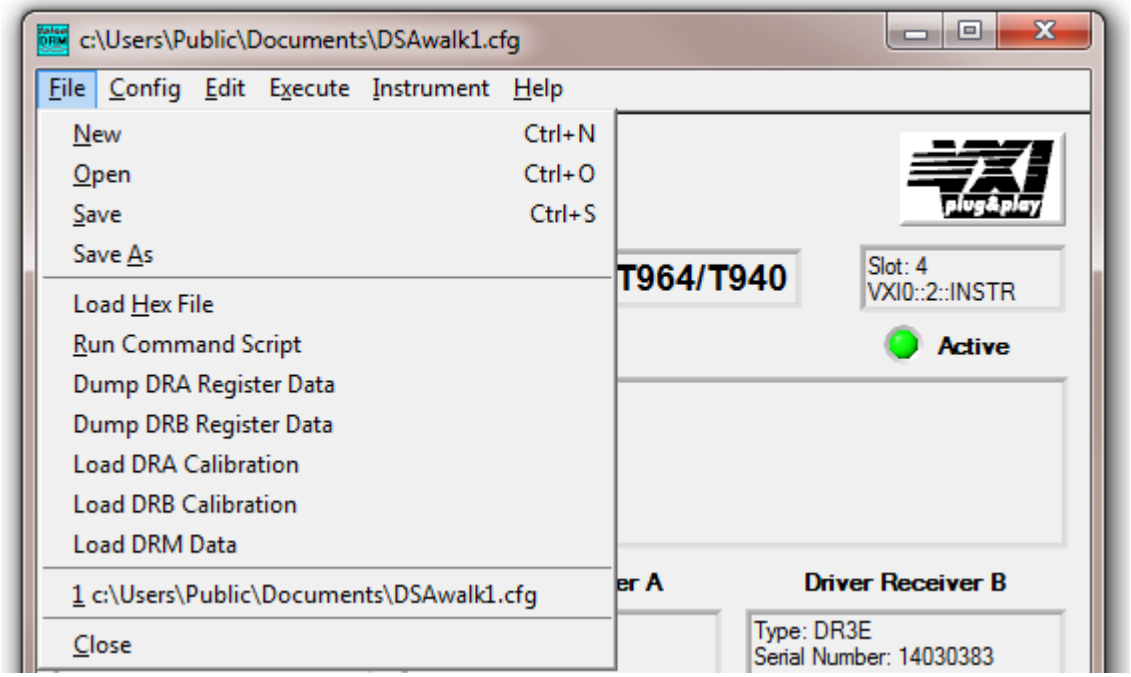


Figure 5-7: File Menu

The File Menu is used to manage the loading and saving of test files. With this menu, DRM SFP project files are created, loaded, saved and renamed. There are also diagnostic loads, register dumps and calibration data loads. A file history list permits quick reloading of recently accessed test files. The SFP can also be closed from this menu.

Table 5-1: File Menu Descriptions

Menu Option	Description
New	Clears the DRM hardware to power up reset settings [tat964_reset]
Open	Opens a file browser for choosing a configuration file. The chosen file is loaded and displayed on the title bar

Menu Option	Description
	and inserted in the history list [tat964_loadConfiguration]
Save	Updates the configuration file with the latest editing changes [tat964_saveConfiguration]
Save As	Creates a new configuration file with the latest editing changes. It then becomes the current configuration file [tat964_saveConfiguration]
Load Hex File	Low level utility routine for hardware checkout
Run Command Script	Low level utility routine for message based command checkout
Dump DRA Register Data	Saves the register contents of the DRA Pin Electronics devices to an ASCII file
Dump DRB Register Data	Saves the register contents of the DRB Pin Electronics devices to an ASCII file
Load DRA Calibration	Loads calibration data for the DRA Driver/Receiver board [tat964_loadCalibrationFile]
Load DRB Calibration	Loads calibration data for the DRB Driver/Receiver board [tat964_loadCalibrationFile]
Load DRM Data	Loads the DRM data [tat964_loadDrmFile]
Close	Closes the DRM session and exits the SFP [tat964_close]

Config Menu

The Configuration (Config) Menu is used to configure the DRM hardware.

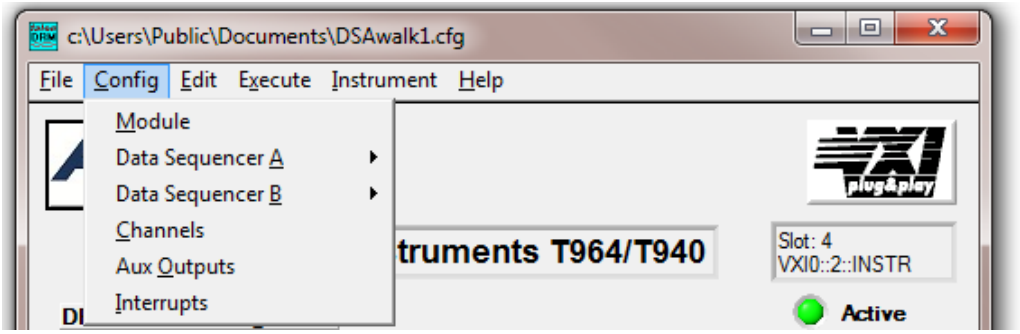


Figure 5-8: Config Menu

Table 5-2: Config Menu Descriptions

Menu Option	Description
Module	Displays the panel for programming module parameters
Data Sequencer A	Displays the panel for programming DSA parameters
Data Sequencer B	Displays the panel for programming DSB parameters
Channels	Displays the panel for programming channel parameters

AUX Outputs	Displays the panel for programming auxiliary output parameters
Interrupts	Displays the panel for programming the interrupt parameters

Edit Menu

The Edit Menu is used to create, program and modify timing sets, pattern sets and sequences.

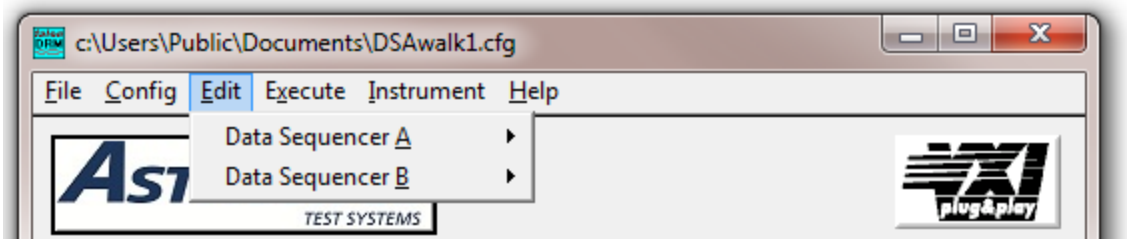


Figure 5-9: Edit Menu

Table 5-3: Edit Menu Descriptions

Menu Option	Description
Data Sequencer A	Displays the panels for programming DSA timing sets, patterns, sequence parameters, and sequence steps
Data Sequencer B	Displays the panels for programming DSB timing sets, patterns, sequence parameters, and sequence steps

Execute Menu

The Execute Menu is used to program the run option and run the sequences.

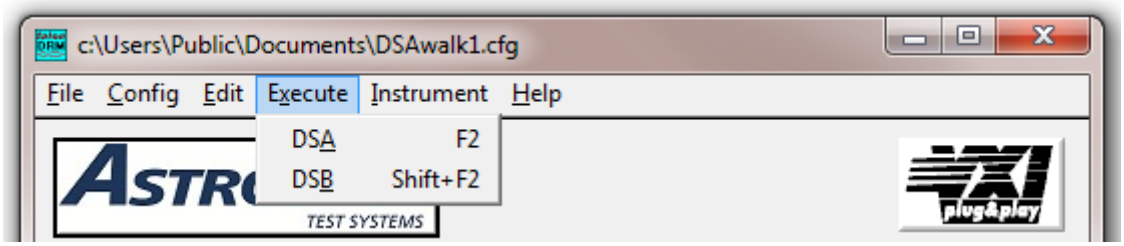


Figure 5-10: Execute Menu

Table 5-4: Execute Menu Descriptions

Menu Option	Description
DSA	Displays the execution panel for DSA
DSB	Displays the execution panel for DSB

Instrument Menu

The Instrument Menu is used to run self-test, calibration and monitor routines on the DRM hardware.

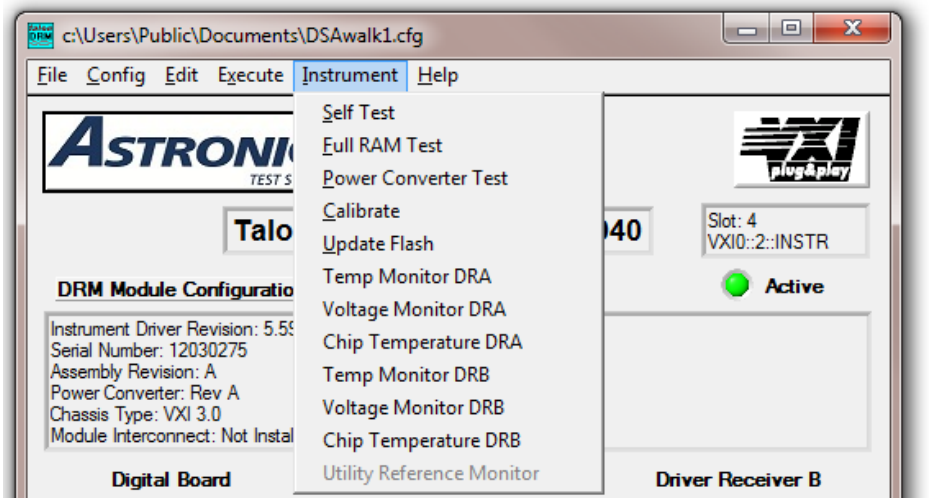


Figure 5-11: Instrument Menu

Table 5-5: Instrument Menu Descriptions

Menu Option	Description
Self-Test	Runs the self-test
Full RAM Test	Runs the full RAM test
Calibrate	Displays the calibration panel
Update Flash	Displays a file select dialog to select the Flash update file
Temp Monitor	Displays the temperature monitor panel
Voltage Monitor	Displays the voltage monitor panel
Chip Temperature	Displays the chip temperature panel

Help Menu

The Help Menu is used to open the instrument driver help contents and display the SFP programming information panel.

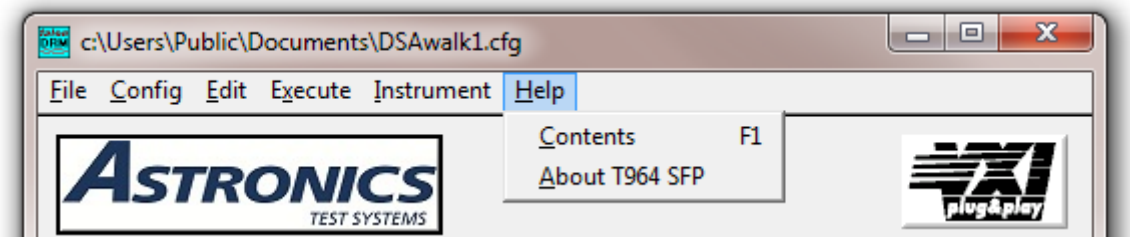


Figure 5-12: Help Menu

Table 5-6: Help Menu Descriptions

Menu Option	Description
Contents	Displays the VXIPNP API help file table of contents
About DRM	Displays revision data for the DRM Soft Front Panel executable

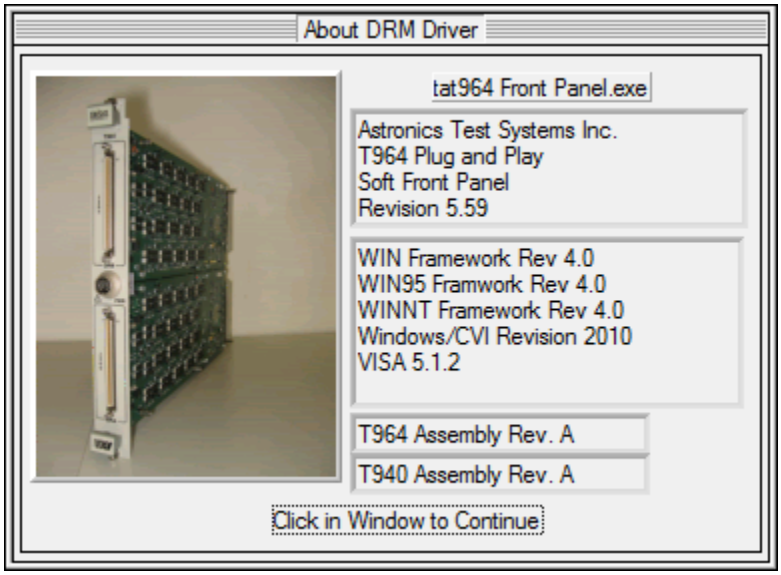


Figure 5-13: About DRM Driver Screen

Opening a VXI DRM Session

Starting the SFP initiates a search for all DRMs using the VISA library. Once all the DRMs have been identified, a selector panel will display (only if more than one DRM is found). Selecting one of the modules opens a VXI session with that module and then displays the main panel.

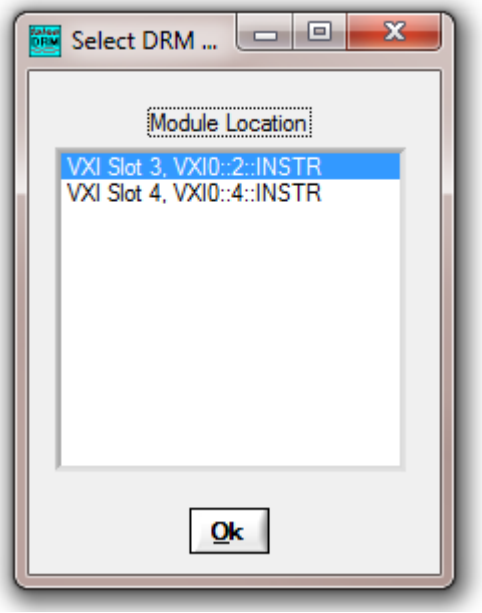


Figure 5-14: Opening a VXI DRM Session

Relevant VXI*plug&play* API functions include:

- tat964_init
- tat964_autoConnectToAll
- tat964_autoConnectToFirst
- tat964_autoConnectToLA
- tat964_autoConnectToSlot

Configuring the Global Hardware Parameters

Configuring the global hardware parameters is done from three panels: Configure Module, Configure Data Sequencer A, and Configure Data Sequencer B.

Configure Module Panel

Access this panel from the menu bar: **Config > Module**.

The Configure Module panel is used to program the inter-module mode, power converter mode/state, Linked Trigger bus routing, signal delays, VXI TRG routing, driver/receiver properties, and record settings.

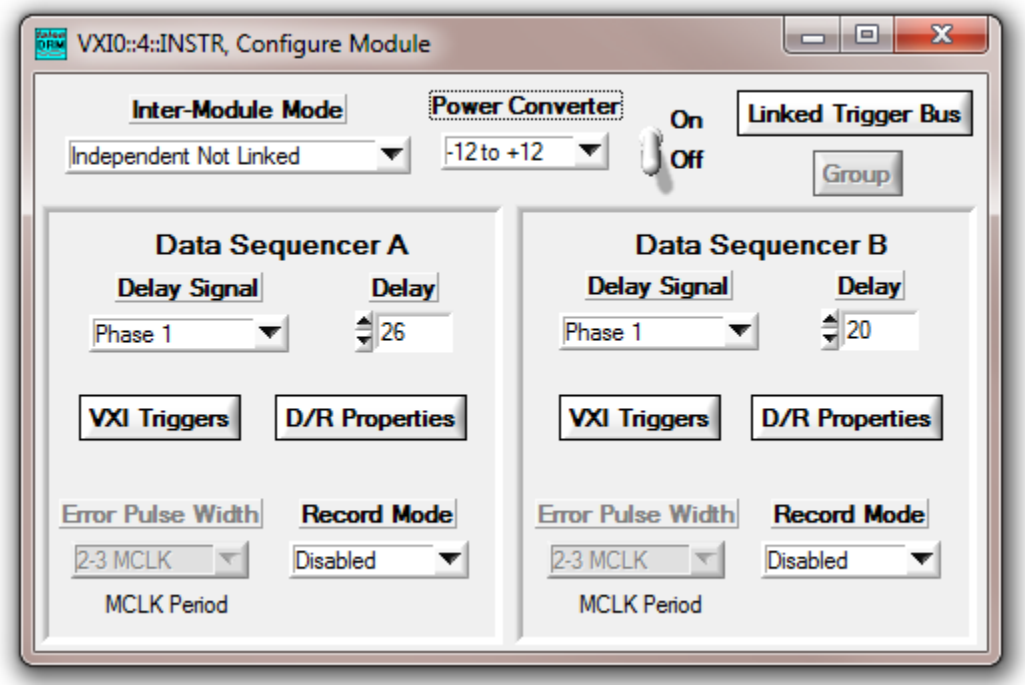


Figure 5-15: Configure Module Panel

The following sections describe the Configure Module panel controls.

Inter-Module Mode

This pull-down control programs the control source for the DSA and DSB sequencers. The T940 chain and termination are set via jumpers. If a jumper is not installed, the DRM can only be configured as Independent Not Linked or Independent Linked.

The DRM uses the VXI local bus signals to link multiple modules together. The inter-module configuration options consist of the types shown in Table 5-7.

Table 5-7: Inter-Module Types

DRM Type	Description
Independent	Independent modules do not pass the local bus chain and must not be placed between a Primary and Terminator module. Two Independent modes are available: 1. Independent Not Linked- DSA and DSB are not linked together. 2. Independent Linked - DSA and DSB are linked.

DRM Type	Description
Primary	The Primary module must be located in the rightmost slot position in the VXI chassis relative to the DRM modules that will be coupled. DSA provides all the timing for the sequencers that are part of the coupled chain . Two Primary modes are available: 1. Primary DSA Coupled – DSA coupled to DRS and DSB independent. 2. Primary DSA and DSB Coupled – DSA and DSB coupled to DRS chain.
Secondary	The Secondary module(s) are the DRMs located between the Primary and Terminator modules. Five Secondary modes exist: 1. Secondary Not Linked - DSA and DSB not linked and are independent. 2. Secondary Linked - DSA and DSB linked and independent. 3. Secondary DSA Coupled - DSA coupled to DRS and DSB independent. 4. Secondary DSB Coupled - DSB coupled to DRS and DSA independent. 5. Secondary DSA and DSB Coupled - Both DSA and DSB coupled to the DRS.
Terminator	The Terminator module is the DRM leftmost slot. Five Terminator modes exist: 1. Terminator Not Linked – DSA and DSB not linked and are independent. 2. Terminator Linked – DSA and DSB linked and independent. 3. Terminator DSA Coupled - DSA coupled to DRS and DSB independent 4. Terminator DSB Coupled - DSB coupled to DRS and DSA independent. 5. Terminator DSA and DSB Coupled – Both DSA and DSB coupled to the DRS.

All the selections for the Inter-Module Mode pull-down control are listed below. Only valid selections are displayed based on the jumper setting:

Table 5-8: Inter-Module Mode Settings

Setting	DSA Control	DSB Control	DRM Type
Independent Not Linked	DSA	DSB	Independent
Independent Linked	DSA	DSA	Independent
Primary DSA Coupled	DRS	DSB	Primary
Primary DSA and DSB Coupled	DRS	DRS	Primary
Secondary Not Linked	DSA	DSB	Secondary
Secondary Linked	DSA	DSA	Secondary
Secondary DSA Coupled	DRS	DSB	Secondary

Setting	DSA Control	DSB Control	DRM Type
Secondary DSB Coupled	DSA	DRS	Secondary
Secondary DSA and DSB Coupled	DRS	DRS	Secondary
Terminator Not Linked	DSA	DSB	Terminator
Terminator Linked	DSA	DSA	Terminator
Terminator DSA Coupled	DRS	DSB	Terminator
Terminator DSB Coupled	DSA	DRS	Terminator
Terminator DSA and DSB Coupled	DRS	DRS	Terminator

The relevant VXI*plug&play* API function is:

- tat964_setModuleInterconnect

Power Converter

This pull-down control programs the power converter voltage levels so that the driver receiver boards can operate over the specified range. The On/Off toggle switch enables/disables the power converter outputs. Ranges and suggested Voltage Mode settings (see **D/R Properties** panel).

Table 5-9: Power Converter Ranges

Type 1 and 3 Power Converters	Type 4 Power Converters	Suggested Voltage Mode Setting
-12 to +12	-7 to +7	-15V to +17V
-15 to +5	-15 to +2	-15V to +17V
-10 to +10	-10 to +9	-15V to +17V
-2 to +7	-3 to +7	Either mode
-5 to +15	-5 to +5	Either mode
0 to +24	0 to +16	-7V to +24V
-2 to +22	-2 to +14	-7V to +24V

The pull down control is disabled (dimmed) for DR installed power converters.

The relevant VXI*plug&play* API functions are:

- tat964_setPowerConverter
- tat964_setPowerConverterState

Linked Trigger Bus

The Linked Trigger Bus (LTB) signals are used to pass signals between DSA and DSB.

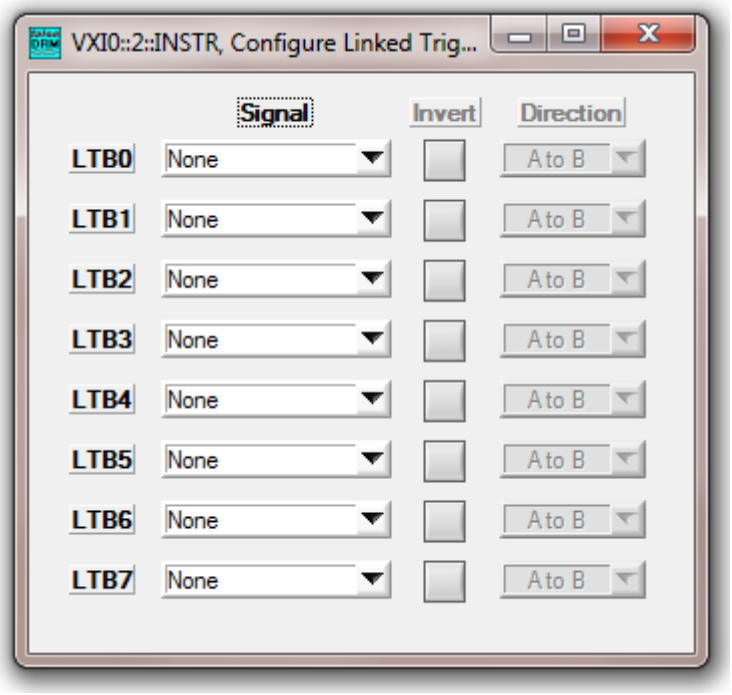


Figure 5-16: Configure Linked Trigger Bus Panel

LTBn Signal

This pull-down control programs the signal source for the specified LTB trigger. The selections for this pull-down control are:

Table 5-10: LTB Signal Pull-Down Settings

Setting	Description
None	Disables the TTLTRG driver
AUX1-AUX12	Selects the specified AUX input signal from the front panel
Halted	Used for linked halt operation between DSA and DSB
Static Pulse	Used for static operation between DSA and DSB
Pulse Generator	Selects the pulse generator signal
Sequence Flag 1-2	Selects the specified sequence flag
Sync 1-2	Selects the specified sync signal
CHT1-4	Selects the specified channel test signal
Idle Active	Idle active flag
Sequence Active	Sequence active flag
Error	DRM error flag
Pass Valid	DRM Pass Valid signal
Waveform 5	Waveform 5
DRM Sync	DRM Sync signal
Driver Disable	DRM driver disable command
Waveform 6	Waveform 6

The relevant VXI*plug&play* API function is:

- tat964_setLtbTriggers

Invert

This Invert button is used to invert the associated signal.

The relevant VXI*plug&play* API function is:

- tat964_setLtbTriggers

Direction

The direction pull-down sets the signal direction.

Table 5-11: Direction Settings

Setting	Description
A to B	Signal sourced by sequencer A and sensed by sequencer B
B to A	Signal sourced by sequencer B and sensed by sequencer A

The relevant VXI*plug&play* API function is:

- tat964_setLtbTriggers

Group

This command button displays the group configuration panel and is only valid for group enabled front end modules like the DR4.

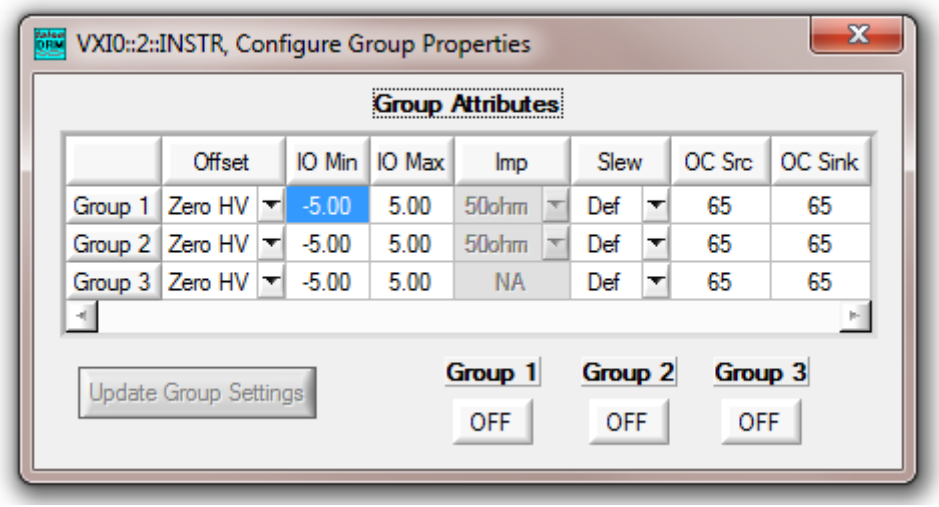


Figure 5-17: Configure Group Panel

Group Attributes

This table control programs the following group attributes.

Offset

The group offset specifies the operating voltage window of the group channels. The selections for this pull-down control are:

Table 5-12: Group Offset Attribute Settings

Setting	Description
Zero HV	-15.5V to 15.5V
Pos	0V to +31V
Neg	-31V to 0V

Verify that the Min and Max settings are within the window before updating.

The group state must be off to update this attribute and all group IO levels are set to 0V.

The relevant VXI*plug&play* API function is:

- tat964_setGroupAttribute

IO Min

This numeric entry specifies the minimum drive/compare level that can be programmed for the selected group. This level also establishes the group V- voltage level.

The IO Min valid range is -31 V to 0 V and must be lower than IO Max.

The group state must be off to update this attribute and all group IO levels are set to 0V.

The relevant VXI*plug&play* API function is:

- tat964_setGroupMinMax

IO Max

This numeric entry specifies the maximum drive/compare level that can be programmed for the selected group. This level also establishes the group V+ voltage level.

The IO Max valid range is 0 V to +31 V and must be high than IO Min.

The group state must be off to update this attribute and all group IO levels are set to 0V.

The relevant VXI*plug&play* API function is:

- tat964_setGroupMinMax

Slew

The group slew specifies the slew of the group channels. The selections for this pull-down control are:

Table 5-13: Group Slew Attribute Settings

Setting	Description
Fast	Fast recommended for low voltage swings and fast data rates.
Med	Medium
Slow	Slow
Def	Default
Low	Low recommended for high voltage swings and low data rates.

The slew attribute is updated immediately when changed.

The relevant VXI*plug&play* API function is:

- tat964_setGroupAttribute

OC Src

This numeric entry specifies the over current source setting in mA for the selected group.

The over current source valid range is 10mA to 85mA.

The OC Src attribute is updated immediately when changed.

The relevant VXI*plug&play* API function is:

- tat964_setGroupAttribute

OC Sink

This numeric entry specifies the over current sink setting in mA for the selected group.

The over current sink valid range is 10mA to 85mA.

The OC Sink attribute is updated immediately when changed.

The relevant VXI*plug&play* API function is:

- tat964_setGroupAttribute

Update Group Settings

This command button is disabled (dimmed) until any of the following group attributes are modified:

- Offset
- IO Min
- IO Max

When enabled (un-dimmed) this button programs the offset, IO min and IO max group attributes.

The relevant VXI*plug&play* API function is:

- tat964_setGroupAttribute

Group [1..3]

These toggle buttons turn the group state on or off.

The relevant VXI*plug&play* API function is:

- tat964_setGroupState

Delay Signal

The DRM uses the VXI local bus signal to function in a multi-module operation. During the alignment process, the local bus signals need to be delayed in order to align the timing skew between modules.

The selections for this pull-down control are:

Table 5-14: Delay Signal Settings

Setting	Description
Phase1-4	Phase timing signals
Window 1-4	Window timing signals
SEQ_CLK	Sequence Clock
SEQ_CLK_D	Delayed Sequence Clock
T0_CLK	Pattern Clock
Jump	Jump signal

The relevant VXI*plug&play* API function is:

- tat964_setLocalBusDelay

Delay

This control is used to specify the delay value for the signal specified by the Delay Signal control. The valid delay range is from 0 to 63 and the delay is 0.15 ns/step.

The relevant VXI*plug&play* API function is:

- tat964_setLocalBusDelay

Note: *Once alignment for an Independent, Linked, or DRS configuration is performed, these delays should not be changed.*

VXI Triggers

This command button displays the “Set VXI Triggers” panel so the TTLTRG and ECLTRG signals can be programmed for the selected sequencer. The panel contains a pull-down control and Invert button for each TTLTRG/ECLTRG signal.

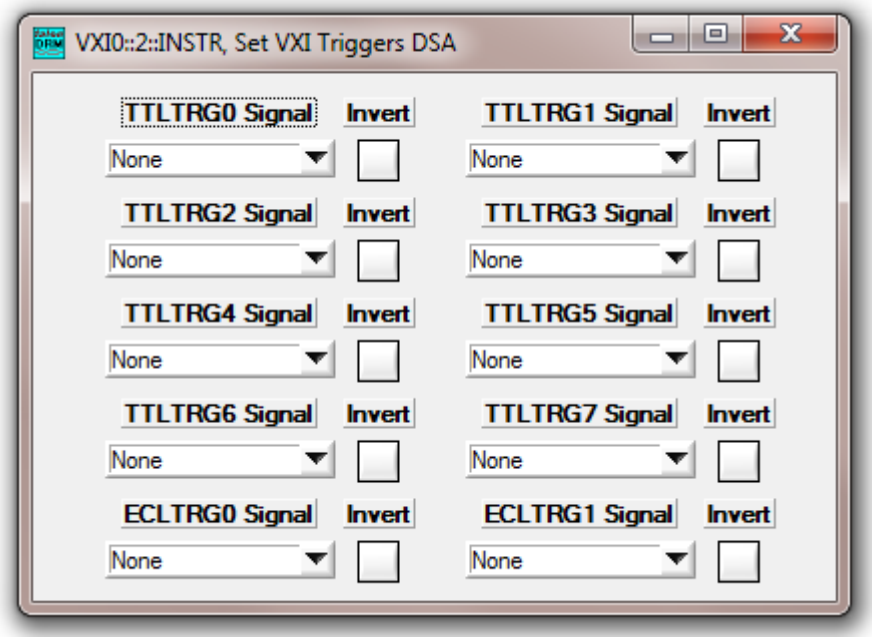


Figure 5-18: Set VXI Triggers DSA Panel

The TTLTRG lines are open collector on the VXI backplane. The chassis provides a split termination which provides a weak pull-up (thus there is a slow rising edge recovery time). Programming an active high signal on this panel will actually drive the backplane signal low. This allows multiple DRMs to actively drive the same trigger line and form a wired-OR condition. The DRM module receiving the signal knows to invert the incoming signal to re-create an active high. But non-DRM VXI modules which receive triggers from a DRM or send triggers to the DRM will need to know this protocol.

The ECLTRG lines are more like an open emitter on the VXI backplane. The chassis provides 50 ohm termination for these ECLTRG lines which results in a sharp trailing edge. In this case, programming an active high signal on this panel will drive the backplane signal high. This also allows multiple DRMs to actively drive the same trigger line and form a wired-OR condition.

Under certain circumstances, it may be desired to form a wired-AND or wired-OR on the backplane such as when doing channel tests. This is discussed further in the **T940 VXI Backplane Trigger Bus** section of Chapter 8. There is substantially more information in this section regarding the use of the TTLTRG Bus and ECLTRG Bus.

TTLTRG and ECLTRG Signal

This pull-down control programs the signal source for the specified VXI trigger. The selections for this pull-down control are:

Table 5-15: Signal Pull-Down Settings

Setting	Description of the VXI Trigger Source Signal
None	Disables the TTLTRG driver

Setting	Description of the VXI Trigger Source Signal
AUX1-AUX12	Selects the specified AUX input signal from the front panel
Halted	Used for DRS halt operation between coupled sequencers
Probe Button	Selects the state of the probe button
Pulse Generator	Selects the pulse generator signal
Sequence Flag 1-2	Selects the specified sequence flag
Sync 1-2	Selects the specified sync signal
CHT1-4	Selects the specified channel test signal
Idle Active	Idle active flag
Sequence Active	Sequence active flag
Error	DRS error flag
Pass Valid	DRS Pass Valid signal
Sequence Reset	DRS sequence reset command
DRS Sync	DRS Sync signal
Driver Disable	DRS driver disable command
Master Reset	DRS master reset

All DRS coupled sequencers must select the same TTLTRG/ECLTRG for the last six listed signals, if used. These signals are used for DRS signaling.

The relevant VXI*plug&play* API functions are:

- tat964_setTtlTriggers
- tat964_setEclTriggers

Invert

This Invert button is used to invert the associated signal before it is driven onto the selected backplane trigger line. The relevant VXI*plug&play* API functions are:

- tat964_setTtlTriggers
- tat964_setEclTriggers

D/R Properties

This command button displays the “Configure DS*n* D/R Properties” panel so the configuration settings can be programmed for applicable Driver/Receiver boards.

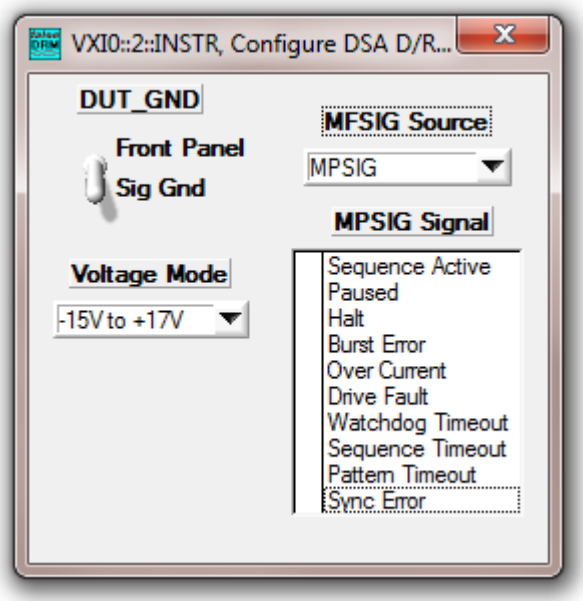


Figure 5-19: Configure DS*n* D/R Properties Panel

DUT_GND

For the DR3e/DR4/DR9/UR14, this control is used to program a relay that will connect the DUT_GND reference for the Pin Electronics to either a front panel DUT_GND or to signal ground. The former is used to correct for ground reference offsets due to cabling.

The relevant VXI*plug&play* API function is:

- tat964_setPowerSettings

Note: *This function is inoperable for the DR1, DR2, DR7, and DR8. Signal Ground is always used for these Driver/Receiver boards for single-ended signals.*

Voltage Mode

This pull-down control programs the voltage mode for the DR3e/DR9/UR14 Driver/Receiver boards. The selections for this pull-down control are:

Table 5-16: Voltage Mode Settings

Setting	Description	Recommended Usage
Mode 0	Selects voltage mode 0 (DR3e/DR9/UR14 = -15 V to +17 V)	For any Power Converter range except for the 0 to +24V and -2V to +22V
Mode 1	Selects voltage mode 1 (DR3e/DR9/UR14 = -7 V to +24 V)	For any Power Converter range except for the -12V to +12V, -15V to +5V and the -10 to +10V ranges on Type 1 and 3 Power Converters and except for the -15V to +2V and -10V to +9V ranges on the Type 4 Power Converter.

Refer to specific Driver/Receiver board specifications for voltage range levels.

The relevant VXI*plug&play* API function is:

- tat964_setVoltageRangeMode

Note: *This function is inoperable for the DR1, DR2, DR4, DR7, and DR8.*

MFSIG Source

This pull-down control programs the power connector MFSIG signal function.

The DR3e Driver/Receiver boards have an optional front panel power connector that is used to provide the V+/V- rail voltages to the Pin Electronics devices.

In addition, a signal is provided that can be programmed to generate a shutdown level to the external voltage source or to light an LED. The selections for this pull-down control are:

Table 5-17: MFSIG Settings

Setting	Description
Shutdown High	Signal goes high on voltage or temperature fault condition
Shutdown Low	Signal goes low on voltage or temperature fault condition
Disabled	Signal is not driven
MPSIG	Signal is assigned to the sequencer MPSIG signal

The relevant VXI*plug&play* API function is:

- tat964_setPowerSettings

MPSIG Signal

This control sets the source of the MPSIG. All checked signals are ORed together.

Table 5-18: MPSIG Source

Setting	Description
Sequence Active	MPSIG goes high when sequence active is true.
Paused	MPSIG goes high when the sequencer is paused.
Halt	MPSIG goes high when the sequencer is halted.
Burst Error	MPSIG goes high when burst error is true.
Over Current	MPSIG goes high when over current is true.
Drive Fault	MPSIG goes high when drive fault is true.
Watchdog Timeout	MPSIG goes high when the watchdog timeout is true.
Sequence Timeout	MPSIG goes high when the sequence timeout is true.
Pattern Timeout	MPSIG goes high when the pattern timeout is true.
Sync Error	MPSIG goes high when the sync error is true.

The relevant VXI*plug&play* API function is:

- tat964_setMpsigSource

Error Pulse Width

This pull-down programs the error signal pulse width.

The error pulse is a DRS signal used for counting and recording errors.

The error pulse width is set during the DRS timing bus calibration with the Rev J driver or later and sequencer revision 0.20 or later.

The pulse width needs to be set the same in all coupled sequencers. When the DRM is configured as a primary and not coupled to another sequencer, use a setting of 2-3 MCLKs. If linked, refer to table 5-21 below for the optimal error signal pulse width. Note: In all cases, the data period must be greater than the error pulse width + 4 ns. If a TTL trigger line is used to transmit the error pulse, the data period will need to be approximately 2-3 times longer than the error pulse.

The selections for this pull-down control are given along with the recommended error pulse width (assuming a 500 MHz master clock):

Table 5-19: Error Pulse Width Settings

Setting	Description	Typical Usage
2-3 MCLK	The error pulse will be from 2 to 3 MCLK periods	Recommended for un-linked sequencers.
3-4 MCLK	The error pulse will be from 3 to 4 MCLK periods	Recommended for a DRS of size 2-4 DRMs.
4-5 MCLK	The error pulse will be from 4 to 5 MCLK periods	Recommended for a DRS of size 5-8 DRMs.
5-6 MCLK	The error pulse will be from 5 to 6 MCLK periods	Recommended for a DRS of size 9-12 DRMs.

The relevant VXI*plug&play* API function is:

- tat964_setErrorPulseWidth
- tat964_calibrateDrsTimingBus

Record Mode

This pull-down control programs the sequencer record mode.

The sequencer record mode selects what the sequencer does to the record memory when the sequence **Step Record Mode** is set to either None or Record Count (see the section on **Step Record Mode** later in this chapter).

***Note**: If **Step Record Mode** is set to either Record Error or Record Response, then the Record Mode setting will be ignored.*

The selections for this pull-down control are:

Table 5-20: Record Mode Settings

Setting	Description	Typical Usage
Disabled	The contents of the record memory will not change during the next burst if Step Record Mode is set to either None or Record Count.	Setting Record Mode to Disabled insures that the record memory will not be written to when Step Record Mode is set to either None or Record Count. This means that if errors were recorded in a previous burst, they will remain in memory throughout the current burst.
Non-Error(0)	The contents of the record memory will be set to 0 during the next burst if Step Record Mode is set to either None or Record Count.	Setting Record Mode to Non-Error(0) when Step Record Mode is set to either None or Record Count clears the record memory during the next burst, insuring that any previously recorded errors will not persist.

The relevant VXI*plug&play* API function is:

- tat964_setSequencerRecordMode

Config Data Sequencer A/B

The Configure Data Sequencer A/B panel is used to program the clock settings, sequence control signals, timeout values, overcurrent, and record settings.

Access this panel from the menu bar: **Config > Data Sequencer *x***. (Where "x" is the sequencer you wish to configure.)

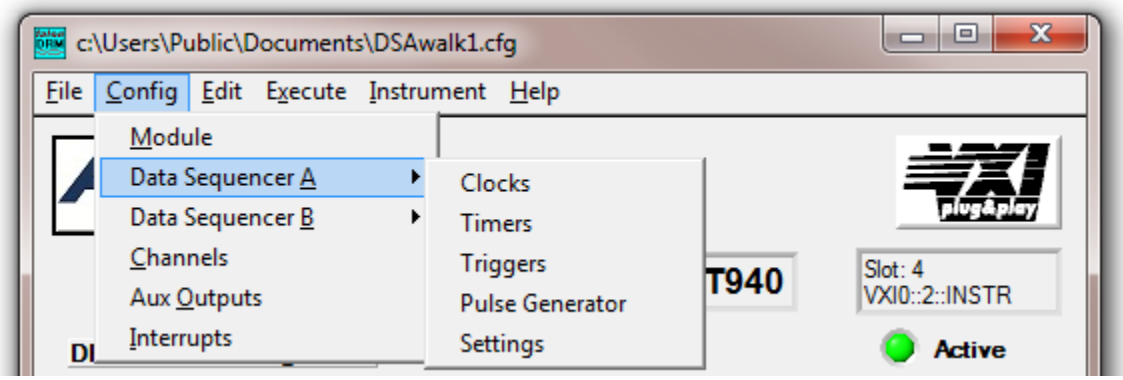


Figure 5-20: Configure Data Sequencer

Configure Clocks

Access this panel from the menu bar: **Config > Data Sequencer *x*> Clocks**. (Where "x" is the sequencer you wish to configure.)

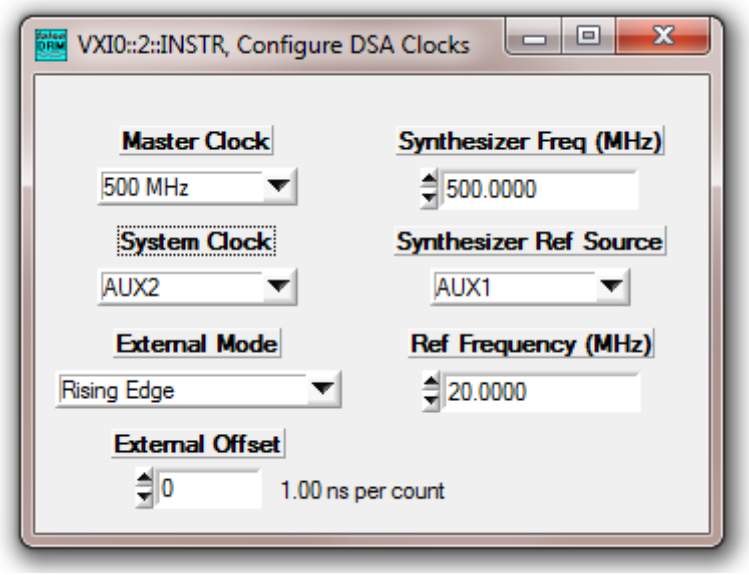


Figure 5-21: Configure Clocks

Master Clock

This pull-down control programs the sequencer master clock source.

The master clock defines the sequencer timing resolution. The resolution is half of the master clock period.

The selections for this pull-down control are:

Table 5-21: Master Clock Source Settings

Setting	Description	Typical Usage
500 MHz	Sequencer timing resolution set to 1ns	Default case; 1 ns timing resolution is required; no frequency reference
Frequency Synthesizer	Sequencer timing resolution set to 1 / (2 * FS) For example; if FS = 100 MHz Resolution = 1 / (2 * 100,000,000) Resolution = 5ns	1 ns timing resolution is required; an external frequency reference will be used to train the master clock, or when a non-standard, exact data rate is required. For example, if a 48 MHz data rate is required, the synthesizer set to 480 MHz gives 1.04167 ns per count timing. 20 counts gives a 20.8333 ns period or 48 MHz. Using the 500 MHz clock with 21 counts yields a data rate of 47.619 MHz, the closest pattern rate achievable using the 500 MHz clock.

The relevant VXI*plug&play* API function is:

- tat964_setMasterClockSource

System Clock

This pull-down control programs the sequencer System Clock source.

The System Clock signal defines the pattern period.

The selections for this pull-down control are:

Table 5-22: System Clock Source Settings

Setting	Description	Typical Usage
Internal T0CLK	System Clock source set to the internal period defined by the sequencer step.	DRM or DRS where internal master clock timing is acceptable.
AUX1-AUX12	System Clock source set to the external front panel signal.	Auxiliary line is assigned the function of external clock where: AUX1-4: 1kHz-50 MHz (when a programmable threshold or load is required with the clock) AUX5-8: LVTTL source 1kHz-50 MHz AUX9-12: Single-ended or differential ECL source from 1 kHz to 50 MHz
ECLTRG0	System Clock source set to the VXI ECLTRG0.	External clock from another VXI instrument provided across the VXI backplane.
Pulse Generator	System Clock source set to the internal pulse generator signal.	For test purposes or for when pulse width control of the system clock is required.
Frequency Synthesizer	System Clock source set the to the internal frequency synthesizer signal.	For the purpose of having a self-test.

The relevant VXI*plug&play* API function is:

- tat964_setSystemClockSource

External Mode

This pull-down control selects the clock edge mode when the System Clock source is set to any non T0CLK selection.

The selections for this pull-down control are:

Table 5-23: External Mode Settings

Setting	Description
Rising Edge	Use the rising edge of the external signal as the active edge
Falling Edge	Use the falling edge of the external signal as the active edge
Both Edges	Use the rising and falling edge of the external signal as the active edge
Divide by 2 Rising Edge	Divide the external signal by two and use the rising edge as the active edge
Divide by 2 Falling Edge	Divide the external signal by two and use the falling edge as the active edge

The relevant VXI*plug&play* API function is:

- tat964_setSystemClockParameters

External Offset

This control is used to specify the external System Clock offset in order to align the clock/data relationship. The valid offset range is from 0 to 65534 (even numbers only) and the resolution is 1/2 the MCLK period. For example if the MCLK is set to 100 MHz then the resolution is 5 ns (1/2 of 10 ns).

The relevant VXI*plug&play* API function is:

- tat964_setSystemClockParameters (SCLK Mode, SCLK Offset)

Synthesizer Freq (MHz)

This input control is used to specify the Frequency Synthesizer setting. The valid frequency range is from 40 kHz to 500 MHz. Setting the control to **0** turns off the frequency synthesizer.

The relevant VXI*plug&play* API function is:

- tat964_setFreqSynth

Synthesizer Ref Source

This pull-down control programs the frequency synthesizer reference source.

The selections for this pull-down control are:

Table 5-24: Synthesizer Ref Source Settings

Setting	Description
Internal	Reference source set to internal 20 MHz
AUX1-AUX12	Reference source set to front panel signal
VXICLK10	Reference source set to VXI backplane 10 MHz
LCLK50	Reference source set to VXI backplane LCLK100 / 2. VXI 4.0 slot 0 and chassis are required.

The relevant VXI*plug&play* API function is:

- tat964_setFreqSynth

Reference Freq (MHz)

This input control is used to specify the external reference frequency and only appears when an external synthesizer reference source is selected. In these cases, the frequency synthesizer needs to be scaled so that it can produce the desired output frequency given the nominal external reference frequency. The valid external reference frequency range is from 5 MHz to 80 MHz.

The relevant VXI*plug&play* API function is:

- tat964_setFreqSynth

Configure Timers

Access this panel from the menu bar: **Config > Data Sequencer *x*> Timers**. (Where "x" is the sequencer you wish to configure.). The DRM has five timers:

- Watchdog
- Sequence Timeout
- Pattern Timeout
- Pattern Delay 1
- Pattern Delay 2

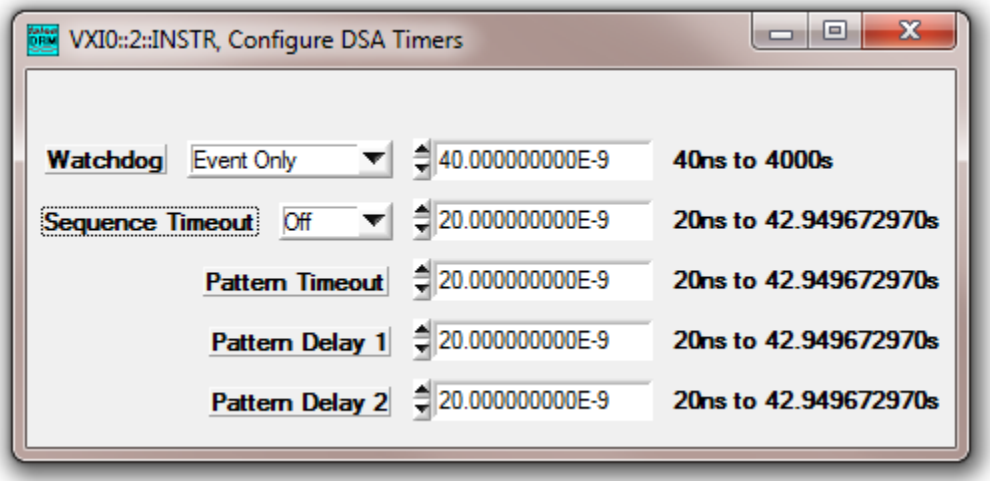


Figure 5-22: Configure Timers

Watchdog

The watchdog timer is a real-time timer that performs specific actions if the Dynamic Test does not finish within the specified time period:

- The Watchdog Timeout Timer starts when SEQACT begins. This timer does not stop during a Pause or Halt (including single-stepping).
- Generates an event (WDTO) if the sequence active time exceeds the specified value.
- If the watchdog action is set to Disable Drivers, all 32 drivers will tri-state when a timeout occurs (but any active load or resistive loading remains).

Sequence Timeout

The sequence timeout timer is a real-time timer intended to be used in a Sequence Step that has a conditional loop where one is waiting for a termination condition to proceed to the next Sequence Step:

- There is a global enable.
- It starts when the first branch takes place.

- The timer is reset at the beginning of every step unless the sequence timeout continue flag is set in the Edit Sequence Step panel.
- Cannot be nested.
- Does not stop during a Pause or Halt (including single-stepping).
- A timeout will generate an event and the occurrence of this particular event can be enabled to generate an interrupt so the S/W can query the events to see which one occurred.
- The continuous conditional loop will continue to branch unless the termination condition is subsequently met, whereby execution will advance to the next Sequence Step as usual. If it doesn't, the user can manually halt or stop the Sequence.
- The sequence timeout can be used to generate an event to indicate that a sequence step (or steps) has taken too long to complete

Pattern Timeout

The pattern timeout timer is a real-time timer which can be used in a sequence step that has a Pause:

- In the Sequence Step, the **Handshake Modifier** can be set to the Pattern Timeout.
- The Timer starts when the Pause begins.
- The Pattern Timeout Timer will generate an event when the timer times out. The Pause will continue unless the termination condition is subsequently met, whereby execution will resume. If it doesn't, the user can manually resume or stop the Sequence.

Pattern Delay

The two pattern delay timers are real-time timers which can be used in a sequence step that has a Pause:

- In the Sequence Step, the **Handshake Modifier** can be set to Pattern Delay 1 or 2.
- The Timer starts when the Pause begins.
- A Pattern Delay Timer timeout will cause a resume to be generated.

Watchdog Action

This toggle control is used to enable/disable the watchdog timeout Event Only/Driver Disable feature.

Table 5-25: Watchdog Action

Setting	Description
Event Only	Set bit in event register only when a watchdog timeout occurs.
Disable Drivers	Set bit in event register and disable the drivers when a watchdog timeout occurs.

The relevant VXI*plug&play* API function is:

- tat964_setWatchdogTimer

Watchdog Time

This numeric control is used to specify the watchdog timeout count.

The timeout is programmed in 20 ns steps with a range of 40 ns to 4000 s.

The watchdog timer set resolution adjusts based on the timeout value:

Table 5-26: Watchdog Timer Resolution Ranges

Timer Setting	Resolution
Less than 10 ms	20 ns
From 10ms to < 10 s	100 ns
From 10 s to 4000 s	1 us

The relevant VXI*plug&play* API function is:

- tat964_setWatchdogTimer

Sequence Timeout State

This toggle control is used to enable/disable the sequence timeout feature.

Table 5-27: Sequence Timeout State Action

Setting	Description
Off	Disable sequence timeout bit in event register.
On	Enable sequence timeout bit in event register.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceTimer

Sequence Timeout Time

This numeric control is used to specify the sequence timeout count.

The timeout is programmed in 10 ns steps with a range of 20 ns to 42.949672970 s.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceTimer

Pattern Timeout

This numeric control is used to specify the pattern timeout count.

The timeout is programmed in 10 ns steps with a range of 20 ns to 42.949672970 s.

The relevant VXI*plug&play* API function is:

- tat964_setPatternTimer

Pattern Delay 1-2

This numeric control is used to specify the pattern delay.

The pattern delay is programmed in 10 ns steps with a range of 20 ns to 42.949672970 s.

The relevant VXI*plug&play* API function is:

- tat964_setPatternDelayTimer

Configure Triggers

Access this panel from the menu bar: **Config > Data Sequencer *x*> Triggers**. (Where “x” is the sequencer you wish to configure.)

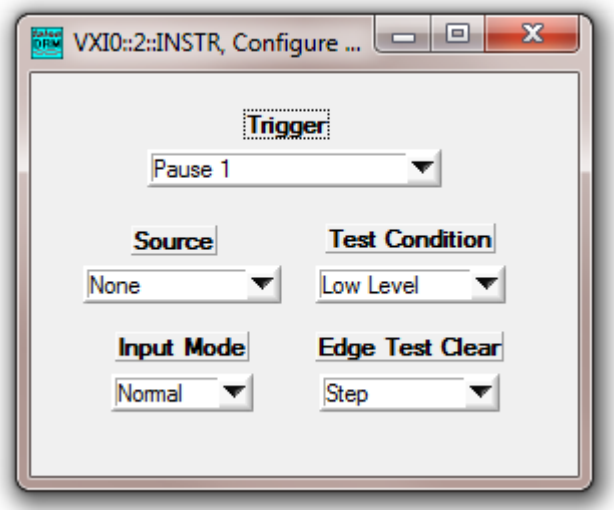


Figure 5-23: Configure Triggers Panel

Pause Trigger and Pause Resume Trigger

The pause triggers are used to stop the pattern timing during a burst. The corresponding resume trigger re-starts the pattern timing from where it was stopped.

A pause/resume can be based on the true/false state of any of the two pause triggers. For example; if Pause 1 Trigger was set to AUX1 'Low Level' and Pause 1 Resume was set to AUX1 'High Level', then the timing would stop when AUX1 is low and continue when AUX1 goes high.

Phase Resume Triggers

If the pattern timing is paused by either the assert or return edge of a phase, then this trigger is used to resume the timing.

Halt Trigger

The halt trigger causes the sequencer to halt based on the current halt mode.

Execute Start Trigger

The execute start trigger causes the selected sequence step to start. Selecting a sequence step consists of arming the sequence step. In a linked or DRS configuration, all of the coupled sequencers need to be armed first.

Execute Stop Trigger

The execute stop trigger causes the sequencer to stop based on the current stop mode.

Jump Trigger

Four sequence jump triggers are available. The sequence jump triggers are used for conditional jumping/looping. A jump/loop can be based on the true/false state of any of the four sequence jump triggers. For example; if jump trigger 1 test mode is set to 'Low Level', then a jump if trigger 1 true would occur if the selected jump trigger 1 source is low.

Trigger

This pull-down control selects the trigger to program.

The selections for this pull-down control are:

Table 5-28: Trigger Settings

Setting	Description
Pause Trigger 1	Select Pause Trigger 1 to edit
Pause Trigger 1 Resume	Select Pause Trigger 1 Resume to edit
Pause Trigger 2	Select Pause Trigger 2 to edit
Pause Trigger 2 Resume	Select Pause Trigger 2 Resume to edit
Phase 1 Resume	Select Phase 1 Resume to edit
Phase 2 Resume	Select Phase 2 Resume to edit
Phase 3 Resume	Select Phase 3 Resume to edit
Phase 4 Resume	Select Phase 4 Resume to edit
Execute Start	Select Execute Start to edit
Execute Stop	Select Execute Stop to edit
Halt	Select Halt to edit
Jump 1	Select Jump 1 to edit
Jump 2	Select Jump 2 to edit
Jump 3	Select Jump 3 to edit
Jump 4	Select Jump 4 to edit

Note: *See the* ***Jumping, Halting, Counting and Logging Errors*** *section of Chapter 8 for a more in-depth explanation.*

Source

This pull-down control programs the trigger source.

The selections for this pull-down control are:

Table 5-29: Trigger Source Settings

Setting	Description
None	No trigger source selected
AUX1-AUX12	Trigger source set to front panel signal
CHT1	Trigger source set to channel test 1
ECLTRG0,1	Trigger source set to VXI ECL trigger
TTLTRG0-7	Trigger source set to VXI TTL trigger
LTB0-7	Trigger source set to Linked Trigger bus signal

The relevant VXI*plug&play* API functions are:

- tat964_setHandshakePauseTrigger
- tat964_setHandshakeResumeTrigger
- tat964_setPhaseResumeTrigger
- tat964_setJumpTrigger
- tat964_setHaltTrigger
- tat964_setExecuteStartTrigger
- tat964_setExecuteStopTrigger
- tat964_armIdleSequence
- tat964_armSequence

Test Condition

This pull-down control programs the trigger test condition.

The selections for this pull-down control are:

Table 5-30: Trigger Test Condition Settings

Setting	Description
Low Level	Test for a low level
High Level	Test for a high level
Rising Edge	Test for a rising edge
Falling Edge	Test for a falling edge

The relevant VXI*plug&play* API functions are:

- tat964_setHandshakePauseTrigger
- tat964_setHandshakeResumeTrigger

- tat964_setPhaseResumeTrigger
- tat964_setJumpTrigger
- tat964_setHaltTrigger
- tat964_setExecuteStartTrigger
- tat964_setExecuteStopTrigger

Input Mode

This pull-down control programs the trigger input mode.

The selections for this pull-down control are:

Table 5-31: Trigger Input Mode Settings

Setting	Description
Normal	Do not modify input signal before testing.
Inverted	Invert input signal before testing.

The relevant VXI*plug&play* API functions are:

- tat964_setHandshakePauseTrigger
- tat964_setHandshakeResumeTrigger
- tat964_setPhaseResumeTrigger
- tat964_setJumpTrigger
- tat964_setHaltTrigger
- tat964_setExecuteStartTrigger
- tat964_setExecuteStopTrigger

Edge Test Clear

This pull-down control programs the trigger event clear.

The event clear allows the user to program when the rising/falling edge flip-flops are cleared during operation for the following triggers:

- Pause 1-2
- Halt
- Jump 1-4

The selections for this pull-down control are:

Table 5-32 Trigger Event Clear Settings

Setting	Description
Start	Clear flip-flops at start of burst
Step	Clear flip-flops at start of every sequence step
Event True	Clear flip-flops when trigger event tests true

The relevant VXI*plug&play* API functions are:

- tat964_setPauseTriggerReset
- tat964_setHaltTriggerReset
- tat964_setJumpTriggerReset

Configure Pulse Generator

Access this panel from the menu bar: **Config > Data Sequencer *x*> Pulse Generator** (where "x" is the sequencer you wish to configure).

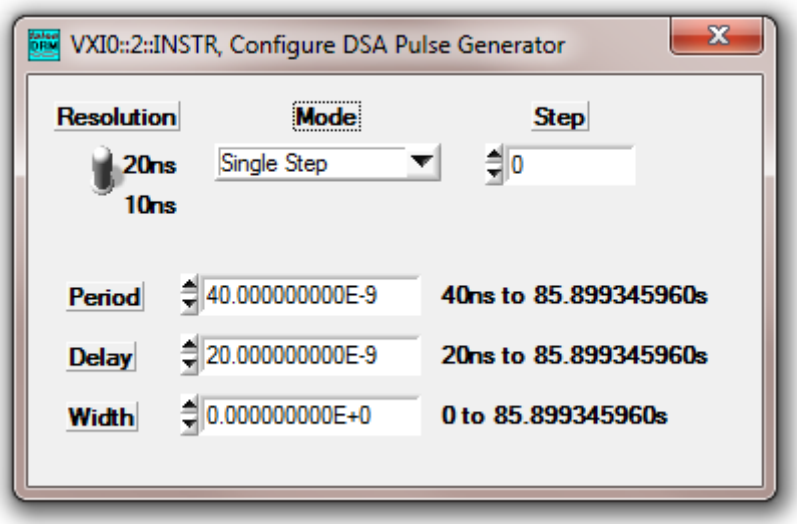


Figure 5-24: Configure Pulse Generator

Each data sequencer has a programmable pulse generator that can be routed to the following signals:

- Data sequencer System Clock
- VXI TTLTRG
- VXI ECLTRG
- Front panel AUX

Resolution

This toggle control is used to program the pulse generator resolution to either 10 ns or 20 ns.

The relevant VXI*plug&play* API function is:

- tat964_setPulseParameters

Mode

This pull-down control programs the pulse generator mode.

The selections for this pull-down control are:

Table 5-33: Pulse Generator Mode Settings

Setting	Description
Continuous	The pulse generator begins continuous output when armed
Continuous Start	The pulse generator begins continuous output from the start of the sequence when armed
Single Start	The pulse generator outputs a single pulse from the start of the sequence when armed
Single Step	The pulse generator outputs a single pulse from the start of the specified step when armed. Note: if looping the sequence step or bursting the entire sequence, the pulse generator will re-trigger.

The relevant VXI*plug&play* API function is:

- tat964_setPulseParameters

Step

This input control is used to specify the step number when the Mode is set to Single Step.

The Step is programmed with a range of 0 to 4095.

The relevant VXI*plug&play* API function is:

- tat964_setPulseParameters

Note: *This setting is hidden unless the Single Step Mode is selected.*

Period

This input control is used to specify the pulse generator period.

If the resolution is 10 ns, the period is programmed in 10 ns steps with a range of 20 ns to 42.949672970 s.

If the resolution is 20 ns, the period is programmed in 20 ns steps with a range of 40 ns to 85.899345920 sec.

The pulse period is not required for Single Start and Single Step mode.

The relevant VXI*plug&play* API function is:

- tat964_setPulsePeriod

Delay

This input control is used to specify the pulse generator delay from the start of the sequence or sequence step. Delay is not applicable when the Pulse Generator is in Continuous mode.

If the resolution is 10 ns, the delay is programmed in 10 ns steps with a range of 20 ns to 42.949672970 s (with an uncertainty of ±5 ns).

If the resolution is 20 ns, the delay is programmed in 20 ns steps with a range of 20 ns to 85.899345920 s (with an uncertainty of ±5 ns).

The relevant VXI*plug&play* API function is:

- tat964_setPulseDelay

Width

This input control is used to specify the pulse generator width.

If the resolution is 10 ns, the width is programmed in 10 ns steps with a range of 0 to 42.949672950 s.

If the resolution is 20 ns, the width is programmed in 20 ns steps with a range of 0 to 85.8993459 s.

If the width is equal to or greater than the period in Continuous and Continuous Start mode, then the result will be a continuously true pulse.

If the width plus the delay is greater than the period in Continuous and Continuous Start mode, then the pulse width will be reduced proportionately and vanish at some point.

The relevant VXI*plug&play* API function is:

- tat964_setPulseWidth

Configure Data Sequencer Settings

Access this panel from the menu bar: **Config > Data Sequencer *x*> Settings**. (Where “x” is the sequencer you wish to configure.)

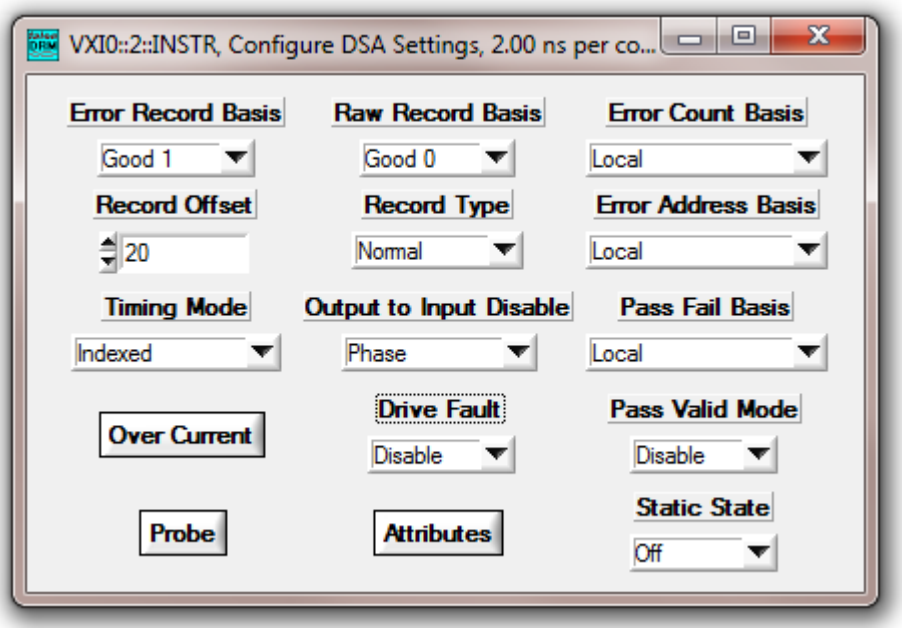


Figure 5-25: Data Sequencer Configure Settings Panel

Error Record Basis

This pull-down control programs the sequencer error record basis.

This control allows the user to select how the response data will be evaluated for errors when the record mode is set to **Record Errors**.

The selections for this pull-down control are:

Table 5-34: Error Record Basis Settings

Setting	Description
Dual	Use both good 1 and good 0 comparator levels
Good 1	Use only the good 1 comparator (Single threshold)

These two choices are provided for use with the DR3e Driver/Receiver only.

The relevant VXI*plug&play* API function is:

- tat964_setRecordParameters

Raw Record Basis

This pull-down control programs the sequencer raw record basis.

This control allows the user to select which comparator will be used to determine the data level when the record mode is set to **Record Response**.

The selections for this pull-down control are:

Table 5-35: Raw Record Basis Settings

Setting	Description
Good 0	Use good 0 comparator levels (only available on dual threshold Driver/Receiver boards like the DR3e). Note: The Good 0 is complemented when recorded
Good 1	Use good 1 comparator levels

These two choices are provided for use with the DR3e Driver/Receiver.

The relevant VXI*plug&play* API function is:

- tat964_setRecordParameters

Record Offset

The record offset allows the user to shift the record signals (pattern code expect and mask, record offset, window strobes) to accommodate system and UUT

delay. See the **Record Offset** section in Chapter 8 for more details about using this feature.

The valid offset range is from 0 to 63 MCLKs.

The relevant VXI*plug&play* API function is:

- tat964_setRecordParameters

Note: *Once calibrated for an Independent, Linked or DRS configuration, this offset should not be changed.*

Record Type

This pull-down control programs the record type.

The selections for this pull-down control are:

Table 5-36: Record Type Settings

Settings	Description
Normal	Data stored in the record memory will be at the same offset as the pattern set memory.
Indexed	Data stored in the record memory will begin at offset 0. The record index memory contains the information needed to realign the record memory with the sequence step data.

The relevant VXI*plug&play* API function is:

- tat964_setRecordParameters

Error Count Basis

This pull-down control programs the sequencer error count basis.

This control allows the user to select which error signal to use to determine the error count.

The selections for this pull-down control are:

Table 5-37: Error Count Basis Settings

Setting	Description	Typical Usage
Local	Use local error	Error counting is globally enabled
Qualified Local	Use BERREN qualified local error	Error counting is enabled per pattern by the BERREN bit qualifier
DRS/Linked	Use DRS/Linked error	DRS/Linked error counting is globally enabled
Qualified DRS/Linked	Use BERREN qualified DRS/Linked error	DRS/Linked error counting is enabled per pattern by the BERREN bit qualifier

If the Error Count Basis is enabled for DRS or Linked operation, then the ERROR signal must be coupled between DRMs/Sequencers via the TTL/ECL or Linked TRG bus respectively. The ECL TRG Bus is recommended for data rates greater than 10 MHz. This is discussed in more detail in the **Jumping, Halting,**

Counting and Logging Errors section in **Chapter 8** including data rate limitations.

The relevant VXI*plug&play* API function is:

- tat964_setErrorParameters

Error Address Basis

This pull-down control programs the sequencer error address basis.

This control allows the user to select which error signal causes an error to be recorded in the Error Address Memory.

The selections for this pull-down control are:

Table 5-38: Error Address Basis Settings

Setting	Description	Typical Usage
Local	Use local error	Error recording is globally enabled
Qualified Local	Use BERREN qualified local error	Error recording is enabled per pattern by the BERREN bit qualifier
DRS/Linked	Use DRS/Linked error	DRS/Linked error recording is globally enabled
Qualified DRS/Linked	Use BERREN qualified DRS/Linked error	DRS/Linked error recording is enabled per pattern by the BERREN bit qualifier

If the Error Address Basis is enabled for DRS or Linked operation, then the ERROR signal must be coupled between DRMs/Sequencers via the TTL/ECL or Linked TRG bus respectively. The ECL TRG Bus is recommended for data rates greater than 10 MHz. This is discussed in more detail in the **Jumping, Halting, Counting and Logging Errors** section in **Chapter 8** including data rate limitations.

The relevant VXI*plug&play* API function is:

- tat964_setErrorParameters

Timing Mode

This pull-down control programs the timing mode, which selects one of three available timing set organization methods.

The selections for this pull-down control are:

Table 5-39: Timing Mode Settings

Setting	Description
Per Step Multi	1024 steps with four phase/window pairs per step.
Per Step Single	4096 steps with one phase/window pair per step.

Indexed	4096 sequence steps with 256 timing sets indexed. Four phase/window signals per timing set.

The relevant VXI*plug&play* API function is:

- tat964_setTimingMode

Output-to-Input Disable

This pull-down control programs the output-to-input disable setting.

When a channel transitions from an output pattern code to an input pattern code, this enable can be set to disable the output at the beginning of the pattern (System Clock) or on a phase assert.

The selections for this pull-down control are:

Table 5-40: Output-to-Input Disable Settings

Setting	Description
System Clock	Disable output on System Clock
Phase	Disable output on Phase Assert

The relevant VXI*plug&play* API function is:

- tat964_setDriverEnableControl

Pass Fail Basis

This pull-down control programs the sequencer pass fail basis.

The control allows the user to select which error signal to use to determine the PASS/FAIL state for jumping.

The selections for this pull-down control are:

Table 5-41: Pass Fail Basis Settings

Setting	Description
Local	Use local error
Qualified Local	Use CONDEN qualified local error
DRS/Linked	Use DRS/Linked error
Qualified DRS/Linked	Use CONDEN qualified DRS/Linked error

If the Pass Fail Basis is enabled for DRS or Linked operation, then the ERROR signal must be coupled between DRMs/Sequencers via the TTL/ECL or Linked TRG bus respectively. And, if used, the PASS_Valid signal must also be coupled between DRMs/Sequencers via the TTL/ECL or Linked TRG. The ECL TRG Bus is recommended for data rates greater than 10 MHz. This is discussed in more detail in the **Jumping, Halting, Counting and Logging Errors** sections in

Chapter 8.

The relevant VXI*plug&play* API function is:

- tat964_setPassFailParameters

Pass Valid Mode

This pull-down control programs the sequencer pass valid mode.

This control allows the user to define the Pass as a Valid Pass. A Valid Pass is one where no channel errors were detected but there must be at least one valid pattern expect code for each pattern in the sequence step.

If Pass Valid is enabled for a DRS, then the Pass Valid signal must be coupled between DRMs via the TTL or ECL TRG bus. The ECL TRG Bus is recommended for data rates greater than 10 MHz. This is discussed in more detail in the **Jumping, Halting, Counting and Logging Errors** section in **Chapter 8**.

The selections for this pull-down control are:

Table 5-42: Pass Valid Mode Settings

Setting	Description
Disable	Do not use pass valid signal
Enable	Use pass valid signal

The relevant VXI*plug&play* API function is:

- tat964_setPassFailParameters

Over-Current

This command button displays the Over-Current panel so the over-current parameters can be programmed for the selected sequencer.

The over-current mode should be used for channels configured in the static mode only. It should not be used for channels configured in dynamic mode because of the long recovery delay from over-current transients due to data transitions. Use Drive Fault to detect an over-current for channels configured as dynamic.

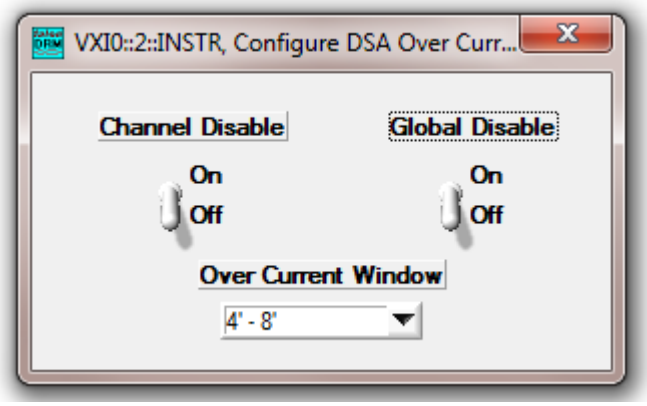


Figure 5-26: Over-Current Panel

Channel and Global Disable

The DR3e, DR4, DR9 and UR14 programmable drivers generate an over-current signal that is monitored.

Setting the Channel Disable control to **On** will cause the channel or channels which have an over-current event to be disabled.

Setting the Global Disable control to **On** causes all of the channels on the Driver/Receiver board to be disabled whenever any channel has an over-current event.

If Driver Disable is coupled between DRMs via the TTL or ECL Trigger bus or coupled between sequencers on the Linked Trigger Bus, then all the channels in the DRS and/or Linked sequencers will be disabled.

The relevant VXI*plug&play* API functions is:

- tat964_setOverCurrentControl

Over-Current Window

An over-current window can be programmed to wait for current transients to subside. These transients are primarily due to cable length. The over-current test window is triggered on the assert or return edge of the selected phase and prevents an over-current event from occurring until after the transient has subsided.

The selections for the over-current window pull-down controls are:

Table 5-43: Over-Current Window Settings

Setting	Description
4' – 8'	Set window to cables between 4 and 8 feet
8.3' – 16.3'	Set window to cables between 8.3 and 16.3 feet
16.6' – 24.6'	Set window to cables between 16.6 and 24.6 feet
25' – 33'	Set window to cables between 25 and 33 feet
33.3' – 41.3'	Set window to cables between 33.3 and 41.3 feet
41.6' – 49.6'	Set window to cables between 41.6 and 49.6 feet
50' – 58'	Set window to cables between 50 and 58 feet
58.3' – 66.3'	Set window to cables between 58.3 and 66.3 feet
66.6' – 74.6'	Set window to cables between 66.6 and 74.6 feet
75' – 83'	Set window to cables between 75 and 83 feet
83.3' – 91.3'	Set window to cables between 83.3 and 91.3 feet
91.6' – 99.6'	Set window to cables between 91.6 and 99.6 feet
100' – 108'	Set window to cables between 100 and 108 feet
108.3' – 116.3'	Set window to cables between 108.3 and 116.3 feet
116.6' – 124.6'	Set window to cables between 116.6 and 124.6 feet
125' – 133'	Set window to cables between 125 and 133 feet

The relevant VXI*plug&play* API function is:

- tat964_setOverCurrentControl

Note: *The actual current limits for over-current detection are programmed in* **Configuring the I/O Channels**, *below. For the DR4, current limits are programmed as shown in the relevant* **Group Attributes** *section.*

Drive Fault

This pull-down control programs the sequencer Drive Fault mode.

If an output pin is enabled to also compare its state (Capture mode programmed and compare levels set), then a drive fault will be generated if the compare level does not match the output state. Drive faults can be used with stimulus only

pattern codes and can be used to detect dynamic over-current conditions.

If enabled a drive fault will disable all channels of the specified sequencer and a drive fault event will be generated.

Use tat964_querySequencerEvent() to query the drive fault event and tat964_querySequencerDriveFault() to query which channel caused the drive fault.

The selections for this pull-down control are:

Table 5-44: Drive Fault Settings

Setting	Description
Disable	Disable drive fault signal
Enable	Enable drive fault signal

The relevant VXI*plug&play* API function is:

- tat964_setDriveFaultState

Probe

This command button displays the Probe panel so the probe parameters can be programmed. The probe module connects to the UR14 J1A connector.

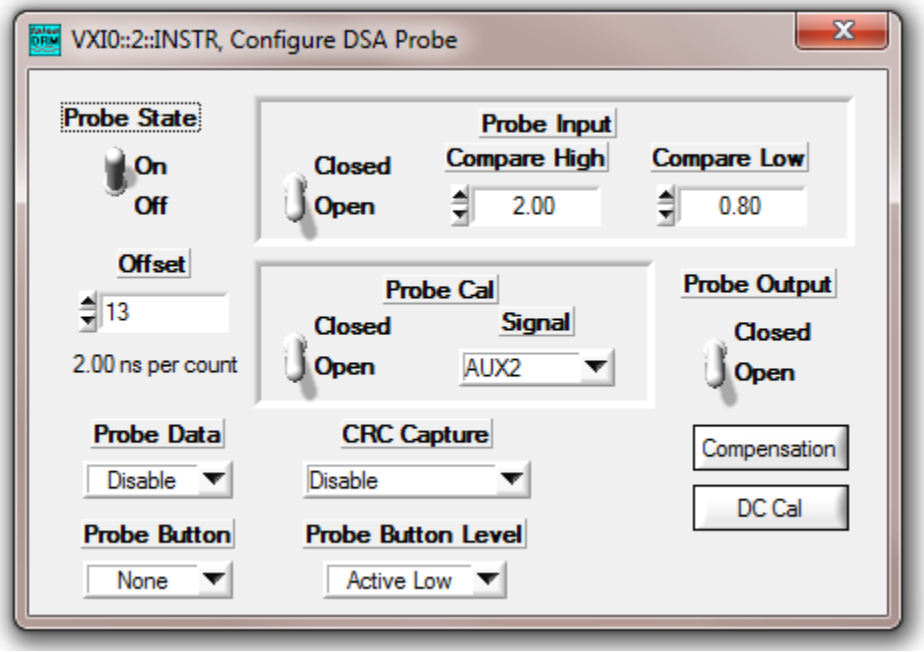


Figure 5-27: Probe Panel

Probe State

This control initializes/resets the probe resources on the UR14 module.

Note: *Disable the Probe State when not in use. See the* **Jumping, Halting,**

Counting and Logging Errors *section of* ***Chapter 8*** *for a discussion on the impact of the Probe State on data rates.*

The relevant VXI*plug&play* API function is:

- tat964_setProbeInterfaceState

Offset

The Probe offset allows the user to shift the probe record signals to accommodate system and UUT delay.

The relevant VXI*plug&play* API function is:

- tat964_setProbeConfiguration

Note: *Once the Probe is calibrated for an Independent, Linked or DRS configuration, this offset should not be changed.*

Probe Data

This sets the probe data memory setting.

Note: *Disable the Probe Data when the probe is not in use. See the* **Jumping, Halting, Counting and Logging Errors** *section of* ***Chapter 8*** *for a discussion on the impact of the Probe Data Setting on data rates.*

The selections for this pull-down control are:

Table 5-45: Probe Data Settings

Setting	Description
Disable	The probe data memory is not written to.
Capture	The probe data memory contains comparator and transition results.
Compare	The probe data memory contains the results of a comparison between probe data and the probe expect data. This mode is only available when the sequencer "Record Type" is set to "Normal". See "tat964_setRecordParameters".

The relevant VXI*plug&play* API function is:

- tat964_setProbeConfiguration

CRC Capture

The capture CRC mode allows the user to select the capture signal for the probe CRC.

The selections for this pull-down control are:

Table 5-46: CRC Capture Settings

Setting	Description
Disable	Disable Probe CRC Capture

Setting	Description
Window 4 Open	Window 4 open edge samples the CRC.
Window 4 Close	Window 4 close edge samples the CRC.

The relevant VXI*plug&play* API function is:

- tat964_setProbeConfiguration

Probe Button

This control sets the probe button action.

The selections for this pull-down control are:

Table 5-47: Probe Button Settings

Setting	Description
None	Disable probe button.
Start	Probe button starts the selected sequence.
Resume	Probe button resumes the paused sequence.
Both	Probe button starts and resumes the sequence.

The relevant VXI*plug&play* API function is:

- tat964_setProbeConfiguration

Probe Button Level

This control sets the active level of the probe button.

Setting options:

- Active Low
- Active High

The relevant VXI*plug&play* API function is:

- tat964_setProbeConfiguration

Probe Input Connect

This control opens and closes the probe input channel connect relay. The probe input is routed through AUX1 A on the UR14 Driver/Receiver board.

The relevant VXI*plug&play* API function is:

- tat964_setProbeConnect

Probe Input Compare High and Low

These two controls set the probe input high and low comparator levels. The

probe input is routed through AUX1 A on the UR14 Driver/Receiver board.

The relevant VXI*plug&play* API function is:

- tat964_setProbeLevels

Probe Cal Connect

This control opens and closes the probe calibration channel connect relay. The probe calibration is routed through AUX2 A on the UR14 Driver/Receiver board.

The relevant VXI*plug&play* API function is:

- tat964_setProbeConnect

Probe Cal Signal

This pull-down control programs the probe calibration signal source.

The selections for this pull-down control are:

Table 5-48: Probe Cal Signal Settings

Setting	Description
AUX2	Calibration signal sourced by AUX2 programmable driver
+10V	Calibration signal sourced from internal +10V reference
+5V	Calibration signal sourced from internal +5V reference
GND	Calibration signal tied to ground
-5V	Calibration signal sourced from internal -5V reference
-10V	Calibration signal sourced from internal -10V reference

The relevant VXI*plug&play* API function is:

- tat964_setProbeCalSignal

Probe Output Connect

This control opens and closes the probe output channel connect relay. The probe output is routed through PROBE OUT signal on the UR14 Driver/Receiver board.

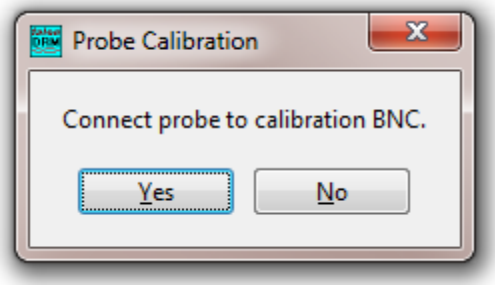
The relevant VXI*plug&play* API function is:

- tat964_setProbeConnect

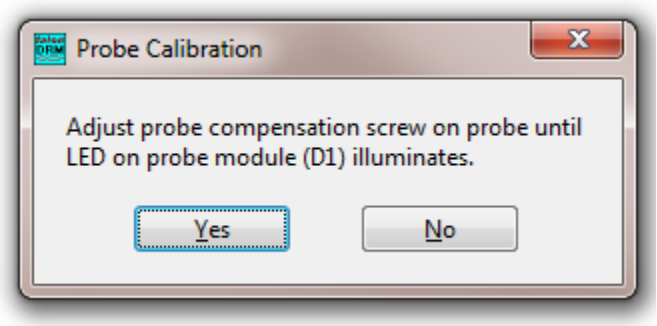
Compensation

This control initiates a compensation calibration.

The user is prompted to connect the probe to the calibration BNC.



The user is then prompted to adjust the probe compensation screw until the probe module LED labeled D1 illuminates.



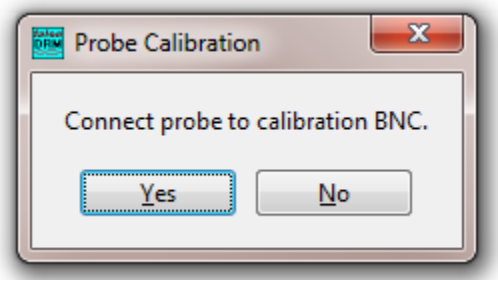
The relevant VXI*plug&play* API function is:

- tat964_probeCalibration

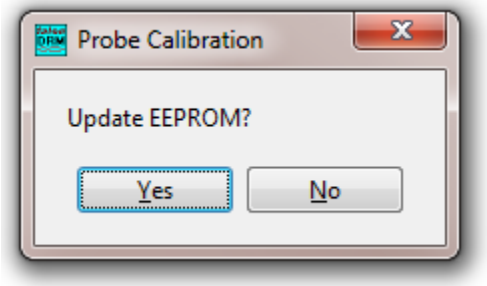
DC Cal

This control initiates a DC level calibration.

The user is prompted to connect the probe to the calibration BNC.



After calibration has been perfomed, the user is prompted to update the EEPROM.



The relevant VXI*plug&play* API function is:

- tat964_probeCalibration

Attributes

This command button on the Configure DSA Settings panel displays the Attribute panel so that the sequencer attributes can be programmed.

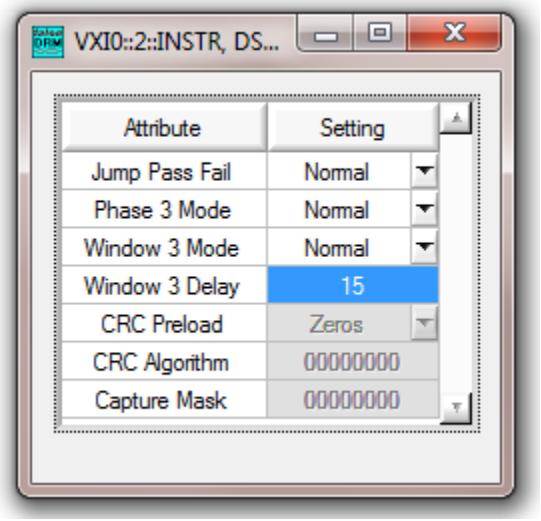


Figure 5-28: Attribute Panel

Jump Pass Fail

This control sets the sequencer step pass/fail accumulator mode.

The selections for this pull-down control are:

Table 5-49: Jump Pass Fail Settings

Setting	Description
Normal	Enable the sequence step pass/fail accumulator (Default).
Legacy	Disable the sequence step pass/fail accumulator.

Note: *See the* ***Jumping on and Counting Errors*** *section in* ***Chapter 8*** *for details on Jump Pass Fail.*

The relevant VXI*plug&play* API function is:

- tat964_setSequencerAttribute

Phase 3 Mode

This control sets the phase 3 signal mode that selects internal or external operation. Internal phase 3 mode uses the normal phase generator to generate phase 3. External phase 3 mode uses the Jump 1 trigger to generate the phase 3 signal. Phase 3 is typically set to Jump 1 to perform a Phase Replacement during a Pause and Resume operation.

The selections for this pull-down control are:

Table 5-50: Phase 3 Mode Settings

Setting	Description	Typical Usage
Normal	Phase 3 is sourced from the internal phase generator. (Default)	Internally programmed timing for drive phases.
Jump 1	Phase 3 is sourced form the Jump 1 trigger signal.	Externally programmed timing controlled by an external stimulus clock tied to the Jump 1 Trigger source.

The relevant VXI*plug&play* API function is:

- tat964_setSequencerAttribute

Window 3 Mode

This control sets the window 3 signal mode that selects internal or external operation. Internal window 3 mode uses the normal window generator to generate window 3. External window 3 mode uses the Jump 2 trigger to generate the window 3 signal. Window 3 is typically set to Jump 2 to perform a Window Replacement during a Pause and Resume operation.

The selections for this pull-down control are:

Table 5-51: Window 3 Mode Settings

Setting	Description	Typical Usage
Normal	Window 3 is sourced from the internal window generator. (Default)	Internally programmed timing for response windows.
Jump 2	Window 3 is sourced from the Jump 2 trigger signal.	Externally programmed timing controlled by an external response clock tied to the Jump 2 Trigger source.

The relevant VXI*plug&play* API function is:

- tat964_setSequencerAttribute

Window 3 Delay

This control is used to delay the window 3 signal and is used when the "Window 3 Mode" attribute is set to Jump 2. Typically, Window 3 Mode can be used with an external response clock connected as the source of Jump Trigger 2. Window 3 Delay can be used to align an external response clock with the incoming response data.

The valid delay range is from 0 to 15 with 2ns resolution.

The relevant VXI*plug&play* API function is:

- tat964_setSequencerAttribute

CRC Preload

This control sets the seed number for the CRC preload and are available in sequencer revision 0.23 and later.

The selections for this pull-down control are:

Table 5-52: CRC Preload Settings

Setting	Description
Zeros	Preload 0's
Ones	Preload 1's
Masked	Mask Preload

The relevant VXI*plug&play* API function is:

- tat964_setSequencerAttribute

CRC Algorithm and Capture Mask

These numeric controls set the number for the CRC algorithm and for the CRC capture mask settings and are available in sequencer revision 0.23 and later.

.

Table 5-53: CRC Algorithm and Mask Settings

Setting	Description
CRC Algorithm	A one in a bit position enables the corresponding CRC register bit feedback path. Bit 0 corresponds to CH1 and bit 31 corresponds to CH32.
CRC Mask	A one masks the corresponding channel's capture data. Bit 0 corresponds to CH1 and bit 31 corresponds to CH32.

The relevant VXI*plug&play* API function is:

- tat964_setSequencerAttribute

Static State

This pull-down control programs the sequencer static state.

The static state is used to enable or disable the channel static mode setting. For sequencer revisions prior to 0.21, when enabled, the pulse generator is locked from user settings and is programmed to generate the output delay and response delay signals for static channels. When disabled, the pulse generator is unlocked and set to power up defaults and all channels are set to dynamic operation.

Sequencer revisions 0.21 and later have dedicated static timing and do not require the pulse generator. Thus, the pulse generator is available for user settings.

The selections for this pull-down control are:

Table 5-54: Static State Settings

Setting	Description
Off	Disable static operation
On	Enable static operation.

The relevant VXI*plug&play* API function is:

- tat964_setStaticState

Configuring the I/O Channels

Configuring the channels is a three step process:

1. Select the channels.
2. Program channel parameters.
3. Configure channel properties.

Access this panel from the menu bar: **Config > Channels**.

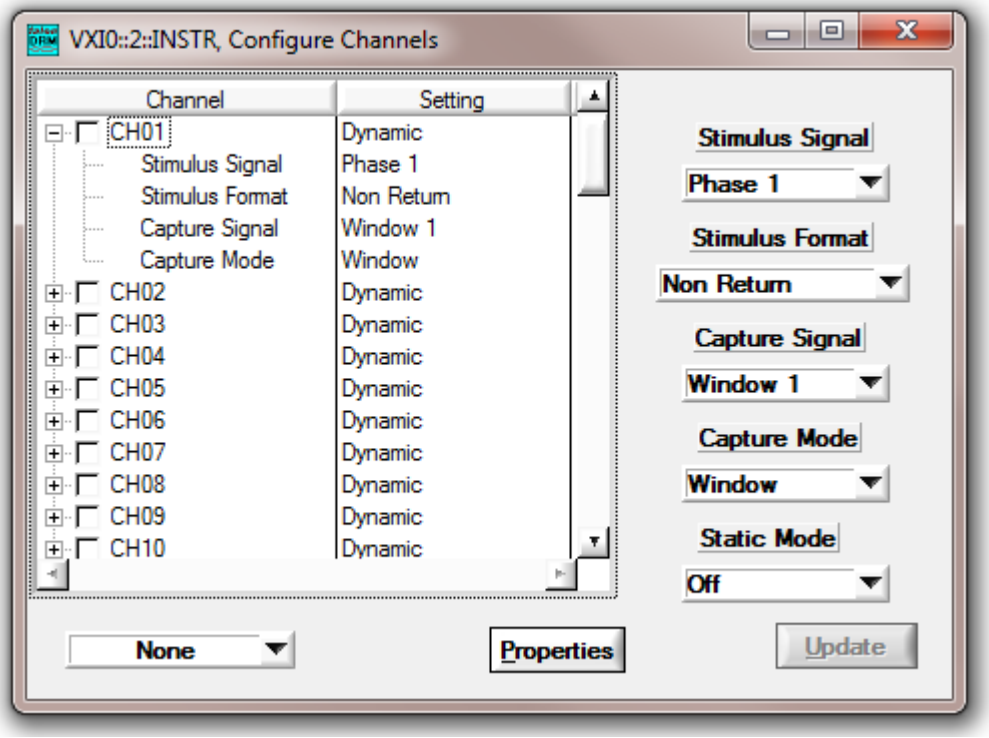


Figure 5-29: Configure Channels Panel

Selecting the Channels

Before the channel parameters or properties can be programmed, the channels must be selected. There are two methods for selecting the channels:

1. Left click on the desired channel in the channel list control. A check mark indicates the channel has been selected. Multiple channels can be selected.
2. Use the pull down list box to select the desired channels and press the **Select** command button. The choices include:
    - None – De-selects all channels.
    - DRA – Selects CH1 through CH32.
    - DRB – Selects CH33 through CH64.
    - DRA & DRB – Selects CH1 through CH64.
    - Group 1 – Selects group 1 channels (DR4 CH1 through CH16)
    - Group 2 – Selects group 2 channels (DR4 CH17 through CH32)
    - Group 3 – Selects group 3 channels (DR4 CH33 through CH48)

Channel Parameters

The channel parameters consist of:

- Stimulus Signal
- Stimulus Format
- Capture Signal
- Capture Mode
- Static Mode

After any of the channel parameters have been changed, the **Update** command button must be depressed in order for the new channel settings to be programmed.

Stimulus Signal

This pull-down control programs the drive phase timing for the selected channel(s) stimulus signal.

The selections for this pull-down control are:

Table 5-55: Stimulus Signal Settings

Setting	Description
Phase 1	Use phase 1 timing signal to control output driver timing.
Phase 2	Use phase 2 timing signal to control output driver timing.
Phase 3	Use phase 3 timing signal to control output driver timing.
Phase 4	Use phase 4 timing signal to control output driver timing.

The relevant VXI*plug&play* API function is:

- tat964_setChannelParameters

Stimulus Format

This pull-down control programs the stimulus data formatting for the selected channel(s).

The selections for this pull-down control are:

Table 5-56: Stimulus Format Settings

Setting	Stimulus Format Description
Non Return	• Phase Assert – Output driver goes to level determined by the Pattern Code instruction in Pattern Memory. • Phase Return – No action.
Return Off	• Phase Assert – Output driver goes to level determined by the Pattern Code instruction in Pattern Memory. • Phase Return – Output driver disables.
Return Zero	• Phase Assert – Output driver goes to level determined by the Pattern Code instruction in Pattern Memory. • Phase Return – Output driver goes to low level.
Return One	• Phase Assert – Output driver goes to level determined by the Pattern Code instruction in Pattern Memory. • Phase Return – Output driver goes to high level.
Return Comp	• Phase Assert – Output driver goes to level determined by the Pattern Code instruction in Pattern Memory. • Phase Return – Output driver goes to complemented level determined by the Pattern Code instruction in Pattern Memory

Setting	Stimulus Format Description
Comp Surround	• Start of Pattern – Output driver goes to complemented level determined by the Pattern Code instruction in Pattern Memory • Phase Assert – Output driver goes to level determined by the Pattern Code instruction in Pattern Memory. • Phase Return –Output driver goes to complemented level determined by the Pattern Code instruction in Pattern Memory **Note:** For this format to work effectively, the assert must be at least 15 ns (depends on the swing and slew-rate programmed).
Force Low	• Output driver goes to low level immediately after an update.
Force High	• Output driver goes to high level immediately after an update.
Force Off	• Output driver goes disables immediately after an update.
Force /Phase	• Phase Assert – Output driver goes from high to low level. • Phase Return – Output driver goes from low to high level. • Output driver coincides with the complement of the phase immediately after an update.
Force Phase	• Phase Assert – Output driver goes from low to high level. • Phase Return – Output driver goes from high to low level. • Output driver coincides with the phase immediately after an update.

Note: *The last five settings, above, will only go to the new output state if the Channels drivers are enabled and power is applied. See* ***Channel Driver*** *and* ***V+/V-*** *in the* ***Execute Panel Modes and Settings*** *section of this chapter).*

The relevant VXI*plug&play* API function is:

- tat964_setChannelParameters

Capture Signal

This pull-down control programs the selected channel(s) capture signal.

The selections for this pull-down control are:

Table 5-57: Capture Signal Settings

Setting	Description
Window 1	Use Window 1 timing signal to control input comparator timing.
Window 2	Use Window 2 timing signal to control input comparator timing.
Window 3	Use Window 3 timing signal to control input comparator timing.
Window 4	Use Window 4 timing signal to control input comparator timing.

The relevant VXI*plug&play* API function is:

- tat964_setChannelParameters

Capture Mode

This pull-down control programs the selected channel(s) capture mode.

The selections for this pull-down control are:

Table 5-58: Capture Mode Settings

Setting	Description
Masked	Disables the channel error test
Open Edge	Channel error test and data capture performed on the Open edge of the window
Close Edge	Channel error test and data capture performed on the Close edge of the window
Window	Channel error test and data capture performed between the Open edge and the Close edge of the window

The relevant VXI*plug&play* API function is:

- tat964_setChannelParameters

Static Mode

This pull-down control programs static mode for the selected channel(s).

When the Static Mode Enable is set to on, the designated channel is put into the Static Mode and whatever is currently in the Static Broadside Stimulus Register will be applied to the output. Channels not in Static Mode will operate in the normal dynamic mode. When the channel is returned from Static to Dynamic Mode, dynamic operation will resume as though it had never been put into the Static Mode.

The selections for this pull-down control are:

Table 5-59: Static Mode Settings

Setting	Description
Off	Static Mode enabled for selected channel(s).
On	Static mode disabled for selected channel(s.

Note: *The static state must be enabled before setting the static mode.*

The relevant VXI*plug&play* API function is:

- tat964_setStaticMode

Properties

This command button allows the user to configure the driver/receiver properties. See next section for additional information.

Configure Channel Properties

The channel properties consist of the following nine elements:

1. Driver Levels
2. Comparator Levels
3. Driver Slew Rate
4. Output Impedance
5. Over-Current Alarm Levels
6. Programmable Load
7. Channel Connect
8. Hybrid Connect
9. Channel Mode

These program the properties of the specific Driver/Receiver boards that are installed. Not every Driver/Receiver board supports all nine elements. If a Driver/Receiver board does not support a property and you select it, a **Soft Front Panel Error** message box, similar to the following, appears. Click **Ignore** to clear the error and return to the control panel.

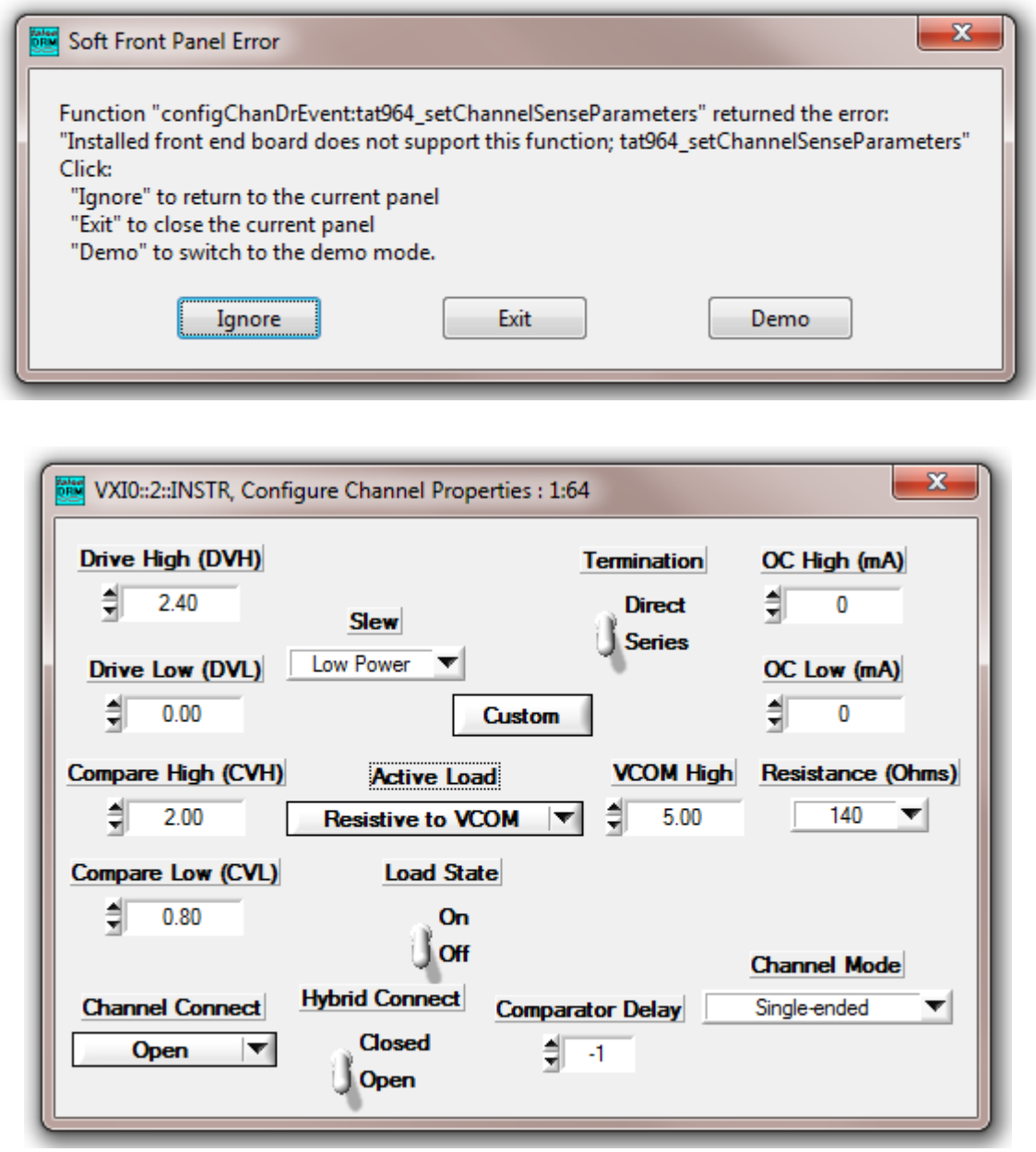


Figure 5-30: Configure Channel Properties Panel

Driver Levels

The driver levels allow the user to set the **Drive High (DVH)** and **Drive Low (DVL)** voltage.

The min/max levels are dependent on the installed Driver/Receiver board as well as the voltage mode.

Note: *The external supply voltages will also need to be adequate for the desired drive levels when using the DR3e with external power option.*

The relevant VXI*plug&play* API function is:

- tat964_setChannelSourceLevels

Comparator Levels

The comparator levels allow the user to set the **Compare High (CVH)** and **Compare Low (CVL)** voltage.

The min/max levels are dependent on the installed Driver/Receiver board as well as the voltage mode.

Note: *The external supply voltages will also need to be adequate for the desired drive levels when using the DR3e external power option.*

The relevant VXI*plug&play* API function is:

- tat964_setChannelSenseLevels

Driver Slew

The driver slew allows the user to set the output **Slew Rate**.

The selections for this pull-down control are:

Table 5-60: Slew Settings

Setting	Description
Fast	Sets the DR3e/DR9/UR14 slew rate to ~1.3 V/ns
Medium	Sets the DR3e/DR9/UR14 slew rate to ~1.0 V/ns
Default	Sets the DR3e/DR9/UR14 slew rate to ~0.7 V/ns
Slow	Sets the DR3e/DR9/UR14 slew rate to ~0.25 V/ns
Low Power	Sets the DR3e/DR9/UR14 slew rate to <0.1 V/ns

Depressing the **Custom** command button allows the user to specify the DR3e/DR9/UR14 **+ Slew Rate**, **- Slew Rate** and **Bias**.

The range for the **+ Slew Rate** and **– Slew Rate** is from 3 (slowest) to 31 (fastest).

The range for the **Bias** is (slowest to fastest) 4, 5, 6, 7, 0, 1, 2, and 3. The fastest slew rate would be with a value of 31 and a bias of 3.

The relevant VXI*plug&play* API functions are:

- tat964_setChannelSlewRate
- tat964_setChannelSourceParameters

Termination

This allows the user to set the termination as direct or series. See specific Driver/Receiver board appendix for termination values.

The relevant VXI*plug&play* API function is:

- tat964_setChannelSourceParameters

Over-Current Alarm Levels

This allows the user to set the over-current high (**OC High (mA)**) and over-current low (**OC Low (mA)**) alarm levels for static current limits on the DR3e, DR9, and UR14 (see **Drive Fault** for dynamic current limiting). When the driver current exceeds the level, an over-current signal will be generated.

The range for **OC High** is from 0 (disable over-current monitor) to 800.

The range for **OC Low** is from 0 (disable over-current monitor) to -800.

The relevant VXI*plug&play* API function is:

- tat964_setChannelSourceParameters

Active Load

Depending on the installed Driver/Receiver board, the user can chose one of several programmable or selectable loads.

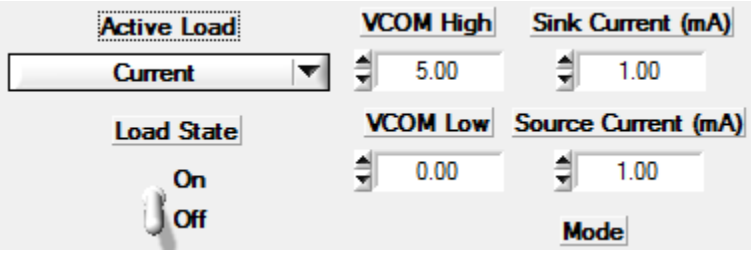
The selections for this pull-down control are:

Table 5-61: Active Load Settings

Setting	Description
None	No active load
Current	Programmable current load
Resistive to VCOM	Selectable resistive load
Resistive to VCC	Fixed resistive load
Resistive to GND	Fixed resistive load
Resistive to VCC+GND	Fixed resistive load

The programmable current load allows the user to specify a source and sink current load and a commutating voltage (VCOM).

Note: *VCC=3.3V for the DR1.*



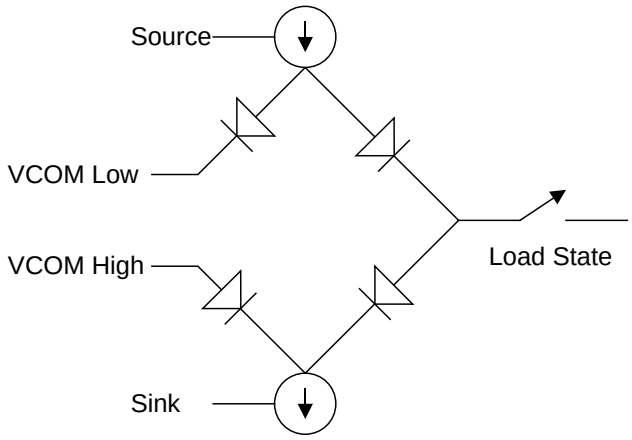


Figure 5-31: Current Load

When the channel voltage is greater than the VCOM High level, the Sink current becomes active. When the channel voltage is less than the VCOM Low level, the Source current becomes active.

The resistive load to VCOM allows the user to select resistance to the VCOM High level.

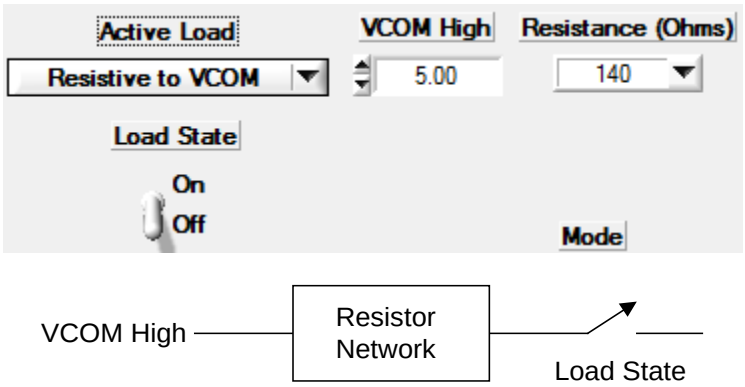


Figure 5-32: Resistive to VCOM Load

The selections for this pull-down control are:

Table 5-62: Resistive Settings

Setting	Description
140	Resistive load set to 140 Ω
151	Resistive load set to 151 Ω
165	Resistive load set to 165 Ω
207	Resistive load set to 207 Ω
240	Resistive load set to 240 Ω
290	Resistive load set to 290 Ω
540	Resistive load set to 540 Ω
1040	Resistive load set to 1040 Ω

The relevant VXI*plug&play* API functions are:

- tat964_setChannelSenseParameters
- tat964_setChannelLoadState

Channel Connect

This control allows the user to control the isolation and analog bypass relays.

The selections for this pull-down control are:

Table 5-63: Channel Connect Settings

Setting	Description
Open	Isolation and Analog Bypass Relay Open
Closed	Isolation Closed, Analog Bypass Open
Analog Bypass	Isolation Open, Analog Bypass Closed

***Note**: DR2 and DR7 Driver/Receiver boards do not have relay isolation. DR9 is the only Driver/Receiver board with the analog bypass relay.*

The relevant VXI*plug&play* API function is:

- tat964_setChannelConnect

Hybrid Connect

This control allows the user to connect any of the I/O channels to a pin on the front panel called EXTFORCE.

***Note**: Despite being called EXTFORCE, it may be used to drive or sense the channel pin.*

When the hybrid connection is turned "On" the driver is forced into high impedance and the front panel "EXTFORCE" pin is connected to the channel. There is a series resistance of ~40 ohms between EXTFORCE and the Channel.

***Note**: The Channel Connect relay also needs to be closed. Note: The bandwidth is also limited to ~3 MHz.*

When the hybrid connection is turned "Off" the driver is enabled and the front panel "EXTFORCE" pin is disconnected from the channel.

The relevant VXI*plug&play* API function is:

- tat964_setChannelHybridState

Comparator Delay

This allows the user to add delay to the comparator inputs for DR3e, DR9, and UR14 front end channels.

The range for **Comparator Delay** is from -1 (bypass delay) to 31 (~19.35ns) 625ps per count.

The relevant VXI*plug&play* API function is:

- tat964_setComparatorDelay

Channel Mode

This control programs the front panel channel mode setting.

The channel mode can be set to:

- Single-ended
- Differential with 100 Ω differential termination
- Differential no termination

When set to differential, adjacent odd and even channels are grouped as a single channel with the odd channel as the positive and the even channel as negative.

For example:

If the channel list is 1, 2, 5, 6, then channel 1 and 2 are grouped and channel 5 and 6 are grouped as follows,

CH1 = Diff CH1+

CH2 = Diff CH1-

CH5 = Diff CH3+

CH6 = Diff CH3-

If no other differential groups are assigned then,

CH3 = Single-ended CH3

CH4 = Single-ended CH4

CH7 = Single-ended CH7

The relevant VXI*plug&play* API function is:

- tat964_setChannelMode

Configure UR14 Channel Properties

The UR14 channel settings consist of a single threshold compare level and an over current detect level programmed in groups of eight channels.

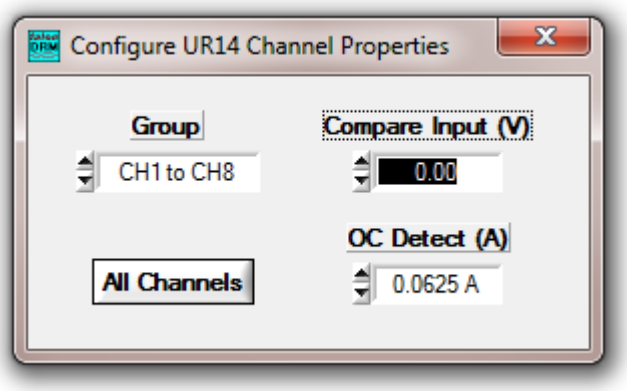


Figure 5-33: Configure UR14 Channel Properties Panel

Compare Input (V)

This control sets the comparator level of the selected channel group.

Min: 0.0

Max: 20.0

The relevant VXI*plug&play* API function is:

- tat964_setUtilitySenseLevel

OC Detect (A)

This allows the user to set the over-current threshold of the selected channel group.

The detect level can be set from 0.0 A to 1 A in increments of 62.5 mA.

The relevant VXI*plug&play* API function is:

- tat964_setUtilitySourceParameter

All Channels

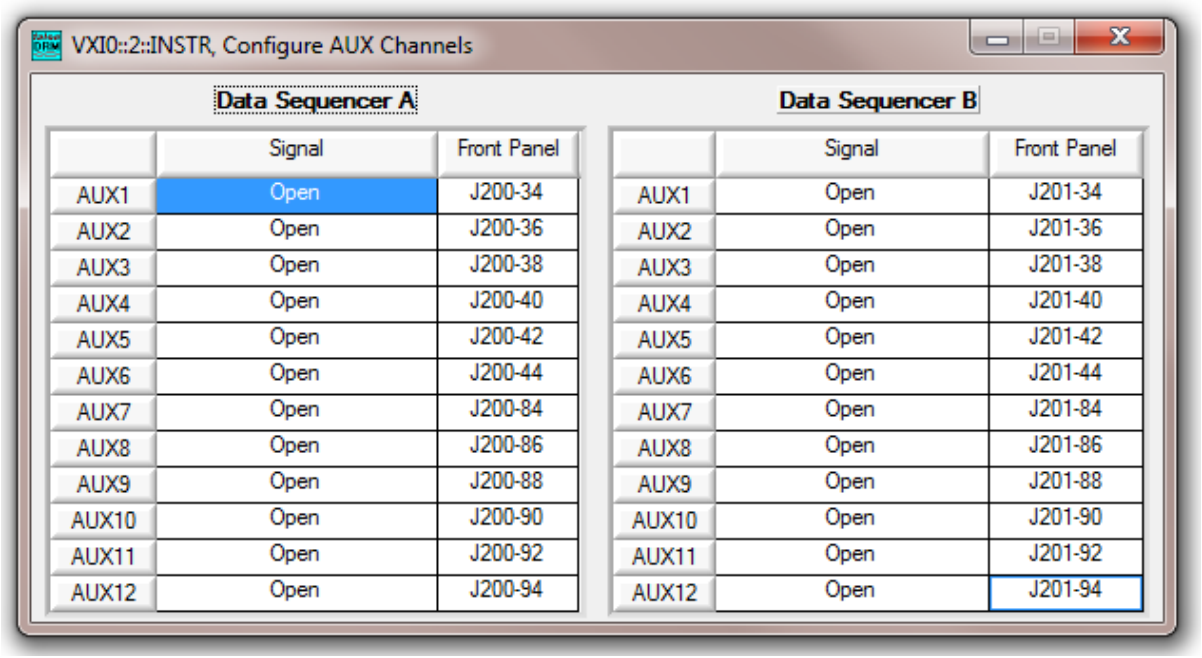
Sets the compare input and OC detect levels of all four channel groups to the current panel settings.

The relevant VXI*plug&play* API functions are:

- tat964_setUtilitySenseLevel
- tat964_setUtilitySourceParameter

Configuring the AUX Channels

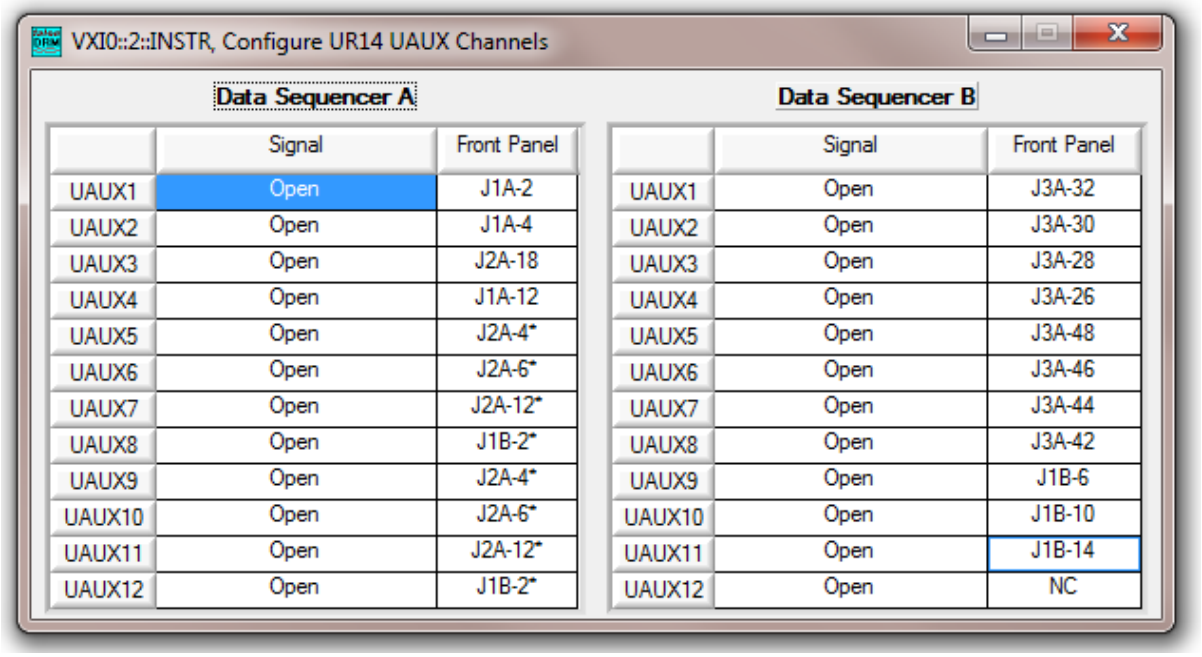
Access this panel from the menu bar: **Config > AUX Outputs**.



	Signal	Front Panel
AUX1	Open	J200-34
AUX2	Open	J200-36
AUX3	Open	J200-38
AUX4	Open	J200-40
AUX5	Open	J200-42
AUX6	Open	J200-44
AUX7	Open	J200-84
AUX8	Open	J200-86
AUX9	Open	J200-88
AUX10	Open	J200-90
AUX11	Open	J200-92
AUX12	Open	J200-94

	Signal	Front Panel
AUX1	Open	J201-34
AUX2	Open	J201-36
AUX3	Open	J201-38
AUX4	Open	J201-40
AUX5	Open	J201-42
AUX6	Open	J201-44
AUX7	Open	J201-84
AUX8	Open	J201-86
AUX9	Open	J201-88
AUX10	Open	J201-90
AUX11	Open	J201-92
AUX12	Open	J201-94

Figure 5-34: Configure AUX Channels Panel



	Signal	Front Panel
UAUX1	Open	J1A-2
UAUX2	Open	J1A-4
UAUX3	Open	J2A-18
UAUX4	Open	J1A-12
UAUX5	Open	J2A-4*
UAUX6	Open	J2A-6*
UAUX7	Open	J2A-12*
UAUX8	Open	J1B-2*
UAUX9	Open	J2A-4*
UAUX10	Open	J2A-6*
UAUX11	Open	J2A-12*
UAUX12	Open	J1B-2*

	Signal	Front Panel
UAUX1	Open	J3A-32
UAUX2	Open	J3A-30
UAUX3	Open	J3A-28
UAUX4	Open	J3A-26
UAUX5	Open	J3A-48
UAUX6	Open	J3A-46
UAUX7	Open	J3A-44
UAUX8	Open	J3A-42
UAUX9	Open	J1B-6
UAUX10	Open	J1B-10
UAUX11	Open	J1B-14
UAUX12	Open	NC

Figure 5-35: Configure AUX Channels Panel UR14

The AUX channels are a set of 12 multi-purpose signals that can be used for any of the following I/O resources:

1. Trigger Source Input
2. Frequency Synthesizer Reference Clock Input
3. System Clock Input

4. Vector Jump Address Input
5. Waveform Output
6. Pulse Generator Output
7. Sync Output
8. Frequency Synthesizer Output
9. Timing Set Output Signals
    a. Phase
    b. Window
    c. T0_CLK
    d. Pattern Clock
10. Sequencer Status Outputs
    a. Idle Active
    b. Sequence Active
    c. Sequence Flag
    d. Pass/Fail
    e. Error
11. Numerous Factory Test Outputs

Table 5-64: DRn AUX Configuration

Driver/Receiver Board	AUX1-AUX4	AUX5-AUX8	AUX9-AUX12
DR1	LVTTL	LVTTL	ECL
DR2	LVDS	LVTTL	ECL
DR3E	Programmable	LVTTL	ECL
DR4	TTL	TTL	Not Installed
DR7	RS422/485	LVTTL	ECL
DR8	TTL	TTL	ECL
DR9	Not installed	LVTTL	Not Installed

Table 5-65: UR14 AUX Configuration

Signal	Logic	Special Use
AUX1 A, AUX2 A	Programmable	Used for probe input (AUX1) and probe cal (AUX2)
AUX3 A, AUX4 A	LVTTL	AUX4 used for probe compensation.
AUX5 A	LVTTL	Shares front panel pin with AUX9 A

Signal	Logic	Special Use
AUX6 A	LVTTL	Shares front panel pin with AUX10 A
AUX7 A	LVTTL	Shares front panel pin with AUX11 A
AUX8 A	LVTTL	Shares front panel pin with AUX12 A
AUX9 A	ECL differential or bipolar	Shares front panel pin with AUX5 A
AUX10 A	ECL differential or bipolar	Shares front panel pin with AUX6 A
AUX11 A	ECL differential or bipolar	Shares front panel pin with AUX7 A
AUX12 A	ECL differential or bipolar	Shares front panel pin with AUX8 A
AUX1 B-AUX4 B	Programmable	General purpose
AUX5 B-AUX8 B	LVTTL/Bipolar ECL selectable	General purpose
AUX9 B-AUX12 B	ECL differential or bipolar	General purpose

Configuring the AUX/UAUX Signals

Configuring the AUX/UAUX signal is done by double clicking the left mouse button on the signal name corresponding to the desired AUX number.

Refer to the specific Driver/Receiver board appendix for AUX capabilities.

All AUX and UAUX signals share the controls listed in the following figure:

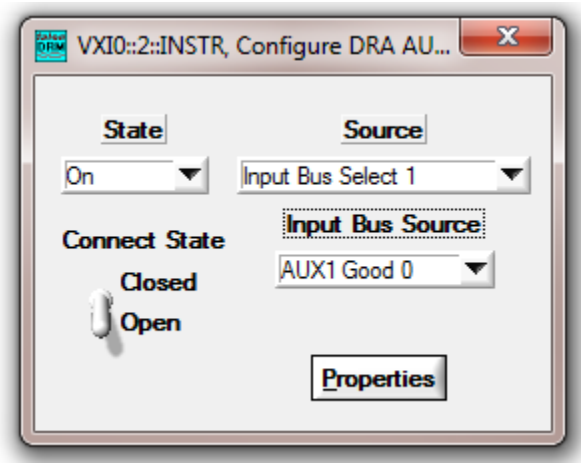


Figure 5-36: Shared AUX/UAUX Controls

State

This control allows the user to set the output state for the selected AUX signal.

Table 5-66: AUX Output State Settings

Setting	Description
Off	Disable the AUX output.
On	Enable the AUX output.
Inv	Enable and invert the AUX output.

The relevant VXI*plug&play* API function is:

- tat964_setAuxOutputSignal

Source

This control is visible when the state is set to **On** or **Inv** and allows the user to set the output source for the selected AUX signal.

Table 5-67: AUX Source Settings

Setting	Description
Phase 1-4	Phase timing signal.
Window 1-4	Window timing signal.
Waveform 1-4	Waveform signal.
Sync 1,2	Sync signal.
Idle Active	1 = Active, 0 = Not Active.
Sequence Active	1 = Active, 0 = Not Active.
Channel good 1*	Channel good 1 comparator signal
Channel good 0*	Channel good 0 comparator signal
Waveform 5	Waveform 5 signal
Waveform 6	Waveform 6 signal
Input Bus Select 1-4**	Input Bus Select Signal
Seq. Flag 1,2	Sequence flag signal.
T0CLK_In	Test signal
Pattern Clock	Test signal
SEQ_CLK In	Test signal
Jump In	Test signal
Raw Error	Test signal
SEQ_CLK_D_In	Test signal
T0CLK Out	Test signal
SEQ_CLK Out	Test signal
Jump Out	Test signal
SEQ_CLK_D_Out	Test signal
Pulse Generator	Pulse generator signal
Record Active	1 = Active, 0 = Not Active.

Setting	Description
FS Reference	Frequency synthesizer reference signal
Frequency Synthesizer	Frequency synthesizer signal
Jump Strobe	Test signal
Int Error	Test signal
Ext Error	Test signal
HIGH	Drive high
PASS	PASS flag
FAIL	FAIL flag
CONDEN	Condition enable flag
BERREN	Burst error enable flag
LSR	Load Sequence Register
LLC	Load Loop Count
CA	Counter Active
CPPD	Clocks per Pattern Done
BCD	Burst Count Done
LCD	Loop Count Done
IN_SUB	Gosub Active
C_LOOP	Counted Loop
SUBRT	Subroutine Return
RTN	Return Flag
LSTSEQ	Last Sequence
Jump Test 1-4	Test signal

*The Channel Good 1/Channel Good 0 selections can select any of the front end channels using the “tat964_setAuxChannelSelect” API.

**The Input Bus Select selections can select any of the AUX, TTL or ECL trigger, Local Trigger Bus, or Channel Test 1 using the “tat964_setAuxInputBusSelect” API.

The relevant VXI*plug&play* API function is:

- tat964_setAuxOutputSignal

Input Bus Source

This control is visible when the Source control is set to one of the four **Input Bus Select** signals. It selects the source for the seleced input bus select.

Table 5-68: Input Bus Select Source Settings

Setting	Description
AUX1 Good 0	Source set to AUX1 Good zero signal.
AUX1-12 Good 1	Source set to AUXn Good one signal.
CHT1	Source set to channel test 1

Setting	Description
ECLTRG0,1	Source set to VXI ECL trigger
TTLTRG0-7	Source set to VXI TTL trigger
LTB0-7	Source set to Linked Trigger bus signal

Connect State

This control allows the user to open or close the isolation relay.

DR2 and DR7 Driver/Receiver boards do not have isolation relays.

The relevant VXI*plug&play* API function is:

- tat964_setAuxConnect

Note: *DR2 and DR7 Driver/Receiver boards do not have relay isolation.*

Properties (Programmable Logic)

This command button displays the panel to allow the user to configure the Programmable AUX Driver/Receiver settings. Refer to **Configure Channel Properties**, earlier in this chapter, for control descriptions for this panel.

The relevant VXI*plug&play* API functions are:

- tat964_setAuxSourceLevels
- tat964_setAuxSourceParameters
- tat964_setAuxSlewRate
- tat964_setAuxSenseLevels
- tat964_setAuxSenseParameters
- tat964_setAuxLoadState

ECL Mode (ECL Differential or Bipolar Logic)

This control allows the user to select the ECL mode.

Table 5-69: ECL Mode Settings

Setting	Description
Bipolar	AUX configured as bipolar ECL.
Differential	AUX configured as differential ECL

The relevant VXI*plug&play* API function is:

- tat964_setAuxEclMode

Logic Mode (LVTTL/Bipolar ECL Logic)

This control allows the user to select the LVTTL/ECL mode.

Table 5-70: Logic Mode Settings

Setting	Description
LVTTL	AUX configured as LVTTL.
ECL Bipolar ECL	AUX configured as differential ECL

The relevant VXI*plug&play* API function is:

- tat964_setAuxLogicMode

Configuring the Interrupts

There are five hardware groups on the T940 that are capable of generating a VXI interrupt. VXI interrupts are generated from events in the hardware. Each event has an enable that allows it to pass the event to the interrupt logic on the digital board.

The five hardware groups are:

1. Data Sequencer A – Enables set in the **Execute > DSA > View > Sequence Events** panel**.**
2. Data Sequencer B – Enables set in the **Execute>DSB > View > Sequence Events** panel**.**
3. Driver/Receiver Board A – Enables set in the **Execute > DSA > View > Driver/Receiver Events** panel**.**
4. Driver/Receiver Board B – Enables set in the **Execute > DSB > View > Driver/Receiver Events** panel**.**
5. Digital Board

The events that can generate an interrupt depend on the specific hardware installed.

The Digital Board can generate these two events:

1. CPU Interrupt
2. Sequencer FPGA Temperature Alert

Access this panel from the menu bar: **Config > Interrupts**.

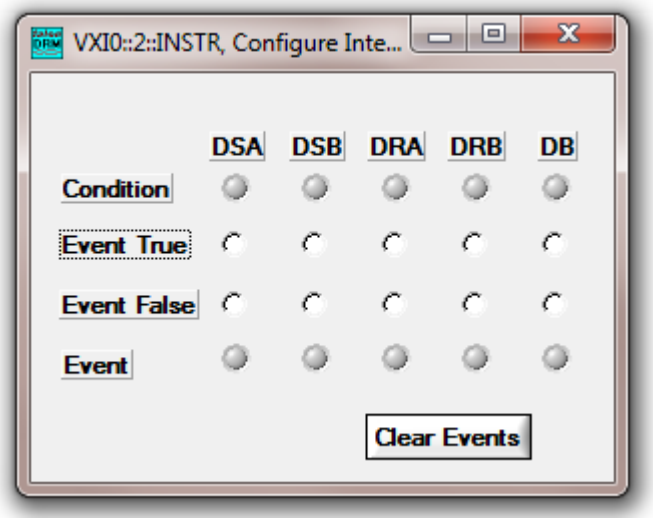


Figure 5-37: Configure Interrupt

Condition

This control indicates that the interrupt condition is currently true.

The relevant VXI*plug&play* API function is:

- tat964_queryInterruptCondition

Event True

This control enables a VXI interrupt to be generated when any of the associated hardware groups enabled event bits goes from false to true.

The relevant VXI*plug&play* API function is:

- tat964_setInterruptMode

Event False

This control enables a VXI interrupt to be generated when any of the associated hardware groups enabled event bits goes from true to false.

The relevant VXI*plug&play* API function is:

- tat964_setInterruptMode

Event

This control indicates that the event is currently true.

The relevant VXI*plug&play* API function is:

- tat964_queryInterruptEvent

Editing the Data Sequencers

Editing the data sequencers consists of programming the following:

1. Timing Sets
2. Patterns
3. Waveforms
4. Sequence Parameters
5. Sequence Steps

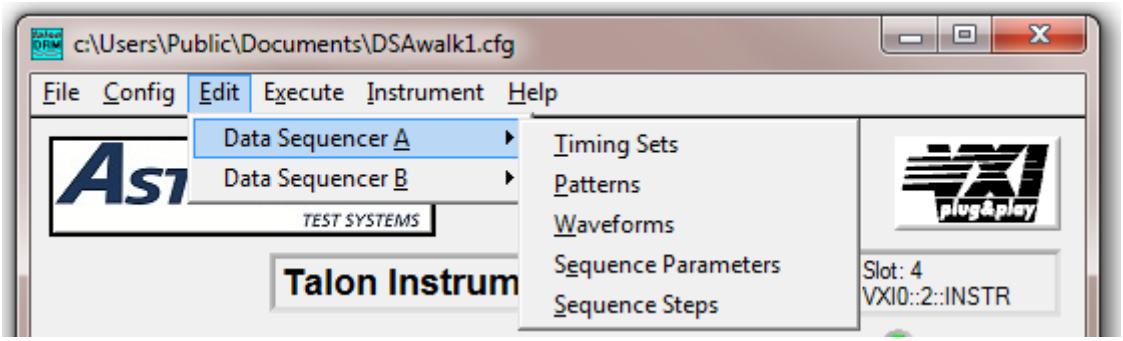


Figure 5-38: Editing the Data Sequencers

Editing the Timing Sets

The timing sets are used to control the channel drivers and receivers. Each timing set has either one or four phase/window groups based on the programmed timing mode.

Phases control the driver operation and consist of an **Assert** and a **Return.** The Assert signal loads the next pattern code in to the output driver. Pattern codes are discussed in the next section. The Return signal is used to enable the format code in the driver. The Return signal is not used for the Non Return format code. (See **Stimulus Format** earlier in this chapter.)

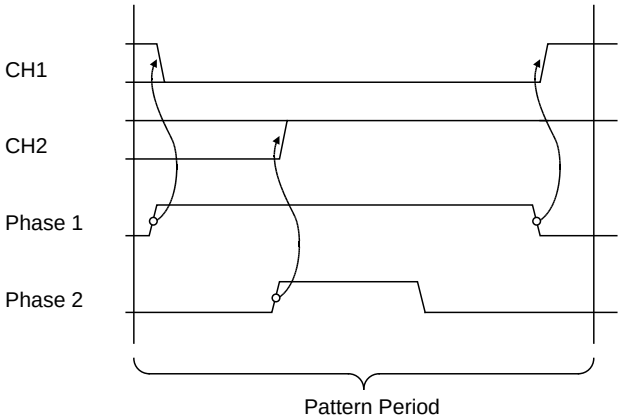


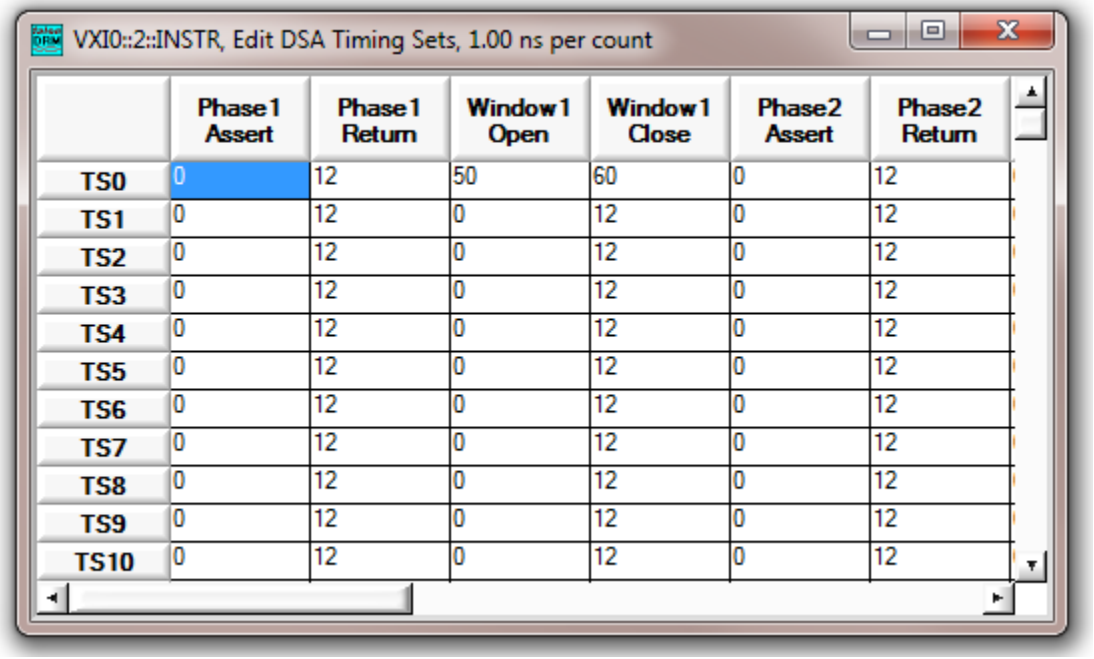
Figure 5-39: Phase Timing

The figure above represents two channels with the following configuration:

- CH1 Output Signal = Phase 1
  Stimulus Format = Return to One
  Pattern Code = Drive Low
- CH2 Output Signal = Phase 2
  Stimulus Format = Non Return
  Pattern Code = Drive High

The **Assert** signal (rising edge) causes the pattern code to be loaded. The **Return** signal (falling edge) causes the Stimulus Format to output. Since CH2 is set to Non Return, the Return signal did not affect the output level.

Access this panel from the menu bar: **Edit > Data Sequencer *x*> Timing Sets**. (Where "x" is the sequencer you wish to configure.)



	Phase1 Assert	Phase1 Return	Window1 Open	Window1 Close	Phase2 Assert	Phase2 Return
TS0	0	12	50	60	0	12
TS1	0	12	0	12	0	12
TS2	0	12	0	12	0	12
TS3	0	12	0	12	0	12
TS4	0	12	0	12	0	12
TS5	0	12	0	12	0	12
TS6	0	12	0	12	0	12
TS7	0	12	0	12	0	12
TS8	0	12	0	12	0	12
TS9	0	12	0	12	0	12
TS10	0	12	0	12	0	12

Figure 5-40: Data Sequencer Timing Sets Panel

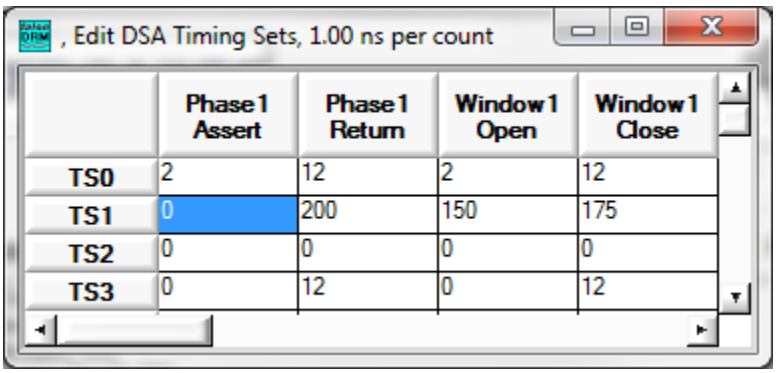
To program a timing set, scroll down the list until the desired timing set number is visible. Timing set numbers are assigned based on the current timing mode:

- Per Step Multi – 1024 timing sets with four phase/window groups per timing set. TS0 is the timing for sequence step 1, TS1 is the timing for sequence step 1, … , timing set 1023 is the timing for sequence step 1023.
- Per Step Single - 4096 timing sets with one phase/window group per timing set. TS0 is the timing for sequence step 1, TS1 is the timing for sequence step 1, … , timing set 4095 is the timing for sequence step 4095.

- Indexed – 256 timing sets with four phase/window groups per timing set and 4096 sequence steps where each sequence step points to one of the 256 timing sets.

Double-click on one of the available Assert/Return/Open/Close cells. Enter the desired value using the numeric keys or the up/down arrows followed by the Enter key. The timing value resolution is displayed in the title bar area of the panel. Timing resolution is controlled by the Master Clock setting. Use "tat964_setMasterClockSource" and "tat964_setFreqSynth" API functions to change the timing resolution.

The user can disable the timing set phases/windows by setting Assert/Return and Open/Close values to zero. For example, Phase 1 and Window 1 are disabled during TS2 in the configuration shown below.



The relevant VXI*plug&play* API function is:

- tat964_setTimingSetData

Timing Set Value Rules

For valid timing signal operation, the following rules must be followed:

- Phase pulse width must be greater than seven, i.e., the Return value must be at least eight more than the Assert value.
- Window pulse width must be greater than seven, i.e., the Close value must be at least eight more than the Open value.
- End of pattern dead time. Phase Return and Window Close values must occur eight counts or more before the end of the pattern. Additionally a Window Close must occur 13 ns prior to the end of the pattern period.
- Phases and Windows are allowed to extend past the initial pattern period if multiple clocks per pattern (CPP > 1) are programmed. (See **Clocks per Pattern** later in this chapter.)

Advanced Timing Set Features

Two advanced timing set features are available:

1. Phase/Window Spanning

2. Idle/Standby Timing

Phase/Window Spanning

Phase/Window spanning allows the user to Assert/Open the timing signal in one pattern and Return/Close the signal in a different pattern. The following steps describe how to span timing signals across multiple patterns:

1. Disable the Return signal in the first pattern's timing set by setting the Return value equal to the pattern period.
2. Disable the Assert and Return signal in any patterns between the first and the last pattern being spanned by setting the Assert Value to zero and the Return value equal to the pattern period.
3. Disable the Assert signal in the last pattern by setting the Assert Value to zero.

For example, let's assume we have three patterns and each pattern has a period of 100. We want the Phase 1 Assert at 50 of the first pattern and Return at 75 of the third pattern.

Pattern 1, TS1 = Assert 50, Return 100

Pattern 2, TS2 = Assert 0, Return 100

Pattern 3, TS3 = Assert 0, Return 75

Idle/Standby Timing

One of the unique features of the DRM is the Idle/Standby state. After the execution of a sequence burst, the sequencer will enter the Idle/Standby state. The user can define the Idle/Standby state timing and pattern such that UUT stimulus can be maintained between pattern bursts. A single pattern can be specified so that the pattern memory can be updated (Standby) or a group of patterns can be specified (Idle) during this state.

The user can disable the timing set phases/windows during the Idle/Standby state by setting Assert/Return and Open/Close values to zero.

Editing the Patterns

Patterns are the memory element that contains the instructions for each channel during a sequence burst. These instructions, called pattern codes, define whether a channel will drive high, drive low, test high, etc.

Once a sequence step has been initialized, a pattern set is assigned to the step. A **Pattern Set** is one or more patterns. A **Pattern** is the pattern codes for all the channels that will be applied at the same time. (See **Patterns** in **Chapter 5**.)

Access this panel from the menu bar: **Edit > Data Sequencer *x* > Patterns**. (Where "x" is the sequencer you wish to configure.)

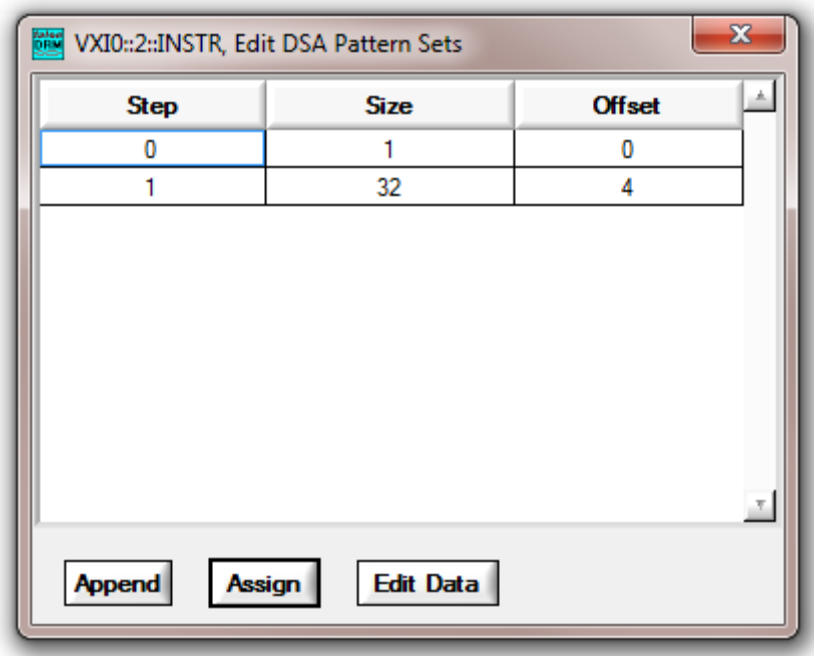


Figure 5-41: Edit Patterns Panel

This panel lists all the defined pattern sets. The associated step number, size and offset are displayed.

The size of a pattern set can be from 1 to 262144.

The offset can be from 0 to 262140 and must be a multiple of four.

The relevant VXI*plug&play* API functions are:

- tat964_queryPatternSet
- tat964_queryPatternSetList

Append

This control allows the user to append more patterns to the selected pattern set.

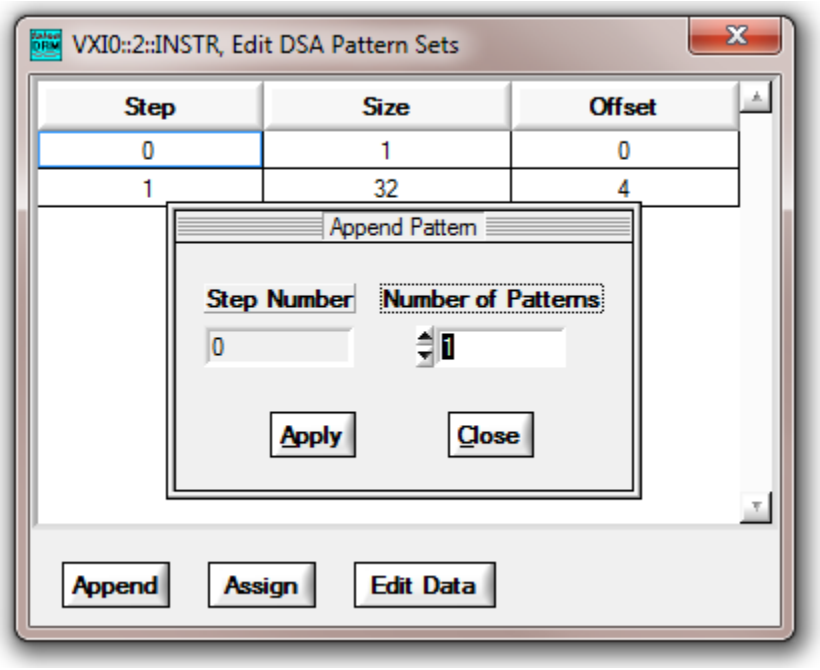


Figure 5-42: Append Data Sequencer Pattern Sets Panel

Enter the **Number of Patterns** to append and press the **Apply** command button. Append pattern memory will be initialized to Pattern Code “R”, which repeats the previous code.

The driver allows pattern set overlaps when appending patterns. If you don’t want pattern sets to overlap, make sure there’s enough space for the appended patterns. This can be facilitated by assigning the pattern offset initially (see **Assign** function next).

Press the **Close** command button to exit the panel without any changes.

The relevant VXI*plug&play* API function is:

- tat964_appendPattern

Assign

This control allows the user to assign a new size and/or offset to the selected pattern.

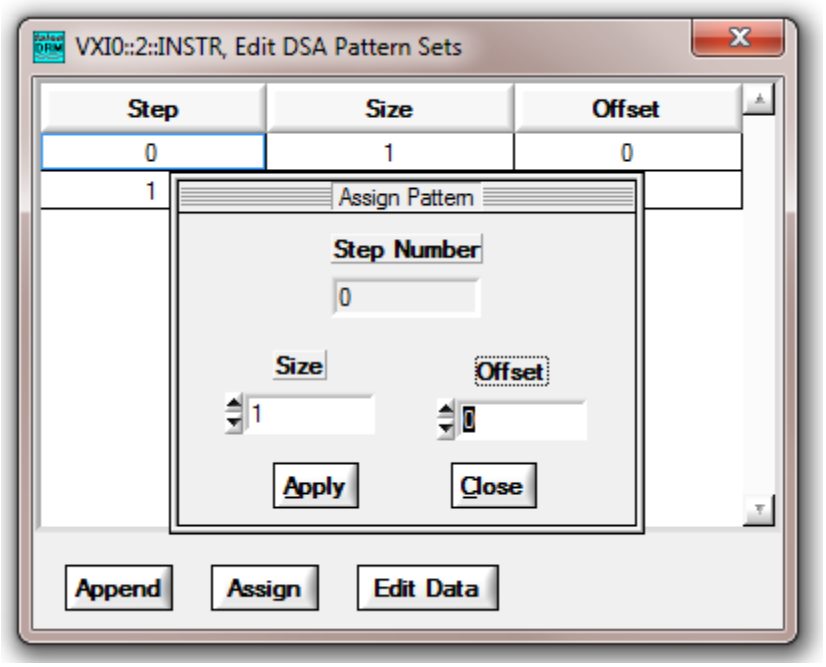


Figure 5-43: Assign Data Sequencer Pattern Sets Panel

Enter the new **Size** and/or **Offset** and press the **Apply** command button. Assigned pattern memory will not be initialized.

Press the **Close** command button to exit the panel without any changes.

The relevant VXI*plug&play* API function is:

- tat964_assignPatternSet

Edit Data

This control displays the view/edit pattern set panel. This panel allows the user to view/edit the contents of the pattern set memory. Double-clicking on the desired pattern set can also open this panel.

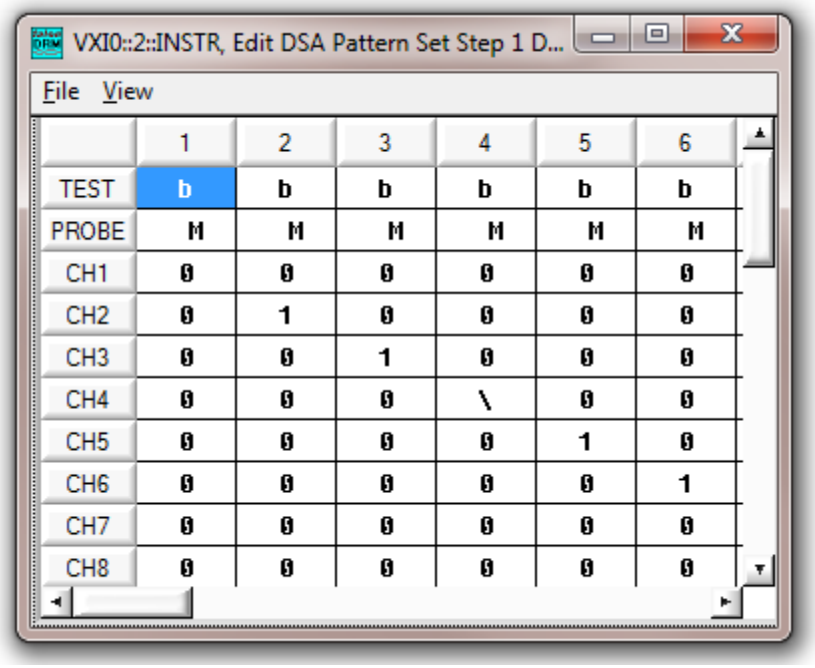


Figure 5-44: Pattern Set Sequencer Data Panel

Each column contains the TEST code, PROBE code and the pattern codes for all the channels. The pattern codes are described in Figure 5-47 and Table 5-TTT.

The pattern set is displayed in pages of 32 patterns. The View menu bar lists the page control shortcuts listed below:

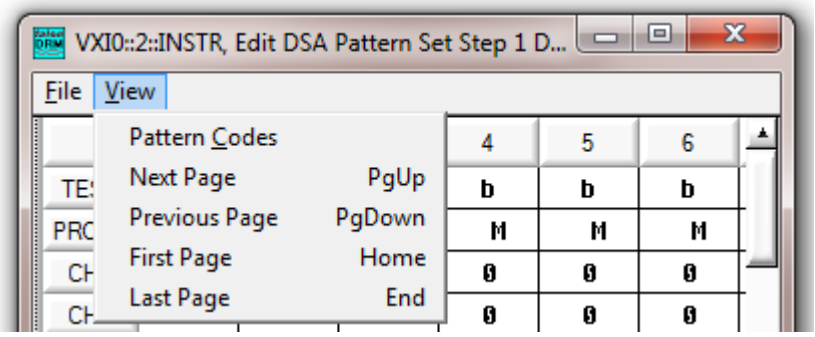


Figure 5-45: Pattern Set Data – View Menu

To jump to a specific pattern number, right click in any of the cells to display the **Goto Pattern** panel

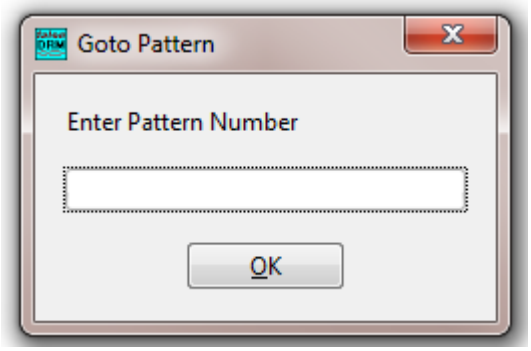


Figure 5-46: Goto Pattern Panel

The menu bar: **View > Pattern Codes** displays a legend of all the available TEST and CH entries.

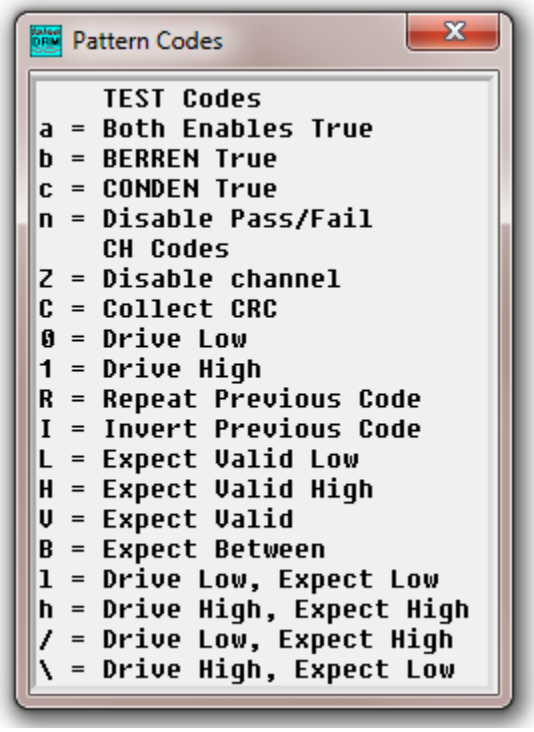


Figure 5-47: Pattern Codes

The row labeled “TEST” displays the test code for each pattern. There are two test flags per pattern:

1. BERREN – Burst Error Enable. This flag allows the user to designate which patterns will be examined for Burst Error, Burst Error counting and the logging of errors in the Error Address Memory.
2. CONDEN – Condition Enable. This flag allows the user to designate which patterns will be considered for PASS/FAIL jump tests.

The row labeled “PROBE” displays the probe expect code for each pattern. There are thirty four probe expect codes:

```
  FE   = Falling Edge 'a'
  FEG  = Falling Edge Glitch 'b'
  FEGM = Falling Edge Glitch Middle 'c'
    H  = High 'd'
   HG  = High Glitch 'e'
   HM  = High Middle 'f'
   HP  = High Pulse 'g'
  HGM  = High Glitch Middle 'h'
  HPL  = High Pulse Low 'i'
  HPM  = High Pulse Middle 'j'
  HGFE = High Glitch Falling Edge 'k'
    L  = Low 'l'
   LG  = Low Glitch 'm'
   LM  = Low Middle 'n'
   LP  = Low Pulse 'o'
  LGM  = Low Glitch Middle 'p'
  LPH  = Low Pulse High 'q'
  LPM  = Low Pulse Middle 'r'
  LGRE = Low Glitch Rising Edge 's'
    M  = Middle 't'
   MH  = Middle High 'u'
   ML  = Middle Low 'v'
  MFE  = Middle Falling Edge 'w'
  MRE  = Middle Rising Edge 'x'
  MGH  = Middle Glitch High 'y'
  MGL  = Middle Glitch Low 'z'
  MHG  = Middle High Glitch '0'
  MLG  = Middle Low Glitch '1'
  MPH  = Middle Pulse High '2'
  MPL  = Middle Pulse Low '3'
  MPM  = Middle Pulse Middle '4'
   RE  = Rising Edge '5'
  REG  = Rising Edge Glitch '6'
  REGM = Rising Edge Glitch Middle '7'
✔   X  = Mask off compare '8'
```

Figure 5-48: Probe Codes

Table 5-71: Probe Expect Codes

Expect Code	Shortcut	Description	Probe Code
FE	a	Signal starts above RH and crosses the RH and RL once and ends below RL.	C9
FEG	b	Signal starts above RH, crosses RH once, crosses RL three or more times and ends below RL.	E9
FEGM	c	Signal starts above RH, crosses RH once, crosses RL two or more times and ends between RL and RH.	E1
H	d	Signal remains above RH.	05
HG	e	Signal starts above RH, crosses the RH two or more times and ends above RH.	55
HM	f	Signal starts above RH, crosses RH once and ends between RL and RH.	41
HP	g	Signal starts above RH, crosses RH and RL two or more times and ends above RH.	F5
HGM	h	Signal starts between RL and RH, crosses the RH two or more times and ends between RL and RH.	51
HPL	i	Signal starts above RH, crosses RL and RH three or more times and ends below RL.	F9
HPM	j	Signal starts above RH, crosses RH three or more times, RL two or more times and ends between RL and RH.	F1
HGFE	k	Signal starts above RH, crosses the RH three or more times, crosses RL once and ends below RL.	D9
L	l	Signal remains below RL.	0A
LG	m	Signal starts below RL, crosses the RL two or more times and ends below RL.	AA
LM	n	Signal starts below RL, crosses the RL once and ends between RL and RH.	22
LP	o	Signal starts below RL, crosses RL and RH two or more times and ends below RL	FA
LGM	p	Signal starts below RL, crosses the RL three or more times and ends between RL and RH.	A2
LPH	q	Signal starts below RL, crosses RL and RH three or more times and ends above RH.	F6
LPM	r	Signal starts below RL, crosses RL three or more times, RH two or more times and ends between RL and RH.	F2
LGRE	s	Signal starts below RL, crosses the RL	B6

Expect Code	Shortcut	Description	Probe Code
		three or more times, crosses RH once and ends above RH.	
M	t	Signal remains between RL and RH	00
MH	u	Signal starts between RL and RH, crosses the RH once and ends above RH.	14
ML	v	Signal starts between RL and RH, crosses the RL once and ends below RL.	88
MFE	w	Signal starts between RL and RH, crosses the RH two or more times, crosses RL once and ends below RL.	D8
MRE	x	Signal starts between RL and RH, crosses the RL two or more times, crosses RH once and ends above RH.	B4
MGH	y	Signal starts between RL and RH, crosses the RH three or more times and ends above RH.	54
MGL	z	Signal starts between RL and RH, crosses the RL three or more times and ends below RL.	A8
MHG	0	Signal starts between RL and RH, crosses the RH two or more times and ends between RL and RH.	50
MLG	1	Signal starts between RL and RH, crosses the RL two or more times and ends between RL and RH.	A0
MPH	2	Signal starts between RL and RH, crosses RL two or more times, RH three or more times and ends above RH.	F4
MPL	3	Signal starts between RL and RH, crosses RL three or more times, RH two or more times and ends below RL.	F8
MPM	4	Signal starts between RL and RH, crosses RH and RL two or more times and ends between RL and RH.	F0
RE	5	Signal starts below RL and crosses the RL and RH once.	36
REG	6	Signal starts below RL, crosses RL once, crosses RH three or more times and ends above RH.	76
REGM	7	Signal starts below RL, crosses RL once, crosses RH two or more times and ends between RL and RH.	72
X	78	Signal starts below RL, crosses RL once, crosses RH two or more times and ends between RL and RH.	NA

The rows labeled CH1 through CH*n* contain the pattern codes for the specified channels. There are fourteen pattern codes. The following table lists how each

pattern code affects the driver/comparator.

Table 5-72: Pattern Codes

Pattern Code	Driver		Comparator Expect	Invert Code
	Mode	Level		
Disable Channel 'Z'	Off	X	None	Disable Channel 'Z'
Collect CRC 'C'	Off	X	Enable CRC	Collect CRC 'C'
Drive High '1'	On	DVH	None	Drive Low '0'
Drive Low '0'	On	DVL	None	Drive High '1'
Repeat Previous Code 'R'	Repeats the last non repeat/invert code.			
Invert Previous Code 'I'	Inverts the last non repeat/invert code. Refer to Invert Code column of this table.			
Expect Valid Low 'L'	Off	X	< CVL	Expect Valid High 'H'
Expect Valid High 'H'	Off	X	> CVH	Expect Valid Low 'L'
Expect Valid 'V'	Off	X	< CVL or > CVH	Expect Between 'B'
Expect Between 'B'	Off	X	> CVL and < CVH	Expect Valid 'V'
Drive Low, Expect Low 'l'	On	DVL	< CVL	Drive High, Expect High 'h'
Drive High, Expect High 'h'	On	DVH	> CVH	Drive Low, Expect Low 'l'
Drive Low, Expect High '/'	On	DVL	> CVH	Drive High, Expect Low '\'
Drive High, Expect Low '\'	On	DVH	< CVL	Drive Low, Expect High '/'

The relevant VXI*plug&play* API functions are:

- tat964_setPatternData
- tat964_setPatternTestEnable
- tat964_setProbeExpectData

The pattern data can be imported/exported using the **File** menu bar selection.

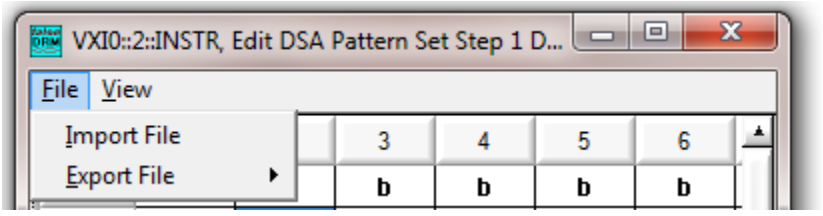


Figure 5-49: Pattern Set Data – File Menu

The import/export formats include:

- Pattern data as ASCII Hex
- Pattern data as ASCII String
- Pattern data as Binary
- Pattern data and flags as ASCII Hex
- Pattern data and flags as ASCII String
- Pattern data and flags as Binary

The relevant VXI*plug&play* API functions are:

- tat964_savePatternMemory
- tat964_loadPatternMemory

Import/Export File Format

The import/export file format consists of a header followed by the data.

The header identifies the number of patterns and the format, and must be the first line of the file.

Header Format

The format of the header is:

[TAT964 PAT DUMP <dd> <nnnnnn>]

where:

<dd> is the format;

00 = Pattern Data ASCII Hex.

01 = Pattern Data Binary

02 = Pattern Data ASCII String

03 = Pattern Data, Flags and Probe Expect ASCII Hex.

04 = Pattern Data, Flags and Probe Expect Binary

05 = Pattern Data, Flags and Probe Expect ASCII String

<nnnnnn> is the number of patterns.

Data Format

The data format consists of three types, ASCII hex, Binary and ASCII string. In addition, each of the three data formats can include or exclude the pattern flags and probe expect.

ASCII Hex

The ASCII hex format represents pattern data as viewable ASCII hex characters, one character per channel. The following table lists the pattern code to ASCII/Binary value translation.

Table 5-73: ASCII/Binary Data Format

Pattern Code	ASCII/Binary Value
'Z'	0
'C'	1
'0'	2
'1'	3
'R'	6
'I'	7
'L'	8
'H'	C
'V'	D
'B'	9
'l'	A
'h'	F
'/'	E
'\'	B

Flag Code	Bit15, Bit 14 Code
'a'	3
'b'	2
'c'	1
'n'	0

Probe Expect	Bit 13 through Bit 8
'a'	0
'b'	1
'c'	2
• • •	• • •
'y'	18
'z'	19
'0'	1A
'1'	1B
'2'	1C
'3'	1D
'4'	1E
'5'	1F
'6'	20

Probe Expect	Bit 13 through Bit 8
'7'	21
'8'	3F

The ASCII characters are in four groups of eight characters and one line per pattern. A fifth column of four characters is present if flags and probe expect is included.

```
00000002 00000000 00000000 00000000 8000
00000000 30000000 00000000 00000000 8000
```

The first column contains the data for channels 8 through 1.

The second column contains the data for channels 16 through 9.

The third column contains the data for channels 24 through 31.

The fourth column contains the data for channels 32 through 25.

The fifth column contains the flag and probe expect data followed by 2 trailing zeros.

Each column contains the pattern code for eight channels; the least significant channel data is the right most hex character in each column. In the example above, all channels are set to 'Z' except channel 1 is set to '0' in pattern one. In pattern two all channels are set to 'Z' except channel 16 is set to '1'.

Binary

The binary format represents the pattern data as raw binary data. The pattern data is stored in four sequential 32 bit blocks, five if flags and probe expect are included. The block order is listed below.

Table 5-74: Binary Block Format

Block Number	Contents
1	Channel 8 through 1
2	Channel 16 through 9
3	Channel 24 through 17
4	Channel 32 through 25
5	Flags/probe expect

In blocks one through four, each 32 bit value contains eight pattern codes. The pattern code for each channel requires four bits. The channel mapping for each block is from the lowest channel to the highest channel, i.e., bits 0-3 are channel 1 in block 1, bits 4-7 are channel 2 in block 1, etc.

In block five, each 32 bit value contains the flag codes and the probe expect. The flag code for each pattern requires two bits. Bits 15 and 14 contain the flag code and bits 13 through 8 contain the probe expect code..

Table 5-44 lists the binary value/pattern code translation.

ASCII String

The ASCII string format represents pattern data as viewable ASCII strings, one character per channel, 32 characters per line (34 if flag and probe data are included). Each character is one of the pattern codes listed in Table 5-44. The following example lists two patterns.

```
aZ000RRRRRRRRRRRRRRRRRRRRRRRRRRRm
bCRRRRRRRRRRRRRRRRRRRRRRRRRRRRRn
```

The flag code will be the first character followed by channel 1 through channel 32 and ending with probe expect.

In this example, pattern one has:

- Both flags set (‘a’)
- Channel 1 disabled (‘Z’)
- Channel 2 through channel 4 driven low (‘0’)
- Channel 5 through channel 32 repeating the previous state (‘R’)
- Probe expect low glitch (‘m’)

Pattern two has:

- BERREN flag set (‘b’)
- Channel 1 enabling the CRC (‘C’)
- Channel 2 through channel 32 repeating the previous state (‘R’)
- Probe expect low middle (‘n’)

Editing Waveforms

Up to four waveforms can be defined and output during a pattern for generating UUT handshake or clock stimulus. The first four waveforms are enabled per sequence step and they replace certain Phase/Window signals as mapped below:

- Waveform 1 – Mapped to Phase 4
- Waveform 2 – Mapped to Window 4
- Waveform 3 – Mapped to Phase 3
- Waveform 4 – Mapped to Window 3

Waveforms 1-4 can be programmed to generate complex waveforms with as many transitions that can fit in the pattern period.

The last two waveforms (Waveform 5 and Waveform 6) are not mapped to any of the phase or window signals but are limited to one or two pulses per pattern.

The waveform output repeats for every pattern in the sequence step.

All waveforms can be output on any AUX I/O Channel. Waveform 1 and Waveform 3 can also be output on any channel.

Access this panel from the menu bar: **Edit > Data Sequencer *x*> Waveforms**.

(Where “x” is the sequencer you wish to configure.)

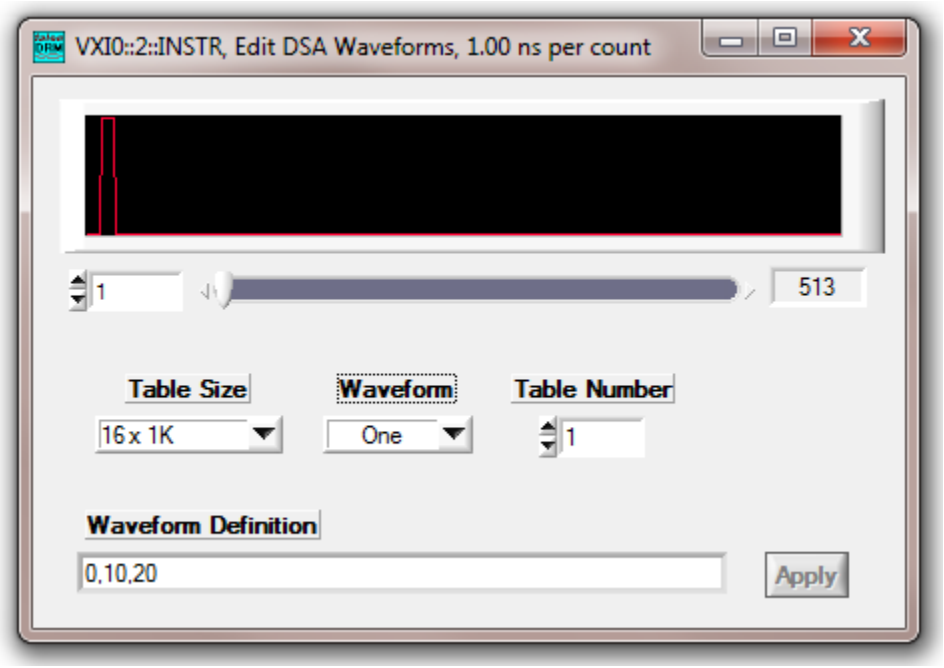


Figure 5-50: Edit Waveforms Panel Waveform 1

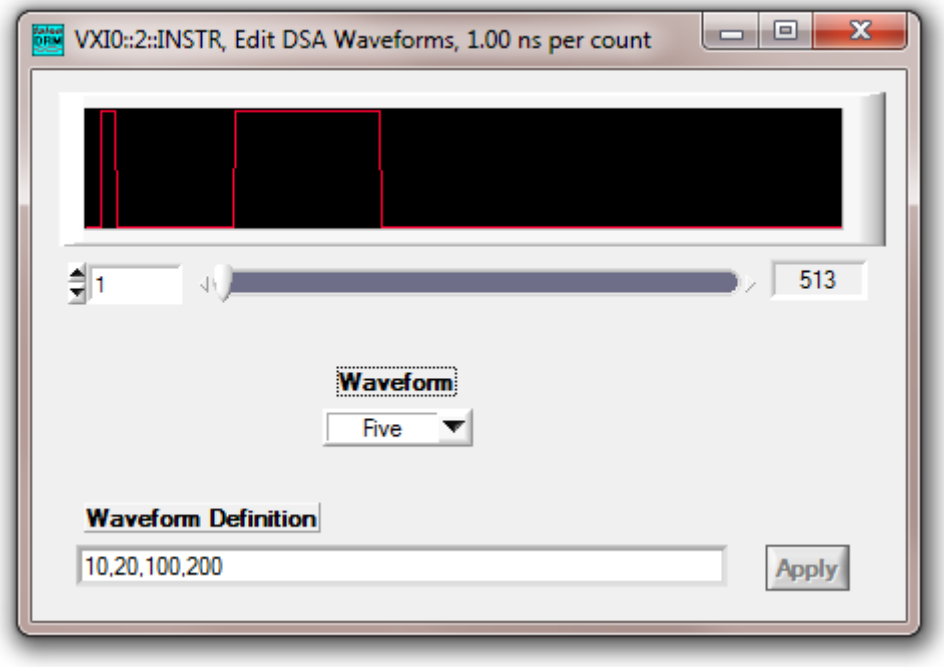


Figure 5-51: Edit Waveforms Panel Waveform 5

Table Size

This pull-down control programs the waveform table size for waveforms 1-4.

Waveforms 5 and 6 are fixed at 65536.

The selections for this pull-down control are:

Table 5-75: Waveform Table Size Settings

Setting	Description
16 x 1K	16 tables each with 1024 bits
8 x 2K	8 tables each with 2048 bits
4 x 4K	4 tables each with 4096 bits
2 x 8K	2 tables each with 8192 bits
1 x 16K	1 table with 16384 bits

The relevant VXI*plug&play* API function is:

- tat964_setWaveformTableSize

Waveform

This pull-down control selects the waveform to view/edit.

Table Number

This control selects the table number to view/edit. Waveforms five and six only have one table.

Waveform Definition

This control allows the user to define the waveform.

Specifying the beginning level and the bit number of subsequent transitions defines the waveform.

Example 1:

0,5,10,15

Beginning Level = 0;

3 Transitions at 5, 10, 15;

Would generate the following waveform;

"00000111110000011111111..."

Bits 1-5 low

Bits 6-10 high

Bits 11-15 low

Bits 16 through the size of the table high.

Example 2:

1

Beginning Level = 1;

No transitions;

Would generate the following waveform;

"111..."

Bits 1 through the size of the table high.

Waveform five and six have a maximum of two transitions.

The relevant VXI*plug&play* API function is:

- tat964_setWaveformData

Editing Sequence Parameters

The sequence parameters consist of the following entries:

1. Loop Counter Mode
2. Pipeline Mask
3. Strobe/Vector Bit/Table Selection
4. Channel Test

Access this panel from the menu bar: **Edit > Data Sequencer *x*> Sequence Parameters**. (Where "x" is the sequencer you wish to configure.)

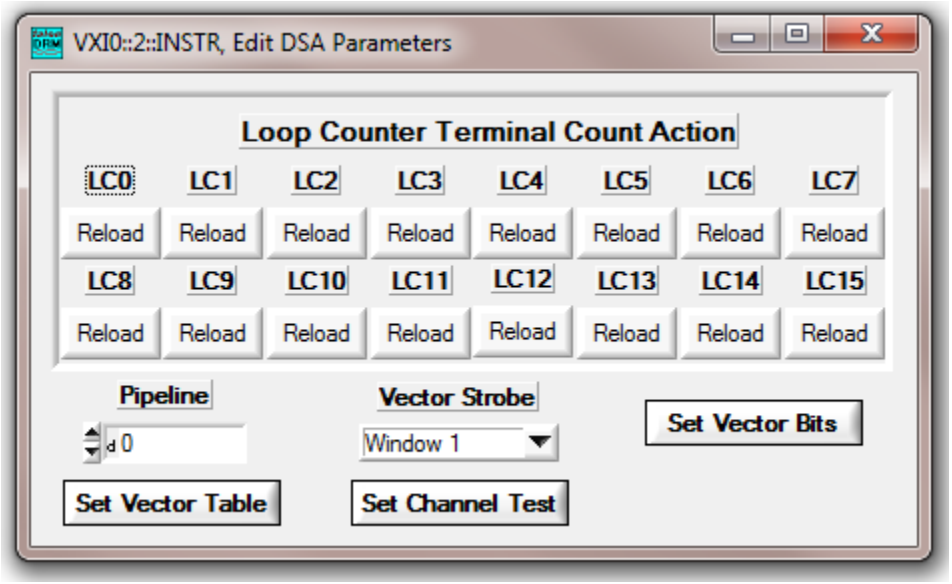


Figure 5-52: Data Sequencer Parameters Panel

LC0 – LC15

These controls program the loop counter mode.

There are sixteen 16-bit loop counters. Each of the sixteen loop counters can be programmed to either reload its count or disable when the terminal count is reached.

Given the following sample loop sequence:

Step 1 jump step 1 using LC0 count 2

Step 2 jump step 1 using LC1 count 3

Example 1:

If both loop counters reload on terminal count, then the step order will be:

1, 1, 2, 1, 1, 2, 1, 1, 2, 1, 1, 2

Example 2:

If loop counter 0 is set to disable, then the step order will be:

1, 1, 2, 1, 2, 1, 2, 1, 2

The relevant VXI*plug&play* API function is:

- tat964_setSequenceLoopMode

Pipeline

This control programs the pipeline depth.

The pipeline may be from 0-31 Patterns deep. The “0” pipeline depth will hereafter be called a “zero pipeline depth”. A pipeline depth of “1-31” will hereafter be called a “non-zero pipeline depth”.

A non-zero pipeline depth offsets the PASS/FAIL result by the corresponding depth of the pipeline in patterns.

See the **Jumping, Halting, Counting and Logging Errors** section in Chapter 8 for a more in-depth explanation of how pipelining affects jumping, counting burst errors and the logging of errors in the error Address Memory.

The relevant VXI*plug&play* API function is:

- tat964_setConditionPipelineMask

Vector Strobe

This control allows the user to set the vector strobe signal.

The closing edge of the selected window will sample the four vector bits VA0 (LSB) to VA3 (MSB). The vector bits are only used if the vector jump bit is set during a sequence jump step. The vector bits form an address into the vector table to determine the jump step and timing set (if timing mode set to indexed).

Table 5-76: Vector Strobe Settings

Setting	Description
Window 1	Sets the closing edge of window 1 as the vector strobe.
Window 2	Sets the closing edge of window 2 as the vector strobe.
Window 3	Sets the closing edge of window 3 as the vector strobe.

Window 4	Sets the closing edge of window 4 as the vector strobe.

The relevant VXI*plug&play* API function is:

- tat964_setVectorJumpStrobe

Set Vector Bits

This command button displays the **Edit Vector Bits** panel so the vector bit signal selection can be programmed for the selected sequencer.

The four vector signals comprise an index into a vector jump table that specifies the jump address as well as the timing set (indexed timing mode only). The vector table/signals are only used if the vector jump bit is set during a sequence jump step.

Configuring the vector signals consists of the following:

1. Select the Source.
2. Program the Input Mode.

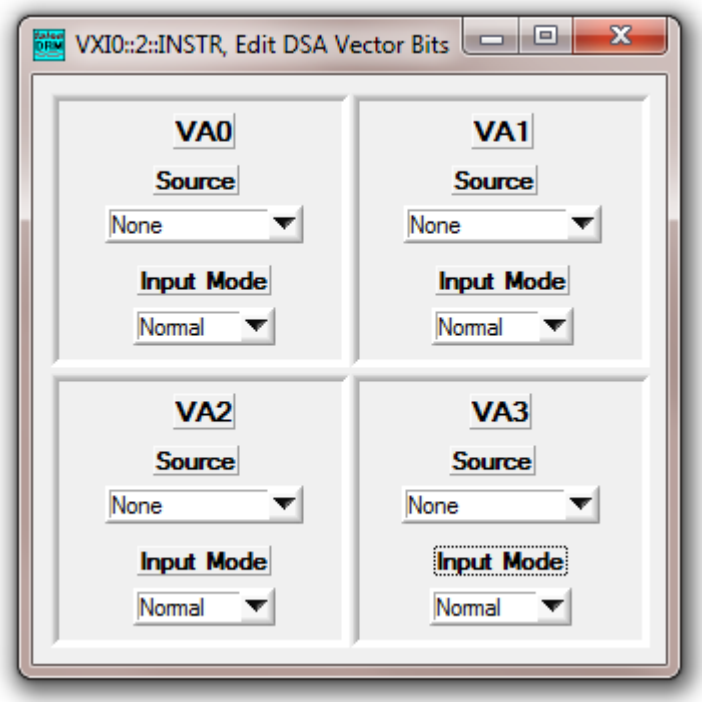


Figure 5-53: Edit Vector Bits Panel

Source

This pull-down control programs the vector bit source.

The selections for this pull-down control are:

Table 5-77: Vector Bit Source Settings

Setting	Description
None	No trigger source selected
AUX1-AUX12	Trigger source set to front panel signal
CHT1	Trigger source set to channel test 1
ECLTRG0,1	Trigger source set to VXI ECL trigger
TTLTRG0-7	Trigger source set to VXI TTL trigger
LTB0-7	Trigger source set to LTB trigger

The relevant VXI*plug&play* API function is:

- tat964_setVectorJumpSignal

Input Mode

This pull-down control programs the trigger input mode for vector jumps.

The selections for this pull-down control are:

Table 5-78: Vector Bit Input Mode Settings

Setting	Description
Normal	Do not modify input signal before testing.
Inverted	Invert input signal before testing.

The relevant VXI*plug&play* API function is:

- tat964_setVectorJumpSignal

Set Vector Table

This command button displays the Edit Vector Table panel so the vector table settings can be programmed for the selected sequencer.

The vector table is indexed by the four vector signals VA0 (LSB) to VA3 (MSB). Each vector table entry supplies the jump address as well as the timing set (indexed timing mode only). The vector table/signals are only used if the vector jump bit is set true in a sequence step.

Configuring the vector table signal consists of the following:

1. Select the Vector Bit Index
2. Select the Vector Jump Step
3. Program the Timing Set (only used in the indexed timing mode).

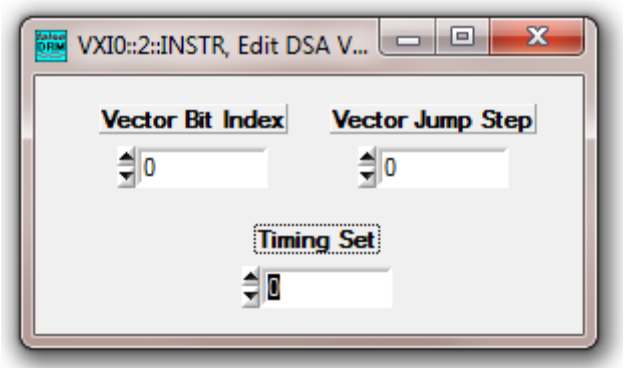


Figure 5-54: Edit Vector Table Panel

Vector Bit Index

This allows the user to enter the index to program. There are 16 indexes that can be set (0 to 15). The index is the binary value of the vector bits (VA0 through VA3).

The relevant VXI*plug&play* API function is:

- tat964_setVectorJumpTable

Vector Jump Step

This allows the user to enter the jump step number for the current vector jump index.

The relevant VXI*plug&play* API function is:

- tat964_setVectorJumpTable

Timing Set

When the timing mode is set to indexed, this control allows the user to specify the timing set for the current vector jump index.

The relevant VXI*plug&play* API function is:

- tat964_setVectorJumpTable

Set Channel Test

This command button displays the Edit Channel Test panel so the channel test settings can be programmed for the selected sequencer.

Configuring the sequence channel test registers consists of the following:

1. Program the expect value
2. Program the mask value

The expect value is compared to the response high (Good 1) of the input channel. A high in the mask, disables the comparison.

The result of all four channel test registers can be routed to the VXI TTL trigger

bus. In addition channel test 1 result can also be routed to any of the sequence triggers.

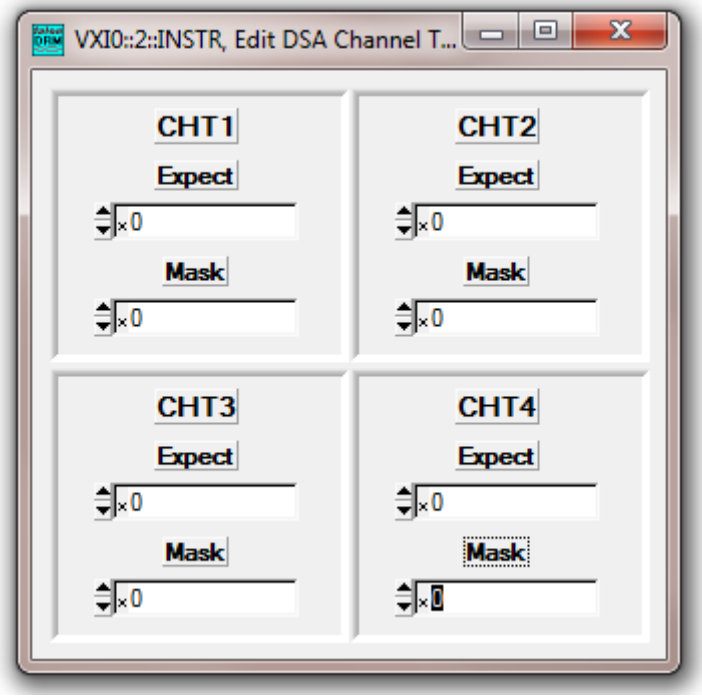


Figure 5-55: Sequencer Channel Test Panel

Expect

This allows the user to enter the expect value for the channel test signal. Bit 0 of the expect value maps to the lowest channel of this sequencer and Bit 31 maps to the highest channel and this is the case for both A and B sequencers. A one represents a valid high test and a zero represents a valid low test.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceChannelTest

Mask

This allows the user to enter the mask value for the channel test signal. Bit 0 of the mask value maps to the lowest channel of this sequencer and Bit 31 maps to the highest channel and this is the case for both A and B sequencers. A one disables the comparison to the expect value and a zero enables the comparison.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceChannelTest

The T940 VXI Backplane Trigger Bus section of Chapter 8 describes how to use Channel Tests to perform a logical OR and logical AND of two or more channels.

Editing Sequence Steps

The sequence steps are used to control the flow of the patterns and assign timing.

Access this panel from the menu bar: **Edit > Data Sequencer *x*> Sequence Steps**. (Where "x" is the sequencer you wish to configure.)

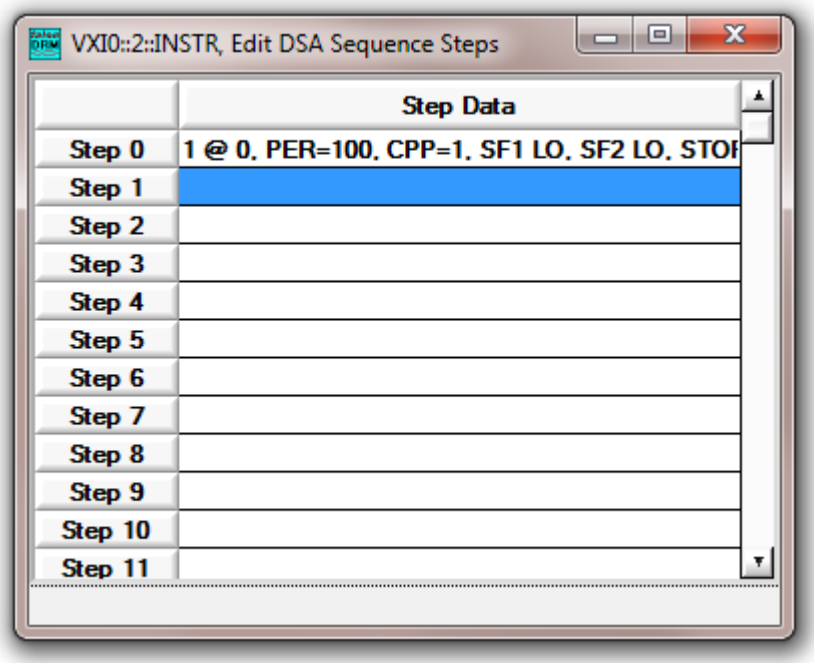


Figure 5-56: Edit Sequence Step Panel

Up to 4096 sequence steps are available for Indexed and Per Step Single timing modes. Up to 1024 sequence steps are available for "Per Step Multi" timing mode.

The Delete key will clear the step data contents, de-allocate any assigned pattern data and initialize the step settings.

A double-click on any of the step number cells opens a Sequence Step Data panel for that cell.

The **T964 Sequencer Operation Details** section in **Chapter 8** provides detailed information on sequencer operation.

The relevant VXI*plug&play* API functions are:

- tat964_selectSequenceStep
- tat964_initSequenceSteps

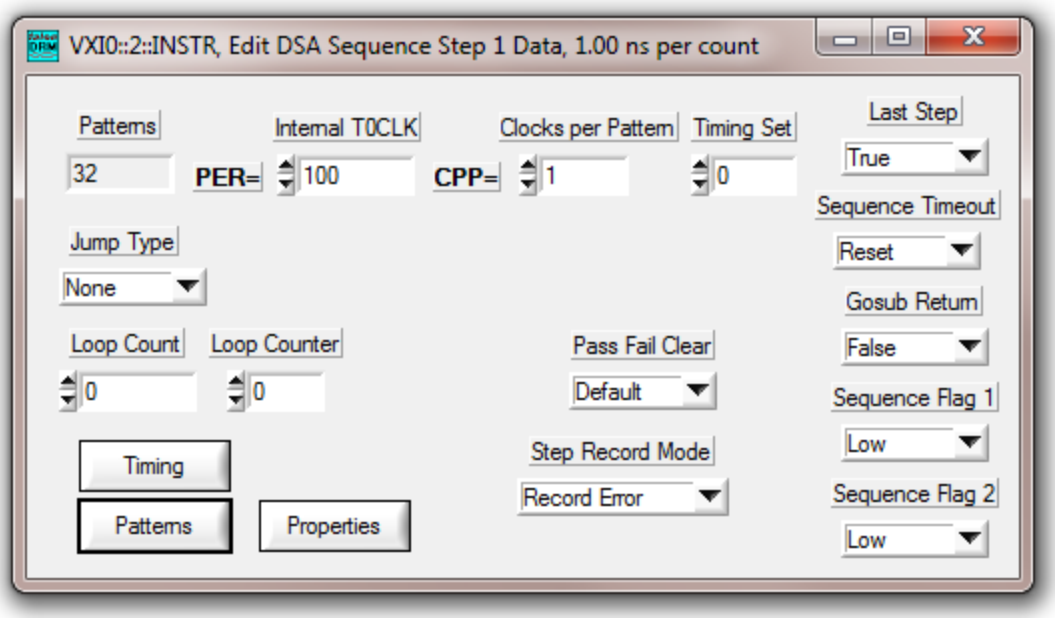


Figure 5-57: Sequence Step Data Panel

Internal T0CLK

This control allows the user to specify the Internal T0CLK period.

When the system clock source is set to internal T0CLK, this control specifies the system clock period. The period is programmed in master clock edges (rising and falling), i.e., 1/2 the master clock period.

For example, if the master clock is set to 500 MHz, then a setting of 20 would result in a system clock period of 20 ns.

20 * (1/2 (2 ns)) = 20 ns.

With a master clock of 100 MHz the system clock period would be 100ns.

20 * (1/2 (10 ns)) = 100 ns.

The valid values for T0CLK are from 20 to 65550.

The relevant VXI*plug&play* API function is:

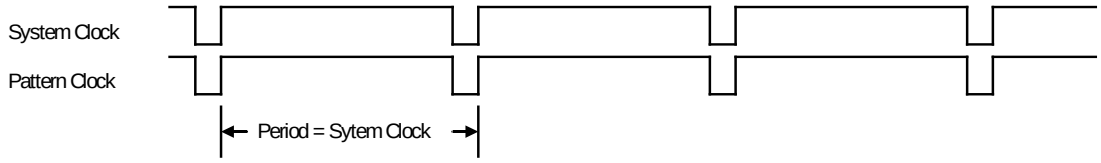
- tat964_setSequenceClock

Clocks per Pattern

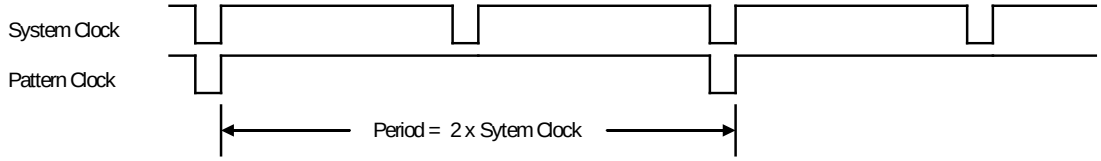
This numeric control defines the Clocks per Pattern (CPP) for each sequence step.

The CPP value determines the number of System Clocks that will be generated for each Pattern Clock. When CPP = 1, then Pattern Clock is equal to System Clock. When CPP = 2, then Pattern Clock is two times the System Clock.

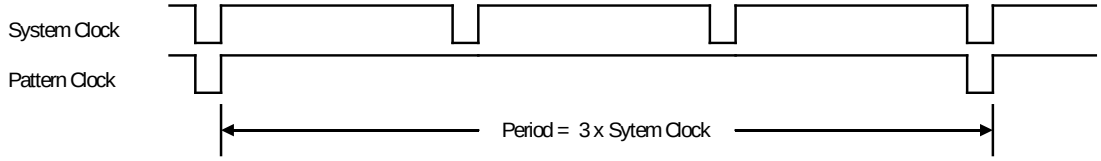
Example 1: CPP = 1



Example 2: CPP = 2



Example 3: CPP = 3



The valid values for CPP are from 1 to 256.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceClock

CPP Phase and Window Triggering

Two clocks are available for triggering the timing phases to begin their programmed definition; System Clock and Pattern Clock (see Phase Trigger Properties in Chapter 5.)

If a Phase is defined to trigger on the System Clock then its span cannot exceed the System Clock period. If a Phase is triggered by the Pattern Clock, and the CPP >1, then that Phase can span the Pattern Clock period.

Windows are only triggered on the Pattern Clock and can span the Pattern Clock period while still observing the Timing Set Value Rules.

Timing Set

This numeric control sets the timing set number for the sequence step.

This control is only visible when the sequencer timing mode is set to indexed (see **Timing Mode** in **Chapter 5**).

The valid values for control are from 0 to 255.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceTimingSet

Last Step

This control allows the user to specify the Last Step flag. This flag indicates whether the current step is the last step of the sequence burst (True) or a sub-step of a multi-step burst (False).

The relevant VXI*plug&play* API function is:

- tat964_setSequenceLastStep

Sequence Timeout

This control allows the user to specify the Sequence Timeout mode. Every step in a multi-step burst can be timed using the sequence timeout timer. When the flag is set to **Reset**, the timer will re-start at the beginning of this step. If this flag is set to **Continue**, then the timer will not reset.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceTimeoutContinue

Gosub Return

This control allows the user to specify the Gosub Return flag. The Gosub Return flag is used to signal the last step of a subroutine.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceGosubReturn

Sequence Flag 1 and Sequence Flag 2

This control allows the user to specify the level of Sequence Flag 1 and Sequence Flag 2 during this step. These general purpose outputs can be routed any of the AUX outputs as well as the VXI TTLTRG and ECLTRG outputs.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceFlags

Jump Type

This pull-down control programs the Jump Type Mode.

Normal sequence step execution proceeds sequentially until the step with the "Last Step" flag is set true. Conditional and unconditional jumps and Gosubs can be added to allow the user to modify sequence step execution order.

Two jump types can be set, Normal and Gosub.

- Normal jumps force the next sequence step number to be replaced by the specified jump step number.
- Gosub jumps save the current step number and forces the next sequence step number to be replaced by the specified step number. The **Gosub Return** flag set true will force the sequence step number to be one more than the saved step number. For example, if step number 5 and 7 had a

Gosub to step 10 and step 13 has the Gosub Return flag set, then the step number sequence starting from 1 would be,

1, 2, 3, 4, 5, 10, 11, 12, 13, 6, 7, 10, 11, 12, 13, 8, 9 …

The selections for this pull-down control are:

Table 5-81: Jump Type Settings

Setting	Description
None	Disable the jump logic for this step.
Normal	After executing this step's patterns, perform a normal jump if jump condition is true.
Gosub	After executing this step's patterns, perform a Gosub jump if the jump condition is true.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceJump

Jump Step

This numeric control programs the Jump Step number.

This control is only visible if the jump type is set to Normal or Gosub.

If the jump condition is true, then the next step number will be the value specified by the Jump Step instead of the next sequential step number.

The jump action takes precedence over the Last Step flag.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceJump

Jump Condition

This pull-down control programs the Jump Type Mode.

This control is only visible if the jump type is set to Normal or Gosub.

Jumps can be conditional or unconditional. Conditional jumps require a specified condition to be true in order for the jump to be enabled. Unconditional jumps are always enabled.

The selections for this pull-down control are:

Table 5-79: Jump Condition Settings

Setting	Description
Always	Jump always (Unconditional)
Step Not PASS	Jump if the PASS/FAIL flag is NOT a PASS (i.e. FAIL or Indeterminate)
Step Not FAIL	Jump if the PASS/FAIL flag is NOT a FAIL (i.e. PASS or Indeterminate)

Setting	Description
Step FAIL	Jump if the PASS/FAIL flag is equal to FAIL
Step PASS	Jump if the PASS/FAIL flag is equal to PASS
Sequence FAIL	Jump if Burst Error Count is not equal to zero.
Sequence PASS	Jump if Burst Error Count is equal to zero.
Jump Trigger 1 True	Jump if “Jump Trigger 1” true.
Jump Trigger 1 not True	Jump if “Jump Trigger 1” not true.
Jump Trigger 2 True	Jump if “Jump Trigger 2” true.
Jump Trigger 2 not True	Jump if “Jump Trigger 2” not true.
Jump Trigger 3 True	Jump if “Jump Trigger 3” true.
Jump Trigger 3 not True	Jump if “Jump Trigger 3” not true.
Jump Trigger 4 True	Jump if “Jump Trigger 4” true.
Jump Trigger 4 not True	Jump if “Jump Trigger 4” not true.

The true/false state of the jump triggers is based on the jump trigger test condition. If the jump trigger test condition is set to “Low Level”, then “True” would indicate the jump trigger signal is low and “not True” would indicate the jump trigger signal is high.

Note: *Any CONDEN enabled FAIL during the Sequence Step will prevent a PASS.*

See the **Jumping, Halting, Counting and Logging Errors** section of **Chapter 8** for a detailed explanation of Jumping based on Errors. Also see the **Jumping on a Step or Burst Error** section of **Chapter 8**.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceJump

Loop Count

This numeric control programs the Loop Count number.

Jumps can be qualified by a loop counter. The loop count can be set from 0 (no qualification) to 65536. A count qualified jump only allows the jump to occur a maximum of “count” times. This allows single or multiple steps to be looped.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceJump

Loop Counter

This numeric control programs the Loop Counter number.

Jumps can be qualified by a loop counter. Sixteen loop counters are available. Nested loops are supported including up to all 16 counters.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceJump

Vector Jump

This control allows the user to specify the Vector Jump flag. This flag indicates whether the vector jump mode is enabled (true) or disabled (false).

If the vector jump mode is enabled, then the sequence step number to jump to is specified in the vector jump table which is addressed by the Vector Bits which form the Vector Bit Index. If the vector jump mode is disabled, then the sequence step number to jump to is specified by the **Jump Step** control.

This control is only visible if the jump type is set to Normal or Gosub.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceJump

Pass Fail Clear

This control programs the Pass Fail Clear Mode during this step.

The T940 pass fail flag is used for conditional jumping and indicates the results of a channel compare pattern code. The pass fail flag can be set to clear at the beginning of each sequence step (default) or to hold the previous state (mask).

The selections for this pull-down control are:

Table 5-80: Step Record Mode Settings

Setting	Description
Default	Clear Pass Fail
Mask	Hold Previous Pass Fail

Note: *See the* ***Jumping on and Counting Errors*** *section of* ***Chapter 8*** *for a more in-depth explanation.*

The relevant VXI*plug&play* API function is:

- tat964_setSequencePassFailClear

Step Record Mode

This control programs the Step Record Mode during this step.

The T940 contains three memories that store error data from a sequence

burst:

1. Error Address Memory
2. Record Index Memory
3. Record Memory

There is also the Error Counter which counts the number of pattern errors that occurred during the previous sequence burst. The Error Count can be queried using the "tat964_queryErrorFlags" function.

The Error Address Memory stores the sequence step, address and index of each pattern that generated an error during the previous sequence burst. The Error Address Memory can be queried using the “tat964_queryErrorAddress" function.

Note: *The Error Counter and the Error Address Memory only count/log errors that are enabled with BERREN.*

The Record Index Memory contains the data required to align the record memory contents when data is stored sequentially (Record Type = Indexed) for the previous sequence burst.

The Record Memory contains either the error flag or response data for the previous sequence burst.

The selections for this pull-down control are:

Table 5-81: Step Record Mode Settings

Setting	Description
None	Error counting and all three record memories are disabled.
Record Count	Error Counting enabled.
Record Error	Error counting and all three memories are enabled and the Record Memory is set to record error data.
Record Response	Error counting and all three memories are enabled and the Record Memory is set to record response data.

For the **Record Count** settings, the record memory can either be set to record all zeros (No Error) or disabled (see **Record Mode** in **Chapter 5**).

See the **Jumping, Halting, Counting and Logging Errors** section of **Chapter 8** for more details regarding the counting and recording of errors in the Error Address Memory.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceRecordMode

Timing

This command button displays the Edit Timing Set panel so the phase and window settings can be programmed for the selected sequencer step (see

Editing the Timing Sets in **Chapter 5**).

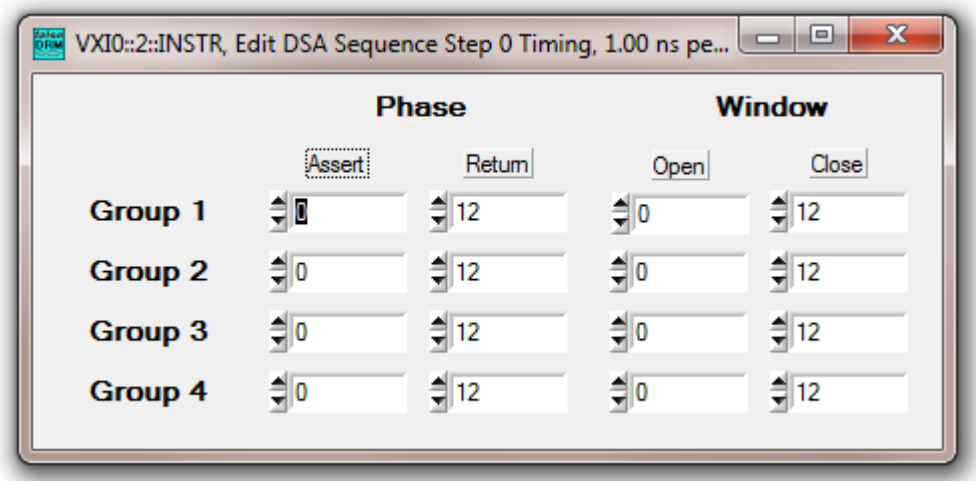


Figure 5-58: Edit Timing Set Panel

The relevant VXI*plug&play* API function is:

- tat964_setSequenceTimingData

Patterns

If the **Patterns** control reads 0, then this command button displays the **Initialize Step Pattern Set** panel.

This panel allows the user to assign a block of pattern memory to the current sequence step.

The **Number of Patterns** control specifies how many patterns will be assigned and initialized to the current sequence step.

The **Memory Offset** control specifies the location of the first pattern. If the offset is set to -1, the driver automatically increments the offset to the next higher multiple of 4 from the previous offset. Any other number between 0 and 262140, in multiples of 4, sets the offset.

Click **Apply** to initialize the patterns or **Close** to cancel.

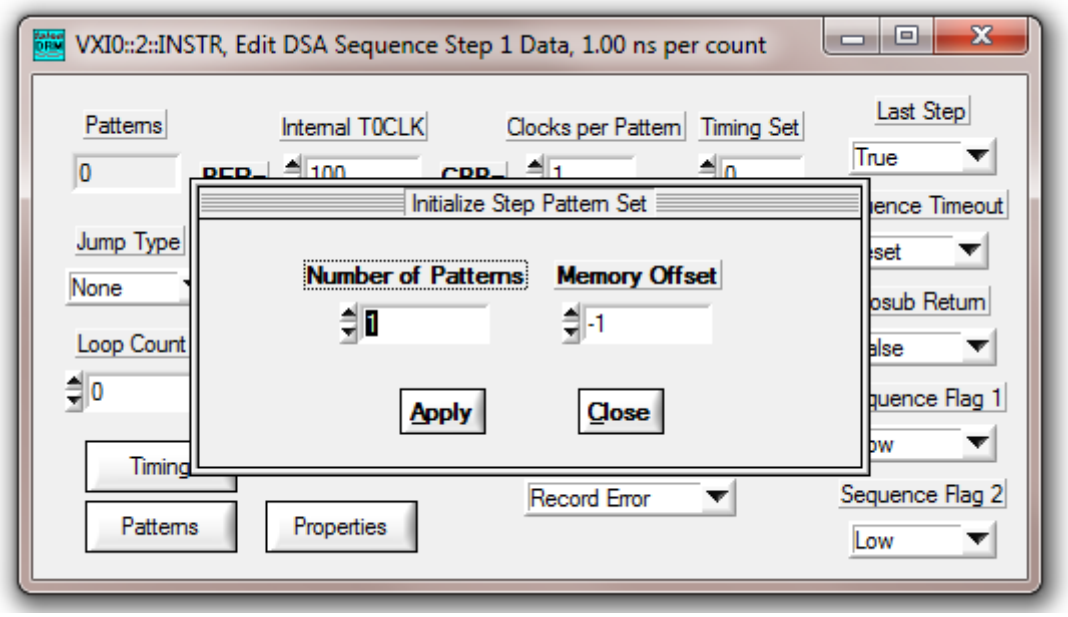


Figure 5-59: Initialize Step Pattern Set Panel

The relevant VXI*plug&play* API function is:

- tat964_initPatternSet

If the **Patterns** control reads a number greater than zero, then this command button displays the Edit Pattern Data panel (see **Editing the Patterns** in **Chapter 5**).

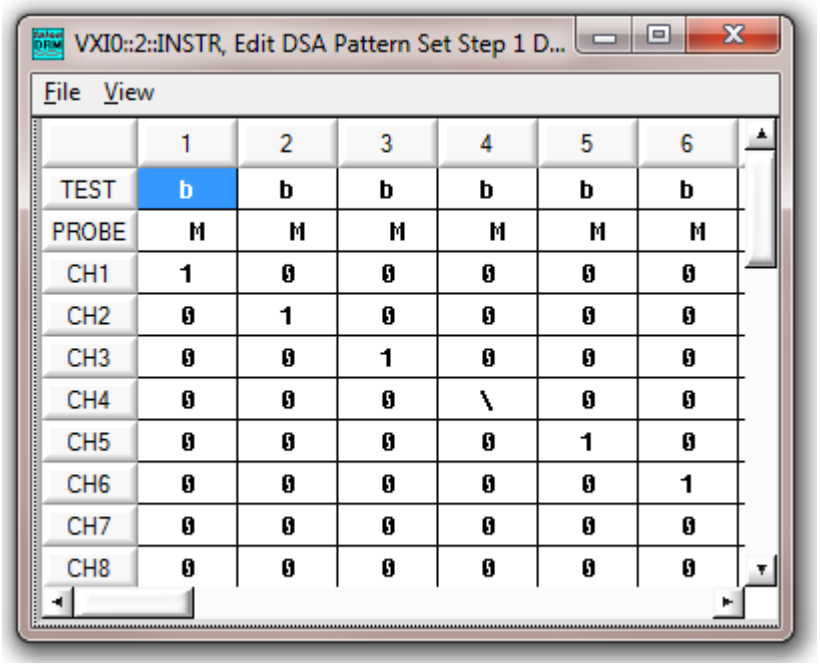


Figure 5-60: Edit Pattern Set Panel

Properties

This command button displays the Sequence Step Properties panel.

The sequence step properties consist of the following hardware settings:

1. Handshake Control (Pause/Resume)
2. Waveform
3. Phase Trigger

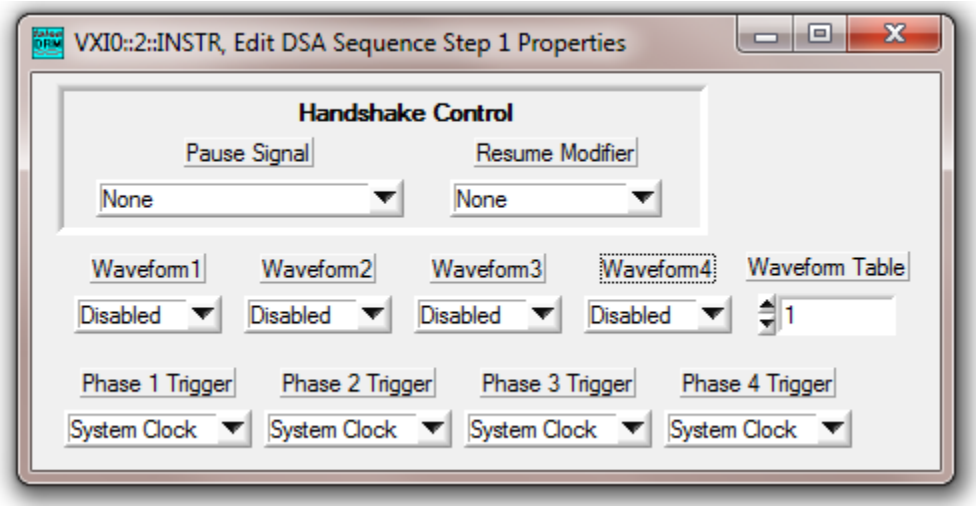


Figure 5-61: Sequence Step Properties Panel

Handshake Control

The handshake control allows the user to assign a signal (Pause) that can be either internal or external, which will pause the sequencer. When paused, the following will stop:

- Phases
- Windows
- Waveforms

For each pause signal selection, there is a corresponding signal that will continue (Resume) sequence operation. See the **Pause and Halt** section of Chapter 8 for additional details about the use of pause.

Pause Signal

This pull-down control programs the Handshake Pause signal.

The selections for this pull-down control are:

Table 5-82: Handshake Pause Signal

Setting	Pause Signal	Resume Signal
None	Handshake mode disabled	NA

Setting	Pause Signal	Resume Signal
Pause Trigger 1 True	Pause Trigger 1 signal true	Pause Trigger 1 Resume
Pause Trigger 1 Not True	Pause Trigger 1 signal not true	Pause Trigger 1 Resume
Pause Trigger 2 True	Pause Trigger 2 signal true	Pause Trigger 2 Resume
Pause Trigger 2 Not True	Pause Trigger 2 signal not true	Pause Trigger 2 Resume
Phase 1 Assert	Phase 1 Assert edge occurs	Phase 1 Resume Trigger
Phase 1 Return	Phase 1 Return edge occurs	Phase 1 Resume Trigger
Phase 2 Assert	Phase 2 Assert edge occurs	Phase 2 Resume Trigger
Phase 2 Return	Phase 2 Return edge occurs	Phase 2 Resume Trigger
Phase 3 Assert	Phase 3 Assert edge occurs	Phase 3 Resume Trigger
Phase 3 Return	Phase 3 Return edge occurs	Phase 3 Resume Trigger
Phase 4 Assert	Phase 4 Assert edge occurs	Phase 4 Resume Trigger
Phase 4 Return	Phase 4 Return edge occurs	Phase 4 Resume Trigger

The true/false state of the pause triggers is based on the pause trigger test condition. If the pause trigger test condition is set to “Low Level”, then true would indicate the pause trigger signal is low and false would indicate the pause trigger signal is high.

Note: *The Resume Signal selection is covered in the* **Configure Triggers** *section in* **Chapter 5***.*

The relevant VXI*plug&play* API function is:

- tat964_setSequenceHandshake

Resume Modifier

This pull-down control programs the Handshake Resume Modifier.

The resume modifier allows the handshake to resume normally (None) or allows for the following modifications:

- Pattern Delay 1 or 2: Continue either on the presence of the specified resume signal or at the exhaustion of Pattern Delay timer 1 or 2 (the Delay Timer started when the Pause signal was received).
- Pattern Timeout: Set the pattern timeout (PTO) flag if the specified resume signal is not received by the time the Pattern Timeout timer has exhausted (the Pattern Timeout timer started when the Pause signal was

received).

The selections for this pull-down control are:

Table 5-83: Handshake Modifier Settings

Setting	Resume Modifier
None	No modifier, resume on 'Resume Signal" only
Pattern Delay 1	Pattern Delay 1 timer
Pattern Delay 2	Pattern Delay 2 timer
Pattern Timeout	Pattern timer (PTO also set)

The relevant VXI*plug&play* API function is:

- tat964_setSequenceHandshake

Waveform Properties

The waveform logic allows the user to enable up to six waveforms per sequence step (see **Editing Waveforms** in **Chapter 5**). Waveform 1 through Waveform 4 have to be enabled per sequence step to replace the timing signals they are paired with. Waveforms 5 and 6 are dedicated and do not need to be enabled.

Waveform1 – Waveform4

This control allows the user to enable/disable the specific waveform number.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceWaveform

Waveform Table

This numeric control allows the user to program the waveform table for the sequence step. Numeric values can range from Waveform Tables 1 through 16.

The relevant VXI*plug&play* API function is:

- tat964_setSequenceWaveform

Phase Trigger Properties

The phase trigger logic allows the user to select the phase trigger signal source for the four phases between the "System Clock" and the "Pattern Clock (PCLK)". In "System Clock" mode, another Phase is output for each System Clock. In "Pattern Clock" mode, another Phase is output for each Pattern Clock, which results in the Phase output rate being at a multiple of the System Clock period if CPP>1 ($PER_{PCLK} = PER_{SCLK} * CPP$).

The relevant VXI*plug&play* API function is:

- tat964_setSequencePhaseTrigger

Execute the Sequence

Sequence execution and control is performed from the Execute panel.

Access this panel from the menu bar: **Execute > DS*x***. (Where "x" is the sequencer you wish to execute.)

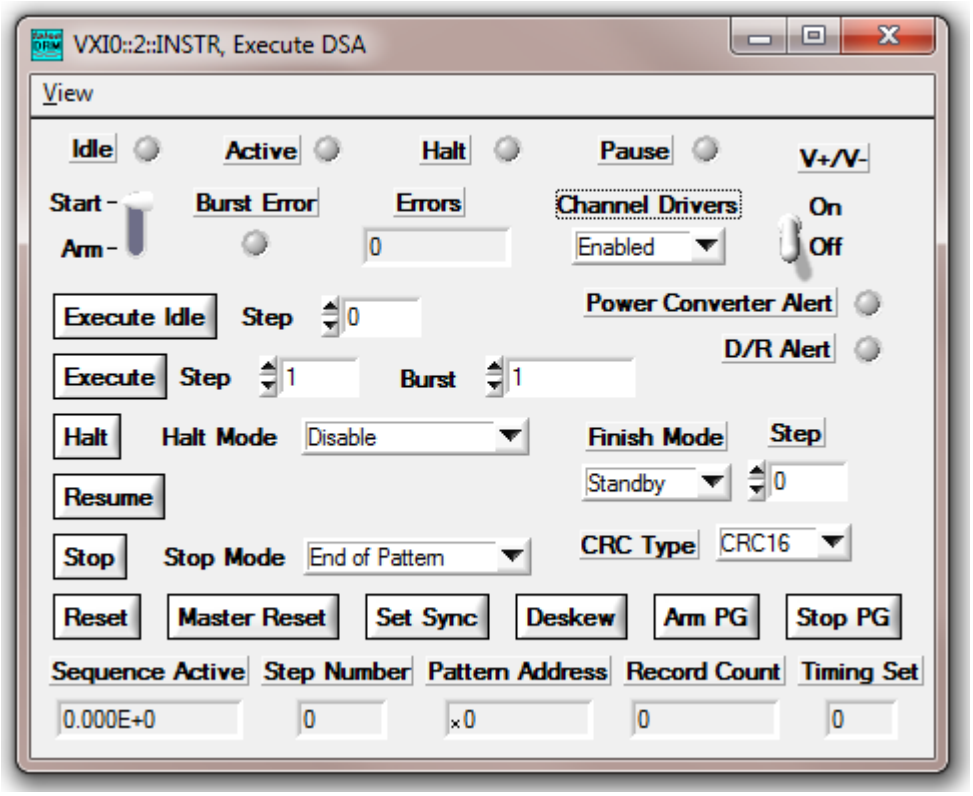


Figure 5-62: Executing a Sequence Panel

The following sections describe the execution overview as well as the indicators and controls of the execute panel.

Execution Overview

The sequencer execution state diagram is illustrated in the following figure.

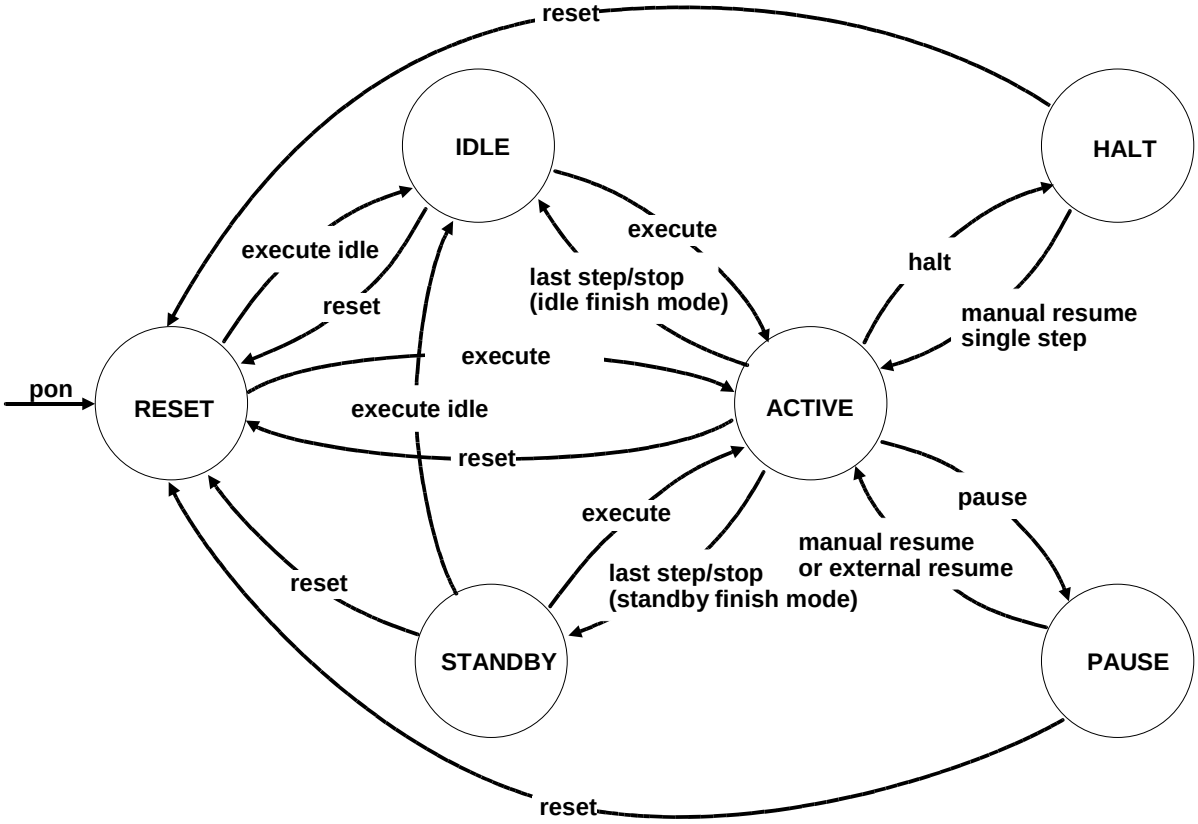


Figure 5-63: Execute State Diagram

The following table describes the six execute states of the DRM and how the state is entered.

Table 5-84: Execute State Description

Setting	Description	Entry Condition
RESET	1. Idle Active: false 2. Sequence Active: false 3. Halt flag: false 4. Paused flag: false 5. Active step: 0 6. Pattern Memory: Free	“pon”, “reset”
STANDBY	1. Idle Active: false 2. Sequence Active: false 3. Halt flag: false 4. Paused flag: false	“last step/stop (standby finish mode)”

Setting	Description	Entry Condition
	5. Active step: User 6. Pattern Memory: Free	
IDLE	1. Idle Active: true 2. Sequence Active: false 3. Halt flag: false 4. Paused flag: false 5. Active step: User 6. Pattern Memory: Busy	"execute idle", "last step/stop idle finish mode"
ACTIVE	1. Idle Active: false 2. Sequence Active: true 3. Halt flag: false 4. Paused flag: false 5. Active step: User 6. Pattern Memory: Busy	"execute", "resume"
HALT	1. Idle Active: false 2. Sequence Active: true 3. Halt flag: true 4. Paused flag: false 5. Active step: User 6. Pattern Memory: Free	"halt"
PAUSE	1. Idle Active: false 2. Sequence Active: true 3. Halt flag: false 4. Paused flag: true 5. Active step: User 6. Pattern Memory: Busy	"pause"

The following table describes the state transitions and the execute panel control to perform it.

Table 5-85: Execute State Transition Description

Transition	Description	Soft Front Panel Control
pon	Power on	NA
reset	Sequencer reset	• Depress **Reset** command button. • Depress **Master Reset** command button (also disables output drivers).
execute idle	Execute idle sequence	• Enter step number and depress **Execute Idle** command button.
execute	Execute sequence	• Enter step number and depress **Execute** command button.

Transition	Description	Soft Front Panel Control
last step/stop (idle finish mode)	Sequence completes step with last step flag true or stop command. Finish Mode set to Idle	• Set **Finish Mode** to "Idle" • Enter step number and depress **Execute** command button. • If sequence is still active, depress the **Stop** command button.
last step/stop (standby finish mode)	Sequence completes step with last step flag true or stop command. Finish Mode set to Standby	• Set **Finish Mode** to "Standby" • Enter step number and depress **Execute** command button. • If sequence is still active, depress the **Stop** command button
halt	Halt the active sequence.	• Make sure the **Halt Mode** is not set to "Disabled" • Depress the **Halt** command button. If sequence was active, **Halt LED** should be red (halted). If sequence was not running, **Halt LED** should be green (armed).
resume/single step	Halt resume or single step	While in HALT state: • Depress **Resume** command button to resume. • Depress **Halt** command button to single step.
pause	Pause the primary sequence	No control to manually pause the primary sequence.
resume	Pause resume	While in PAUSE state: • Depress **Resume** command button to resume.

Execute Panel Indicators

There are eleven indicators that display the current sequencer status. These indicators are updated every 50 ms.

Idle LED

When green, indicates that the sequencer is in the IDLE state.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerStatus

Active LED

When green, indicates that the sequencer is in the ACTIVE state.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerStatus

Halt LED

When green, indicates that the halt mode has been armed. When red, indicates that the sequencer is in the HALT state.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerStatus

Pause LED

When green, indicates that the sequencer is in the PAUSE state.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerStatus

Burst Error LED

When red, indicates that one or more burst errors have occurred in the previous sequence run.

The relevant VXI*plug&play* API function is:

- tat964_queryErrorFlags

Errors

This numeric indicator displays the number of pattern errors from the previous sequence burst.

The relevant VXI*plug&play* API function is:

- tat964_queryErrorFlags

Power Converter Alert

Illuminated red indicates that one or more fault bits are set in the Power Converter Condition register.

Illuminated yellow indicates that the High Current bit is set in the Power Converter Condition register.

The relevant VXI*plug&play* API function is:

- tat964_queryPowerConverterCondition

D/R Alert

Illuminated red indicates that one or more bits are set in the Driver/Receiver event register.

The relevant VXI*plug&play* API function is:

- tat964_queryFrontEndCondition

Sequence Active

This numeric indicator displays the execution time of the previous sequence burst (10 ns resolution ± 10 ns with an accuracy of 500 ppm up to~43 sec).

The relevant VXI*plug&play* API function is:

- tat964_querySequenceActive

Step Number

This numeric indicator displays the current sequence step address.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerStatus

Pattern Address

This numeric indicator displays the current pattern address.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerStatus

Record Count

This numeric indicator displays the current record count.

The relevant VXI*plug&play* API function is:

- tat964_queryRecordCount

Timing Set

This numeric indicator displays the current timing set index (only visible in indexed timing mode).

The relevant VXI*plug&play* API function is:

- tat964_querySequencerTimingSet

Execute Panel Modes and Settings

There are ten controls that set the execution mode settings.

Start/Arm Selector

This slide selects whether the **Execute Idle** or **Execute** command buttons arm or start the specified action (See **Execute Idle** and **Execute** command button descriptions).

Channel Drivers

This pull-down control programs the channel drivers.

The selections for this pull-down control are:

Table 5-86: Channel Drivers Settings

Setting	Description
Disabled	All the channel drivers are forced off (disabled).
Enabled	Channel drivers in normal mode. Level and state are determined by pattern code and channel parameters and properties.

Note: *The following events can cause force the drivers to be disabled:*

- *A Watch Dog Timeout, if enabled to do so*
- *A local or DRS global over-current event, if enabled to do so*
- *A local or DRS global drive fault event, if enabled to do so*
- *A channel over-voltage event for Driver/Receiver modules employing this feature.*

The relevant VXI*plug&play* API function is:

- tat964_setDriverEnable

V+/ V-

This control allows power to be applied to those D/R boards which require power. It also enables the isolation relays to be closed if they're designated to be closed by the Connect State.

Note: *The following Driver/Receiver Event will automatically force the V+ and V- power switch off (or not allow it to be turned on) protecting the module pin drivers.*

- *V+ too high*
- *V- too low*
- *V+/ V- Delta too great*
- *Temperature Fault detected*
- *OVP detect (DR3e, DR9 and UR14)*

*A ground fault or I^2C Error will **not** shut the V+ and V- off.*

The relevant VXI*plug&play* API function is:

- tat964_setPowerConnect

Execute Idle Step

This control sets the idle step number for the **Idle** command button operation.

The relevant VXI*plug&play* API function is:

- tat964_setIdleSequence

Execute Step

This control sets the step number for the **Execute** command button operation.

The relevant VXI*plug&play* API functions are:

- tat964_executeSequence
- tat964_armSequence

Burst

This control sets the burst count for the **Execute** command button operation. The burst count determines how many times the sequence will be looped. A count of 0 causes continuous looping. Maximum burst count is 1048576.

The relevant VXI*plug&play* API function is:

- tat964_setBurstCount

Halt Mode

This pull-down control programs the halt mode. The halt mode determines where execution will halt following either a manual halt (**Halt** command button) or an external halt trigger. See the **Jumping, Halting, Counting and Logging Errors** section in Chapter 8 for additional details about the use of halt.

The selections for this pull-down control are:

Table 5-87: Halt Mode Settings

Setting	Description
Disable	Halt signal ignored.
Pattern	Halt the current sequence at the end of the next pattern.
Step	Halt the current sequence at the end of the next step.
Sequence	Halt the current sequence at the end of the next sequence loop.
Sync 1	Halt the current sequence at the end of the next pattern according to where the Sync Pulse 1 is positioned.
Sync 2	Halt the current sequence at the end of the next pattern according to where the Sync Pulse 2 is positioned.
Pattern Fail	Halt the current sequence at the end of the next pattern if the pass/fail flag is set to fail.

Setting	Description
Step Fail	Halt the current sequence at the end of the next sequence step if the pass/fail flag is set to fail.
Sequence Fail	Halt the current sequence at the end of the next sequence if the pass/fail flag is set to fail.
Pattern Pass	Halt the current sequence at the end of the next pattern if the pass/fail flag is set to pass.
Step Pass	Halt the current sequence at the end of the next sequence step if the pass/fail flag is set to pass.
Sequence Pass	Halt the current sequence at the end of the next sequence if the pass/fail flag is set to pass.

The relevant VXI*plug&play* API function is:

- tat964_setHaltMode

Finish Mode

This pull-down control programs the finish mode. When a sequence execution completes, the sequencer will enter either the **Standby** or **Idle** state. The **Standby** state outputs the first pattern of the specified step and pattern memory can be accessed by the user while the sequencer is in Standby. The **Idle** state outputs the entire pattern set of the specified step and pattern memory cannot be accessed while the sequencer is idling.

The selections for this pull-down control are:

Table 5-88: Finish Mode Settings

Setting	Description
Standby	Go to **Standby** after sequence completes.
Idle	Go to **Idle** after sequence completes.

The relevant VXI*plug&play* API function is:

- tat964_setFinishSequence

Finish Mode Step

This control sets the finish mode step number.

The relevant VXI*plug&play* API function is:

- tat964_setFinishSequence

Stop Mode

This pull-down control programs the stop mode. The stop mode controls what action a CPU generated stop or a triggered stop will perform if received. The selections for this pull-down control are:

Table 5-89: Stop Mode Settings

Setting	Description
Disable	Stop signal will be ignored.
End of Pattern	The stop signal causes the current sequence burst to terminate at the end of the next pattern.
Looping	The stop signal causes the next jump to be ignored. Sequence execution resumes at the step sequentially following the step with the ignored jump.
End of Sequence	The stop signal causes the current sequence burst to terminate at the end of the sequence of a continuous or looped burst.

The relevant VXI*plug&play* API function is:

- tat964_setStopMode

CRC Type

This pull-down control programs the CRC type for the next burst. The selections for this pull-down control are:

Table 5-90: CRC Type Settings

Setting	Description
CRC16	CRCs generated in the next burst will be CRC16 polynomials.
CRC32	CRCs generated in the next burst will be CRC32 polynomials.
Custom	Custom CRC algorithms are only available with sequencer revisions 0.23 and later.

The relevant VXI*plug&play* API function is:

- tat964_setCRCType

Set Sync

This command button displays the **Set Sync** panel so that Sync 1 and Sync 2 signals can be programmed to generate a pulse.

These two sync outputs can be routed to any of the AUX, ECLTRG or TTLTRG

outputs. The sync parameters consist of an offset and a length. Once the programmed sync event occurs, the sync pulse will begin after the "offset" and last for "length". Both "offset" and "length" are specified in pattern clocks. The sync pulse will not extend past the end of the sequence. In the "Step" event, the sync pulse will not extend beyond the specified step.

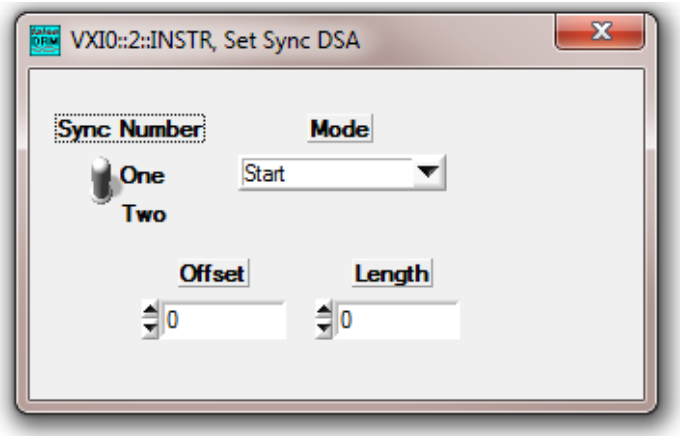


Figure 5-64: Set Sync Panel

Sync Number

This control selects which sync pulse signal to program, either Sync 1 or Sync 2.

Event (and Step)

This pull-down control programs the sync event. The sync pulse event can be set to either the start of a sequence or a specific step.

The selections for this pull-down control are:

Table 5-91: Finish Mode Settings

Setting	Description
Start	The sync pulse begins from the start of the sequence.
Step	The sync pulse begins from the specified step.

The relevant VXI*plug&play* API function is:

- tat964_setSyncEvent

Offset

This control sets the offset from the sync event before the sync pulse starts. The offset can be set from 0 to 1048575 patterns.

The relevant VXI*plug&play* API function is:

- tat964_setSyncParameters

Length

This control sets the length for the sync pulse from 0 (no pulse) to 4095 patterns.

The relevant VXI*plug&play* API function is:

- tat964_setSyncParameters

Execute Panel Command Buttons

There are ten command buttons that control DRM sequence, deskew and pulse generator execution.

Execute Idle

If the **Start/Arm** control is set to Start, this command button starts the Idle sequence at the sequence step specified in the **Execute Idle Step** control. If the **Start/Arm** control is set to Arm, this command button arms the Idle sequence at the sequence step specified in the **Execute Idle Step** control. Arming the idle sequence would be used in conjunction with an external start trigger. It is also used if this is not the Primary Sequencer in a DRS.

The relevant VXI*plug&play* API functions are:

- tat964_executeIdleSequence
- tat964_armIdleSequence

Execute

If the **Start/Arm** control is set to Start, this command button starts the sequence at the sequence step specified in the **Execute Step** control. If the **Start/Arm** control is set to Arm, this command button arms the sequence at the step specified in the **Execute Step** control. Arming the sequence would be used in conjunction with an external start trigger. It is also used if this is not the Primary Sequencer in a DRS.

The relevant VXI*plug&play* API functions are:

- tat964_executeSequence
- tat964_armSequence

Halt

The **Halt** command button halts the sequence based on the **Halt Mode** selection. Once halted (indicated by a red **Halt LED**), another push of the **Halt** command button resumes the sequence and then halts it again (single step). See the **Pause and Halt** section in **Chapter 8** for additional details about the use of halt.

The relevant VXI*plug&play* API function is:

- tat964_haltSequence

Resume

The **Resume** command button terminates a pause or halt state and sequence execution continues. See the **Pause and Halt** section in **Chapter 8** for additional details about resuming a pause or halt.

The relevant VXI*plug&play* API function is:

- tat964_resumeSequence

Stop

The **Stop** command button stops the sequence based on the **Stop Mode** selection. The standby or idle state will become active based on the **Finish Mode** setting. Pressing the **Stop** command button when the sequence is not active latches the stop command until the sequence is active.

The relevant VXI*plug&play* API function is:

- tat964_stopSequence

Reset

The **Reset** command button forces the sequence to the reset state (Sequence Step 0) with the **Channel Drivers** setting unchanged.

The relevant VXI*plug&play* API function is:

- tat964_resetSequence

Master Reset

The **Master Reset** command button forces the sequence to the reset state (Sequence Step 0) and also sets the **Channel Drivers** to Disabled.

The relevant VXI*plug&play* API function is:

- tat964_masterResetSequence

Deskew

The **Deskew** command button activates the end-of-cable deskew procedure. Only closed channels will be deskewed.

The relevant VXI*plug&play* API function is:

- tat964_deskewDrsChannels

Arm PG

The **Arm PG** command button arms the pulse generator.

Note: *The Pulse Generator will not work in any of its modes until armed.*

The relevant VXI*plug&play* API function is:

- tat964_armPulseGenerator

Stop PG

The **Stop PG** command button stops the pulse generator.

The relevant VXI*plug&play* API function is:

- tat964_stopPulseGenerator

Analyze the Execution Results

After sequence execution has been performed, the final step is to analyze the results to determine if the recorded input data is valid and if it matches the expected results.

The **Burst Error LED** and **Errors** are result indicators located on the execution panel. Additional result data can be accessed from the **Execute > DS*x*** menu bar, **View** selection. (Where "x" is the sequencer you wish to query.)

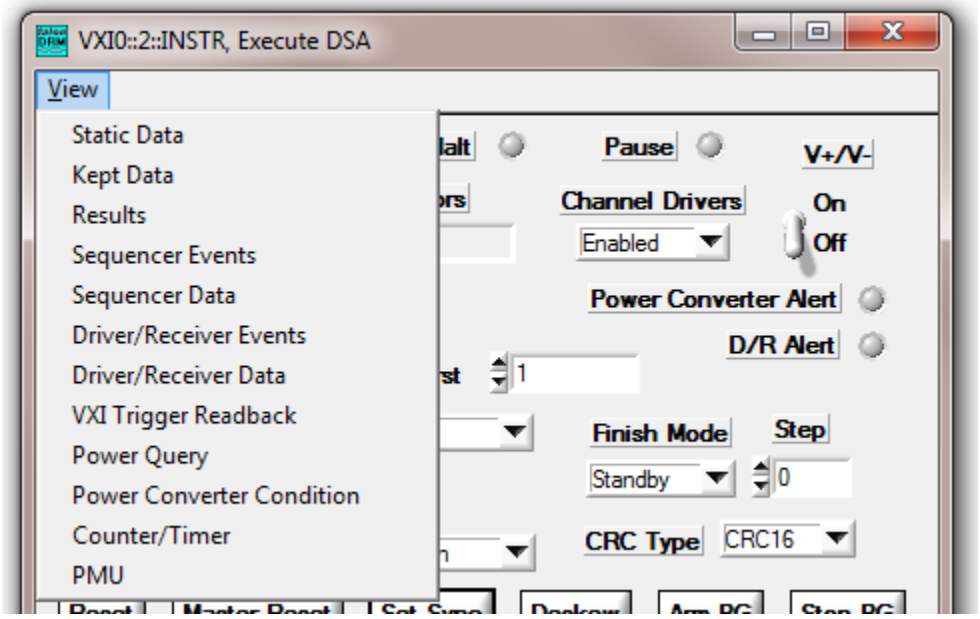


Figure 5-65: Execute DSA View Menu

These panels allow the user to query the recorded memory results and status indicators from the previous sequence execution.

Static Data

The static data display is accessed from the **Execute > DS*x* > View > Static Data** menu bar selection (where "x" is the sequencer you wish to query).

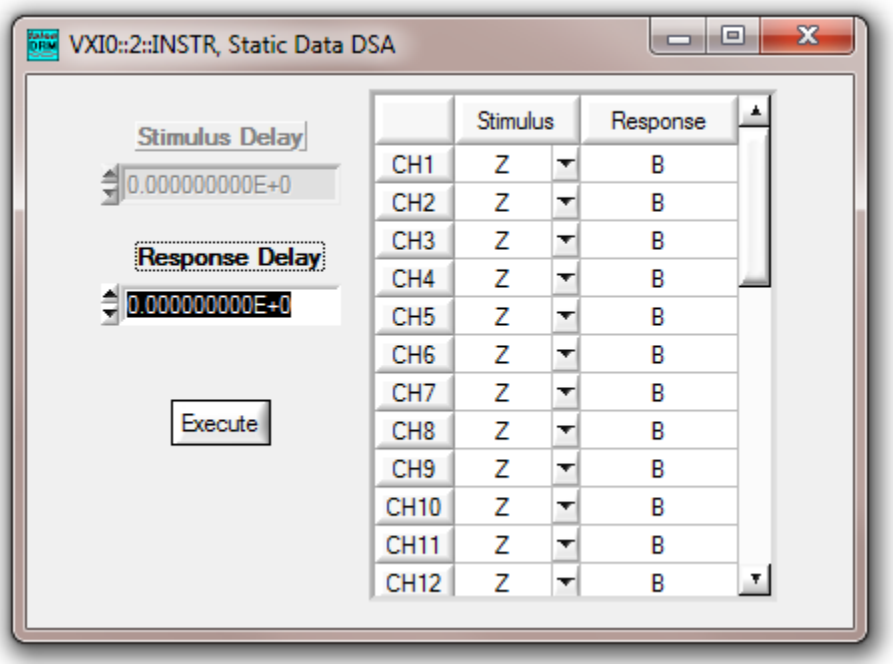


Figure 5-66: Static Data Panel

The static data panel contains controls that program the static timing and stimulus data and displays the current static response data.

Prior to sequencer revision 0.21, the static timing uses the pulse generator to specify the stimulus delay and the response delay for all the static channels to within 15ns. Both delays are with respect to the start of a sequence.

Sequencer revision 0.21 and later uses a dedicated timing source that specifies the response delay from 0 to 6.5ms. Stimulus delay is no longer supported.

Stimulus Delay

This control sets the delay from the start of a sequence execution to when the stimulus pattern will be output and is only available in sequencer revisions prior to 0.21.

The delay can be set from 20ns to 40s with 10ns resolution.

Note: *The Stimulus Delay must be less than the Response Delay.*

The relevant VXI*plug&play* API function is:

- tat964_setStaticTiming

Response Delay

Prior to sequencer revion 0.21 this control sets the delay from the start of a sequence execution to when the static pins will be sampled.

The delay can be set from Stimulus Delay + 10ns to Stimulus Delay + 40s with 10ns resolution. ***Note:*** *The Response Delay must be greater than the Stimulus Delay.*

For sequencer revision 0.21 and later, this control sets the delay when the static input pins will be sampled from 0 to 6.5ms with 100ns resolution. The delay is from the execution of the “tat964_executeStaticPattern” API.

The relevant VXI*plug&play* API function is:

- tat964_setStaticTiming
- tat964_executeStaticPattern

Stimulus

This table column contains pull down selections that sets the stimulus output state.

The selections for the table column pull-down control are:

Table 5-92: Static Stimulus Settings

Setting	Description
Z	Disable the channel.
0	Drive to low level.
1	Drive to high level.
X	Uninstalled channel

The relevant VXI*plug&play* API function is:

- tat964_setStaticData

Response

This table column contains the stimulus input state of the previous static execution.

The selections for the table column pull-down control are:

Table 5-93: Static Stimulus Settings

Code	Description
B	Response between high and low.
L	Response low level.
H	Response high level.
?	Unknown

The relevant VXI*plug&play* API function is:

- tat964_queryStaticResponse

Kept Data

The kept data display is accessed from the **Execute > DS*x* > View > Kept Data**

menu bar selection. (Where “x” is the sequencer you wish to query.)

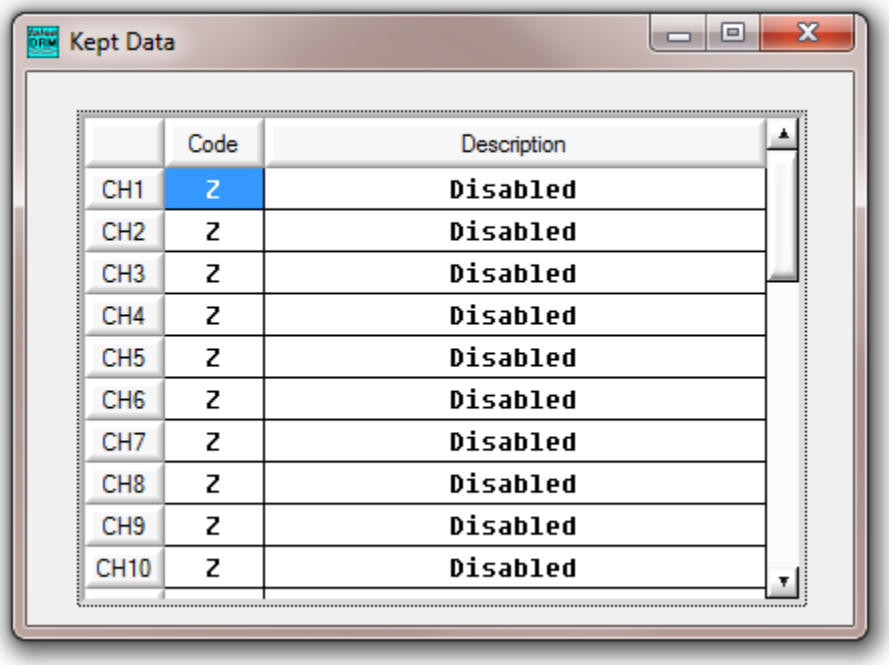


Figure 5-67: Kept Data Panel

The kept data represents the current pattern code that is not “Invert Previous Code” or “Repeat Previous Code”.

Note: *The Kept Data is updated at the end of a pattern so the contents of the kept data when halted or paused will contain the codes from the previous pattern.*

The relevant VXI*plug&play* API function is:

- tat964_queryKeptPattern

Results

The Results data display is accessed from the **Execute > DS*x* > View > Results** menu bar selection. (Where “x” is the sequencer you wish to query.)

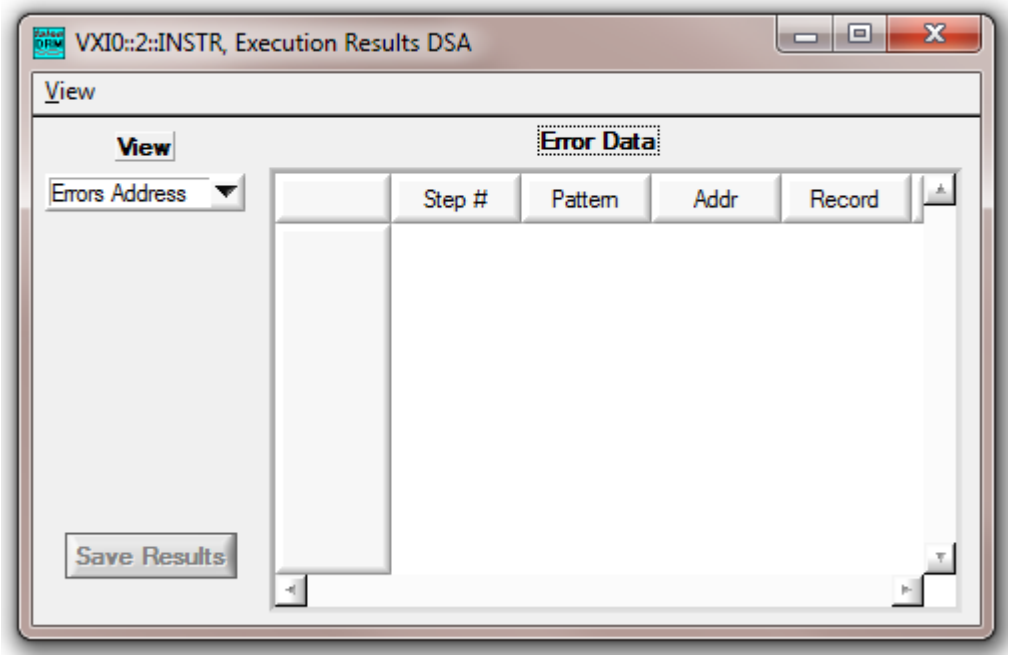


Figure 5-68: View Results Data Panel

View

This pull-down control selects the results to view.

The selections for this pull-down control are:

Table 5-94: Results View Settings

Setting	Description
CRCs	Display the CRC data from the previous sequence execution.
Error Address	Display the error address data from the previous sequence execution.
Record Index	Display the error address data from the previous sequence execution.
Record Data	Display the error address data from the previous sequence execution.
Probe Data	Display the error address data from the previous sequence execution.

Save Results

This command button will display a file save panel that allows the user to select and existing file or create a file to store the result data as a comma separated list (.csv). All numeric values are displayed as decimal.

CRC Save File Format

The CRC results are saved in the following format:

<id>,<crc><lf>

Where:

<id> CH01 through CH32, PG0 and PG1.

<crc> The CRC value.

Error Address Save File Format

The Error Address results are saved in the following format:

<header><line feed>

<step>,<offset>,<pma>,< data><line feed>

Where:

<header> “STEP,OFFSET,PMA,RECORD DATA”

<step> Step number of the error.

<offset> Pattern number.

<pma> Pattern Memory Address.

<data> Record memory.

Record Index Save File Format

The Record Index results are saved in the following format:

<header><line feed>

<step>,<offset><line feed>

Where:

<header> “STEP,OFFSET”

<step> Step number of the error.

<offset> Record memory offset where the results are saved.

Record Data Save File Format

The Record Data results are saved in the following format:

<header><line feed>

<step>,<offset>,<data><line feed>

Where:

<header> “STEP,OFFSET,RECORD DATA”

<step> Step number of the error.

<offset> Pattern number.

<data> Record Memory contents.

Probe Data Save File Format

The Record Data results are saved in the following format:

<header><line feed>

<step>,<offset>,<data><line feed>

Where:

<header>	"STEP,OFFSET,RECORD DATA"
<step>	Step number of the error.
<offset>	Pattern number.
<data>	Probe Memory contents.

CRCs Display

The CRC memory display is accessed from the **Execute > DS*x* > View > Results** menu bar selection and setting the **View** control to **CRCs**. (Where "x" is the sequencer you wish to query.)

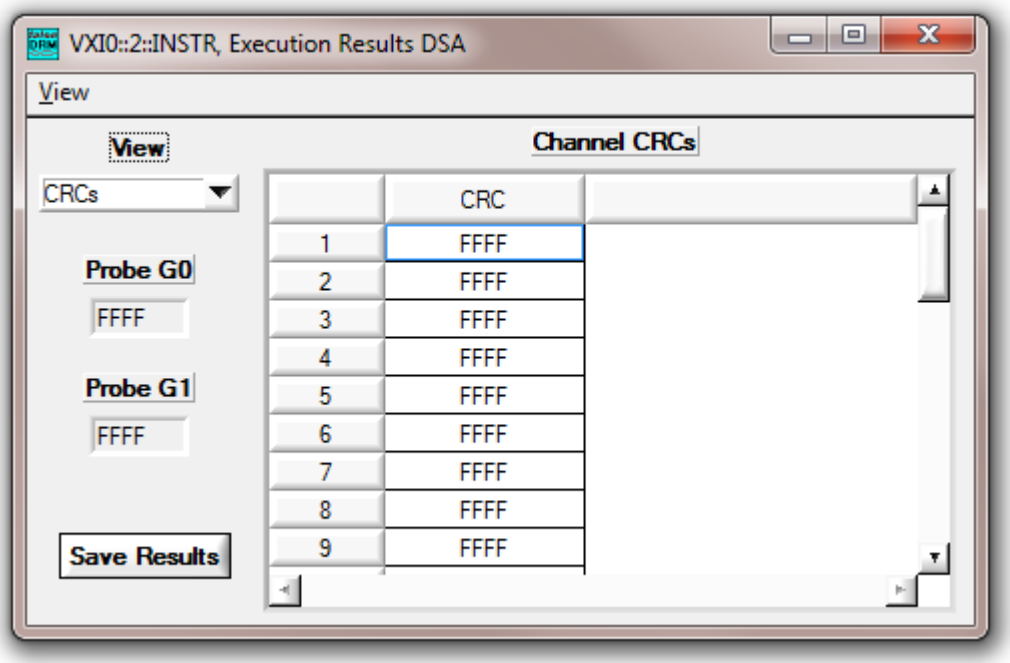


Figure 5-69: View CRC Panel

CRCs can be accumulated for all 32 channels as well as AUX1 which is dedicated for the probe channel (shown at the left).

The relevant VXI*plug&play* API functions are:

- tat964_queryCrc
- tat964_queryProbeCrc

Error Address Display

The Error Address memory display is accessed from the **Execute > DS*x* > View > Results** menu bar selection and setting the **View** control to **Errors Address**. (Where "x" is the sequencer you wish to query.)

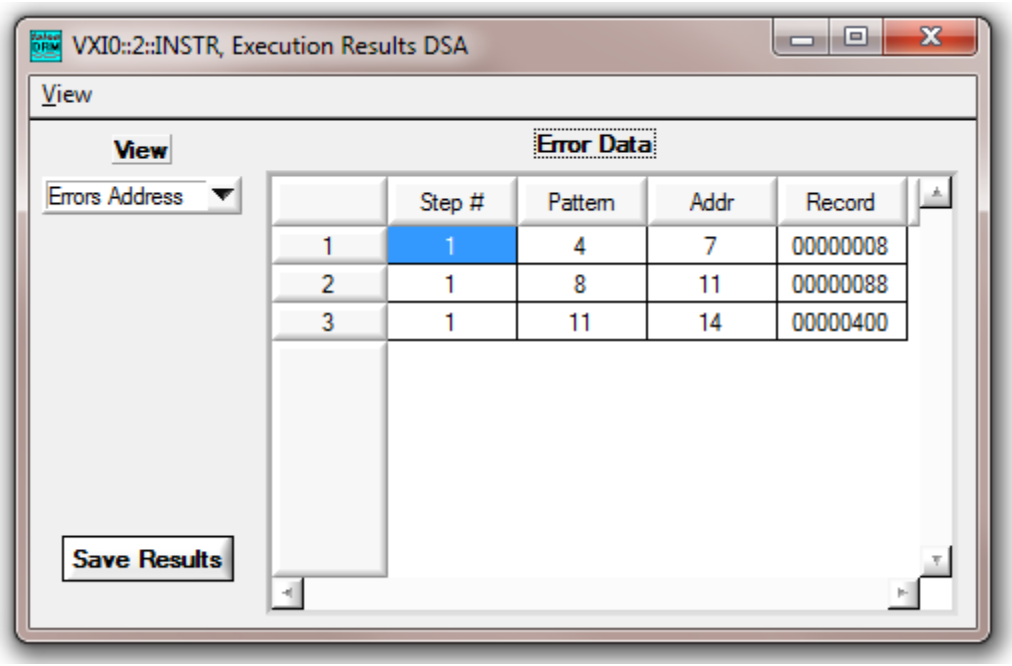


Figure 5-70: View Errors Address Panel

The error address memory records the sequence step and pattern address of the first 1024 errors of a sequence execution and is displayed in the **Step #** and **Addr** columns. The **Pattern** column is calculated based on the **Record Type** setting and **Record** column is read from the record memory.

The relevant VXI*plug&play* API function for **Step #** and **Addr** data is:

- tat964_queryErrorAddress

The relevant VXI*plug&play* API function for **Record** data is:

- tat964_queryRecordData

The relevant VXI*plug&play* API function for **Pattern** data is:

- tat964_queryPatternSet (if **Record Type** set to Normal)
- tat964_queryRecordIndex (if **Record Type** set to Indexed)

The View menu selection allows the address column of the error address panel to toggle between decimal and hexadecimal.

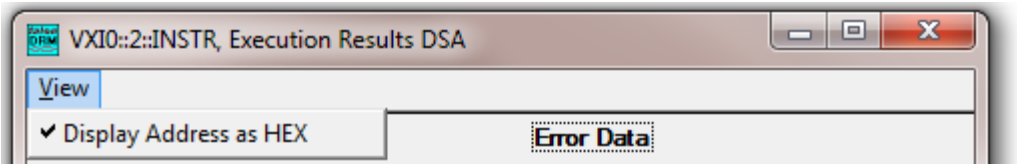


Figure 5-71: Execution Results View Menu

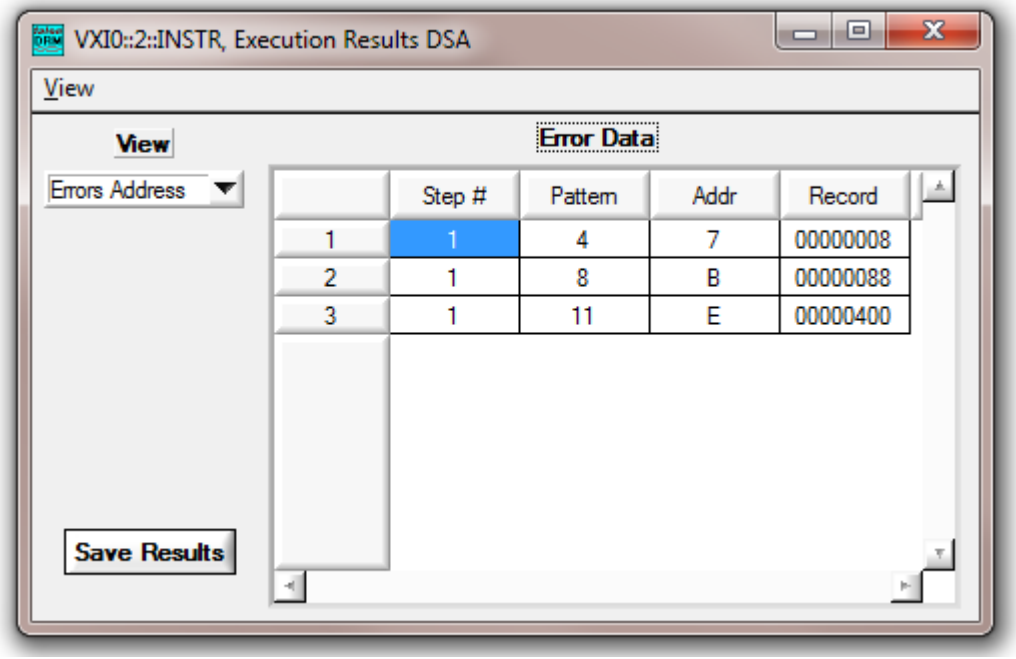


Figure 5-72: View Errors Address Panel Hex

Record Index Display

The record index memory display is accessed from the **Execute > DS*x* > View > Results** menu bar selection and setting the **View** control to **Record Index**. (Where "x" is the sequencer you wish to query.)

The record index memory stores the sequence step and pattern index of the first 1024 steps of a sequence execution.

When the record type is set to indexed, the sequence results are stored sequentially in the record memory starting at offset 0. The record index memory allows the user to determine sequence step order that filled the record memory.

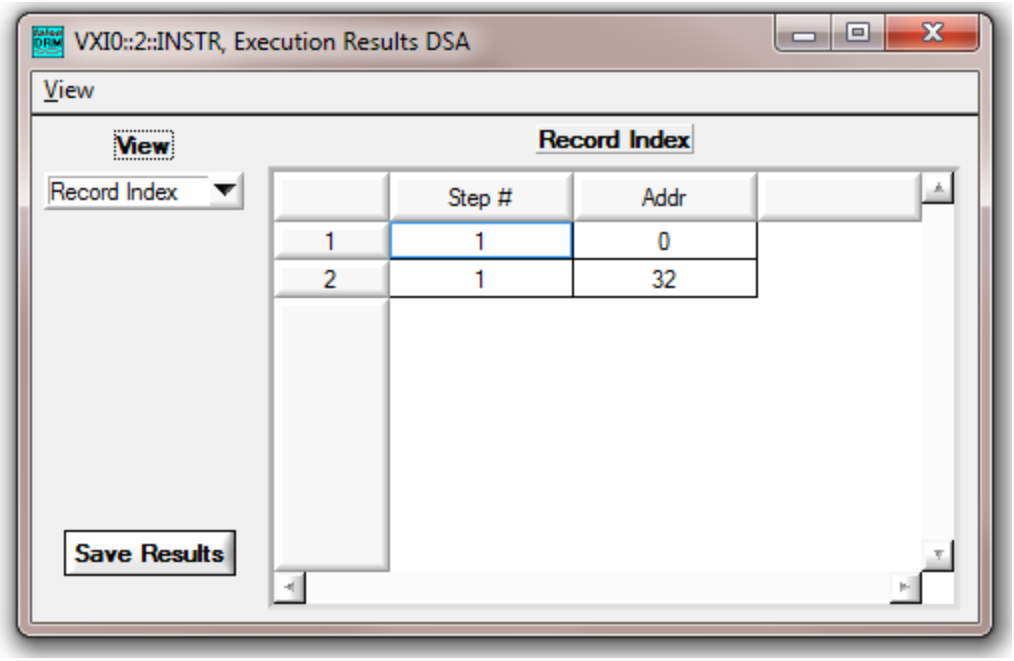


Figure 5-73: Record Index Panel

The relevant VXI*plug&play* API function is:

- tat964_queryRecordIndex

Record Data Display

The record memory display is accessed from the **Execute > DS*x* >View>Results** menu bar selection and setting the **View** control to **Record Data**. (Where “x” is the sequencer you wish to query.)

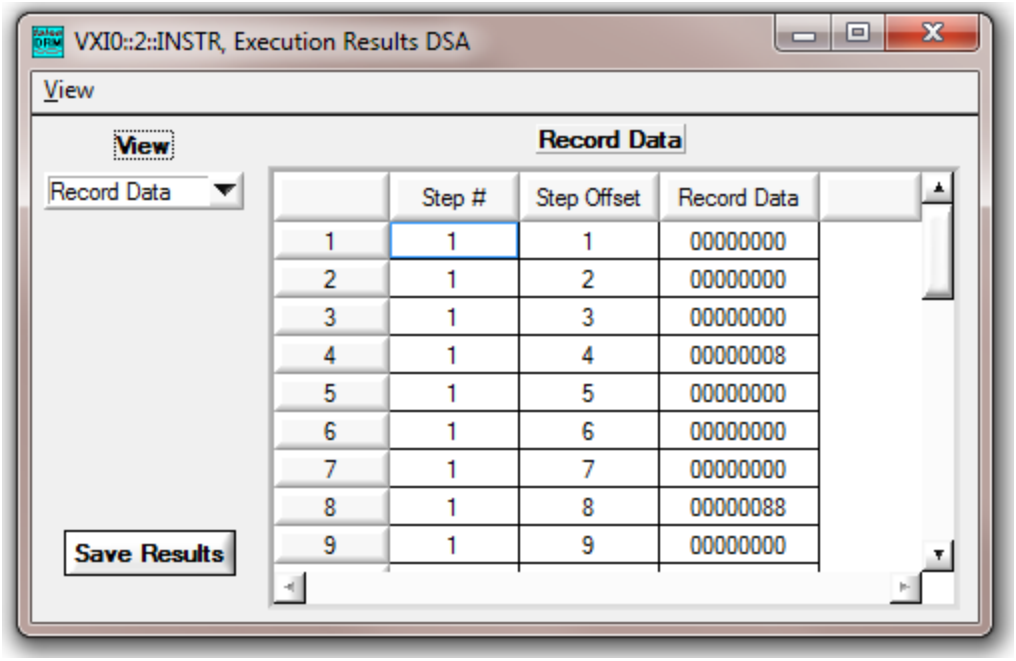


Figure 5-74: View Record Data Panel

The Record Data contains either the error or response results from the previous sequence burst (see **Step Record Mode** in **Chapter 5**).

The least significant bit of the record data (in hex) represents the error/response for channel 1 and the most significant bit represents channel 32. Error data stores a 1 to indicate a channel did not match its programmed expect value and a 0 indicates no error. Response data stores a 1 to indicate a high level and a 0 to indicate a low level. The compare level used for recoding response data is set by the Raw Record Basis (see **Raw Record Basis** in **Chapter 5**).

Note: *If there is a Capture Fault on a channel for one or more patterns, an error will be registered. If an error is not registered it means that the channel for this pattern was not only as expected but also that there was a valid capture. If an error is registered it could mean that the channel for this pattern was either not as expected or there was a capture fault. Capture faults are registered separately so that one can determine if there was a capture fault for this channel on one or more patterns. If so, one can look for programming faults and fix them first. Once the capture faults are taken care of, any remaining errors will now be bona fide errors (channel data not as expected). See the following* **Sequence Events** *and* **Driver/Receiver Data Panel** *sections for more information about capture faults.*

The relevant VXI*plug&play* API function is:

- tat964_queryRecordData

Probe Data Memory Display

The probe data memory display is accessed from the **Execute > DS*x* > View > Results** menu bar selection and setting the **View** control to **Probe Data**. (Where "x" is the sequencer you wish to query.)

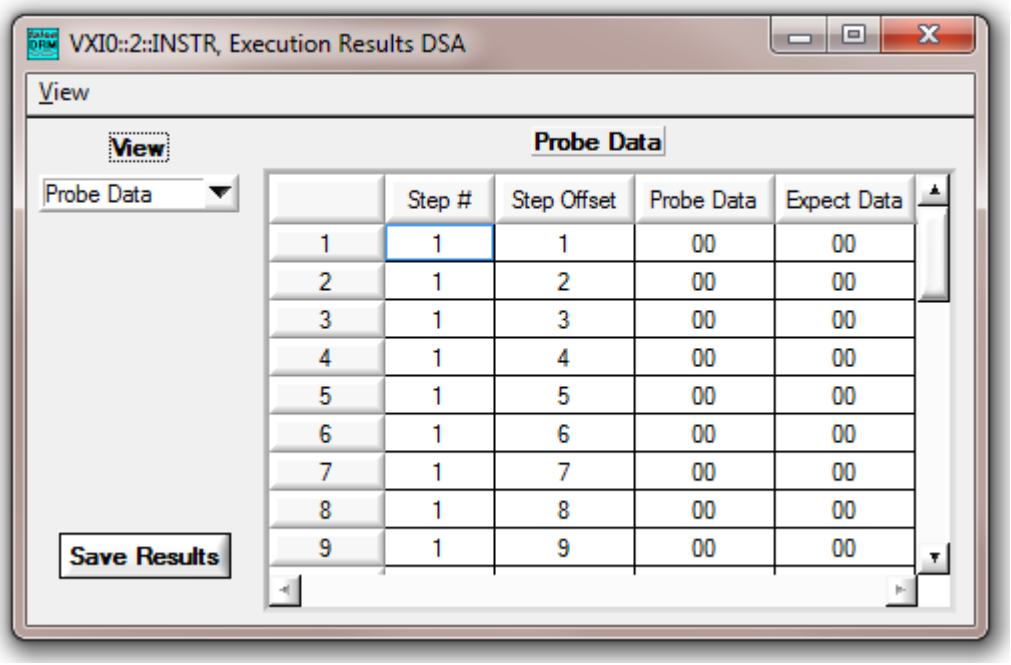


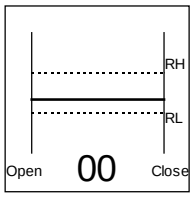
Figure 5-75: Probe Data Panel

The probe memory stores eight bits of data from the 1 input for every pattern.

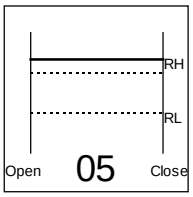
Table 5-95: Probe Memory Bit Descriptions

Bit	Description
0	Good 1 level at window 4 open
1	Good 0 level at window 4 open
2	Good 1 level at window 4 close
3	Good 0 level at window 4 close
4	Positive transition at good 1 level
5	Positive transition at good 0 level
6	Negative transition at good 1 level
7	Negative transition at good 0 level

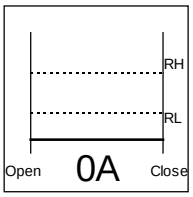
The combination of the eight bits allows the following probe states:



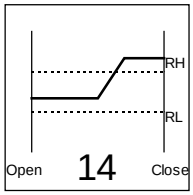
Middle – Signal remains between RL and RH.



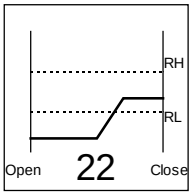
High – Signal remains above RH.



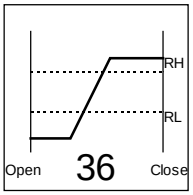
Low – Signal remains below RL.



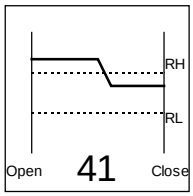
Middle High – Signal starts between RL and RH, crosses the RH once and ends above RH.



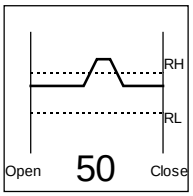
Low Middle – Signal starts below RL, crosses the RL once and ends between RL and RH.



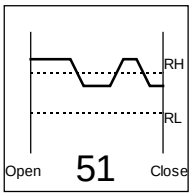
Rising Edge – Signal starts below RL and crosses the RL and RH once.



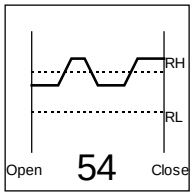
High Middle – Signal starts above RH, crosses RH once and ends between RL and RH.



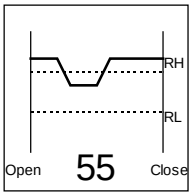
Middle High Glitch - Signal starts between RL and RH, crosses the RH two or more times and ends between RL and RH.



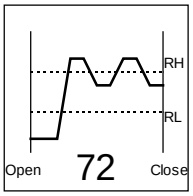
High Glitch Middle – Signal starts above RH, crosses the RH three or more times and ends between RL and RH.



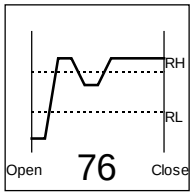
Middle Glitch High - Signal starts between RL and RH, crosses the RH three or more times and ends above RH.



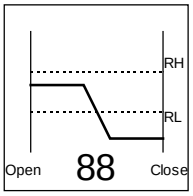
High Glitch – Signal starts above RH, crosses the RH two or more times and ends above RH.



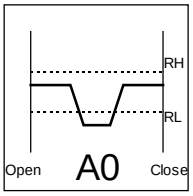
Rising Edge Glitch Middle – Signal starts below RL, crosses RL once, crosses RH two or more times and ends between RL and RH.



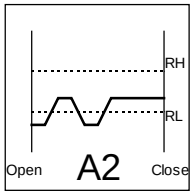
Rising Edge Glitch – Signal starts below RL, crosses RL once, crosses RH three or more times and ends above RH.



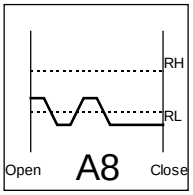
Middle Low – Signal starts between RL and RH, crosses the RL once and ends below RL.



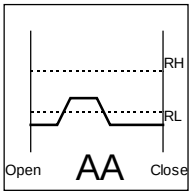
Middle Low Glitch - Signal starts between RL and RH, crosses the RL two or more times and ends between RL and RH.



Low Glitch Middle - Signal starts below RL, crosses the RL

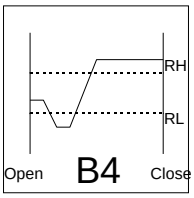


Middle Glitch Low - Signal starts between RL and RH,



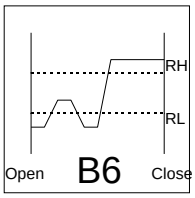
Low Glitch - Signal starts below RL, crosses the RL two or more times and ends below RL.

three or more times and ends between RL and RH.

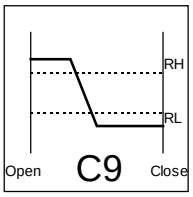


Middle Rising Edge - Signal starts between RL and RH, crosses the RL two or more times, crosses RH once and ends above RH.

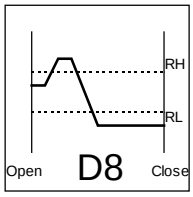
crosses the RL three or more times and ends below RL.



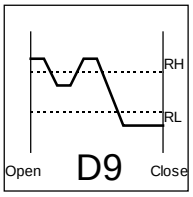
Low Glitch Rising Edge - Signal starts below RL, crosses the RL three or more times, crosses RH once and ends above RH.



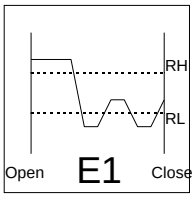
Falling Edge – Signal starts above RH and crosses the RH and RL once and ends below RL.



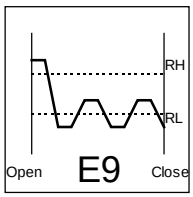
Middle Falling Edge - Signal starts between RL and RH, crosses the RH two or more times, crosses RL once and ends below RL.



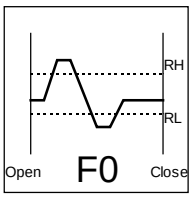
High Glitch Falling Edge - Signal starts above RH, crosses the RH three or more times, crosses RL once and ends below RL.



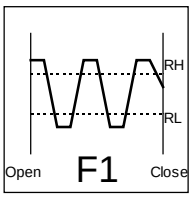
Falling Edge Glitch Middle – Signal starts above RH, crosses RH once, crosses RL two or more times and ends between RL and RH.



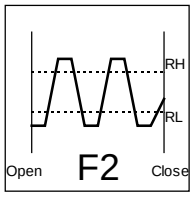
Falling Edge Glitch – Signal starts above RH, crosses RH once, crosses RL three or more times and ends below RL.



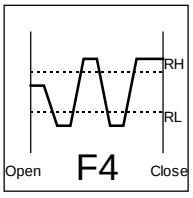
Middle Pulse Middle – Signal starts between RL and RH, crosses RH and RL two or more times and ends between RL and RH.



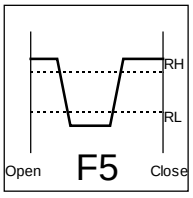
High Pulse Middle – Signal starts above RH, crosses RH three or more times, RL two or more times and ends between RL and RH.



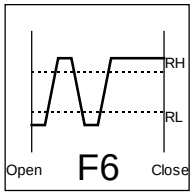
Low Pulse Middle – Signal starts below RL, crosses RL three or more times, RH two or more times and ends between RL and RH.



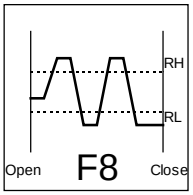
Middle Pulse High – Signal starts between RL and RH, crosses RL two or more times, RH three or more times and ends above RH.



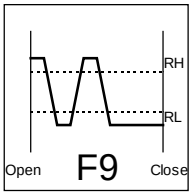
High Pulse – Signal starts above RH, crosses RH and RL two or more times and ends above RH.



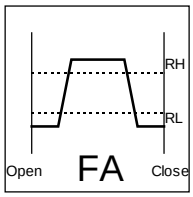
Low Pulse High – Signal starts below RL, crosses RL and RH three or more times and ends above RH.



Middle Pulse Low – Signal starts between RL and RH, crosses RL three or more times, RH two or more times and ends below RL.



High Pulse Low – Signal starts above RH, crosses RL and RH three or more times and ends below RL.



Low Pulse – Signal starts below RL, crosses RL and RH two or more times and ends below RL.

The relevant VXI*plug&play* API function is:

- tat964_queryProbeData

Status Indicator Panels

The status indicator panels allow the operator to view the available status results to determine if the previous execution sequence is valid. The following panels are available:

- Sequencer Events
- Sequencer Data
- Driver/Receiver Events
- Driver/Receiver Data
- VXI Trigger Readback
- Power Query
- Power Converter Condition
- Counter/Timer
- PMU

Sequencer Events

The sequence events display is accessed from the **Execute > DS*x* > View > Sequencer Events** menu bar selection. (Where “x” is the sequencer you wish to query.)

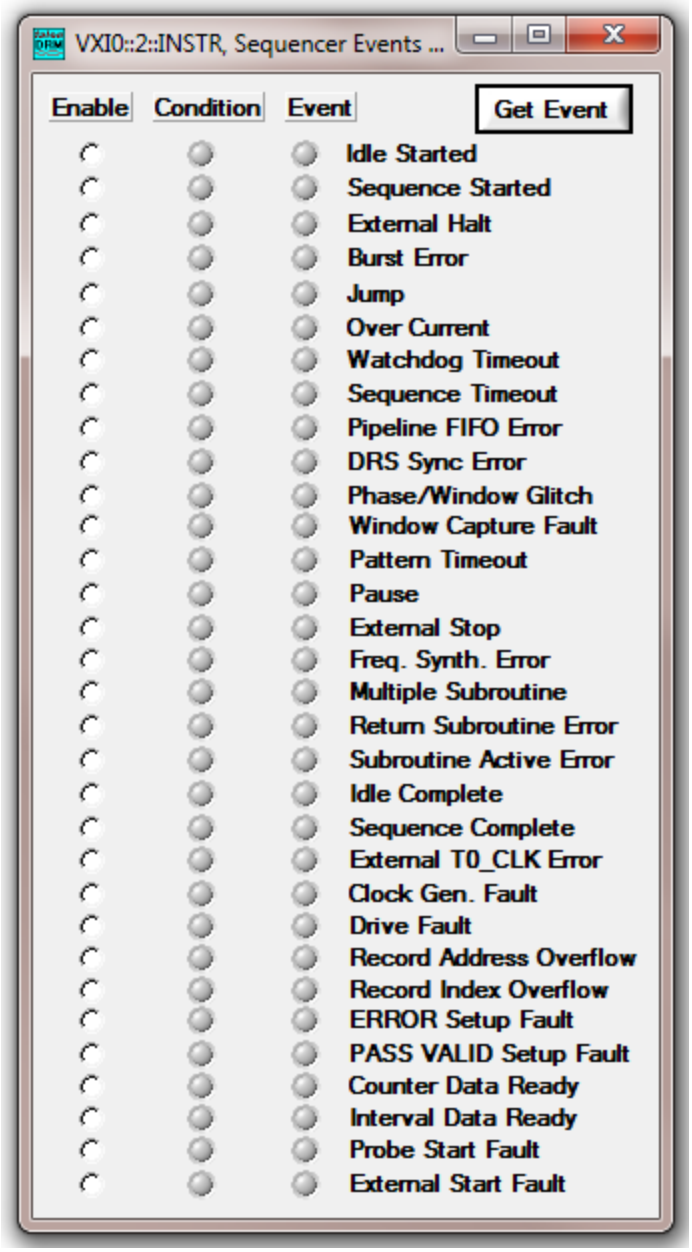


Figure 5-76: Sequencer Event Status Panel

The following sequencer enable, condition and event bits are defined:

Table 5-96: Sequence Enable/Condition/Event Bit Descriptions

Bit	Name	Description
0	Idle Started	The idle state has been entered
1	Sequence Started	The sequence active state has been entered.
2	External Halt	One or more external halts occurred.
3	Burst Error	One or more errors occurred.
4	Jump	One or more jumps occurred.

Bit	Name	Description
5	Over-Current	One or more channels generated an over-current event.
6	Watchdog Timeout	A watchdog timeout occurred.
7	Sequence Timeout	A sequence timeout occurred.
8	Pipeline FIFO Error	Pipeline depth inadequate for the Data Rate.
9	DRS Sync Error	The DRS sync error flag is set. The error step and error pattern address are available in the sequencer status panel.
10	Phase/Window Glitch	A phase or window pulse less than 8ns was detected.
11	Window Capture Fault	An expect pattern code was programmed on a channel with the capture mode set to none or the window was missing.
12	Pattern Timeout	A pattern timeout occurred.
13	Pause	A pause occurred.
14	External Stop	External stop signal received.
15	Freq. Synth. Error	The frequency synthesizer is selected as the master clock and is running slower than 40 kHz.
16	Multiple Subroutine	Attempt to jump to a subroutine when already in one.
17	Return Subroutine Error	Return encountered when not in a subroutine.
18	Subroutine Active Error	Sequence completed while still in a subroutine.
19	Idle Complete	Idle sequence completed.
20	Sequence Complete	Sequence completed.
21	External T0_CLK Error	The external T0_CLK is too fast or glitchy. The edges which cause the “too fast” condition are ignored such that the resultant T0_CLK period will not be allowed to be <16 Master clocks when the probe is enabled (<10 Master Clocks when not) OR, the T0_CLK is too slow (period >65.5 us with a 500 MHz master clock...or proportionately slower for a slower master clock).
22	Clock Gen. Fault	The fault is automatically corrected but one or more patterns may have been corrupted.
23	Drive Fault	A Drive Fault occurred.
24	Record Address Overflow	Indicates that the data recorded at the last memory address may be corrupted.
25	Record Index Overflow	Indicates that there is more data recorded than can be reconstructed.
26	ERROR Setup Fault	DRS/Linked Error Signal not assigned.
27	PASS VALID Setup Fault	DRS/Linked Pass Valid Signal not assigned.
28	Counter Data Ready	Frequency counter data ready.
29	Interval Data Ready	Interval Timer data ready.

Bit	Name	Description
30	Probe Start Fault	Probe button pushed while probe is not enabled or memory is not granted.
31	External Start Fault	External start signal while memory is not granted.

Enable

These radio buttons enable/disable the associated event from setting the sequencer interrupt event.

The relevant VXI*plug&play* API function is:

- tat964_setEventEnable

Condition

These LEDs indicate the current state of the associated signal.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerCondition

Event

These LEDs indicate if the state of the associated signal went true.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerEvent

Clear Event

This command button resets the event LEDs.

Sequencer Data Panel

The sequence status display is accessed from the **Execute > DS*x* > View > Sequencer Data** menu bar selection. (Where “x” is the sequencer you wish to query.)

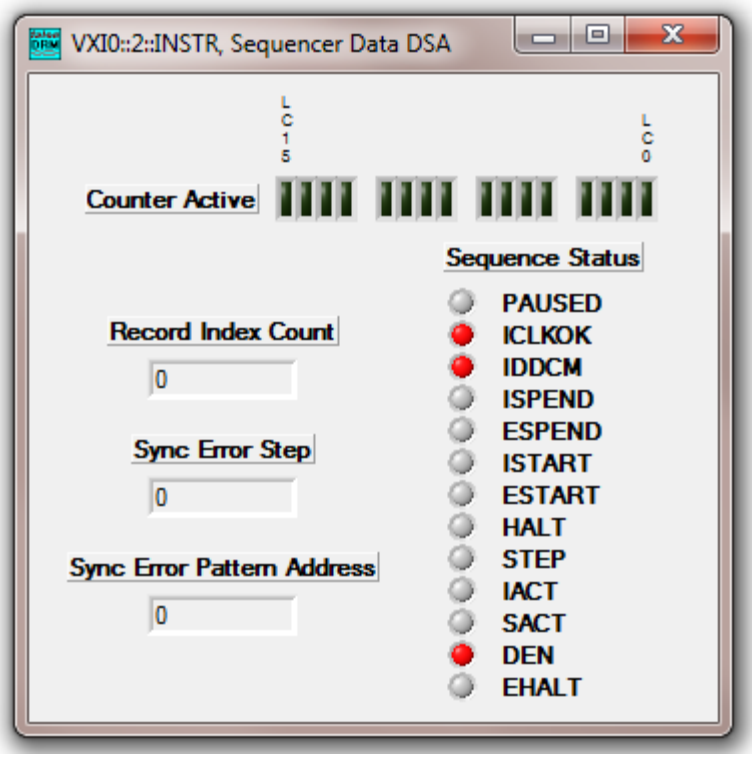


Figure 5-77: Sequencer Data DSA Panel

Counter Active

This set of LEDs indicates whether the loop counter is active or not. An active counter will have its LED illuminated.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerCounterStatus

Record Index Count

This indicator displays the number of valid entries in the record index memory.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerRecordIndex

Sync Error Step

This indicator displays the step number that was active when the DRS sync error occurred.

The relevant VXI*plug&play* API function is:

- tat964_querySequencerSyncError

Sync Error Pattern Address

This indicator displays the pattern address that was active when the DRS sync

error was detected.

Note: *This pattern address may be up to 5 patterns later than the first detection of a sync error. Also, the Sync Error Step and Pattern Address is only relevant on coupled sequencers.*

The relevant VXI*plug&play* API function is:

- tat964_querySequencerSyncError

Status

These LED indicators display the sequence status bits.

The following sequencer status bits are defined:

Table 5-97: Sequence Status Bit Descriptions

Bit	Name	Description
0	PAUSED	Sequencer is paused
1	ICLKOK	500 MHz Clock OK
2	IDDCM	Input Delay DCM locked
3	ISPEND	Internal Stop Pending
4	ESPEND	External Stop Pending
5	ISTART	Internal Start Pending
6	ESTART	External Start Pending
7	HALT	Sequencer is Halted
8	STEP	Single Step Pending
9	IACT	Idle Sequence Active
10	SACT	Sequence Active
11	DEN	Drivers Enabled
12	EHALT	External Halt Pending

The following sequencer status bits are defined:

The relevant VXI*plug&play* API function is:

- tat964_querySequencerStatus

Driver/Receiver Events Panel

The Driver/Receiver events display is accessed from the **Execute > DS*x* > View > Driver/Receiver Events** menu bar selection. (Where “x” is the sequencer you wish to query.)

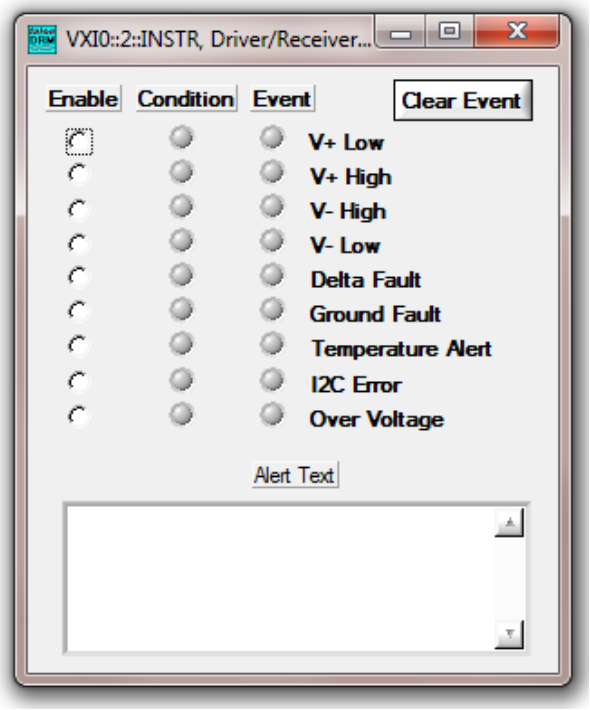


Figure 5-78: DR3E/DR9/UR14 Driver/Receiver (D/R) Events Panel

The following DR3e/DR9/UR14 Driver/Receiver event bits are defined:

Table 5-98: Sequence Status Bit Descriptions

Name	Description	DR3 Threshold	DR3e/DR9/UR14 Threshold
V+ Low	V+ too low error.	< +9.65	< +8.84
V+ High	V+ too high error.	< +29.00	< +29.70
V- High	V- too high error.	> -2.80	> -2.91
V- Low	V- too low error	< -19.50	< -19.8
Delta Fault	The V+ to V- delta error	> +34.00	> +34.3
Ground Fault	DUT_GND to SIG GND delta error greater than ~390 mV (even if it's not being used as the DUT_GND for the Pin Electronics devices).	> 0.39	> 0.39
Temperature Alert	One or more of the Pin Electronics devices has exceeded the specified temperature.	NA	NA
I^2C Error	The I2C communication bus has had an error in the communication protocol.	NA	NA
Over-voltage Fault	One or more channels had an over-voltage.	NA	NA

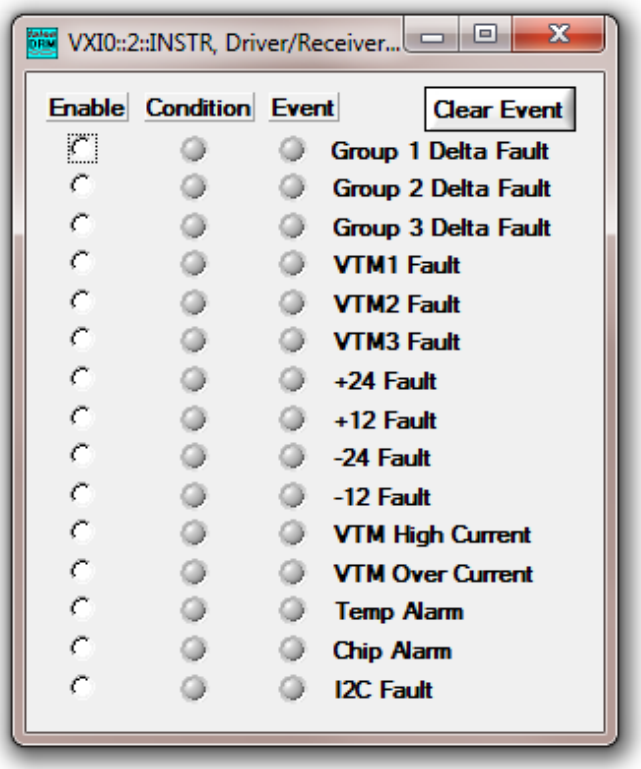


Figure 5-79: DR4 Driver/Receiver (D/R) Events Panel

The following DR Driver/Receiver event bits are defined:

Table 5-99: Sequence Status Bit Descriptions

Name	Description	Threshold
Group 1 Delta Fault	Group 1 V+ to V- delta too large.	+36.0
Group 2 Delta Fault	Group 2 V+ to V- delta too large.	+36.0
Group 3 Delta Fault	Group 3 V+ to V- delta too large.	+36.0
VTM1 Fault	Power converter VTM1 fault set	NA
VTM2 Fault	Power converter VTM2 fault set	NA
VTM3 Fault	Power converter VTM3 fault set	NA
+24V Fault	The +24 V fuse reports open	NA
+12V Fault	The +12 V fuse reports open	NA
-24V Fault	The -24 V fuse reports open	NA
-12V Fault	The -12 V fuse reports open	NA
VTM Over Current Fault	VTM exceeded output current and shutdown.	>3.25A
VTM High Current Warning	VTM High current warning	>2.8A

Name	Description	Threshold
Temp Alarm	Temp alarm set from the temperature monitor chip	NA
Chip Alarm	Chip alarm set from the driver/receiver chip.	NA
I2C Error	The I2C communication bus has had an error in the communication protocol.	NA

Enable

These radio buttons enable/disables the associated event from setting the Driver/Receiver interrupt event.

The relevant VXIplug&play API function is:

- tat964_setEventEnable

Condition

These LEDs indicate the current state of the associated signal.

The relevant VXIplug&play API function is:

- tat964_queryFrontEndCondition

Event

These LEDs indicate if the state of the associated signal went true.

The relevant VXIplug&play API function is:

- tat964_queryFrontEndEvent

Clear Event

This command button resets the event LEDs.

Note: *Any one of these faults (except for Ground Fault or I2C Error) will open the power relays.*

Alert Text

This indicator displays the channel that generated the temperature alert event.

The alert is returned as a 32 bit number and then converted to text by the soft front panel.

Table 5-100: Alert Bit Descriptions

Bit	DR3e Channel	DR9 Channel	UR14 Channel
0	CH9, CH10	CH1, CH2	AUX3 B
1	CH3, CH4	CH7, CH8	AUX4 B
2	CH25, CH26	CH4	AUX1 A
3	CH13, CH14	CH5	AUX2 A
4	AUX1, AUX2	CH6	AUX1 B
5	CH23, CH24	CH3	AUX2 B
6	Local D1	Local D1	Local D1
7	CH17, CH18	CH9, CH10	NU
8	CH1, CH2	CH15, CH16	NU
9	CH7, CH8	CH12	NU
10	CH31, CH32	CH13	NU
11	CH27, CH28	CH14	NU
12	AUX3, AUX4	CH11	NU
13	D2 Local	D2 Local	NU
14	CH19, CH20	CH17, CH18	NU
15	CH21, CH22	CH23, CH24	NU
16	CH5, CH6	CH20	NU
17	CH11, CH12	CH21	NU
18	CH15, CH16	CH22	NU
19	CH29, CH30	CH19	NU
20	D3 Local	D3 Local	NU

The relevant VXI*plug&play* API function is:

- tat964_queryFrontEndAlert

Driver/Receiver Data Panel

The Driver/Receiver data display is accessed from the **Execute > DS*x* > View > Driver/Receiver Data** menu bar selection. (Where “x” is the sequencer you wish to query.)

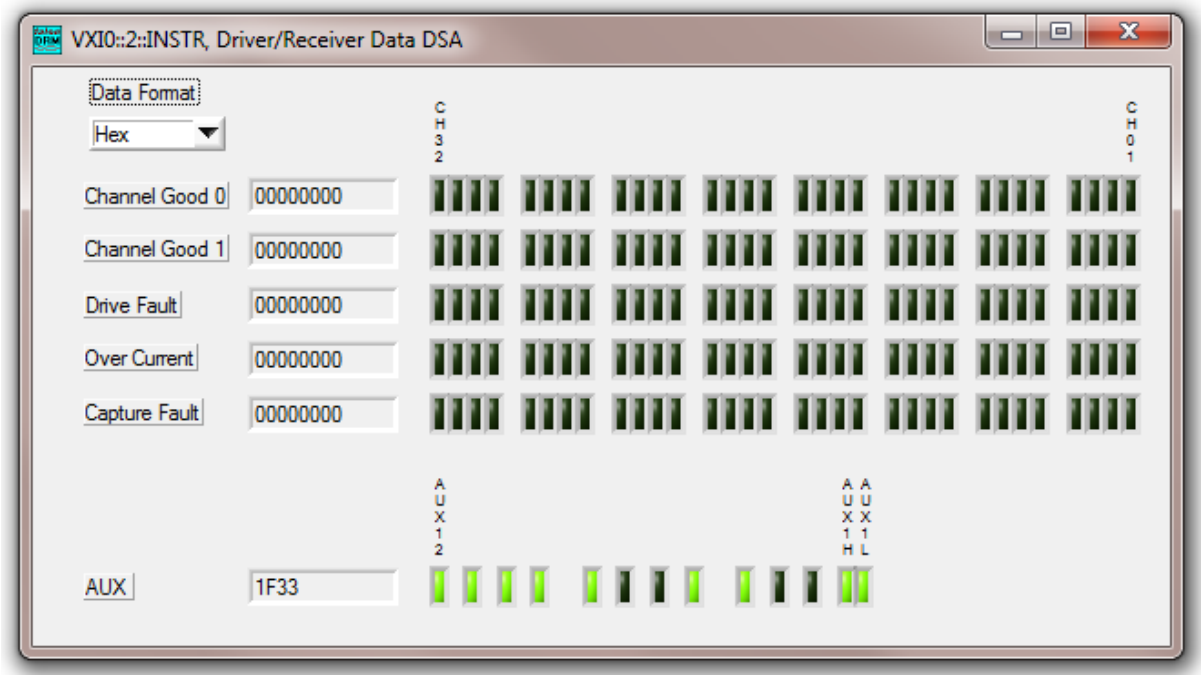


Figure 5-80: Driver/Receiver Data Panel

This panel displays the following Driver/Receiver data:

Channel Good 0	A '1' (LED illuminated) indicates that the channel is currently lower than the low comparator (CVL).
Channel Good 1	A '1' (LED illuminated) indicates that the channel is currently higher than the high comparator (CVH).
Drive Fault	A '1' (LED illuminated) indicates that the channel has triggered a drive fault event.
Over-Current	A '1' (LED illuminated) indicates that the channel has triggered an over-current event.
Capture Fault	A '1' (LED illuminated) indicates that the channel has triggered a Capture Fault.
AUX	A '1' (LED illuminated) indicates that the channel is currently higher than the high comparator. The DR3e AUX1 signal is a dual comparator, AUX1L indicates the low comparator and AUX1H indicates the high comparator.

The relevant VXI*plug&play* API functions are:

- tat964_querySequencerChannels
- tat964_querySequencerAux

- tat964_querySequencerDriveFault
- tat964_querySequencerOverCurrent
- tat964_queryCaptureFault

VXI Trigger Readback Panel

The VXI trigger readback display is accessed from the **Execute > DS*x* > View > VXI Trigger Readback** menu bar selection. (Where "x" is the sequencer you wish to query.)

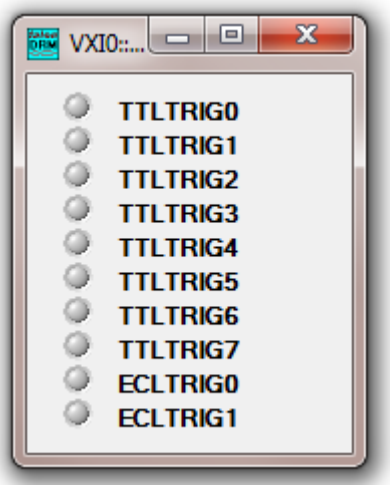


Figure 5-81: VXI Trigger Readback Panel

This panel displays the current level of the eight TTL and two ECL VXI backplane triggers. The LED illuminated indicates a high state.

Note: *A "high" TTLTRG signal is active "low" on the backplane.*

The relevant VXI*plug&play* API function is:

- tat964_queryVxiTrigger

Query Power Results Message

The query power results display is accessed from the **Execute > DS*x* >View>Power Query** menu bar selection. (Where "x" is the sequencer you wish to query.)

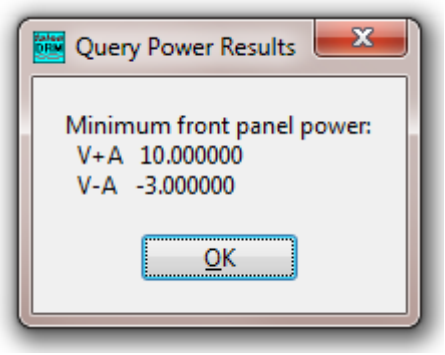


Figure 5-82: Query Power Results Message

This display shows the external power minimum requirements based on the current level settings programmed on the Driver/Receiver board.

The relevant VXI*plug&play* API function is:

- tat964_queryPowerOverhead

Power Converter Condition Panel

The power converter conditions display is accessed from the **Execute > DS*x* > View > Power Converter Condition** menu bar selection. There is only one power converter per DRM so the DSA and DSB selection will display the same panel.

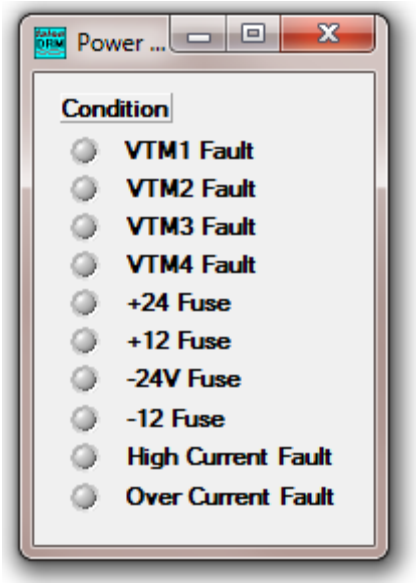


Figure 5-83: Power Converter Condition Panel

The following power converter bits are defined:

VTM1 Fault	Power converter VTM1 failure.
VTM2 Fault	Power converter VTM2 failure.

VTM3 Fault	Power converter VTM3 failure.
VTM4 Fault	Power converter VTM4 failure.
+24V Fuse	The +24V level is too low.
+12V Fuse	The +12V level is too low.
-24V Fuse	The -24V level is too high.
-12V Fuse	The -12V level is too high.
High Current Fault	High current condition detected.
Over Current Fault	Over current condition detected and shut down the power converter.

The relevant VXI*plug&play* API function is:

- tat964_queryPowerConverterCondition

Counter/Timer Panel

The / Counter/Timer Panel is accessed from the **Execute > DS*x* > View > Counter/Timer** menu bar selection where ***x*** is sequencer A or B. One Counter/Timer is provided for each sequencer.

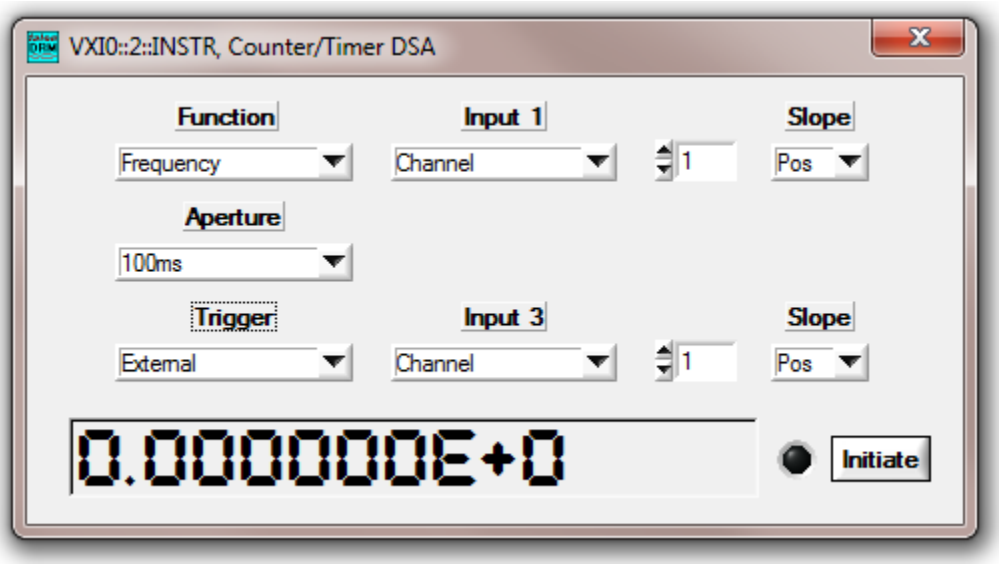


Figure 5-84: Timer/Counter Panel

Function

This pull-down control programs the counter/timer function.

The selections for this pull-down control are:

Table 5-101: Counter/Timer Function Settings

Setting	Description
Frequency	**Initiate** command button performs a frequency measurement on input 1.
Period	**Initiate** command button performs a period measurement on input 1.
Time Interval	**Initiate** command button performs a time interval measurement from input 1 to input 2.
Totalize	**Initiate** command button counts the input 1 transitions during input 3.
Timed Totalize	**Initiate** command button counts input 1 transitions during the specified aperture time.
Positive Pulse	**Initiate** command button performs a time interval measurement from the rising edge input 1 to the falling edge of input 1.
Negative Pulse	**Initiate** command button performs a time interval measurement from the falling edge input 1 to the rising edge of input 1.

The relevant VXI*plug&play* API function is:

- tat964_setCounterFunction
- tat964_queryCounterFunction

Input <1-3> Source

These controls allow the counter input source to be selected.

The selections for this pull-down control are:

Table 5-102: Counter/Timer Input <1-3> Source

Source	Description
Channel	Channel 1 through 32
AUX	AUX 1 through 12
Freq. Synth.	Frequency Synthesizer
VXICLK10	10 MHz VXI backplane clock.
250 MHz	500 MHz clock divided by 2.
Pulse Generator	Pulse Generator.

The relevant VXI*plug&play* API function is:

- tat964_setCounterInput
- tat964_queryCounterInput

Input <1-3> Slope

These controls allow the counter input slope to be selected.

Table 5-103: Counter/Timer Input <1-3> Slope

Source	Description
Pos	Select rising edge.
Neg	Select falling edge.

The relevant VXI*plug&play* API function is:

- tat964_setCounterInput
- tat964_queryCounterInput

Aperture

This control sets the gate aperture time for the frequency, period and timed totalize functions.

Table 5-104: Counter/Timer Aperture

Setting	Description
1us	One microsecond gate time.
10us	Ten microsecond gate time.
100us	One hundred microsecond gate time.
1ms	One millisecond gate time.
10ms	Ten millisecond gate time.
100ms	One hundred millisecond gate time.
1s	One second gate time.
10s	Ten second gate time.

The relevant VXI*plug&play* API function is:

- tat964_setCounterAperture
- tat964_queryCounterAperture

Trigger

This pull-down control programs the trigger source.

The selections for this pull-down control are:

Table 5-105: Timer/Counter Trigger Source

Source	Description
None	Disables the timer/counter.
External	Sets input 3 as the trigger source.
Internal Continuous	Enables Continuous Measurements.
Internal Single	Performs one measurement with initiate.

The relevant VXI*plug&play* API function is:

- tat964_setCounterTrigger
- tat964_queryCounterTrigger

Initiate

Generates an immediate trigger to the timer/counter.

The relevant VXIplug&play API function is:

- tat964_CounterInitiateTrigger

Results

Retrieve the results of the selected counter/timer function.

The relevant VXIplug&play API function is:

- tat964_measureCounterResults

PMU Panel

The PMU display is accessed from the **Execute > DS*x* >View>PMU** menu bar selection.

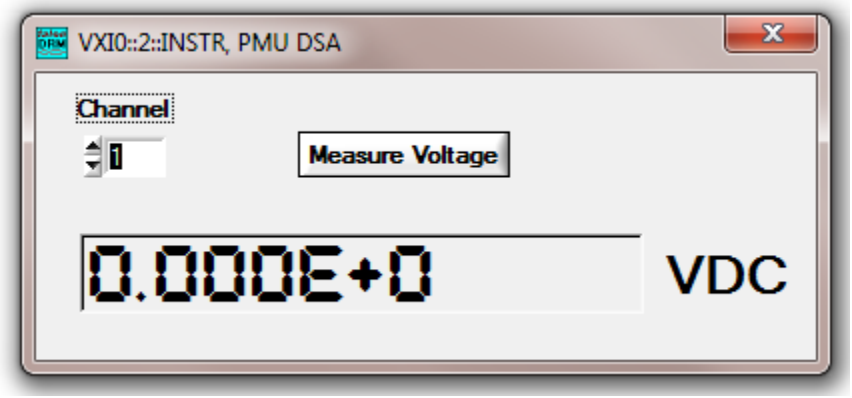


Figure 5-85: PMU Panel

Channel

This control sets the channel number to measure.

The relevant VXIplug&play API functions are:

- tat964_pmuMeasureVoltage

Measure Voltage

This control initiates a voltage measurement.

The relevant VXI*plug&play* API function is:

- tat964_pmuMeasureVoltage

Instrument Functions

The Instrument menu bar selections allow the user to perform the following:

- Self-test functions
- Calibration
- Firmware Updates
- Temperature Monitoring
- Voltage Monitoring

The instrument functions are dependent on the Driver/Receiver boards installed. For example; the DR1 Driver/Receiver board does not require voltage calibration and does not contain voltage and temperature monitoring hardware.

Self Test

The self-test function is accessed from the **Instrument >Self Test** menu bar selection.

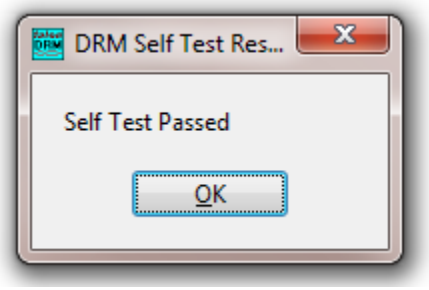


Figure 5-86: Self Test Result Message

The self-test function resets the instrument and performs a short RAM test on all the internal memories. The short RAM test tests each RAM at the major address bits locations, i.e., 0, 1, 2, 4, 8, 16 . . . etc.

The self-test result codes are:

Table 5-106: Self Test Result Code Descriptions

Code	Description
0	Self Test Passed
1	DSA 500 MHz clock test failed
2	DSA frequency synthesizer test failed
3	DSA VXICLK10 test failed
4	DSA pulse generator test failed
5	reserved
6	reserved
7	reserved
8	DSA sequence RAM test failed
9	DSA timing set RAM test failed
10	DSA persistence RAM test failed
11	DSA waveform RAM test failed
12	DSA record index RAM test failed
13	DSA error address RAM test failed
14	DSA pattern 0 (CH1-CH8) RAM test failed
15	DSA pattern 1 (CH9-CH16) RAM test failed
16	DSA pattern 2 (CH17-CH24) RAM test failed
17	DSA pattern 3 (CH25-CH32) RAM test failed
18	DSA record RAM test failed
19	DSA probe/flag RAM test failed
20	DSB 500 MHz clock test failed
21	DSB frequency synthesizer test failed
22	DSB VXICLK10 test failed
23	DSB pulse generator test failed
24	reserved
25	reserved
26	reserved
27	DSB sequence RAM test failed
28	DSB timing set RAM test failed
29	DSB persistence RAM test failed
30	DSB waveform RAM test failed
31	DSB record index RAM test failed
32	DSB error address RAM test failed
33	DSB pattern 0 (CH1-CH8) RAM test failed
34	DSB pattern 1 (CH9-CH16) RAM test failed
35	DSB pattern 2 (CH17-CH24) RAM test failed
36	DSB pattern 3 (CH25-CH32) RAM test failed
37	DSB record RAM test failed
38	DSB probe/flag RAM test failed

The relevant VXI*plug&play* API function is:

- tat964_self_test

Full RAM Test

The full RAM test function is accessed from the **Instrument >Full RAM Test** menu bar selection.

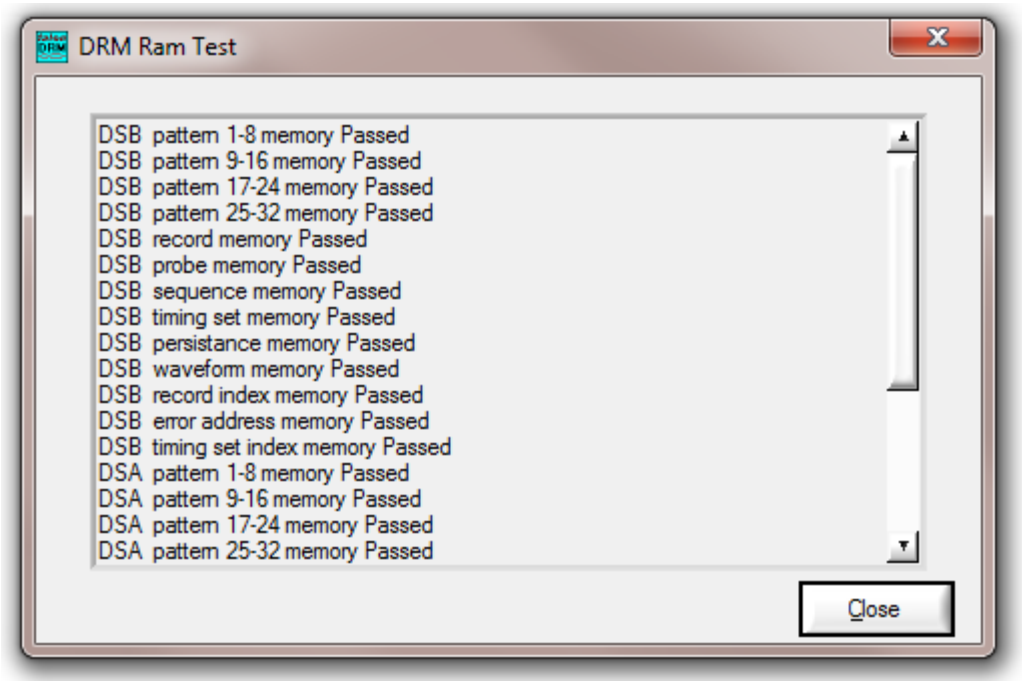


Figure 5-87: Full RAM Test Results Panel

The full RAM test function saves the current memory contents and performs a full RAM test on all the internal memories. The full RAM test performs multiple read/write cycles to each RAM at every address location. The full RAM test utilizes special hardware to test the pattern, record and probe memories at speed.

The relevant VXI*plug&play* API function is:

- tat964_ramTest

Power Converter Test

The power converter test function is accessed from the **Instrument >Power Converter Test** menu bar selection.

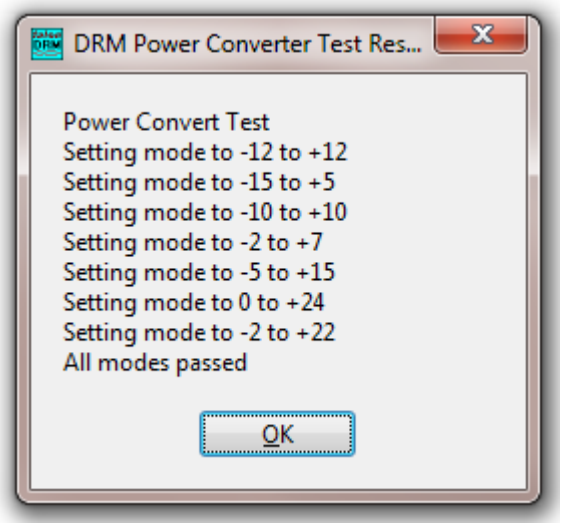


Figure 5-88: Power Converter Test Results Panel

The power converter test saves the current power converter setting and performs a test on all the power converter modes. The power converter test verifies that the positive and negative rails are within 3% of nominal. The min/max thresholds for each mode are listed in the following table:

Table 5-107: Power Converter Test Thresholds

Power Converter Mode	V+ Min	V+ Max	V- Min	V- Max
-12 to +12	15.520	16.480	-16.068	-15.132
-15 to +5	9.312	9.888	-19.776	-18.624
-10 to +10	15.520	16.480	-14.523	-13.677
-2 to +7	11.640	12.360	-9.888	-9.312
-5 to +15	18.624	19.776	-9.888	-9.312
0 to +24	27.936	29.664	-4.635	-4.365
-2 to +22	25.608	27.192	-6.180	-5.820

The relevant VXIplug&play API functions are:

- tat964_setPowerConverter
- tat964_setPowerConverterState
- tat964_queryAdcAverage

Calibration Panel

The calibration function is accessed from the **Instrument >Calibrate** menu bar selection. Reference Chapter 6 Programmable Channel Calibration for field calibration procedure.

Calibration data is stored on the Driver/Receiver board in non-volatile memory.

The calibration procedure requires that the Driver/Receiver boards be reset in order to load the current calibration data. Any unsaved calibration data will be lost.

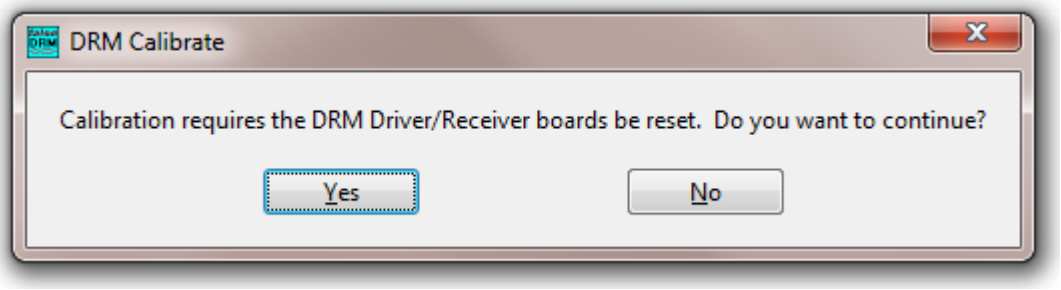


Figure 5-89: Calibration Confirmation Panel

Selecting **Yes** displays the main calibration panel. If the installed Driver/Receiver board requires calibration, the **Calibrate Function** control will list the available calibration items. Not all Driver/Receiver boards require calibration.

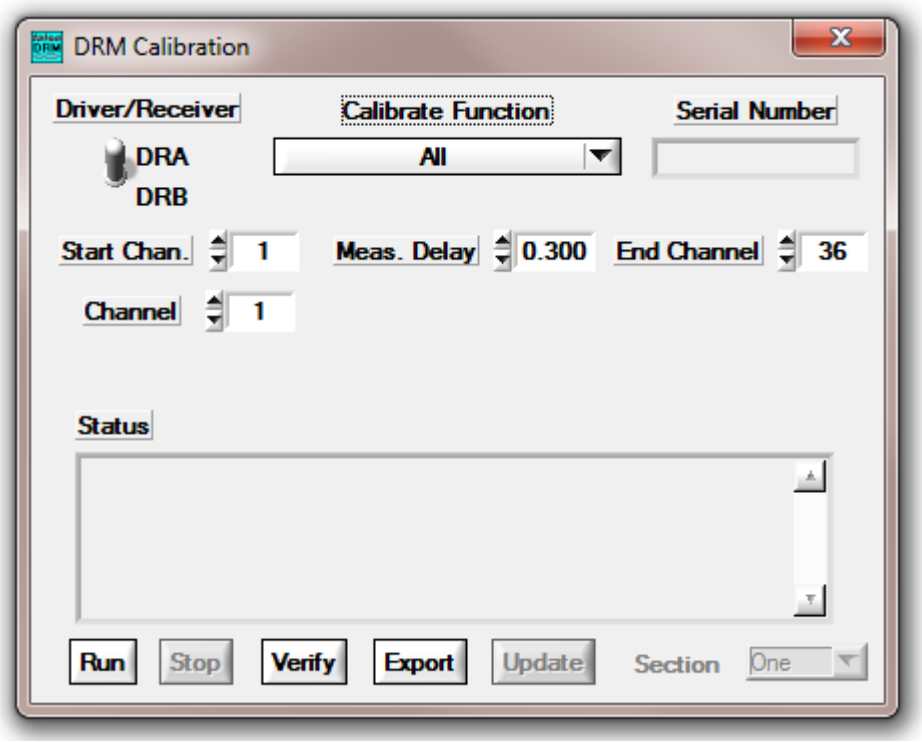


Figure 5-90: Calibration Panel

Driver/Receiver

This control selects which Driver/Receiver board to calibrate.

Calibrate Function

This pull-down control selects the calibrate function.

The selections for this pull-down control are:

Table 5-108: Calibrate Function Settings

Setting	Description
All	Selects the following calibrations: • Monitor + ADC • DVH/DVL • CVH/CVL • Vcom High/Low • Isource/Isink • IAL/IAH
Monitor + ADC	Selects the monitor and ADC calibration.
All DAC Levels	Selects the following calibrations: • DVH/DVL • CVH/CVL • Vcom High/Low
DVH/DVL	Selects the drive high and low level calibration.
CVH/CVL	Selects the compare high and low level calibration.
Vcom High/Low	Selects the commutating high and low level calibration.
ISource/ISink	Selects the source and sink current calibration.
IAL/IAH	Selects the current alarm high and low level calibration.
ADC Reference	Selects the ADC reference voltage calibration.
Source/Sink Load	Selects the source/sink load resistance calibration.
Delete Calibration	Used to delete section two data.

Serial Number

This control displays the Driver/Receiver board serial number.

Start Chan.

This numeric control sets the first channel to be calibrated. The valid range is from 1 (CH1) to 36 (AUX4). This setting is used for testing and should always be set to 1.

Meas. Delay

This numeric control sets the delay (in seconds) between changing a channel level and measuring the channel voltage. The valid range is from 0.010 to 36. This setting is used for testing and should always be set to 0.100.

End Channel

This numeric control sets the number of channels to be calibrated, starting with the **Start Chan.** setting. The valid range is from 1 to 36. This setting is used for testing and should always be set to 36.

Run

This command button executes the selected calibrate function.

The SFP will prompt the operator to confirm the action and then apply power to the Driver/Receiver board.

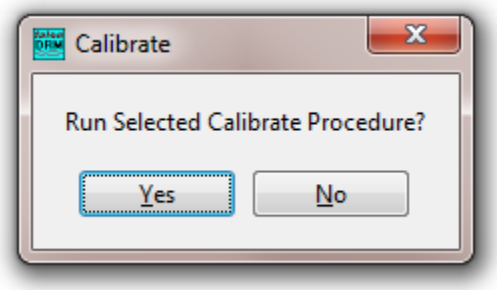


Figure 5-91: Confirm Calibrate Panel

Note *Pin electronic calibration data is stored for each voltage mode (-15 V to +17 V and -7 V to 24 V). Calibration should be performed with the power converter setting that will be used for testing for each voltage mode.*

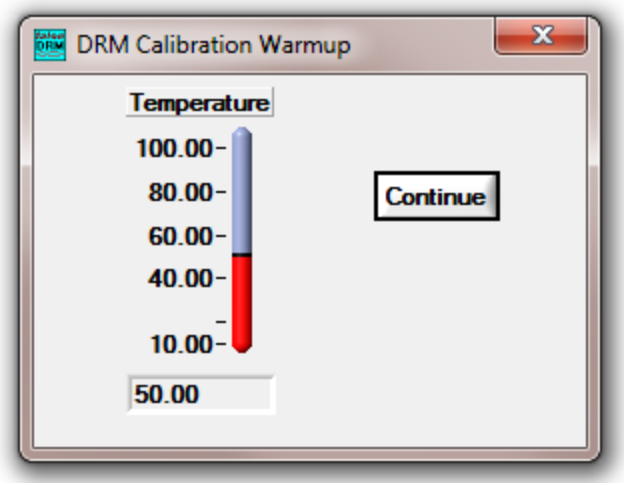


Figure 5-92: Calibrate Warm-up Panel

The selected calibration procedures will begin when the temperature reaches 80º C or the **Continue** command button is pressed. The unit should be calibrated at its normal application temperature. Refer to the **Calibration Temperature** section in **Chapter 6** for more information.

Once calibration has begun, progress data is displayed in the **Status** control.

The calibration run procedure creates a file “calData_<SN>.txt” and writes

calibration data analyses data. This file can be used to validate calibration results.

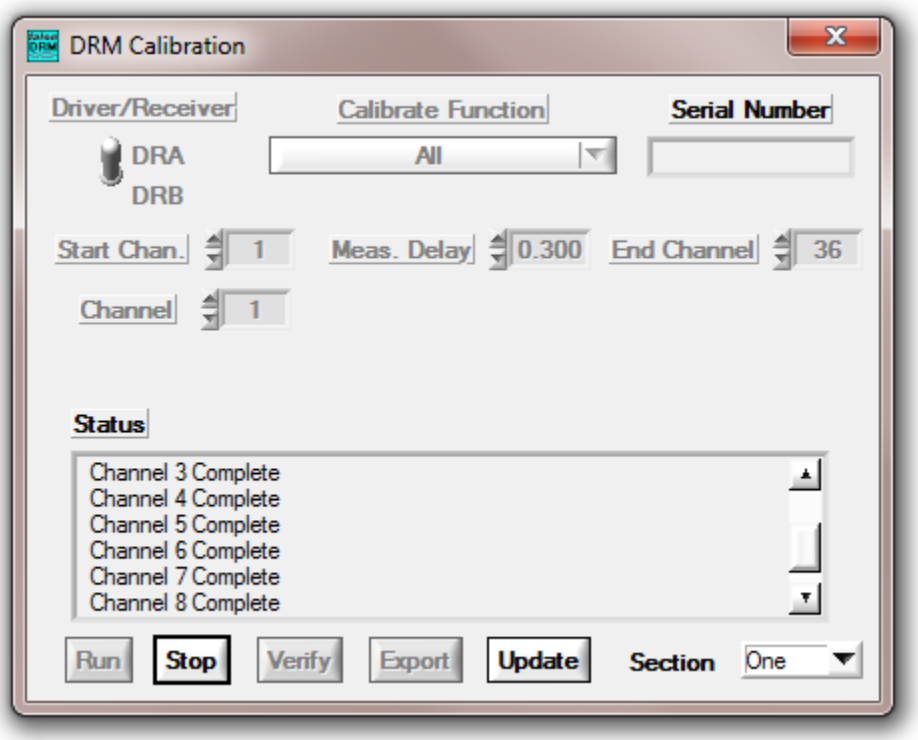


Figure 5-93: Calibrate Run Panel

The relevant VXI*plug&play* API functions are:

- tat964_calibrateChannel
- tat964_setRefOutput
- tat964_setRefVoltage
- tat964_setForceConnect
- tat964_setForceLoad
- tat964_setRefLoad

Verify

This command button executes the selected calibrate function verify routine.

The SFP will prompt the operator to confirm the action and then apply power to the Driver/Receiver board.

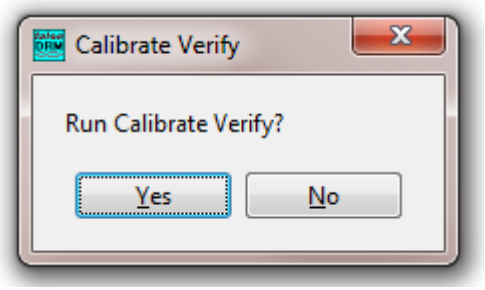


Figure 5-94: Confirm Verify Panel

The operator will be prompted to select the directory where the verification report will be created and saved.

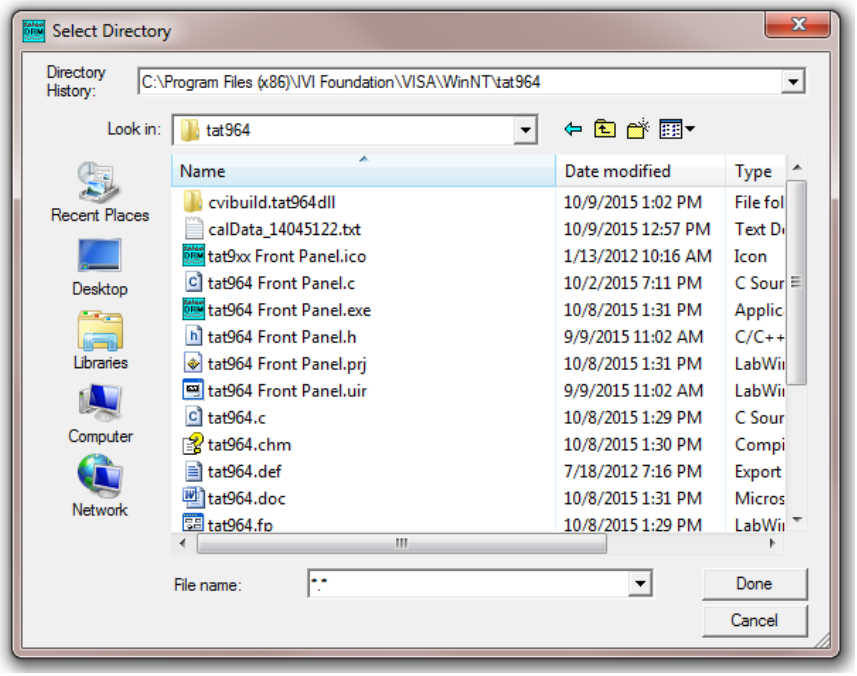


Figure 5-95: Verify Select Directory Panel

Note *Pin electronic calibration data is stored for each voltage mode (-15 V to +17 V and -7 V to 24 V). Verification should be performed with the power converter setting that was used for calibration for each voltage mode.*

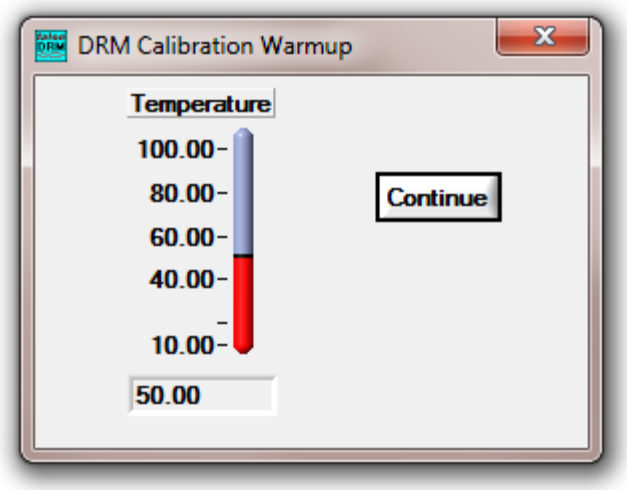


Figure 5-96: Verify Warm-up Panel

Verification will begin when the temperature reaches 80º C or the **Continue** command button is pressed. The unit should be verified at its normal application temperature. Refer to the **Calibration Temperature** section in **Chapter 6** for more information. Once verification has begun, progress data is displayed in the **Status** control.

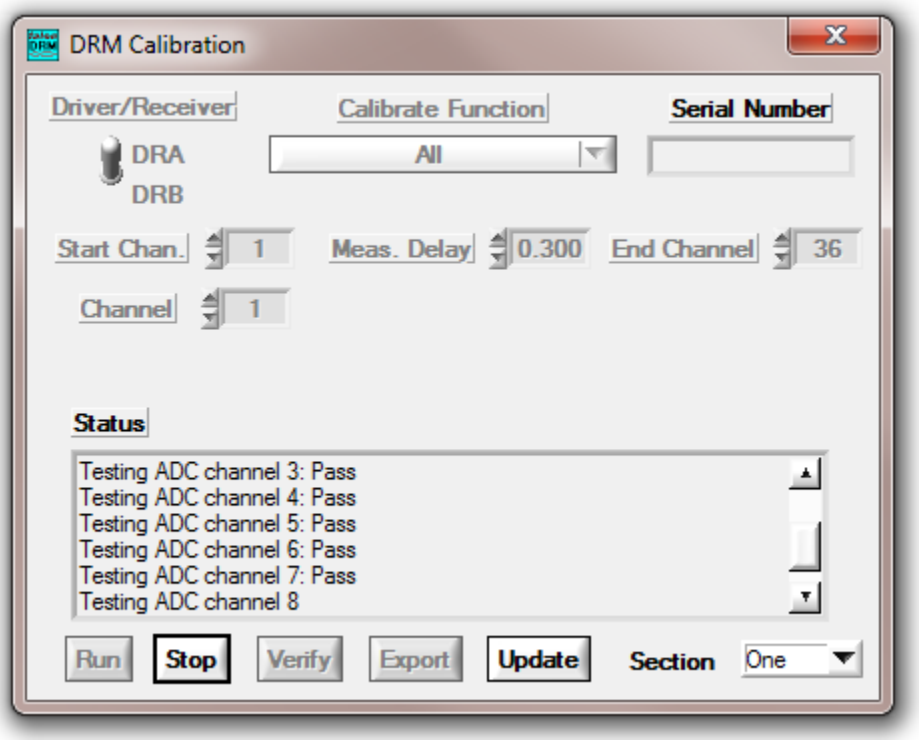


Figure 5-97: Verify Run Panel

The relevant VXI*plug&play* API functions are:

- tat964_verifyChannelCalibration

Export

This command button saves the current calibration data to a comma separated file with a format that can be loaded using the **File > Load DRA/DRB Calibration** menu command.

The relevant VXI*plug&play* API functions are:

- tat964_saveCalibrationFile

Stop

This command button stops a calibration or verification run.

Update

This command button writes the new calibration data to non-volatile memory.

The relevant VXI*plug&play* API function is:

- tat964_updateCalibrationData

Monitor Temperature Panel

This panel shows the temperature of the following components within the DRM:

- Digital Board Sequencer FPGAs
- DR3e, DR9 and UR14 variable voltage pin electronics.

Trip Temperature

This control programs a trip point that will disconnect the power pins from the variable voltage pin electronics and open the connect relays if the specified temperature is exceeded. A Driver/Receiver temperature alert event is also generated.

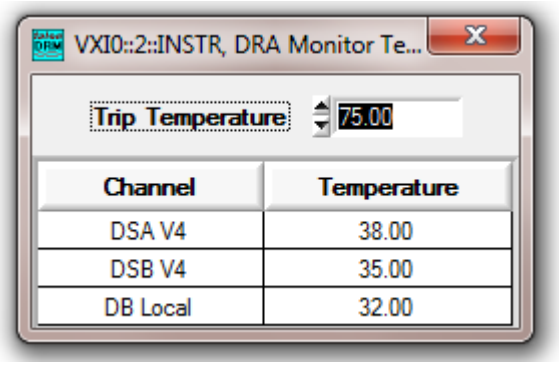
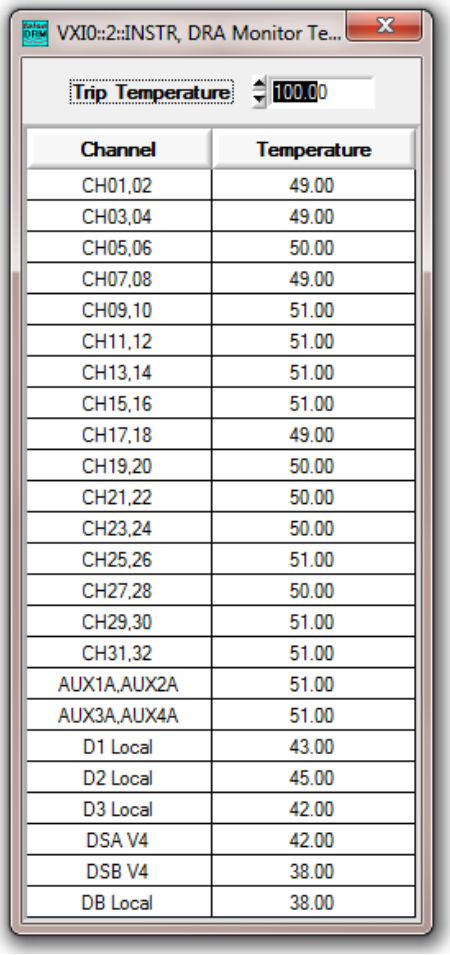
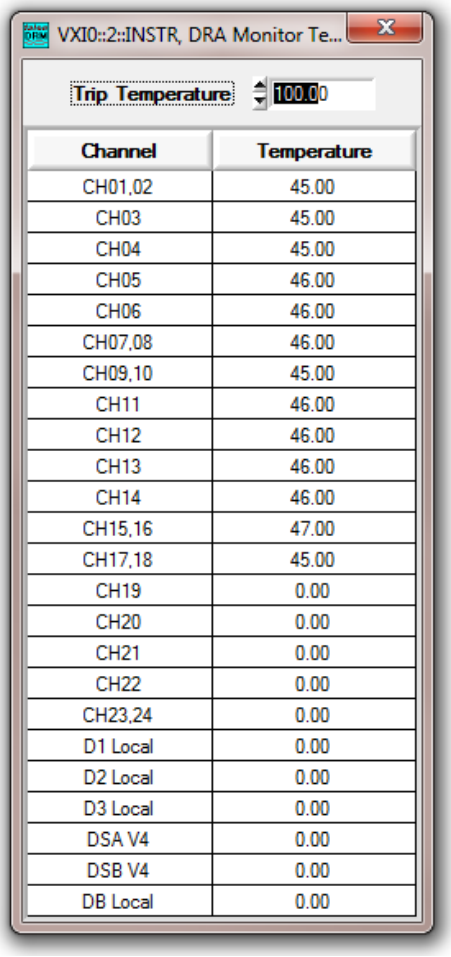


Figure 5-98: DB Monitor Temperature Panel



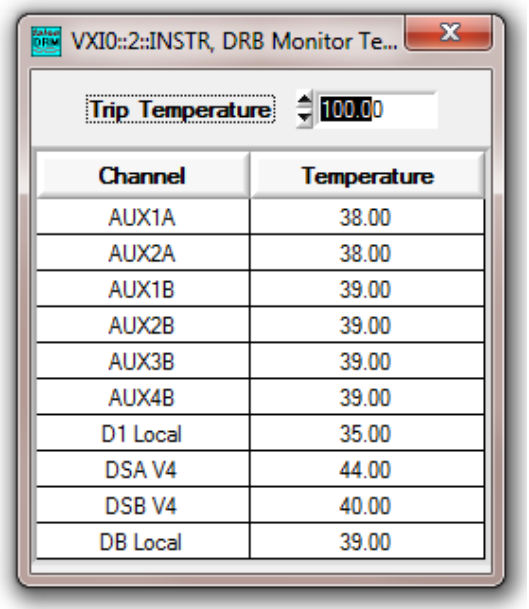
Channel	Temperature
CH01,02	49.00
CH03,04	49.00
CH05,06	50.00
CH07,08	49.00
CH09,10	51.00
CH11,12	51.00
CH13,14	51.00
CH15,16	51.00
CH17,18	49.00
CH19,20	50.00
CH21,22	50.00
CH23,24	50.00
CH25,26	51.00
CH27,28	50.00
CH29,30	51.00
CH31,32	51.00
AUX1A,AUX2A	51.00
AUX3A,AUX4A	51.00
D1 Local	43.00
D2 Local	45.00
D3 Local	42.00
DSA V4	42.00
DSB V4	38.00
DB Local	38.00

Figure 5-99: DR3e Monitor Temperature Panel



Channel	Temperature
CH01,02	45.00
CH03	45.00
CH04	45.00
CH05	46.00
CH06	46.00
CH07,08	46.00
CH09,10	45.00
CH11	46.00
CH12	46.00
CH13	46.00
CH14	46.00
CH15,16	47.00
CH17,18	45.00
CH19	0.00
CH20	0.00
CH21	0.00
CH22	0.00
CH23,24	0.00
D1 Local	0.00
D2 Local	0.00
D3 Local	0.00
DSA V4	0.00
DSB V4	0.00
DB Local	0.00

Figure 5-100: DR9 Monitor Temperature Panel



Channel	Temperature
AUX1A	38.00
AUX2A	38.00
AUX1B	39.00
AUX2B	39.00
AUX3B	39.00
AUX4B	39.00
D1 Local	35.00
DSA V4	44.00
DSB V4	40.00
DB Local	39.00

Figure 5-101: UR14 Monitor Temperature Panel

The relevant VXI*plug&play* API functions are:

- tat964_queryTemperature
- tat964_setTemperatureAlarm

Voltage Monitor Panel

This panel is available with the following Driver/Receiver boards:

- DR3e
- DR9
- UR14
- DR4

DR3E, DR9 and UR14 Voltage Monitor Panel and Controls

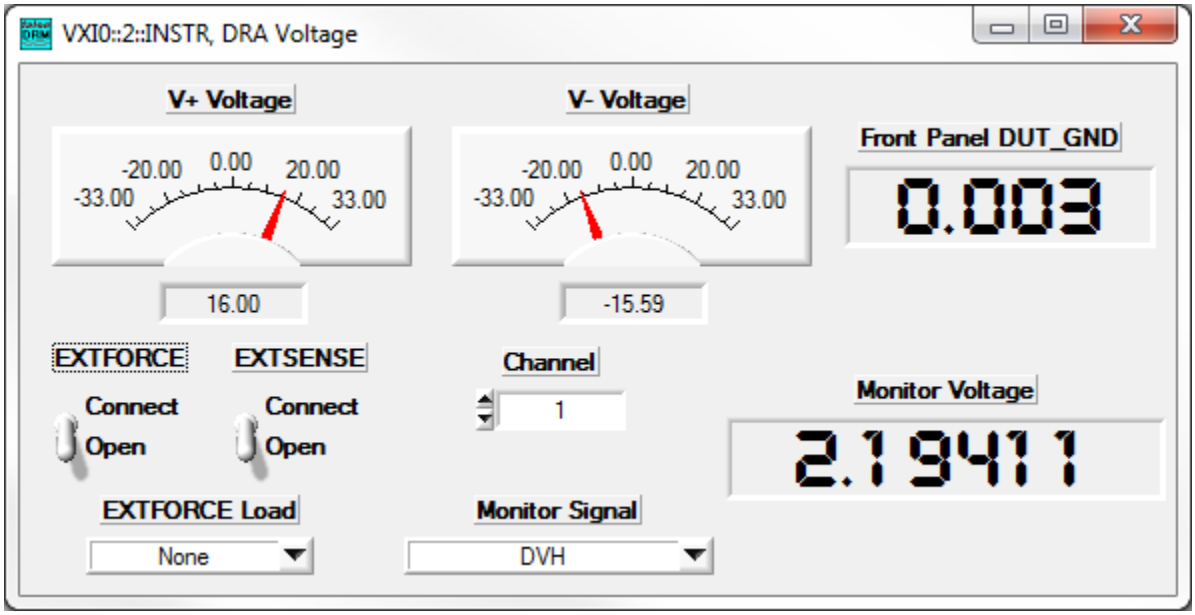


Figure 5-102: DR3E, DR9 and UR14 Voltage Monitoring Panel

V+ Voltage

This control displays the fused V+ bias voltage.

The relevant VXI*plug&play* API functions are:

- tat964_queryAdc
- tat964_queryAdcAverage

V- Voltage

This control displays the fused V- bias voltage.

The relevant VXI*plug&play* API functions are:

- tat964_queryAdc
- tat964_queryAdcAverage

Front Panel DUT_GND

This control displays the DUT_GND voltage. The V+/V- power relay must be closed to activate measurement.

The relevant VXI*plug&play* API functions are:

- tat964_queryAdc
- tat964_queryAdcAverage

EXTFORCE

This control is used to connect or open the EXTFORCE signal to the specified channel.

The relevant VXI*plug&play* API function is:

- tat964_setForceConnect

EXTSENSE

This control is used to connect or open the EXTSENSE signal to the specified channel.

The relevant VXI*plug&play* API function is:

- tat964_setSenseConnect

Channel

This control is used to specify the channel for the **EXTFORCE**, **EXTSENSE** and **Monitor Signal** controls.

The relevant VXI*plug&play* API function is:

- tat964_setMonitorSignal

Monitor Signal

This control is used to specify the channel and signal that will be connected to the monitor output.

The relevant VXI*plug&play* API function is:

- tat964_setMonitorSignal

Monitor Voltage

This control displays the selected monitor signal voltage.

The relevant VXI*plug&play* API functions are:

- tat964_queryAdc
- tat964_queryAdcAverage

DR4 Voltage Monitor Panel and Controls

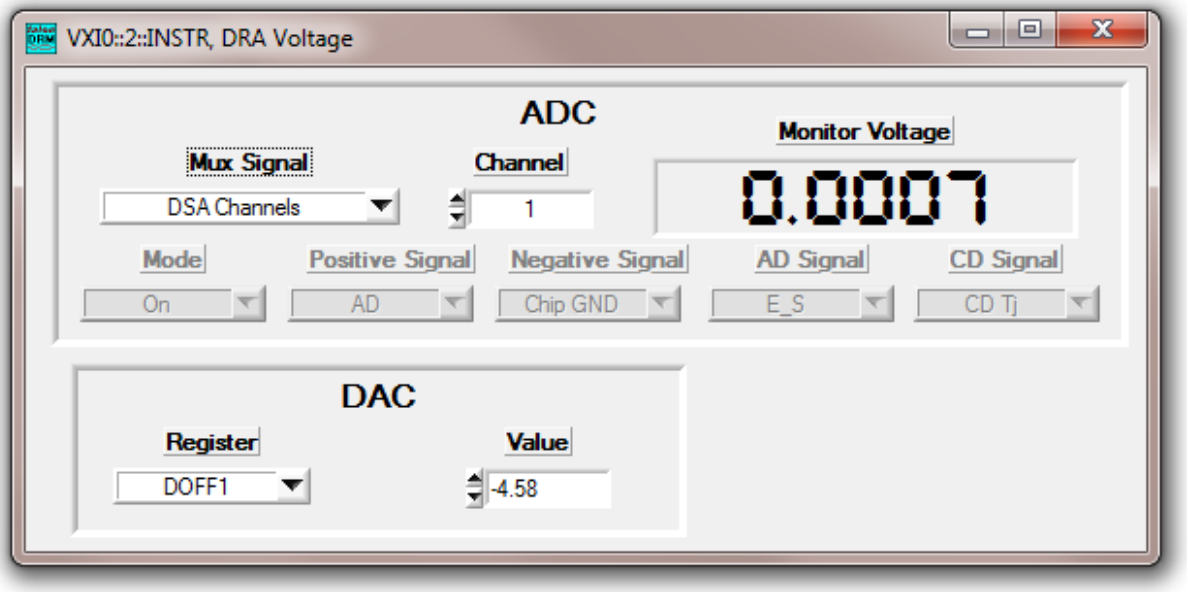


Figure 5-103: DR4 Voltage Monitoring Panel

Mux Signal

This control is used to program the mux tree to select the signal routed to the ADC. The signal selection includes any of the channels as well as test/debug signals for factory use.

The relevant VXI*plug&play* API functions are:

- tat964_setAdcMuxSignal

Channel

This control selects the channel number when the **Mux Signal** is set **to DSA Channels** or **DSB Channels**.

The relevant VXI*plug&play* API functions are:

- tat964_setAdcMuxSignal

Monitor Voltage

This control displays the selected mux signal voltage.

The relevant VXI*plug&play* API functions are:

- tat964_queryAdc
- tat964_queryAdcAverage

Mode

This control sets the monitor signal mode when the **Mux Signal** is set to **Monitor A** or **Monitor B**.

The relevant VXI*plug&play* API functions are:

- tat964_setGroupMonitorSignal

Positive Signal

This control sets the positive monitor signal when the **Mux Signal** is set to **Monitor A** or **Monitor B**.

The relevant VXI*plug&play* API functions are:

- tat964_setGroupMonitorSignal

Negative Signal

This control sets the negative monitor signal when the **Mux Signal** is set to **Monitor A** or **Monitor B**.

The relevant VXI*plug&play* API functions are:

- tat964_setGroupMonitorSignal

AD Signal

This control sets the analog diagnostic signal when the **Mux Signal** is set to **Monitor A** or **Monitor B** and the **Positive Signal** is set to **AD**..

The relevant VXI*plug&play* API functions are:

- tat964_setGroupMonitorSignal

CD Signal or E_S Signal

This control selects the analog diagnostic signal when the **Mux Signal** is set to **Monitor A** or **Monitor B** and the **Positive Signal** is set to **AD** and the **AD Signal** is set to **Central Diag.** (CD Signal) or **E_S** (E_S Signal).

The relevant VXI*plug&play* API functions are:

- tat964_setGroupMonitorSignal

Register

This control is used to select one of the thirty two DAC registers to query for factory test.

The relevant VXI*plug&play* API function is:

Value

This control is used to display the selected DAC register value for factory test.

The relevant VXI*plug&play* API function is:

- NA

Chip Temperature Panel

This panel is available with the following Driver/Receiver boards:

- DR3e
- DR9
- UR14

The temperatures on this panel will usually be less than what's shown on the Monitor Temperature panel. The Monitor Temperature panel monitors the temperature near the output drivers which are usually hotter than the rest of the device.

However, this panel shows all of the Pin Electronics device temperatures at once in their relative positions on the Driver/Receiver board so one can see where the hot spots are.



Figure 5-104: DR3e Chip Temperature

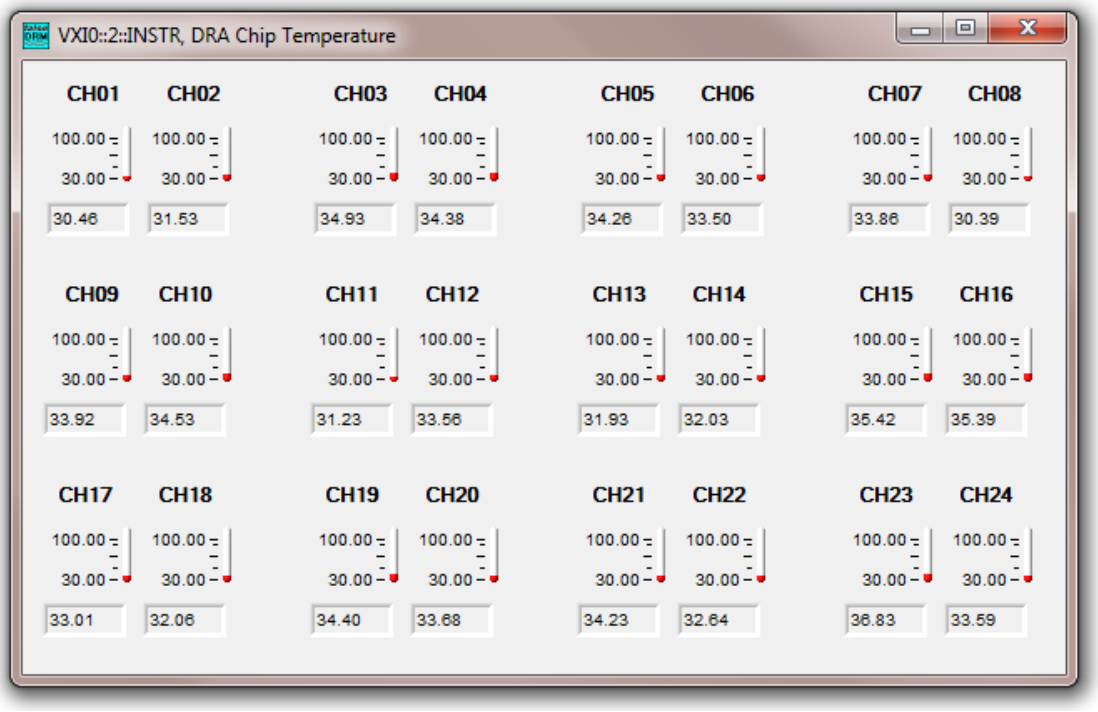


Figure 5-105: DR9 Chip Temperature

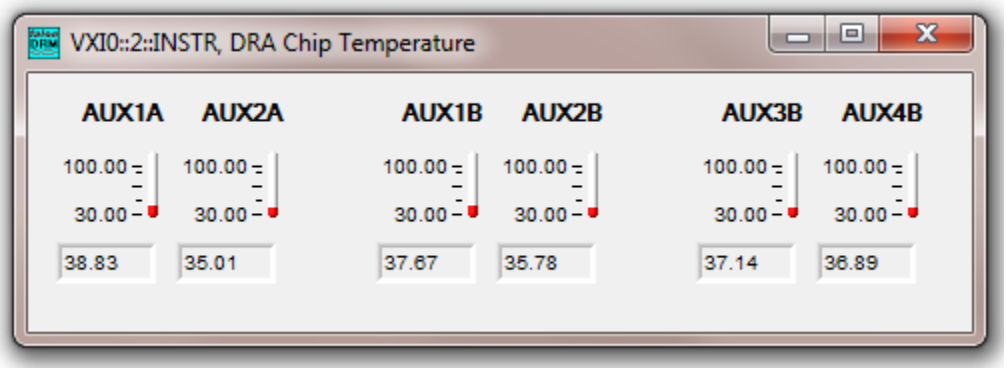


Figure 5-106: UR14 Chip Temperature

The relevant VXI*plug&play* API function is:

- tat964_queryChannelTemp

Utility Reference Monitor

This panel is available when a UR14 board is installed.

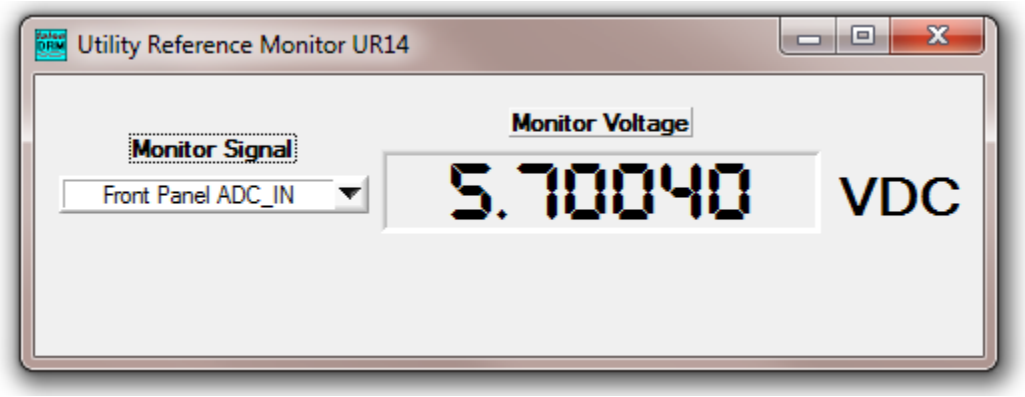


Figure 5-107: Utility Reference Monitor

Monitor Signal

This pull-down control selects the signal for the voltage monitor.

The selections for this pull-down control are:

Table 5-109: UR14 Monitor Signal Settings

Setting	Description
Front Panel ADC_IN	Selects the front panel ADC_IN signal.
VRef5	Selects the +5V reference signal.
Group 1 Compare	Selects the CH1-CH8 comparator level.
Group 2 Compare	Selects the CH9-CH16 comparator level.
Group 3 Compare	Selects the CH17-CH24 comparator level.
Group 4 Compare	Selects the CH25-CH32 comparator level.

The relevant VXI*plug&play* API functions are:

- tat964_queryAdc
- tat964_queryAdcAverage

SFP Close Message

This panel is used to close the soft front panel.

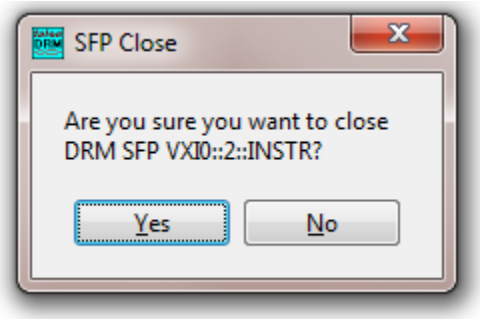


Figure 5-108: SFP Close Message

If “Yes” is selected, the following panel will be displayed:

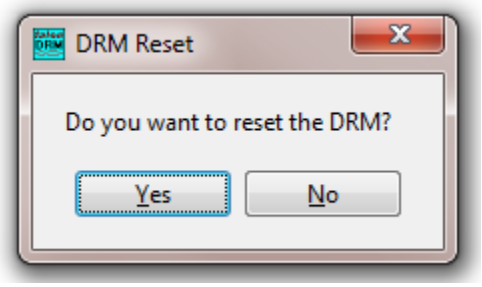


Figure 5-109: SFP Reset Message

The relevant VXI*plug&play* API functions are:

- tat964_close
- tat964_reset

Chapter 6
Programmable Channel Calibration

This chapter provides calibration and verification information for the family of T940 Digital Resource modules which have channels with programmable driver/receiver characteristics. The following table lists the calibration functions and the DRM types that require the calibration:

Table 6-1: Calibration Functions and DRM Requirement

Calibration Function	DRM Types
ADC Reference (via EXTERNAL FORCE port)	DR3E, DR9, UR14
Monitor + ADC	DR3E, DR9, UR14, DR4
Source/Sink Load (via EXTERNAL FORCE port)	DR3E, DR9, UR14
Drive High and Drive Low	DR3E, DR9, UR14, DR4
Compare High and Compare Low	DR3E, DR9, UR14, DR4
$V_{commutating}$ (V_{com}) High and Low	DR3E, DR9, UR14
Current Source and Sink	DR3E, DR9, UR14
Current Alarm High and Low	DR3E, DR9, UR14
Delete (Section two only)	DR3E, DR9, UR14, DR4



CAUTION

ALWAYS PERFORM DISASSEMBLY, REPAIR AND CLEANING AT A STATIC SAFE WORKSTATION.

Performance Verification

Do not attempt to calibrate the instrument before verifying first that the instrument is in working order. A complete set of specifications is listed in the Appendices. If the instrument fails to perform within the specified limits, the instrument must be tested to find the source of the problem.

If there is a reasonable suspicion that an electrical problem exists within the T940 DRM, perform a complete self-test on the instrument prior to running a verification or calibration procedure.

Environmental Conditions

The T940 can operate over an ambient temperature range of 0°C to 45°C. Adjustments should be performed under laboratory conditions having an ambient temperature of 25°C, ±5°C and at relative humidity of less than 80%. Turn on the power to the T940 and allow it to warm up to the desired operating temperature before beginning the adjustment procedure. If the instrument has been subjected to conditions outside these ranges, allow additional time for the instrument to stabilize before beginning the calibration procedure.

Voltage Mode

For the DR3E, DR9 and UR14, there are two voltage mode settings available -15 to +17 and -7 to +24). Each voltage mode requires calibration and the data for both is stored in non-volatile memory. Be sure to select the Voltage Range mode which is required by the application prior to calibration.

V+ and V- Requirements

For the DR3E, DR9 and UR14, the V+ and V- bias voltage level requirements for calibration are listed below.

- V+ must be >= +14 V
- V- must be <= -9 V

The table below lists the recommended power converter settings for calibration for each voltage mode.

Table 6-2: Recommended Power Converter Settings

Voltage Mode	Type 1 or Type 3	Type 4
-15V to +17V	-12 to +12	-5 to +15
-7V to +24V	-10 to +9	-7 to +7

Warm-up Period

Most equipment is subject to a small amount of drift when it is first turned on. To ensure accuracy, turn on the power to the T940 module and allow it to warm-up to the desired operating temperature before beginning the calibration procedure.

Recommended Test Equipment

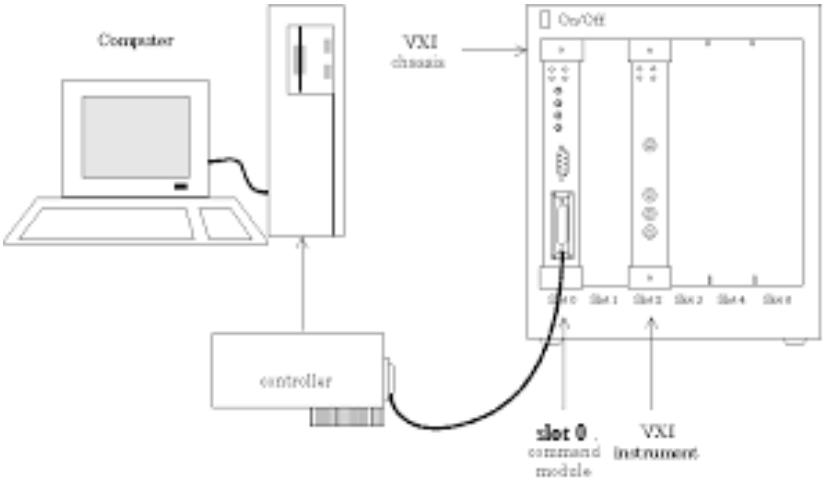
For the DR3E, DR9, and UR14, the recommended equipment for adjustments is listed in Table 6-1. Test instruments other than those listed may be used only if their specifications equal or exceed the required characteristics. Also listed below are accessories required for calibration.

Table 6-3: Recommended Calibration Equipment

Equipment	Model No.	Manufacturer
Digital Multimeter	34401 or equivalent	Keysight
J9A/J9B funnel cal fixture (DR9, UR14)	408626	Astronics Test Systems
J9A/J9B pigtail cal fixture (DR9, UR14)	408626-001	Astronics Test Systems
IDC-50 calibration adapter (DR3e CIB)	409531-050	Astronics Test Systems

Basic Setup

The T940 DRM should be installed in a High Power VXI 4.0 compliant mainframe. A compatible VXI slot 0 controller shall be installed and used to control software execution. At its most basic level, calibration is entirely internal and doesn't require any external instruments unless the references and monitor paths are being re-calibrated. An example configuration is shown in the diagram.



Calibration Interval

The T940 DRM should be calibrated at a regular time interval determined by the accuracy requirements of your application. A one-year interval is adequate for most applications. Accuracy specifications are valid only when calibration is performed at regular time intervals. Accuracy specifications presented herein are not valid beyond the one-year calibration interval. Astronics Test Systems does not recommend extending calibration intervals beyond three years.

Calibration Temperature

The T940 DRM should be calibrated at the nominal temperature of your application. Application temperature can depend on the module type and VXI mainframe characteristics, as well as the exact usage of the features of the module. Using more channels simultaneously at higher selected slew rates, for

example, can create a higher operating temperature. For best accuracy, run the Soft Front Panel during a typical test execution and monitor the programmable channel temperatures on DRB (if installed, otherwise on DRA). The module should settle on a temperature if the test is long enough to establish equilibrium. The highest of these temperatures should be used as the calibration temperature for best accuracy in similar applications.

Calibration Procedures

Use the following procedures to calibrate the T940 Digital Resource module. Calibration is done with the covers closed and the T940 module installed in a VXI chassis. The calibration procedure requires that the T940 Soft Front Panel utility program be installed and interfaced to the instrument. The VISA library is required.

Calibration is performed from the Calibration Panel in the T940 Soft Front Panel. To invoke this panel, access the Calibrate menu item from the Instrument menu as shown in Figure 6-1.

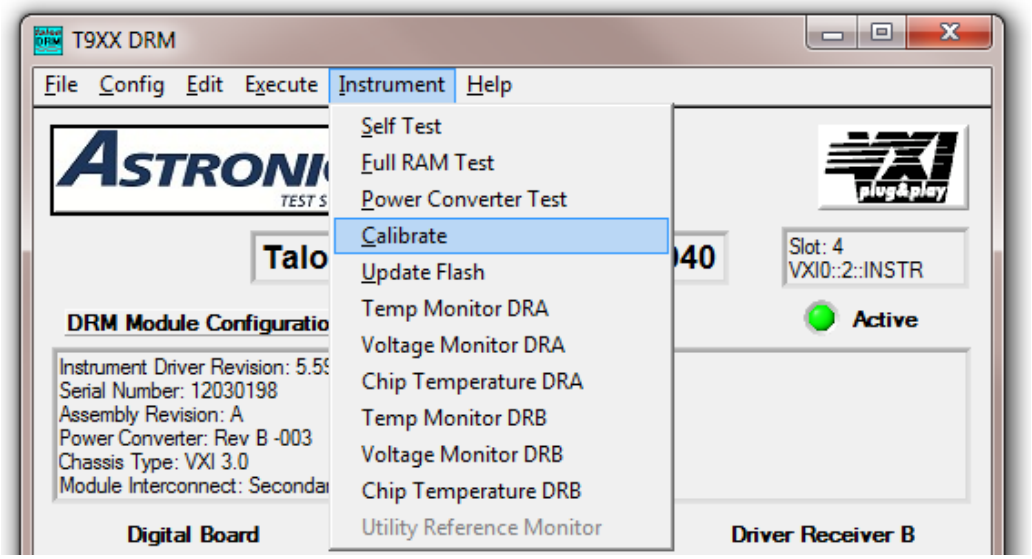


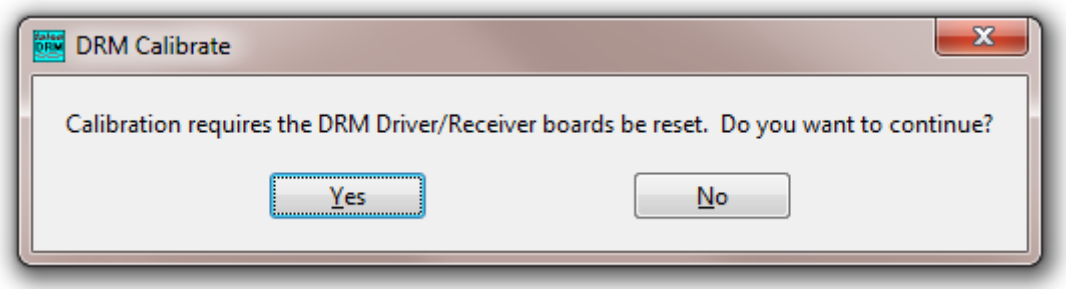
Figure 6-1: Invoke the Calibrate DRM Panel from the SFP

In addition, be sure to select the Voltage Range mode which is required by the application as there are 7 ranges to choose from and two voltage modes. Calibrating in a Voltage Mode range that is different from the range used in the application can cause a reduction in measurement accuracy.

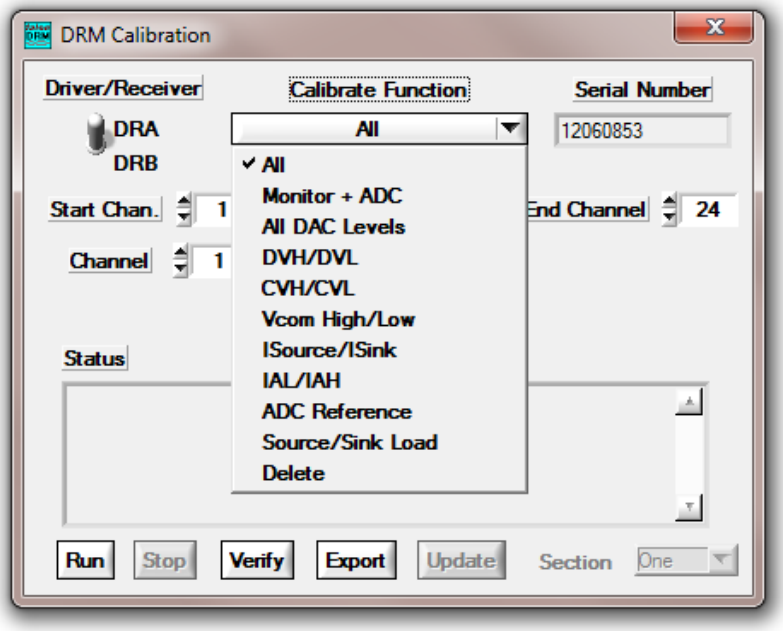
Note: Calibration procedures must be performed in the order shown below. Changing the order of calibration from that which is shown in the procedure can invalidate the results.

The Calibrate panel, before opening, will inform the user that calibration mode requires the instrument to be automatically reset to its power-on defaults. If the instrument settings need to be saved prior to calibration, or if the instrument is

running a critical test, now is the time to exit. Select “Yes” if it is OK to continue, or “No” if DRM calibration mode should be exited.



Access the Calibrate Function to be performed using the Calibrate Function drop-down list. From this list, select the function on the T940 DRM to be calibrated. The sections to follow describe the individual procedures in detail.



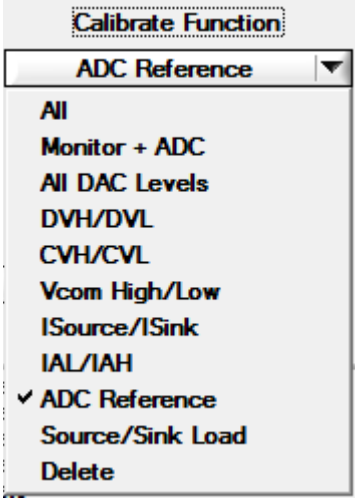
ADC Reference (via EXTERNAL FORCE)

For DR3E, DR9 and UR14 only, the **ADC Reference** calibration is used to measure the reference voltages used to calibrate the **ADC + Monitor** path. Connect the DC calibrator to the EXTERNAL FORCE input on either DRA or DRB (if installed). The Export button can be used to save the calibration factors into a text file for examination and later restore, e.g., File | Load DRA Calibration.

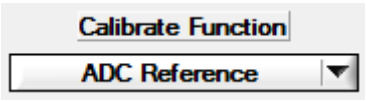
Select Calibrate Function

Equipment: Basic Setup Procedure:

1. Place a check mark next the ADC Reference menu item on the Calibrate Function menu.



2. Verify that the ADC Reference calibrate function is now in focus.



Select Measurement Delay

Equipment: Basic Setup Procedure:

1. Select DRA or DRB (if installed) using the Driver/Receiver switch.
2. The default measurement delay is 200 ms. Increase this value to give the calibration points more time to settle.

Run Calibration

Equipment: Digital multimeter connected to DRA or DRB (if installed) via the EXTERNAL FORCE input.

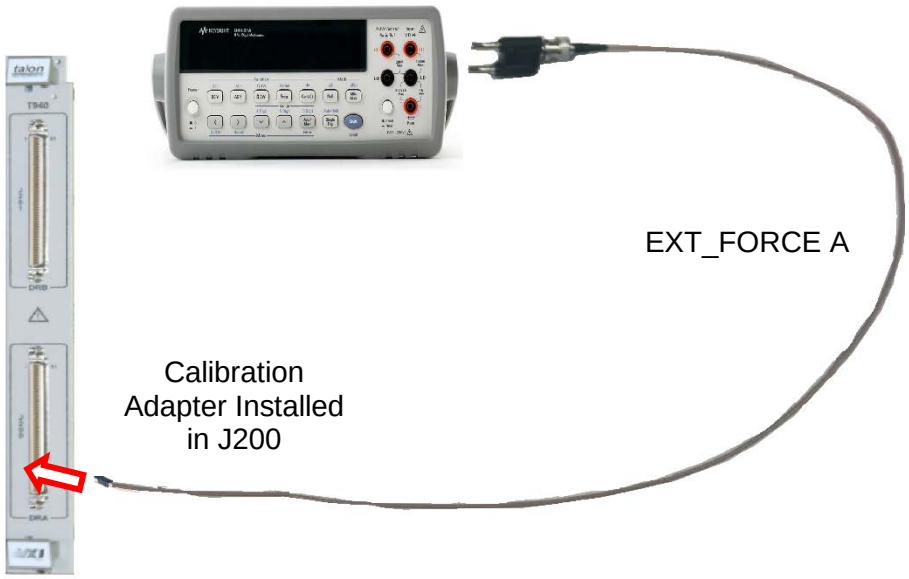


Figure 6-2: T940-DR3e-DR3e Connection Diagram

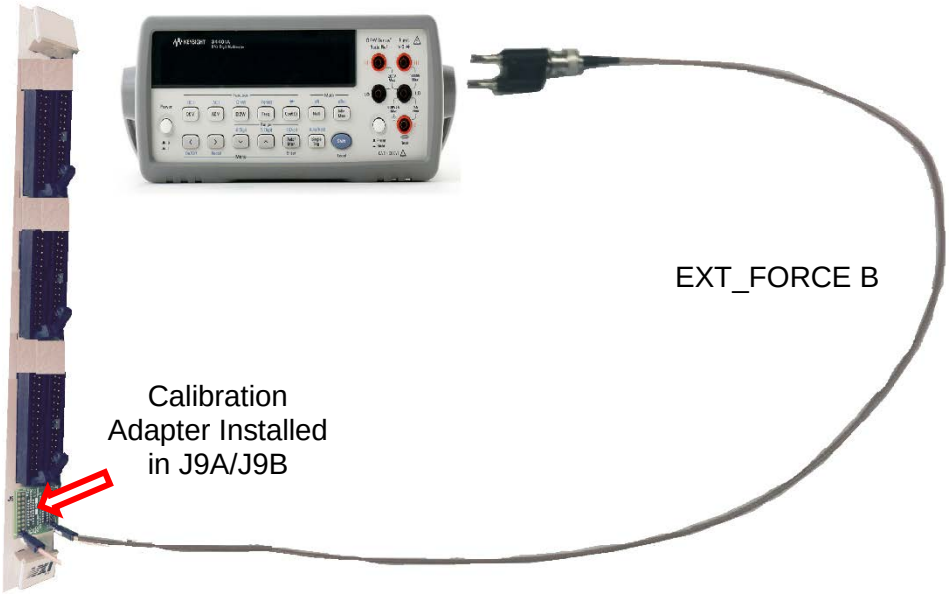
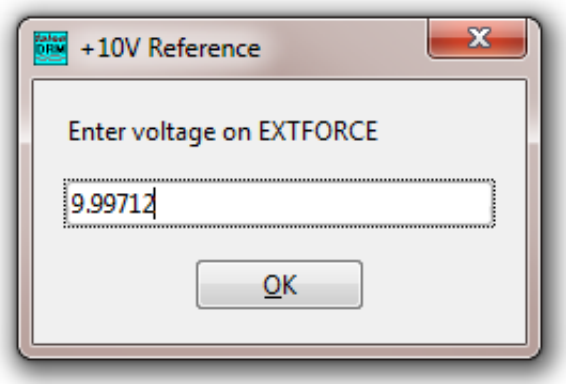


Figure 6-3: T940-DR9-DR9 or T940-UR14 Connection Diagram

Procedure:

1. Select the ADC reference to be calibrated.
2. Connect the DC Calibrator using the calibration adapter cable.
3. Press the Run button.

4. Read the value of the selected ADC reference voltage (+5V, -5V, +10 V or -10 V) from the DMM and enter it into the software.
5. Review the results in the Status window.



6. (Optional) Check the measured voltage in the Value field for each reference.
7. (Optional) Save the calibration to a file for later restore, e.g., File | Load DRA Calibration.
8. (Optional) Update the module to the new calibration factors just obtained using the Update button. If this step is omitted, the calibration factors will revert at the next power cycle.



Monitor + ADC

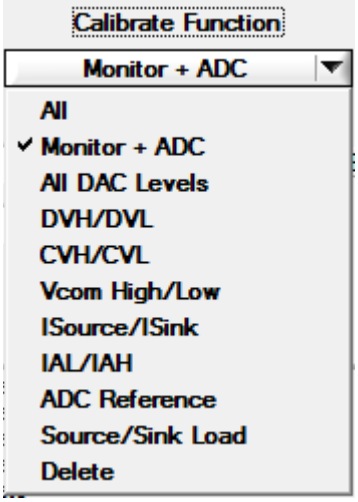
The **Monitor + ADC** calibration calculates the offset and gain of the monitor to ADC path for each channel. The Verify button is available for use both before and after calibration. It is recommended that the calibration be verified before the Update button is used to store the current Monitor + ADC calibration factors. The Export button can be used to save the calibration factors into a text file for examination and later restore, e.g., File | Load DRA Calibration.

Select Calibrate Function

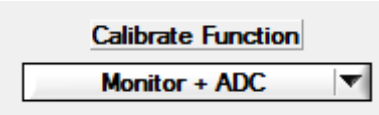
Equipment: Basic Setup

Procedure:

1. Place a check mark next the Monitor + ADC menu item on the Calibrate Function menu.



2. Verify that the Monitor + ADC calibrate function is now in focus.



Select Start and End Channels and Measurement Delay

Equipment: Basic Setup

Procedure:

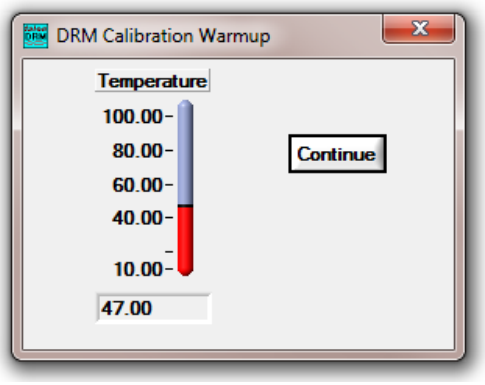
1. Select DRA or DRB (if installed) using the Driver/Receiver switch.
2. Use the Start and End Channel fields to select the I/O and Auxiliary channels to be calibrated.
3. The minimum measurement delay for this calibration is 200 ms. Increase this value to give the calibration points more time to settle.

DRM Calibration Warmup

Equipment: Basic Setup

Procedure:

1. Allow the T940 DRM to warm to its nominal application temperature.
2. Hit the Continue button when the required temperature is reached. If the temperature reaches 80°C, the process continues automatically.

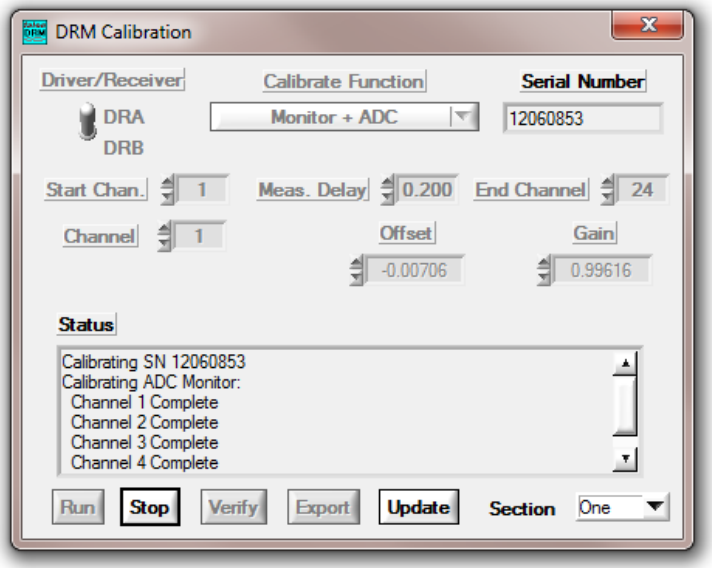


Run Calibration

Equipment: Basic Setup

Procedure:

1. Press the Run button. Use the Stop button at any time to abort execution.
2. Review the results in the Status window.
3. (Optional) Verify the results using the Verify button. Ensure that all channels pass verification.
4. (Optional) Check the individual gain and offset values in the field controls. Verify that all offsets are near zero and that all gains are near unity (1).
5. (Optional) Save the calibration to a file for later restore, e.g., File | Load DRA Calibration.
6. (Optional) Update the module to the new calibration factors just obtained using the Update button. If this step is omitted, the calibration factors will revert at the next power cycle.



Source/Sink Load

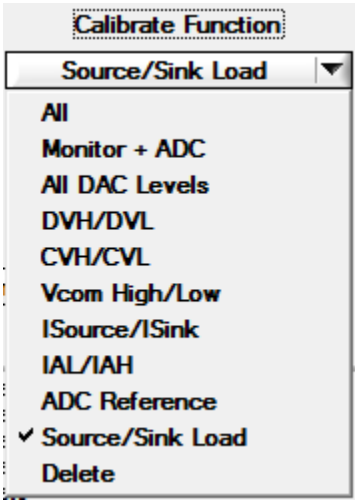
For DR3E, DR9 and UR14 only, the **Source/Sink Load** calibration is used to measure the reference resistor used to calibrate the **Isource/Isink** and **IAL/IAH** levels. The Export button can be used to save the calibration factors into a text file for examination and later restore, e.g., File | Load DRA Calibration.

Select Calibrate Function

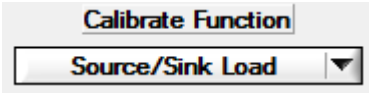
Equipment: Basic Setup

Procedure:

1. Place a check mark next the Source/Sink Load menu item on the Calibrate Function menu.



2. Verify that the Source/Sink Load calibrate function is now in focus.



Run Calibration

Equipment: Digital multimeter connected to DRA or DRB (if installed) via the EXTERNAL FORCE input.

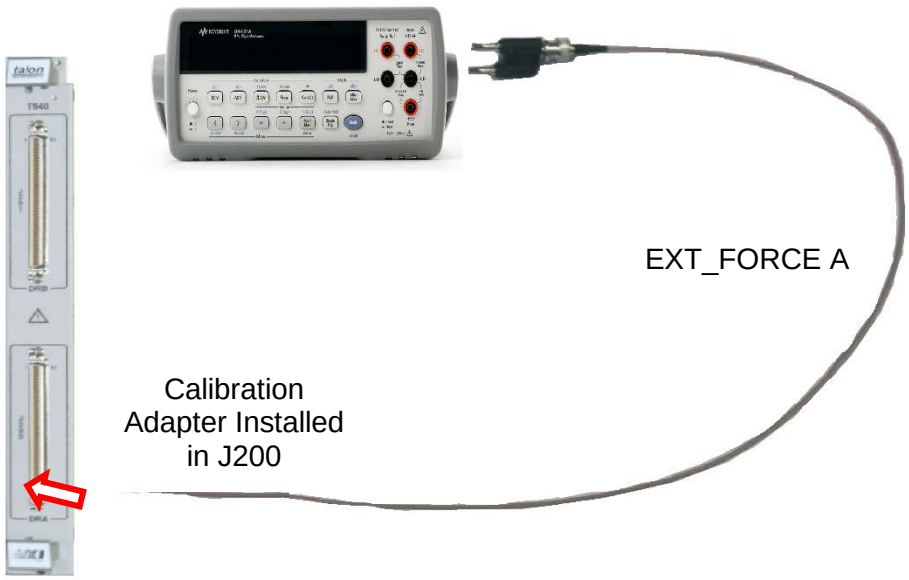


Figure 6-4: T940-DR3e-DR3e Connection Diagram

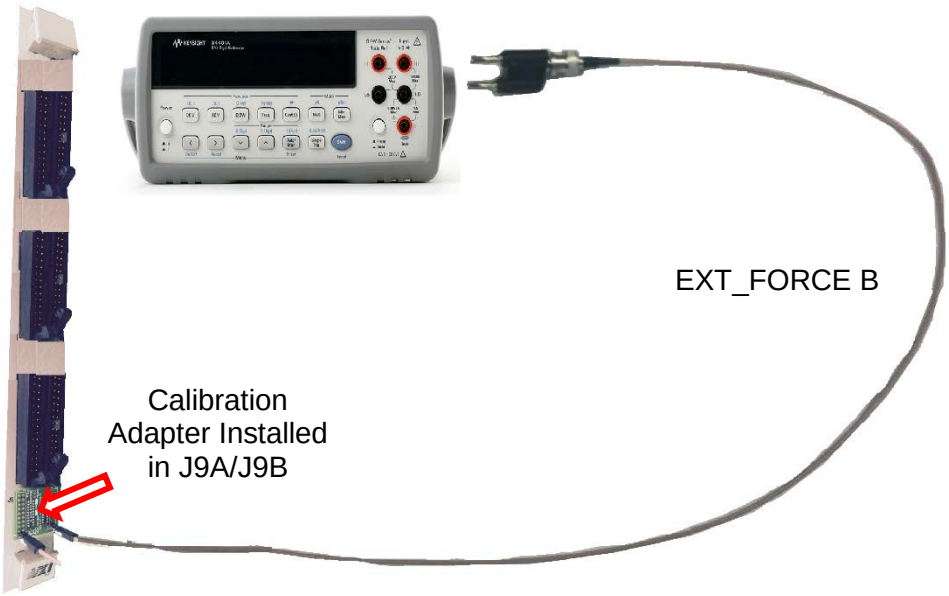
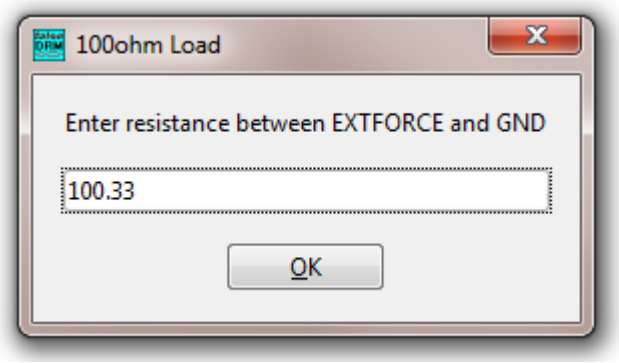


Figure 6-5: T940-DR9-DR9 or T940-UR14 Connection Diagram

Procedure:

1. Press the Run button.
2. Allow the T940 DRM to warm to its nominal application temperature.
3. Enter the resistance readings taken by the DMM.



4. (Optional) Export the calibration to a file for later restore, e.g., File | Load DRA Calibration.
5. (Optional) Update the module to the new calibration factors just obtained using the Update button. If this step is omitted, the calibration factors will revert at the next power cycle.

DVH/DVL

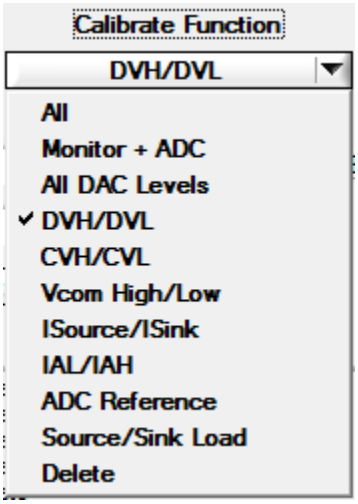
The **DVH/DVL** calibration calculates the offset and gain of the output driver levels. For the DR3E, DR9 and UR14 a separate offset and gain is calculated for each slew rate. For the DR4 a separate offset and gain is calculated for each group offset. The Verify button is available for use both before and after calibration. It is recommended that the calibration be verified before the Update button is used to store the current drive high and drive low calibration factors. The Export button can be used to save the calibration factors into a text file for examination and later restore, e.g., File | Load DRA Calibration.

Select Calibrate Function

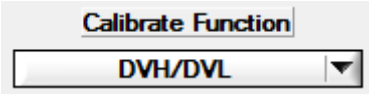
Equipment: Basic Setup

Procedure:

1. Place a check mark next the DVH/DVL menu item on the Calibrate Function menu.



2. Verify that the DVH/DVL calibrate function is now in focus.



Select Start and End Channels and Measurement Delay

Equipment: Basic Setup

Procedure:

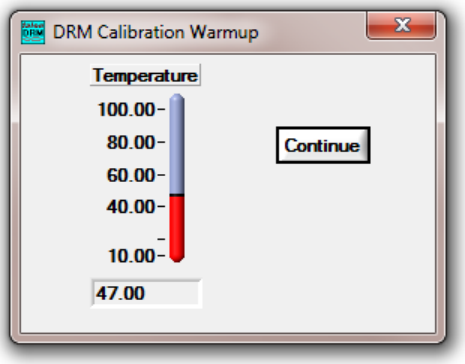
1. Select DRA or DRB (if installed) using the Driver/Receiver switch.
2. Use the Start and End Channel fields to select the I/O and Auxiliary channels to be calibrated.
3. The minimum measurement delay is 100 ms. Increase this value to give the calibration points more time to settle.

DRM Calibration Warmup

Equipment: Basic Setup

Procedure:

1. Allow the T940 DRM to warm to its nominal application temperature.
2. Hit the Continue button when the required temperature is reached. If the temperature reaches 80°C, the process continues automatically.



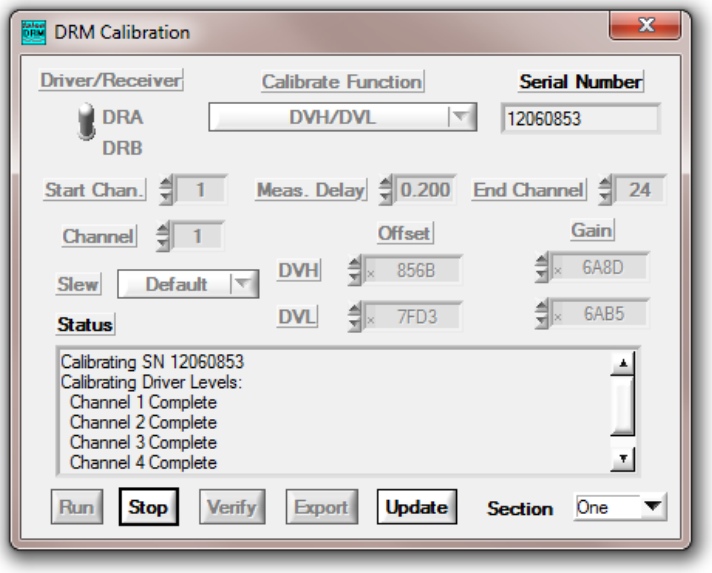
Run Calibration

Equipment: Basic Setup

Procedure:

1. Press the Run button. Use the Stop button at any time to abort execution.
2. Review the results in the Status window.
3. (Optional) Verify the results using the Verify button. Insure that all channels pass verification.
4. (Optional) Check the individual gain and offset values for DVH and DVL in the field controls. These values are not in engineering units.

5. (Optional) Save the calibration to a file for later restore, e.g., File | Load DRA Calibration.
6. (Optional) Update the module to the new calibration factors just obtained using the Update button. If this step is omitted, the calibration factors will revert at the next power cycle.



CVH/CVL

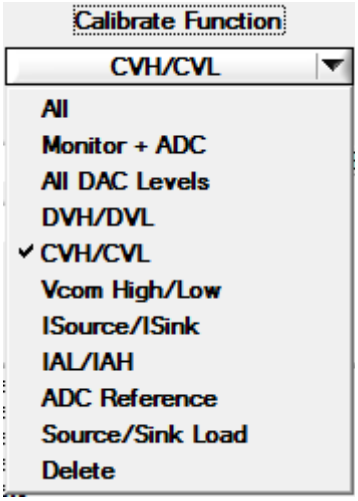
The CVH/CVL calibration calculates the offset and gain of the input comparator levels. For the DR4 a separate offset and gain is calculated for each group offset. The Verify button is available for use both before and after calibration. It is recommended that the calibration be verified before the Update button is used to store the current drive high and drive low calibration factors. The Export button can be used to save the calibration factors into a text file for examination and later restore, e.g., File | Load DRA Calibration.

Select Calibrate Function

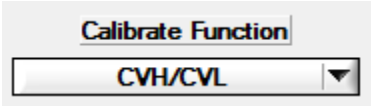
Equipment: Basic Setup

Procedure:

1. Place a check mark next the CVH/CVL menu item on the Calibrate Function menu.



2. Verify that the CVH/CVL calibrate function is now in focus.



Select Start and End Channels and Measurement Delay

Equipment: Basic Setup

Procedure:

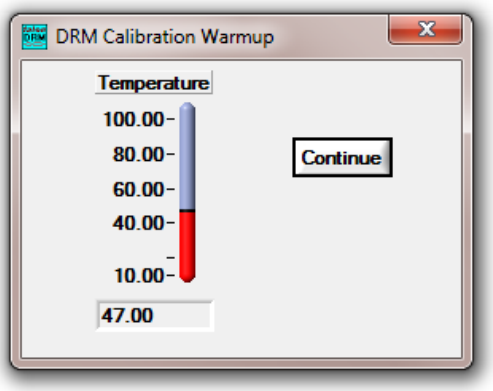
1. Select DRA or DRB (if installed) using the Driver/Receiver switch.
2. Use the Start and End Channel fields to select the I/O and Auxiliary channels to be calibrated.
3. The default measurement delay is 100 ms. Increase this value to give the calibration points more time to settle.

DRM Calibration Warmup

Equipment: Basic Setup

Procedure:

1. Allow the T940 DRM to warm to its nominal application temperature.
2. Hit the Continue button when the required temperature is reached. If the temperature reaches 80°C, the process continues automatically.

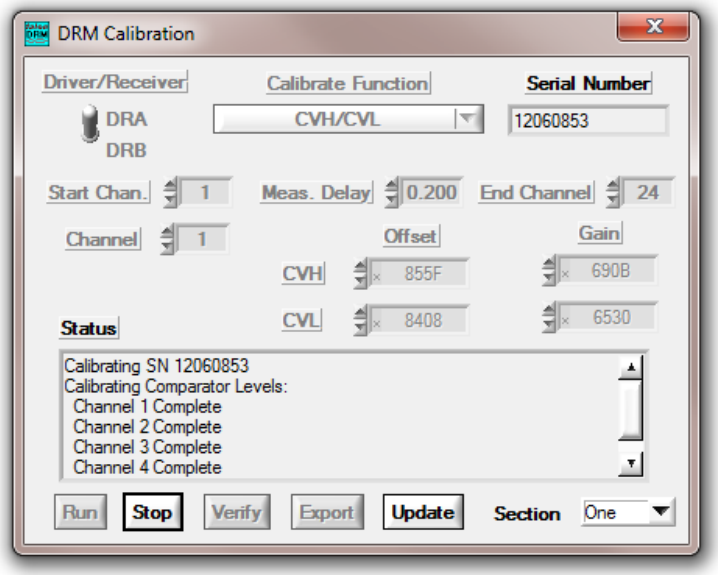


Run Calibration

Equipment: Basic Setup

Procedure:

1. Press the Run button. Use the Stop button at any time to abort execution.
2. Review the results in the Status window.
3. (Optional) Verify the results using the Verify button. Insure that all channels pass verification.
4. (Optional) Check the individual gain and offset values for CVH and CVL in the field controls. These values are not in engineering units.
5. (Optional) Save the calibration to a file for later restore, e.g., File | Load DRA Calibration.
6. (Optional) Update the module to the new calibration factors just obtained using the Update button. If this step is omitted, the calibration factors will revert at the next power cycle.



Vcom High/Low

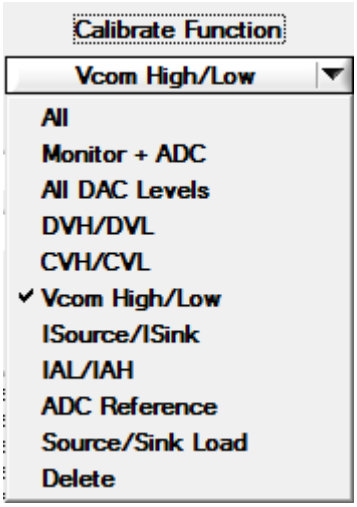
For DR3E, DR9 and UR14 only, the **Vcom High/Low** calibration calculates the offset and gain of the current and resistive commutating voltage levels. The Verify button is available for use both before and after calibration. It is recommended that the calibration be verified before the Update button is used to store the current drive high and drive low calibration factors. The Export button can be used to save the calibration factors into a text file for examination and later restore, e.g., File | Load DRA Calibration.

Select Calibrate Function

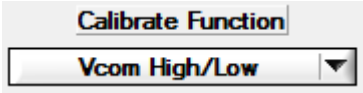
Equipment: Basic Setup

Procedure:

1. Place a check mark next the CVH/CVL menu item on the Calibrate Function menu.



2. Verify that the V_{com} High/Low calibrate function is now in focus.



Select Start and End Channels and Measurement Delay

Equipment: Basic Setup

Procedure:

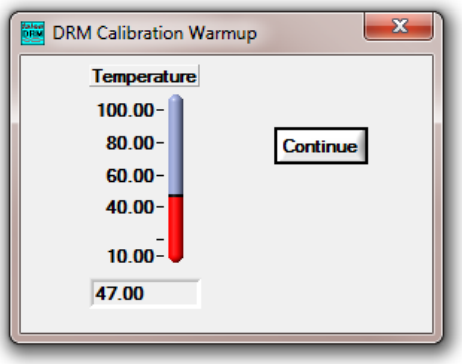
1. Select DRA or DRB (if installed) using the Driver/Receiver switch.
2. Use the Start and End Channel fields to select the I/O and Auxiliary channels to be calibrated.
3. The default measurement delay is 100 ms. Increase this value to give the calibration points more time to settle.

DRM Calibration Warmup

Equipment: Basic Setup

Procedure:

1. Allow the T940 DRM to warm to its nominal application temperature.
2. Hit the Continue button when the required temperature is reached.
3. If the DRM temperature reaches 80°C, the process will continue automatically. If the temperature reaches 80°C, the process continues automatically.

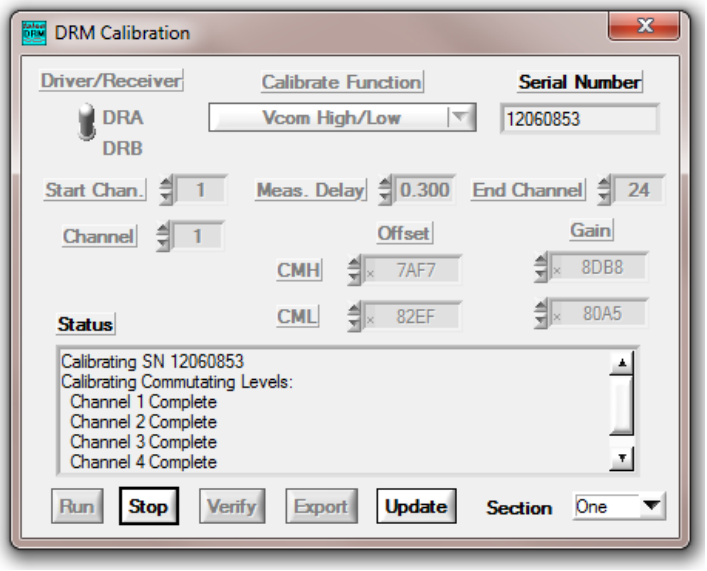


Run Calibration

Equipment: Basic Setup

Procedure:

1. Press the Run button. Use the Stop button at any time to abort execution.
2. Review the results in the Status window.
3. (Optional) Verify the results using the Verify button. Insure that all channels pass verification.
4. (Optional) Check the individual gain and offset values for CMH and CML in the field controls. These values are not in engineering units.
5. (Optional) Save the calibration to a file for later restore, e.g., File | Load DRA Calibration.
6. (Optional) Update the module to the new calibration factors just obtained using the Update button. If this step is omitted, the calibration factors will revert at the next power cycle.



Source/Sink Load

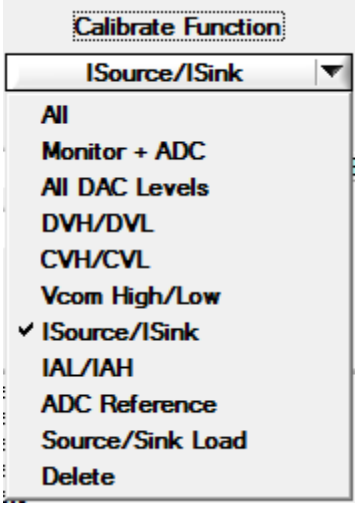
For DR3E, DR9 and UR14 only, the **Source/Sink Load** calibration calculates the offset and gain of the current load levels. The Verify button is available for use both before and after calibration. It is recommended that the calibration be verified before the Update button is used to store the current drive high and drive low calibration factors. The Export button can be used to save the calibration factors into a text file for examination and later restore, e.g., File | Load DRA Calibration.

Select Calibrate Function

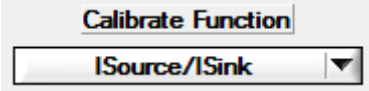
Equipment: Basic Setup

Procedure:

1. Place a check mark next the ISource/ISink menu item on the Calibrate Function menu.



2. Verify that the ISource/ISink calibrate function is now in focus.



Select Start and End Channels and Measurement Delay

Equipment: Basic Setup

Procedure:

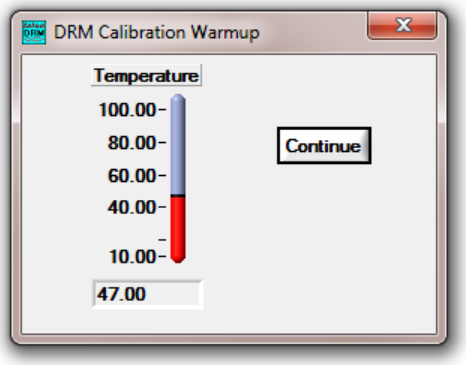
1. Select DRA or DRB (if installed) using the Driver/Receiver switch.
2. Use the Start and End Channel fields to select the I/O and Auxiliary channels to be calibrated.
3. The default measurement delay is 200 ms. Increase this value to give the calibration points more time to settle.

DRM Calibration Warmup

Equipment: Basic Setup

Procedure:

1. Allow the T940 DRM to warm to its nominal application temperature.
2. Hit the Continue button when the required temperature is reached. If the temperature reaches 80°C, the process continues automatically.

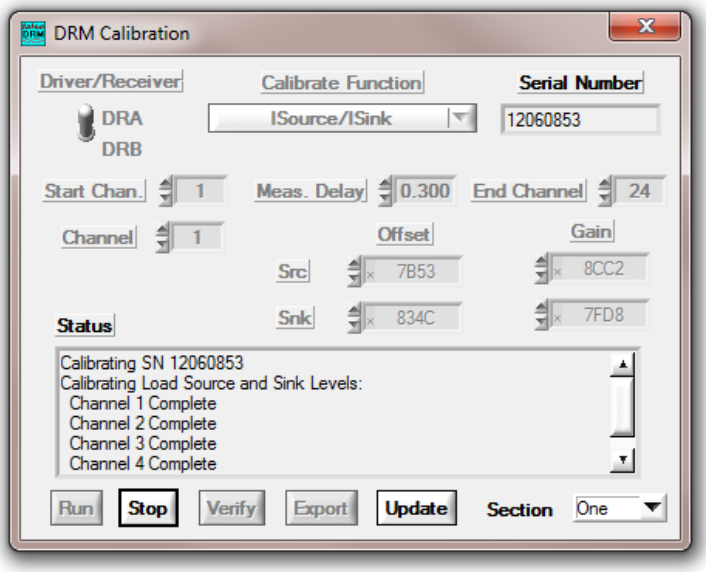


Run Calibration

Equipment: Basic Setup

Procedure:

1. Press the Run button. Use the Stop button at any time to abort execution.
2. Review the results in the Status window.
3. (Optional) Verify the results using the Verify button. Insure that all channels pass verification.
4. (Optional) Check the individual gain and offset values for Src and Snk in the field controls. These values are not in engineering units.
5. (Optional) Save the calibration to a file for later restore, e.g., File | Load DRA Calibration.
6. (Optional) Update the module to the new calibration factors just obtained using the Update button. If this step is omitted, the calibration factors will revert at the next power cycle.



IAL/IAH

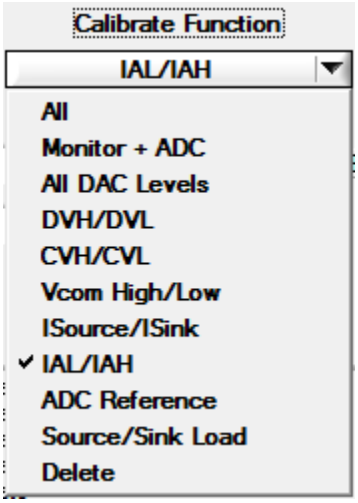
For DR3E, DR9 and UR14 only, the **IAL/IAH** calibration calculates the offset and gain of the over current alarm levels. The Verify button is available for use both before and after calibration. It is recommended that the calibration be verified before the Update button is used to store the current drive high and drive low calibration factors. The Export button can be used to save the calibration factors into a text file for examination and later restore, e.g., File | Load DRA Calibration.

Select Calibrate Function

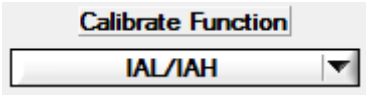
Equipment: Basic Setup

Procedure:

1. Place a check mark next the IAL/IAH menu item on the Calibrate Function menu.



2. Verify that the ISource/ISink calibrate function is now in focus.



Select Start and End Channels and Measurement Delay

Equipment: Basic Setup

Procedure:

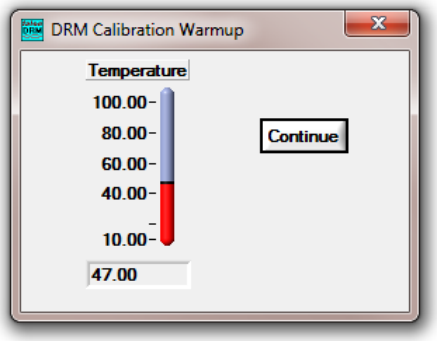
1. Select DRA or DRB (if installed) using the Driver/Receiver switch.
2. Use the Start and End Channel fields to select the I/O and Auxiliary channels to be calibrated.
3. The default measurement delay is 100 ms. Increase this value to give the calibration points more time to settle.

DRM Calibration Warmup

Equipment: Basic Setup

Procedure:

1. Allow the T940 DRM to warm to its nominal application temperature.
2. Hit the Continue button when the required temperature is reached. If the temperature reaches 80°C, the process continues automatically.

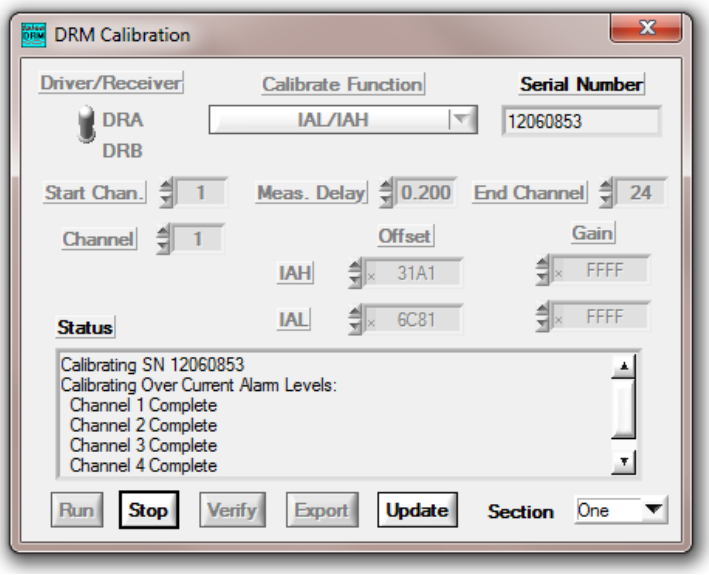


Run Calibration

Equipment: Basic Setup

Procedure:

1. Press the Run button. Use the Stop button at any time to abort execution.
2. Review the results in the Status window.
3. (Optional) Verify the results using the Verify button. Insure that all channels pass verification.
4. (Optional) Check the individual gain and offset values for Src and Snk in the field controls. These values are not in engineering units.
5. (Optional) Save the calibration to a file for later restore, e.g., File | Load DRA Calibration.
6. (Optional) Update the module to the new calibration factors just obtained using the Update button. If this step is omitted, the calibration factors will revert at the next power cycle.



Delete

Allows the user to delete Section Two calibration data stored internally. Saved calibration data can be restored using the restore feature, e.g., File | Load DRA Calibration.

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Chapter 7
Specifications

Each Digital Resource Module (DRM) is comprised of a Digital Board (DB) and one or two Driver/Receiver (D/R) boards. This section contains the specifications the Digital Board (DB) and its logic. The specifications for each available Driver/Receiver board are included in a separate appendix included in this manual.

Timing Characteristics

Internal I/O Data Rate (using the 500 MHz master clock)	~15.256 kHz to 50 MHz (with CPP = 1) 59.6 Hz Min. (with CPP = 256)
Internal I/O Data Rate (using the Freq synthesizer at 40 kHz as the master clock)	~1.22 Hz Min. (with CPP = 1) ~0.048 Hz Min. (with CPP=256)
Timing Set Options (3)	256 Timing Sets with 4 phases and 4 windows and 4K sequence steps 1K Timing Sets with 4 phases and 4 windows and 1K sequence steps (one for each sequence step) 4K Timing Sets with 1 phase and 1 window and 4K sequence steps (one for each sequence step)
T0Cycle Period Range (per Sequence step)	20 ns to ~65.5 µs (using the 500 MHz master clock)
T0Cycle Timing Resolution	1 ns (using the 500 MHz master clock)
Phase Programming Range	0 ns to ~65.5 µs (using the 500 MHz master clock)
Window Programming Range	0 ns to ~65.5 µs (using the 500 MHz master clock)
Phase/Window Timing Resolution	1 ns (using the 500 MHz master clock)
Minimum Phase/Window Pulse Width	8 ns (using the 500 MHz master clock)
Phase/Window Reference	Phases: System or Pattern Clock (selectable per sequence step) Windows: Pattern Clock only
Phase/Window Range	0 to Pattern Period – 8 counts
Window Dead Time	~13 ns at the end of the Pattern period

Clocks per Pattern (CPP)	1 to 256 (selectable per sequence step)
Pause/Pattern Clutch	Phases and Windows are frozen when asserted Can pause based on an external signal (levels or edges) Can pause based on a phase edge Can resume based on an external signal (levels or edges) or CPU Resume Can resume after a programmed delay (2 timers available). Useful to implement a Wait Pattern timeout can be programmed to generate an event if a pattern is paused too long. See the **Pause and Halt** section of **Chapter 8** for additional details about the use of pause.
Halt/System Clutch	All phases will complete their action for the current pattern. Can halt based on an external signal (levels or edges) Can halt on error (at slower data rates) Can halt on a sync pulse (used as a breakpoint) Also used for single-stepping *(The latter three require a CPU Resume: see spec for additional clarification.)* Halting on error is discussed in more detail in the **Pause and Halt** section of **Chapter 8** for additional details about the use of halt.
Pause/Pattern and Halt/System Clutch Sources	TTLTrg0-7, ECLTrg0-1, F/P AUX I/O 1-12, CH 1-32 (with mask/expect), and Phase 1-4 (for Pause)
External T0Cycle Range	< 1 kHz to ~48 MHz
External T0Cycle Edge Selection	Can use either edge or both edges of a signal to define the T0 Cycle period. Can also divide the incoming clock by 2.
External T0Cycle Delay Adjustment	A programmable delay is provided to adjust the timing relationship of the T0Cycle with respect to the Ext. input (2 ns resolution; 0-64K ns range with the 500 MHz master clock).
External T0Cycle Clock Source	F/P AUX I/O 1-12, ECLTRG0

Clock/Waveform Outputs	Up to 4 waveforms can be output during a pattern (each sequencer). They are provided in lieu of certain phases and windows. They can be output on any AUXI/O Channel (two can actually be output on any data channel). They can be any arbitrary or repeating waveform. There are up to 16 waveform tables. Output resolution/step size is 1 ns with the 500 MHz master clock. The width (high or low) should not be too narrow with respect to the driver rise fall time capabilities of the Channel being used to output it.

Stimulus/Capture Characteristics

Testing Modes	Dynamic, Static
Dynamic Mode:	
Output Timing Sources (per channel)	Static selection of phase 1-4
Input Timing Sources (per channel)	Static selection of window 1-4
Data Output Formats (per channel)	Force: lo, hi, tri-state Format: NR, RT, R0, R1, RC, Complement Surround Output the Phase or its complement (used to output waveforms on channels)
Capture Modes (per channel)	Mask Opening edge of window Closing edge of window Window (input data must match “expect” for the entire duration of the window)
Pattern Memory	Size: 256K
Pattern (Stimulus/Expect) Data	Output: H, L, Tristate Expect: Good 1, Good 0, OK, between or mask Keep last Toggle last Accumulate a CRC16 (based on a Good 1 only)

Static Mode	Utilizes a Single Word Sequence Step Delay Range: 1 ns to ~65 µs (master clock @ 500 MHz) Delay Range: 100 ns to 6.5 ms (master clock @ 5 MHz) Resolution: 1 ns (for a 500 MHz master clock) Resolution: 100 ns (using a 5 MHz master clock) Note: Repeat pattern data is updated based on the static drive state
Static Mode Type 2a (available on F/W 0.20 and earlier)	Utilizes an independent static stimulus/response path that doesn't alter the Repeated pattern data of dynamic tests. Static test is run in parallel with a standby Sequence Step. Stimulus and Response capture timing defined by Pulse Generator assert and de-assert timing (set the Pulse Generator for Single Start). Resolution and range based on the Pulse Generation settings. Standby Sequence Step must have a period greater than the de-assert timing.
Static Mode Type 2b (available on F/W 0.21and later)	Utilizes an independent static stimulus/response path that doesn't alter the Repeated pattern data of dynamic tests Static test is not run in parallel with a standby Sequence Step. Response Delay from 100ns to ~6.5ms in 100ns steps.

Recording Mode Characteristics

Recording Modes (per Sequence Step)	Record errors for programmable inputs that have a Good 1 and Good 0 Record errors for single-ended inputs that have only a Good 1 Record raw data based on NOT a Good 0 Record raw data based on a Good 1

Recording Type	Un-expanded: Record data at the same index as the stimulus (will overwrite data when looping) Expanded: Records data sequentially. A separate Record Index Memory stores information that allows the recorded data to be re-aligned with the original data.
Error Address Recording	Separate Error Address Record Memory records where errors occurred in the Record Memory. Limit: 1K errors.
Record Offset	Used to compensate for round-trip driver/receiver delay and also cabling delay to the UUT. Can also be used to allow windows to effectively close at the end of the T0Cycle. Resolution: 1 master clock Range: 2-63 master clocks

Sequencer Characteristics

General	Sequencers: 2 per Digital Resource Module Channels: 32 per sequencer Modes: Static, Dynamic
Sequence Memory	Sequence Size: 1024 or 4096 Steps
Sequence Loop Counters	Loop Counters: 16 Loop Count can be different each time or continuous Loop counters may be nested Loop counters can be optionally re-loaded during a burst Only one can end on a sequence step
Loop Count Range	1-64K or continuous
Subroutine Characteristics	Output one or more Sequence Steps with or without looping. Cannot be nested. Has a designated “Return” Step.
Burst Count Range	1-1M or continuous
Jump Types	Conditional or unconditional Jumps at the end of a sequence step Vectored (1 of 16 destinations)

Conditional Jump Sources (per seq. step)	One of four Test Inputs Seq. Step PASS Seq. Step FAIL Seq. Step NOT a PASS (i.e. FAIL or indeterminate) Seq. Step NOT a FAIL (i.e. PASS or indeterminate) Burst PASS Burst FAIL
Conditional Jump Enable (CONDEN)	Per pattern
PASS/FAIL Pipeline	0-31 patterns
Burst Error Enable (BERREN)	Per pattern
Test Input Sources	TTLTrg0-7, ECLTrg 0-1, F/P AUX I/O 1-12, Chan 1-32 (with mask/expect)
Test Input Sense	Rising edge, Falling edge, Hi-state or Low state
Sync Pulse Outputs	Outputs per Sequencer: 2 Modes: Start of Sequence, Start of Sequence Step Offset Range 0-1M patterns Pulse Width: 1-4095 patterns
AUX Outputs	Sync Pulses (2) Sequence Flags (2) Sequence/Idle Active T0Cycle Waveforms Phases/Windows A multitude of other signals
Sequence Standby Characteristics	A one word continuous sequence step that may be used to output “standby” data on power up or after a sequence reset. The CPU can access pattern data in this state.
Idle Sequence Characteristics	A continuous sequence step that may be used to output data before or after an active sequence. The CPU cannot access pattern data in this state. The Idle Sequence output after the active sequence may be different from the one output before.

Sequence Execution Control	Reset to Standby Sequence (CPU command) Run Idle Sequence (CPU or external command) Run Sequence (CPU or external command) Stop Sequence (CPU or external command) Single step by Pattern or Sequence Step. (see Halt function)
Burst Timeout Timer	A watchdog timer that limits the maximum execution time of a dynamic pattern set independently of pauses, halts and external clocks. On timeout, sets all outputs to tri-state. Can be disabled. Range: 40 ns to ~86 seconds Resolution: 20 ns
Handshaking	See Pause function

Master Clock (MCLK)

Internal Oscillator	500 MHz Accuracy: 50 ppm
Internal Synthesizer	40 KHz to 500 MHz
Internal Reference	20 MHz or VXICLK10
Internal Synthesizer Resolution	4 digits typical
20 MHz Reference Accuracy	50 ppm
External Front Panel Reference	Range: 5 MHz to 80 MHz
Slow Mode	Frequency Synthesizer allows timing to be reduced by a factor of 1 to >10000

Counter/Timer Characteristics

Measurement Modes	Frequency Period Time Interval Totalize Timed Totalize Positive Pulse Negative Pulse
Input Source	CH1-32 (Uses Good 1) AUX1-12 Frequency Synthesizer VXICLK10 250 MHz Pulse Generator
Input Sense	Rising/Pos or Falling/Neg
Frequency/Period Measurement Source	Input 1
Frequency/Period Measurement Range	0.25 Hz to 250 MHz/4 ns to 4 s
Preset Aperture Windows	1 µs to 10 s in decade steps
Aperture Window Accuracy	0.1% +50 ppm
Frequency/Period Measurement Resolution	≥4 Digits with a 1 ms Aperture ≥5 Digits with a 100 ms Aperture ≥6 Digits with a 10 s Aperture
Time Interval Functions	Between Inputs 1 & 2; Positive/Negative Pulse Width of Input 1
Time Interval Range	~2 ns to ~4.29 s
Time Interval Resolution	1 ns
Time Interval accuracy	1 count + input comparator threshold uncertainty
Time Interval Reference Accuracy	50 ppm
Totalize (2 modes)	Timed with a Preset Aperture. Aperture defined by Input 3.
Preset Aperture accuracy	50 ppm
Max. Count	2^32-1
Max. Input Data Rate	250 MHz Note: CH and AUX input technology may limit the max. data rate that can be supported.
Input Trigger	Input 3

Trigger functions for Freq./Period, Time Interval & Totalize (mode 1 only)	Manual External (Input 3) Continuous
Events provided	Indicates when the data is ready to be read (may also generate an interrupt)

Pulse Generator Characteristics

Signal Routing	System Clock VXI Triggers (TTL and ECL) Linked Trigger Bus Any Aux channel Counter Input
Pulse Resolution	10 ns, 20 ns
Run Mode	Continuous Continuous Start Single Start Single Step
Period	10 ns Resolution: Min: 20 ns Max: 42.94967297 s 20 ns Resolution: Min: 40 ns Max: 85.899345960 s
Delay	10 ns Resolution: Min: 20ns Max: 42.94967297 s 20 ns Resolution: Min: 20ns Max: 85.899345960 s
Width	10 ns Resolution: Min: 0ns Max: 42.94967297 s 20 ns Resolution: Min: 0ns Max: 85.899345960 s

Calibration

DAC Basic[1]	Factory stored in EEPROM
D/R channel deskew[2]	Factory stored in EEPROM

ADC/Monitor[1]	Field upgradable stored in EEPROM
DVH/DVL[1]	Field upgradable stored in EEPROM
CVH/CVL[1]	Field upgradable stored in EEPROM
V_{com} High/V_{com} Low[2]	Field upgradable stored in EEPROM
I_{source}/I_{sink}[2]	Field upgradable stored in EEPROM
IAL/IAH[2]	Field upgradable stored in EEPROM
Inter-module timing deskew[3]	Static
End-of-cable deskew[1]	Static
Pipelined operation (for 0.21 F/W and later)	

Note 1: *DR3e, DR9, UR14 and DR4 only*

Note 2: *DR3e, DR9 and UR14 only*

Front Panel I/O

The DB is isolated from the front panel via the Driver/Receiver board(s). Refer to the appropriate appendix for the front panel specifications for the installed Driver/Receiver board.

VXI Interface

Interfaces Supported	Register-based operation
Data Transfers	Address: A16 and A24/A32 Data: D16/D32
VXI Feature Usage	TTLTRG0-7, ECLTRG0-1: Triggering, driver disable, channel tests, DRS sync check, and error reporting LBUS: Inter-module Synchronization Interrupts: An assortment from the Data Sequencers and the Driver/Receiver boards (see **Configuring the Interrupts**, **Sequencer Events** and **Driver Receiver Events** in **Chapter 5**).

Power Requirements

Table 7-1: Power Requirements (DB only)

Voltage	Peak Current	Dynamic Current
+5V	2.9 A	30 mA
-5.2V	370 mA	20 mA
-2V	40 mA	10 mA

Voltage	Peak Current	Dynamic Current
+12V	0	0
-12V	0	0
+24V	0	0
-24V	0	0

Environmental

Temperature	Operating: 0° C to 45° C * Storage: -40° C to 70° C
Humidity (non-condensing)	0° C to 10° C: Not controlled 10° C to 30° C: 5% to 95% ±5% RH 30° C to 40° C: 5% to 75% ±5% RH 40° C to 50° C: 5% to 55% ±5% RH
Altitude	10,000 ft
Cooling Required (10°C Rise; 2 DR3e)	Max: 27.4 l/s @ 8.9 mmH^{2}0 Typ.: 18.9 l/s @ 4.5 mmH^{2}0
VXI Current Requirements (DB only)	V: +24, +12, +5, -2, -5.2 Ipeak (A): 0, 0, 2.9, 0.04, 0.37 Idyn. (A): 0, 0, 0.03, 0.01, 0.02
VXI Current Requirements (With 2 DR3s installed)	V: +24, +12, +5, -2, -5.2 Ipeak (A): 0.02, 0.03, 9.5, 0.26, 5.4 Idyn. (A): 0.01, 0.01, 0.53, 0.01, 0.04
Front Panel PWR Current Requirements (channels unloaded) (per DR3/)	V+: 3.8 A max.; 2.9 A typ. @ 21.5 V V-: 4.3 A max.; 3.4 A typ. @ -10.5 V
MTBF (ground benign)	T940: 180,885 hours
Dimensions	Single slot, “C” size VXI module. (30 x 260 x 350 mm)
EMC (Council Directive 89/336/EEC)	Emission: EN61326-1: 2006, Class A Immunity: EN61326-1: 2006, Table 1 ***Designed to Meet – Testing in Progress***
Safety (Low Voltage Directive 73/23/EEC)	BS EN61010-1: 2010 ***Designed to Meet – Testing in Progress***

* For a DRM with 2 DR3e modules, the 1263 chassis only has sufficient airflow for ~25 ºC max. inlet air temperature at <~2000 ft.

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Chapter 8
Advanced Topics

This section describes advanced topics of the T940, giving more details than what were provided in previous chapters. Because references are made to DRS configurations, relevant API and ARI calls are both provided here.

The topics covered include:

- Jumping, Halting, Counting and Logging on Pass/Fail
- Understanding Record Offset
- Pause and Halt
- Sequencer Operation Details
- VXI Backplane Trigger Bus

Jumping, Halting, Counting and Logging on Pass/Fail Conditions

The T940 has extensive capability when it comes to Jumping or Halting on various Pass/Fail conditions in both Pipelined and non-Pipelined modes. The counting or logging of Errors in the Error Address Memory (EAM), Single Stepping and Record Modes will also be covered since they are interrelated.

This section discusses these topics using the Soft Front Panel (SFP) but *VXIplug&play* API calls and Application Resource Interface (ARI) references are provided.

Topics to be covered in this section include:

- Coupling of signals between Sequencers for Linking and DRS Formation
- Step Record Mode
- Record Type
- Counting and Logging Errors
- Pipelining and non-Pipelining
- Jumping or Halting on Pass/Fail conditions
- Understanding Pass/Fail
- Additional Pipeline Information
- Valid Pass and Capture Fault
- Additional Halt Information
- Calibration

- Performance considerations
- Pipelined Depth Calculation
- Record Offset Limitations
- Two better ways to do a Wait

Coupling Signals between Sequencers for Linking and DRS Formation

First, let's define some terms that will be used in the discussion:

- **Independent**: A single Sequencer (A or B) operating independently of all others.
- **Linked**: In a single DRM Sequencer B is solely linked to Sequencer A and to no other Sequencers.
- **DRS**: Two or more DRMs are needed to create a DRS. The Primary A Sequencer is the Master Sequencer which will typically have all of the other Sequencers (A & B) coupled to it. But one or more may be excluded. The Master must always be included in a DRS but any of the other Sequencers may be excluded. Those excluded may be: simply unused, be independent or for a given DRM, could be Linked. In the latter two cases, they are separate instruments from the remaining sequencers which make up the DRS.
- **Coupled**: A term that's only used when another sequencer is coupled to the Master in a DRS.

Before getting into the details of Jumping, Halting, Counting and Logging, there are signals that may need to be connected/coupled between Sequencers to support these functions in a Linked or DRS Configuration. The table following the figure summarizes the applicable signals and their usage. No signals need to be linked for Independent (Local) operation.

For Linked operation, here are some signals that one might set up. This is accomplished on the Config>Configure Module panel by clicking on the Linked Trigger Bus panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setLtbTriggers
- ARI: AssignPatTimeGroup, AssignPtgTrigger

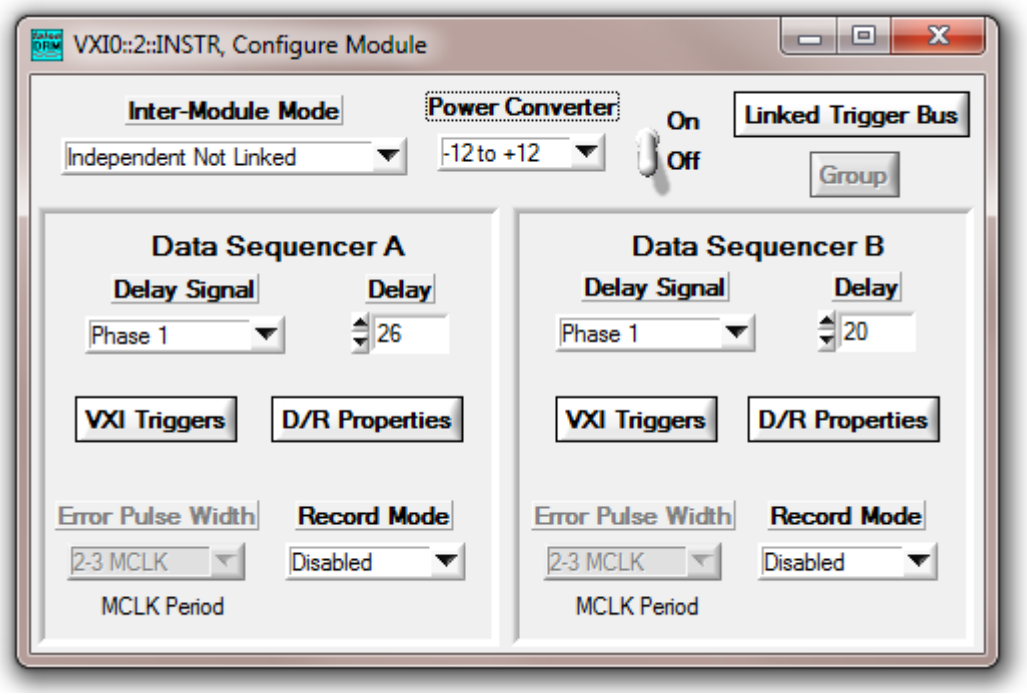


Figure 8-1: Configure Module Panel

On this panel, six signals are set up to be coupled between Sequencers A to B in the directions shown:

- Error
- Pass Valid
- DRM Sync
- Driver Disable
- Halted
- Static Pulse

These six are all of the signals that are potentially useful. Those that are not needed may be excluded. For example, Static Pulse may be excluded if channels will not be used in Static Mode anywhere in the DRS.

The panel automatically handles the direction and sense of these signals, thus the Direction and Invert fields are dimmed.

***Note**: Sequence Reset and Master Reset are automatically handled in the S/W, i.e. a Sequence or Master Reset on either Sequencer will reset the other when they are linked.*

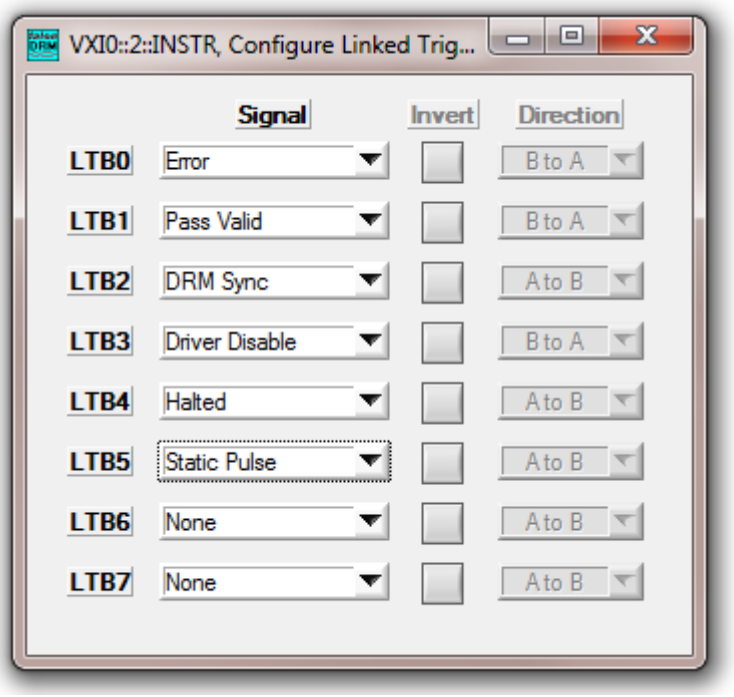


Figure 8-2: Configure Module Panel

For DRS operation, there are additional signals that might need to be setup depending on how the DRS will be operated. From the same Configure Module panel, select VXI Triggers for the Data Sequencer A and/or B depending on whether that Sequencer is included in the DRS configuration or not.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setTtlTriggers, tat964_setEclTriggers
- ARI: AssignPatTimeGroup, AssignPtgTrigger

Additional signals required to be coupled along the backplane to form the DRS include:

- Sequence Reset
- Master Reset

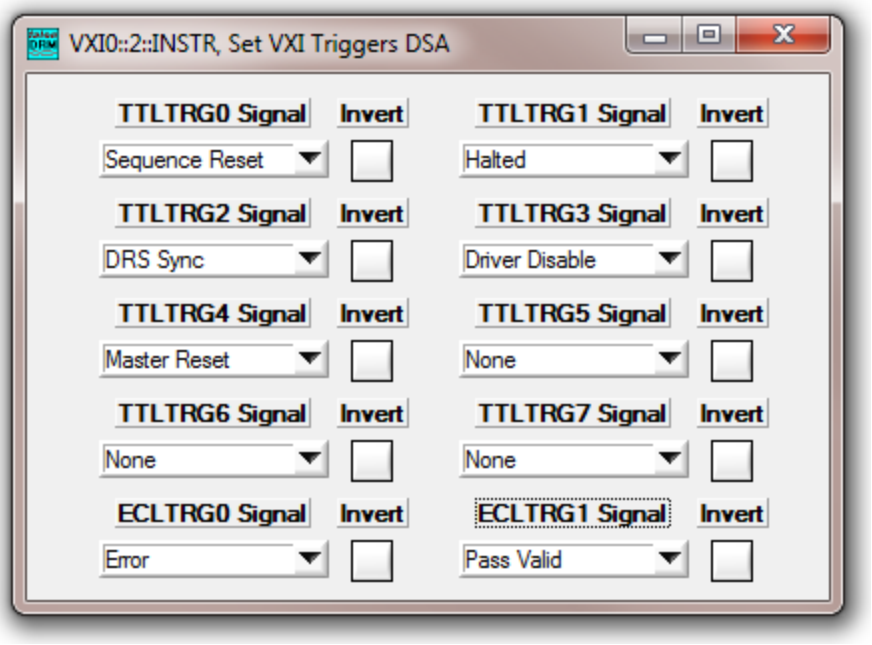


Figure 8-3: Configure VXI Triggers DSA Panel

***Note**: Error and Pass Valid were placed on ECLTRGs. This is necessary for high Data Rates, >~20 MHz because the TTLTRG bus has a slow recovery time.*

Table 8-1 describes these signals and explains when they are needed:

Table 8-1: Summary of When Specific DRS Signals are Needed

Signal	When needed
Error	Whenever Error needs to be connected/coupled to the Master Sequencer for Jumping, Halting, Counting or the Logging of Errors in the EAM.
Pass Valid	Needed whenever Pass Valid Mode is enabled. Error must also be connected/coupled when Pass Valid is used.
Halted	Allows connected/coupled Sequencers to have their Pattern Data and Record memories accessible when halted.
DRS Sync	Allows one to detect and create an event that says that that a connected/coupled Sequencer is out of sync with the Master Sequencer
Sequence Reset	Allows a Sequence Reset performed on the Master or any coupled Sequencer to reset all of the Sequencers coupled together in a DRS. *Note: on the Execute Panel, this is simply called Reset.*
Master Reset	Allows a Master Reset performed on the Master or any coupled Sequencer to reset all of the Sequencers coupled together in a DRS. *Note: a Master Reset disables all of the channel drivers among other things.*

Signal	When needed
Driver Disable	If programmed to do so on each Sequencer, a channel fault which occurs on the Master or any connected/coupled Sequencer will disable all of the channel drivers.
Static Pulse	Couples the Static Stimulus/Response Pulse from the Master to all connected/coupled sequencers. It is only needed if Static Mode is being used.

The signals above, which are desired for a DRS configuration, **must be setup on the same** TRG buses on the Master and each coupled Sequencer.

***Warning**: Do not program the same TRG Bus for Sequencers which are not a part of the DRS.*

Step Record Mode

Step Record Mode is programmed in each Sequencer Step. On the SFP, it is set on the Edit>Data Sequencer A/B>Sequence Steps panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setSequenceRecordMode
- ARI: AssignPtgResponseMode

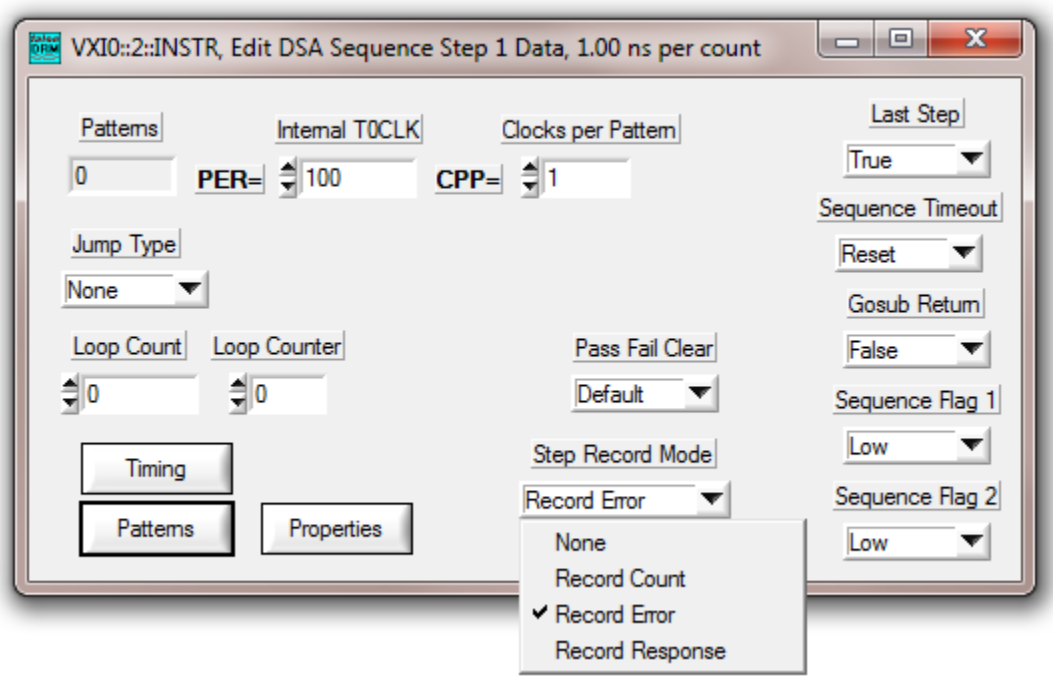


Figure 8-4: Step Record Mode Control on Edit DSA Sequence Step Panel

As shown, the choices are:

- None
- Record Count
- Record Error

- Record Response

For each Sequence Step, this selection can be made. Table 8-2 describes how these selections affects what's recorded in the Record Memory.

Table 8-2: Summary of the Record Memory Action for each Step Record Mode

Step Record Mode	Record Memory Action
None	Don't record anything
Record Count	Don't record anything (or record non-Errors)
Record Errors	Record Errors
Record Response	Record Response

The first choice means that nothing will be recorded in the Record Memory for any pattern in this step. But this means different things based on the Record Type. See the **Record Type** section below for more information.

The second entry provides two choices. This is programmed on the Config>Configure Module panel as shown in Figure 8-4 below.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setSequenceRecordMode
- ARI: AssignPtgRecordMode

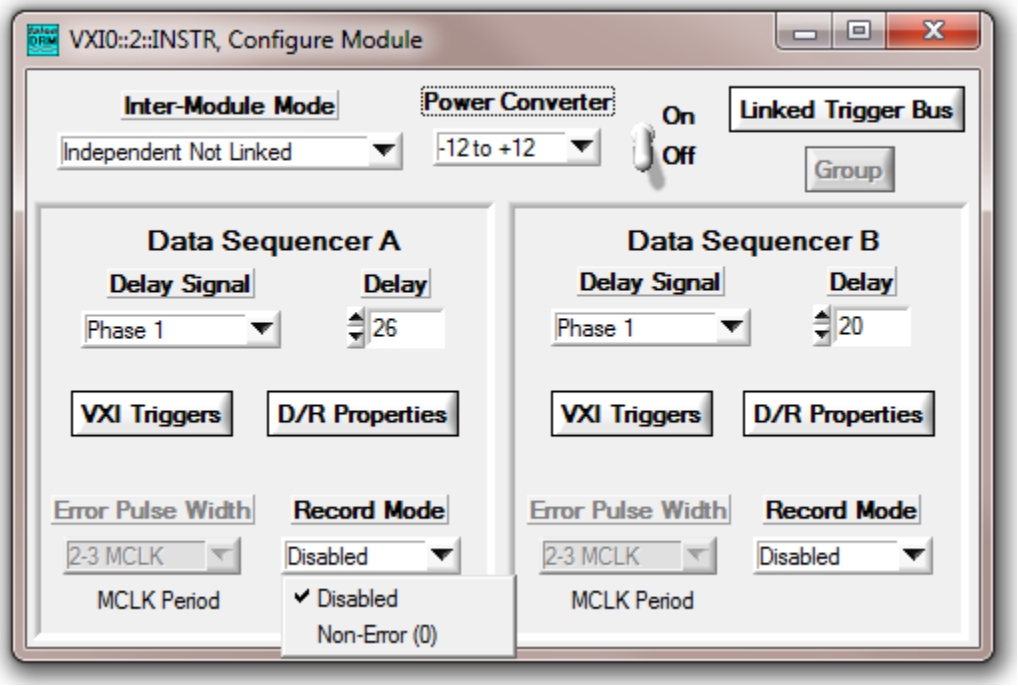


Figure 8-5: Setting the Record Mode Using the Configure Module Panel

Setting the Record Mode to **Disabled** means the same as setting the Step Record Mode to None as shown above.

Setting the Record Mode to **Non-Error** means that “zeros” will be written into the Record Memory for the Patterns on that Sequence Step, effectively clearing the memory.

The last two Step Record Modes effect the Counting and Logging of Errors. Each of these modes will be described in the **Counting and Logging Errors** section below.

Record Type

The Record Type is programmed on the Config>Data A/B Sequencer>Setting Panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setRecordParameter
- ARI: AssignPtgRecordType

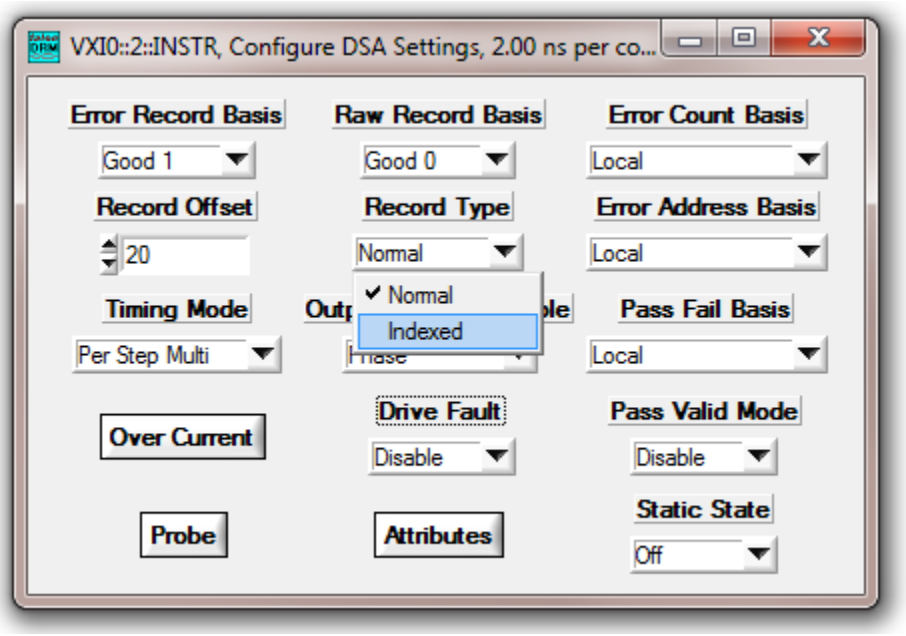


Figure 8-6: Setting the Record Type Using the Configure DSA Settings Panel

The two choices are:

- Normal
- Indexed

Setting the Record Type to **Normal** records into the Record Memory at the same address which corresponds to the Data Pattern. Thus, when looping a Step or repeating a Step at some later point during the Primary Sequence, the data in the Record Memory will be over-written.

Setting the Record Type to **Indexed** recording means that data will be written into the Record Memory consecutively. A Record Index memory keeps track of how the data is written into the Memory so it can be reconstructed, i.e., which data belongs to each step and/or loop.

Table 8-3 summarizes what gets recorded based on the selected Step Record Mode.

Table 8-3: Summary of the Record Memory Action for each Step Record Mode

Action	Normal Record Type	Indexed Record Type
Don't record anything	Don't record anything into the Record Memory at the address that corresponds to the Data Pattern address. Thus whatever is there will not be over-written	Don't record anything into the Indexed Record Memory.
Record non-Errors	Write "zeros" into the Record Memory at the address that corresponds to the Data Pattern address	Write "zeros" into the Indexed Record Memory

***Note**: If using Indexed Recording, "Don't record anything" is the better choice to avoid filling up the Record Memory unnecessarily with "zeros."*

Counting and Logging Errors

Errors can be counted for Independent Sequencers, Linked Sequencers or multiple Sequencers which are part of a DRS. Similarly, Errors can be logged into the EAM for Independent Sequencers, Linked Sequencers or multiple Sequencers which are part of a DRS.

For both of these circumstances, the Errors can be non-qualified Errors or Qualified Errors.

When Non-qualified Errors are chosen all of the Pattern Errors in a Sequence Step are counted if the Step Record mode calls for Errors to be counted.

When Qualified Errors are chosen, only those patterns enabled by BERREN (Burst Error Enable) are counted if the Step Record mode calls for Errors to be counted.

This BERREN bit is set in the Pattern Memory. The Pattern Data can be accessed on either the Edit>Sequencer A/B>Patterns or Sequencer Steps panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setPatternTestEnable
- ARI: LoadPtgStepExpectedPatternBin, LoadPtgStepPatternChar

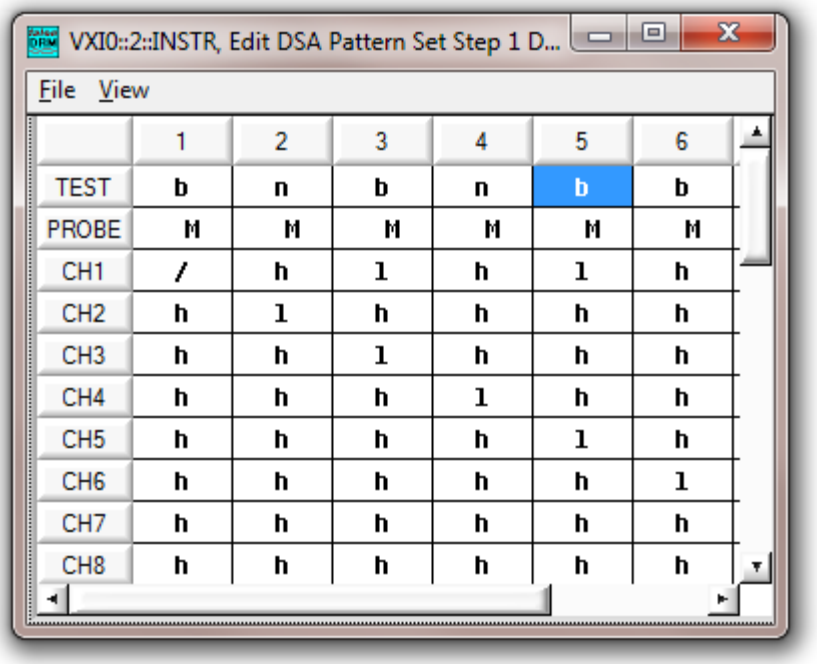


Figure 8-7: Setting the Test Bit in the Edit DSA Pattern Set Step Panel

In the TEST row for each pattern (column), a “b” sets BERREN true whereas an “n” sets it false.

Thus, in the example, above, patterns 1, 3, 5 & 6 have BERREN set whereas patterns 2 & 4 do not have BERREN set.

The “Basis” for Counting Errors is set on the CONFIG>Data Sequencer A/B>Settings Panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setErrorParameters
- ARI: AssignPatTimeGroup

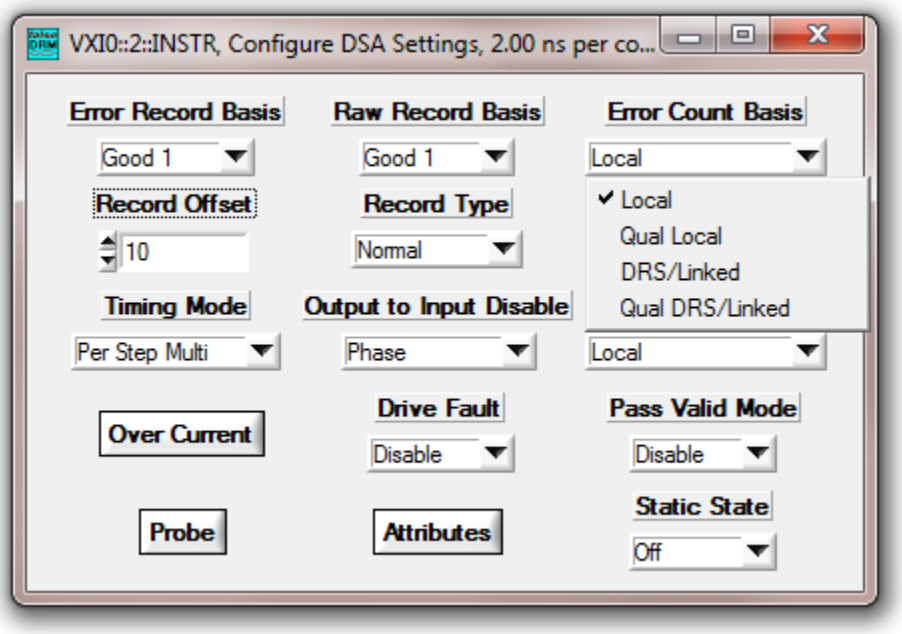


Figure 8-8: Setting Error Count Basis in the Configure DSA Settings Panel

The “Basis” for Logging Errors into the EAM is set on the same Panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setErrorParameters
- ARI: AssignPatTimeGroup

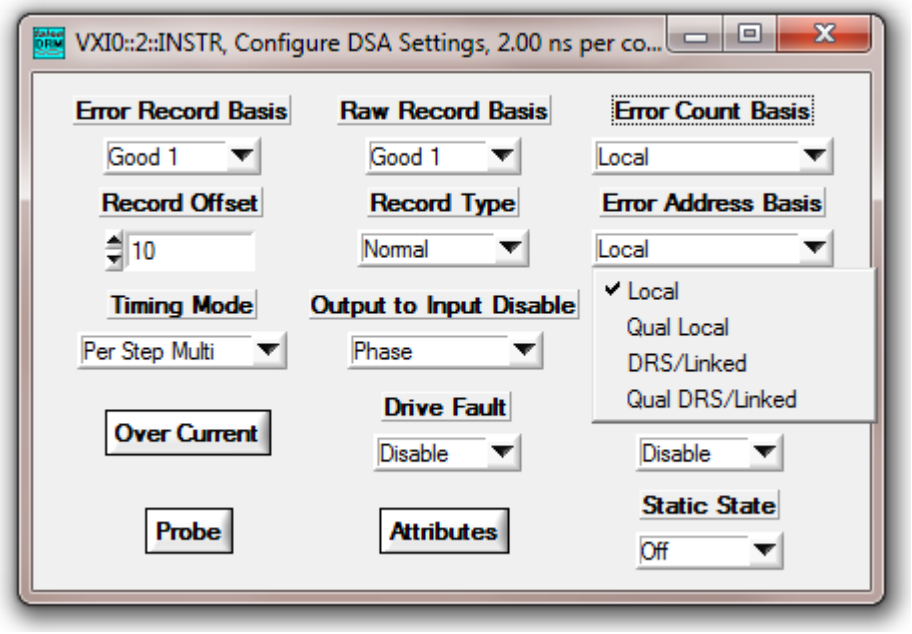


Figure 8-9: Setting Error Address Basis in the Configure DSA Settings Panel

In both cases, the available choices are the same:

- Local

- Qual. Local
- DRS/Linked
- Qual. DRS/Linked

But what is counted or logged varies based on the Step Record Mode.

For Counting Errors, refer to Table 8-4:

Table 8-4: Cross-Reference of Step Record Mode to Error Count Basis

	Step Record Mode			
Error Count Basis↓	**None**	**Record Count**	**Record Error**	**Record Response**
Local	Don't Count Errors	Count Local Errors	Count Local Errors	Count Local Errors
Qual. Local	Don't Count Errors	Count BERREN Qual. Local Errors	Count BERREN Qual. Local Errors	Count BERREN Qual. Local Errors
DRS/Linked	Don't Count Errors	Count DRS/Linked Errors	Count DRS/Linked Errors	Count DRS/Linked Errors
Qual. DRS/Linked	Don't Count Errors	Count BERREN Qual. DRS/Linked Errors	Count BERREN Qual. DRS/Linked Errors	Count BERREN Qual. DRS/Linked Errors

For logging Errors into the EAM, refer to Table 8-5:

Table 8-5: Cross-Reference of Step Record Mode to Error Address Basis

	Step Record Mode			
Error Address Basis↓	**None**	**Record Count**	**Record Error**	**Record Response**
Local	Don't log any Errors	Don't log any Errors	Log Local Errors in the EAM	Log Local Errors in the EAM
Qual. Local	Don't log any Errors	Don't log any Errors	Log BERREN Qual. Local Errors in the EAM	Log BERREN Qual. Local Errors in the EAM
DRS/Linked	Don't log any Errors	Don't log any Errors	Log DRS/Linked Errors in the EAM	Log DRS/Linked Errors in the EAM
Qual. DRS/Linked	Don't log any Errors	Don't log any Errors	Log BERREN Qual. DRS/Linked Errors in the EAM	Log BERREN Qual. DRS/Linked Errors in the EAM

In a DRS, Local Errors can be counted/logged in coupled sequencers while the Master sequencer is simultaneously counting/logging DRS Errors.

In addition, one could use a different BERREN when counting/logging Qualified **Local** Errors if that is useful. But there are limitations. See Appendix A for those limitations.

Notes:

1. *The T940 is designed to accurately count/log DRS Errors in the Master at a 50MHz data rate.*
2. *When a Sequencer is Independent, the "DRS/Linked" option will not Count or Log anything.*

Pipelining and non-Pipelining

Before Jumping and Halting on various Pass/Fail conditions can be presented, an understanding of pipelining is required.

- The pipeline may be from 0-16 Patterns deep. The "0" pipeline depth will hereafter be called a "zero pipeline depth" or "non-pipelined". A pipeline depth of "1-16" will hereafter be called a "non-zero pipeline depth" or "pipelined".
- A zero pipeline depth is primarily used when it's desired to perform a Jump on Pass/Fail in a Seq. Step where the deciding Error may occur on even the last Pattern of the Seq. Step. This allows one to Halt immediately on Patterns that have a Fail or Pass. There are performance limitations for the "zero pipeline depth" covered in the **Performance Considerations** section, below.
- A non-zero pipeline depth means that the Error is offset/delayed by the depth of the pipeline. In this case, a Halt on Pass or Fail will occur later by the depth of the pipeline. For Jumping on a Pass or Fail, there is a Jump Pass/Fail attribute that affects how Jumps are handled. This is detailed in Section 7. The non-zero pipeline depth will handle data rates at 50MHz but there is a minimum pipeline depth required depending on the Data Rate. This is covered in the **Pipelined Depth Calculation** section, below.

The Pipeline Depth is set on the Edit>Data Sequencer A/B>Sequence Parameters panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setConditionPipelineMask
- ARI: AssignPtgPipelineMask

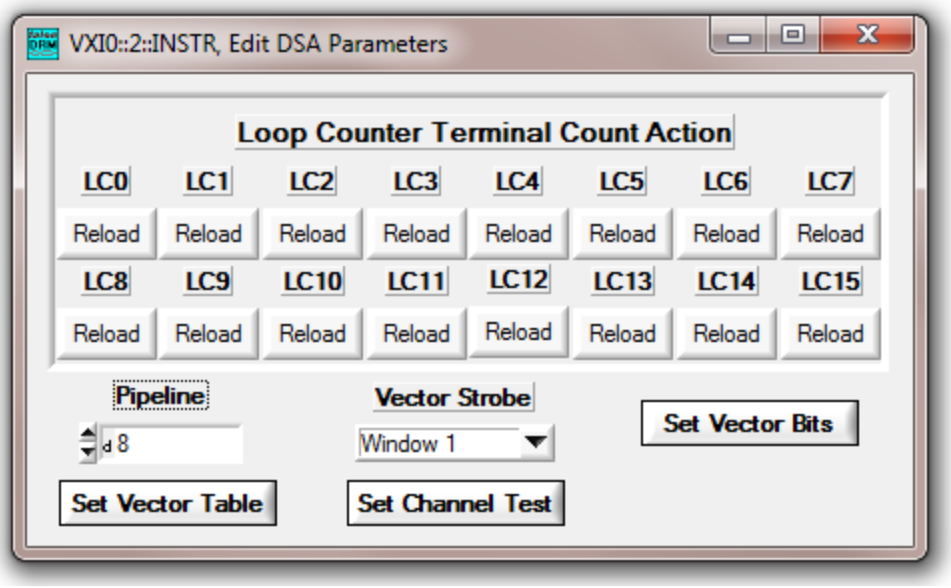


Figure 8-10: Setting the Pipeline Mask in the Edit DSA Parameters Panel

The setting for a pipeline depth of 8 is shown.

Jumping and Halting on Pass/Fail

Similar to the Counting and Logging of Errors there is a Basis for Jumping and Halting on Pass/Fail conditions. Jumping and Halting is programmed on the same panel as before.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setPassFailParameter
- ARI: AssignPatTimeGroup

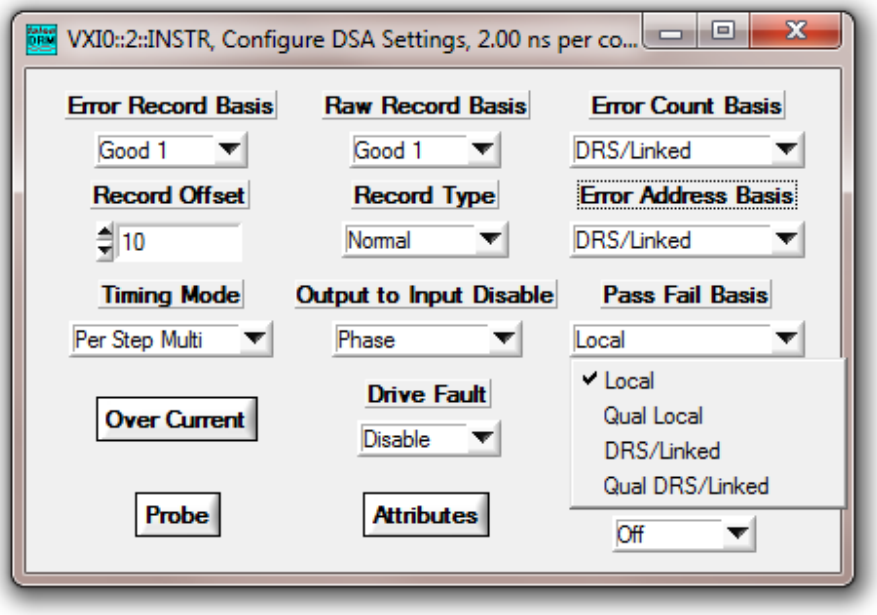
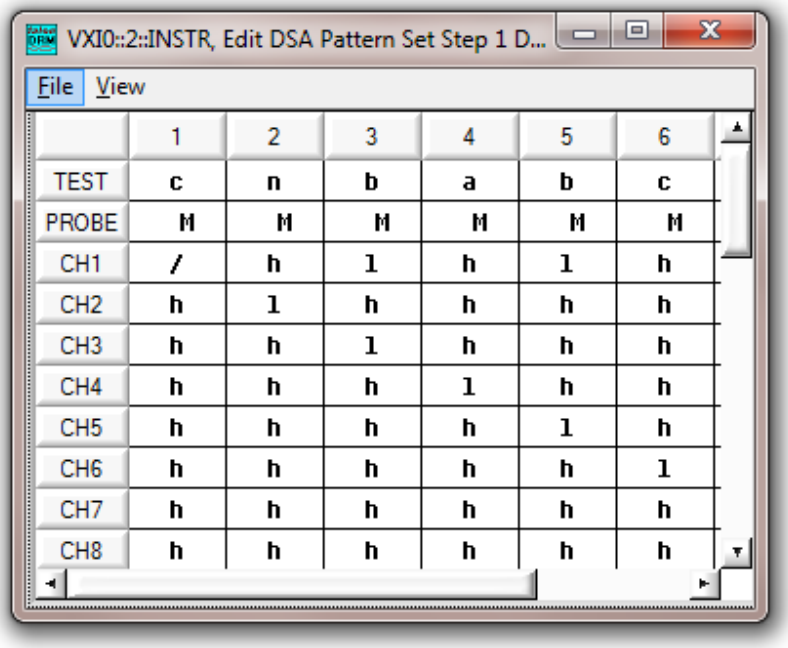


Figure 8-11: Setting the Pass/Fail Basis in the Configure DSA Settings Panel

A qualified Pass Fail Basis, in this case, is based on CONDEN (Condition Enable). CONDEN is programmed in the Pattern Data as follows [PnP: tat964_setPatternTestEnable.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setPatternTestEnable
- ARI: LoadPtgStepExpectedPatternBin, LoadPtgStepPatternChar



	1	2	3	4	5	6
TEST	c	n	b	a	b	c
PROBE	M	M	M	M	M	M
CH1	/	h	l	h	l	h
CH2	h	l	h	h	h	h
CH3	h	h	l	h	h	h
CH4	h	h	h	l	h	h
CH5	h	h	h	h	l	h
CH6	h	h	h	h	h	l
CH7	h	h	h	h	h	h
CH8	h	h	h	h	h	h

Figure 8-12: Setting the Pass/Fail Basis in the Configure DSA Settings Panel

The condition is programmed on the TEST row for each pattern (column). A "c" enables CONDEN. Patterns 1 & 6 have just CONDEN enabled. A "b" means that just BERREN is enabled. An "a" (for all) means that both CONDEN and BERREN are enabled, as on pattern 4.

Unlike for the Counting and Logging of Errors, Jumping and Halting is not based on the Step Record Mode. The same action is taken for all Step Record Modes as shown in Table 8-6.

Table 8-6: Cross-Reference of Step Record Mode to Pass Fail Basis

	Step Record Mode			
Pass Fail Basis↓	**None**	**Record Count**	**Record Error**	**Record Response**
Local	Insert Local Errors and PV* into the Pipeline	Insert Local Errors and PV* into the Pipeline	Insert Local Errors and PV* into the Pipeline	Insert Local Errors and PV* into the Pipeline
Qual. Local	Insert CONDEN Qual. Local Errors and PV* into the Pipeline	Insert CONDEN Qual. Local Errors and PV* into the Pipeline	Insert CONDEN Qual. Local Errors and PV* into the Pipeline	Insert CONDEN Qual. Local Errors and PV* into the Pipeline
DRS/Linked	Insert DRS/Linked Errors and PV* into the Pipeline	Insert DRS/Linked Errors and PV* into the Pipeline	Insert DRS/Linked Errors and PV* into the Pipeline	Insert DRS/Linked Errors and PV* into the Pipeline
Qual. DRS/Linked	Insert CONDEN Qual. DRS/Linked Errors and PV* into the Pipeline	Insert CONDEN Qual. DRS/Linked Errors and PV* into the Pipeline	Insert CONDEN Qual. DRS/Linked Errors and PV* into the Pipeline	Insert CONDEN Qual. DRS/Linked Errors and PV* into the Pipeline

* If Pass Valid (PV) is enabled

The "Pass Valid" mode is described below.

Jump test conditions are programmed on the Edit>Data Sequencer A/B>Sequence Steps panel [PnP: tat964_setSequenceJump; ARI: EndPtgStep]:

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setSequenceJump
- ARI: EndPtgStep

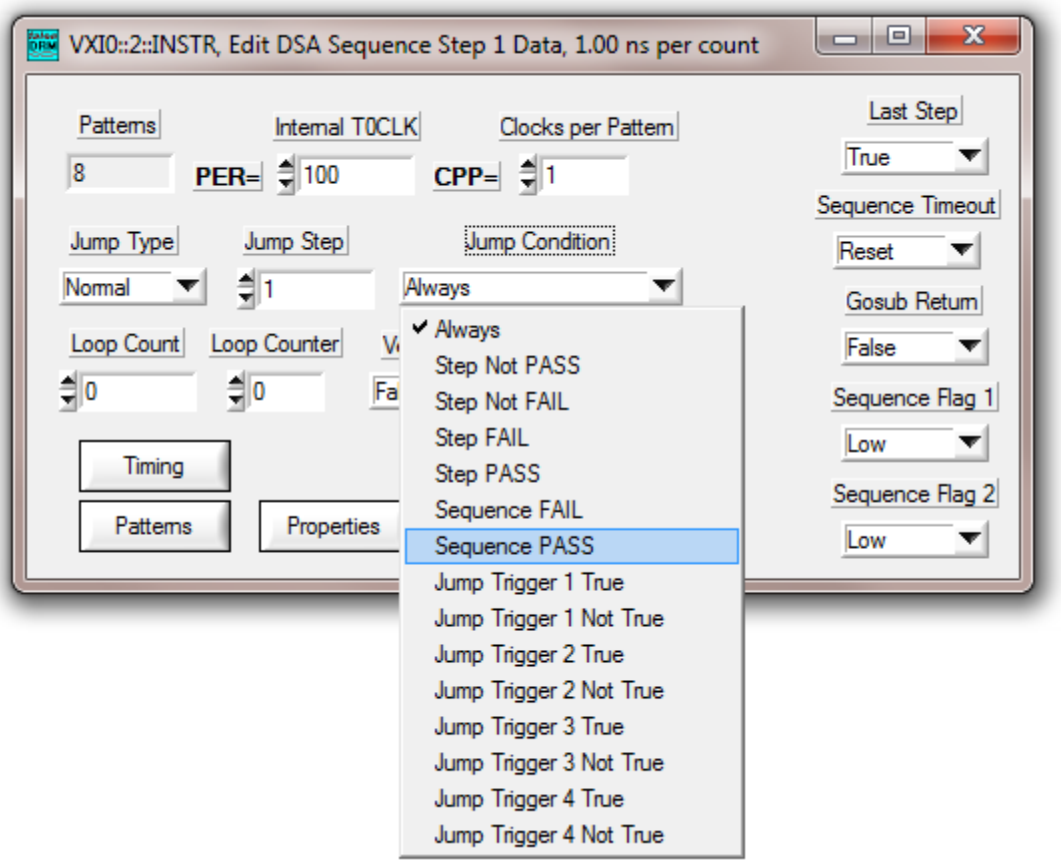


Figure 8-13: Setting the Jump Condition in the Edit DSA Sequence Step Panel

On this pull-down, you'll see that six Jump Conditions based on Pass and Fail.

The Halt Modes are Programmed on the Execute>DSA/DSB panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setHaltMode
- ARI: AssignPtgHaltMode

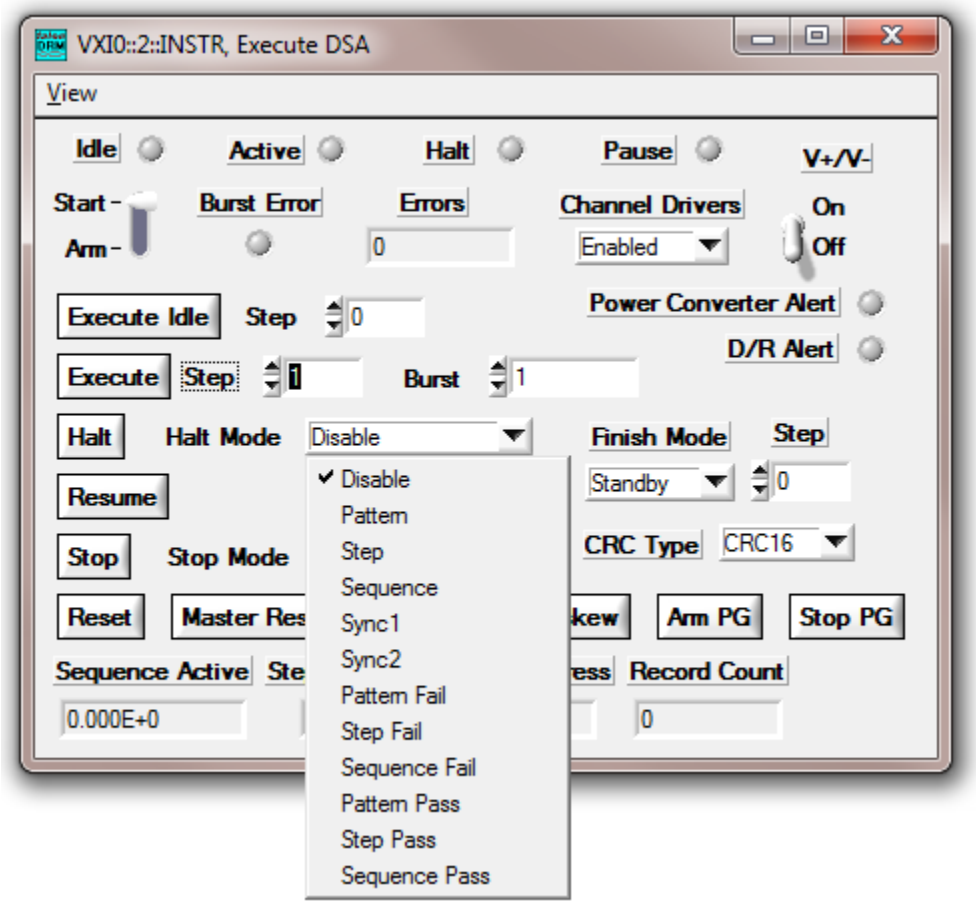


Figure 8-14: Setting the Halt Mode in the Execute DSA Panel

Here, you'll see six Halt Modes qualified either on Pass or Fail conditions.

What a Pass and Fail means is described in the next section called **Understanding Pass and Fail**.

Understanding Pass and Fail

The following items define the uses of Pass and Fail conditions:

- Pass and Fail are only used for Jumping and/or Halting (on Pass/Fail conditions).
- Halting on a Pass/Fail condition may be done on a Pattern, a Sequence Step or a Sequence (as though the Burst Count is set to 1).
- Jumping on a Pass/Fail condition may be done on a Sequence Step or Sequence (as though the Burst Count is set to 1).
- With default settings, Pass/Fail for a Sequence Step represents the cumulative results for that Sequence Step. But there are options that will be covered below.
- With the default settings, a Sequence Step will Fail if any Pattern Error (or Qualified Pattern Error) occurred during the Sequence Step. Similarly, a Sequence will Fail if any pattern Error (or

Qualified Pattern Error) occurred during the Sequence.

- A [simple] Pass says that there were no Pattern Errors (or Qualified Pattern Errors) that occurred during the Sequence Step (or Sequence). It is logically the complement of a Step Fail (or Sequence Fail).
- A "Valid Pass" is one where there were no Pattern Errors (or Qualified Pattern Errors) but it also says that there was at least one channel for each pattern (or Qualified Pattern) with an expect condition in the Sequence Step (or Sequence). This mode on operation is enabled by "Pass Valid Enable" (a static setting). This is set on the Config>Data Sequencer A/B>Settings panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setPassFailParameters
- ARI: AssignPtgPipelineParameters

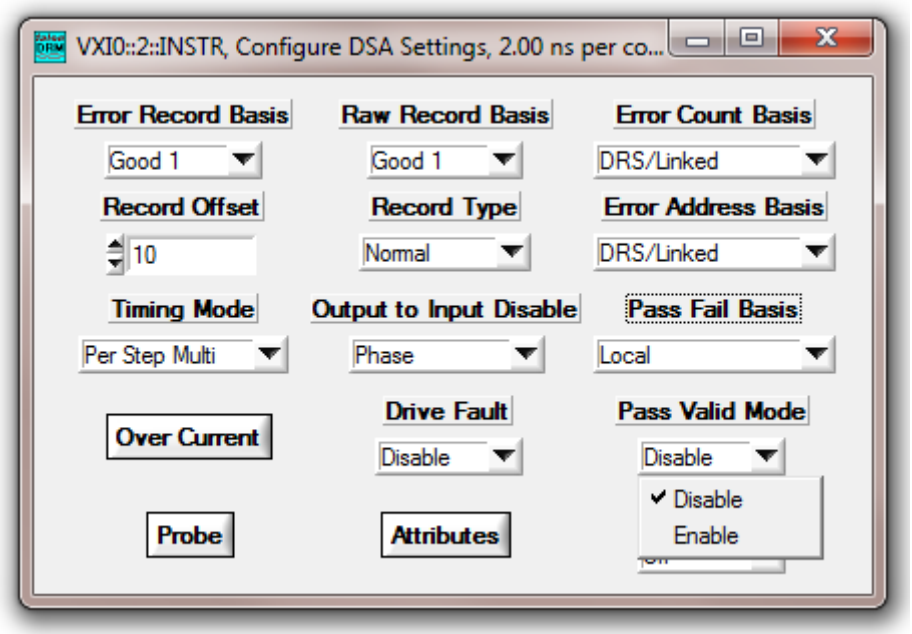


Figure 8-15: Setting the Halt Mode in the Execute DSA Panel

- If there is neither a Valid Pass nor a Fail, it is called "Indeterminate".
- "NOT Pass" is a Fail or Indeterminate
- "NOT Fail" is always the complement of a Fail
- A "Sequence Fail" is any channel Error that occurred during the Sequence (as though the Burst Count is set to 1).
- A "Sequence Pass" says that there were no channel Errors during the Sequence (as though the Burst Count is set to 1).
- The "Pass Valid Enable" option determines if it's a [simple] Pass or a Valid Pass.

Table 8-7 covers the above bullets:

Table 8-7: Truth Table Describing Pass and Fail

Pass Valid Mode	Valid Pass	Error	Qualified Pass/Fail Basis	CONDEN	Pass	Fail	NOT Pass	NOT Fail
X	X	H	L	X	L	H	H	L
L	X	L	L	X	H	L	L	H
H	H	L	L	X	H	L	L	H
H	L	L	L	X	L/I	L	H/I	H
X	X	X	H	L	H	L	L	H
X	X	H	H	H	L	H	H	L
L	X	L	H	H	H	L	L	H
H	H	L	H	H	H	L	L	H
H	L	L	H	H	L/I	L	H/I	H

Code: H=Yes/enabled/active; L=No/disabled/inactive; I=Indeterminate; X=don't care

As mentioned above, with the default settings, the cumulative results of Pass/Fail are used to make the final Jump decision. In particular:

- A cumulative Fail occurs if even one qualified pattern in the Seq. Step has an Error.
- A cumulative Pass can only occur if none of the qualified patterns in the Seq. Step has an Error. And if the Pass Valid Mode is enabled, none of the qualified patterns in the Seq. Step can have a Capture Fault for Pass to occur.

Pipelined handling of Pass/Fail with *default* settings:

Since the Error signal (and Pass Valid, if used) are delayed by the pipeline, these signals will not be aligned with the Jump Test made at the end of an individual Sequence Step (or at the end of a Primary Sequence).

Thus to make a correct Jumping Decision:

- The last N patterns before the end of the Sequence Step (or primary sequence) will not be included in the accumulated Pass/Fail decision.
- The last N patterns of the previous Sequence Step will be included. If these are not to be included in the accumulated Pass/Fail Jumping decision, then they need to not produce any Errors.

The easiest way to not produce any Errors (or Indeterminates) is to employ a Qualified Pass/Fail basis and disable CONDEN for these N Patterns. Using this method, Errors can still be: Recorded, Counted or Logged into the EAM if desired.

Note 1: A Capture Fault will generate an Error. This is discussed further in

Section 9, below.

Note 2: Standby or Idle will not produce any Errors (or Indeterminates).

Pass/Fail Option 1:

This option allows one to accumulate Pass/Fail across consecutive Sequence Steps.

This is programmed on the Edit>Data Sequencer A/B>Sequence Steps panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setSequencePassFailClear
- ARI: AssignPtgPipelineParameters

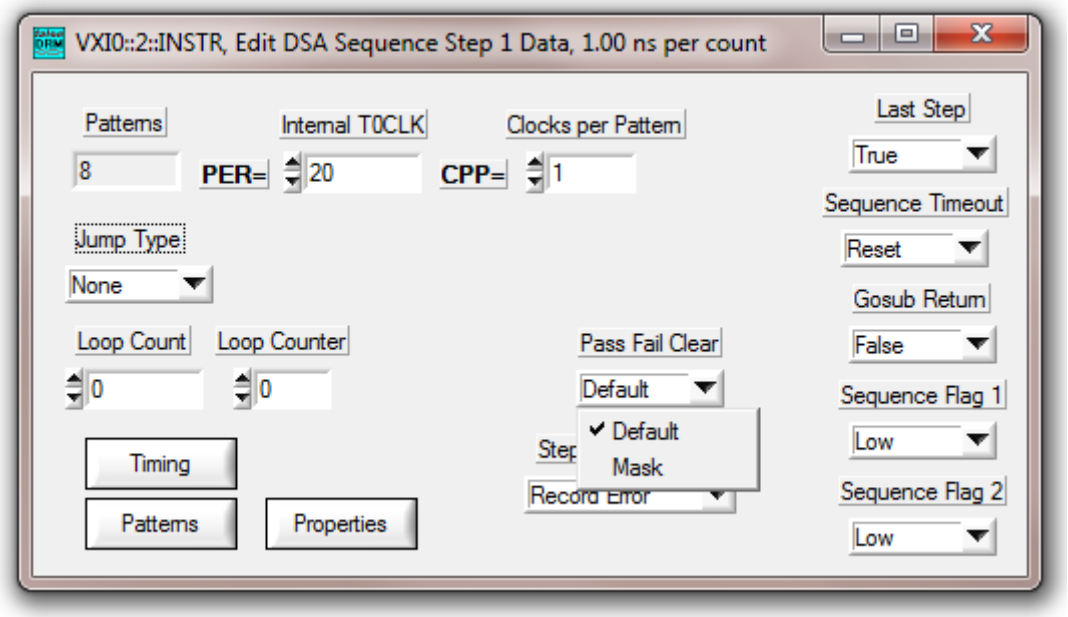


Figure 8-16: Setting the Pass Fail Clear Control in the Edit DSA Sequence Step Panel

"Default" is one of the *default* settings included, above. "Mask" means that at the end of this Sequence Step that the Pass/Fail accumulator will not be cleared.

Pass/Fail Option 2:

This option **disables** the Step Pass/Fail accumulator (but not for the Sequence Pass/Fail accumulator). Thus the Pass/Fail status on any particular pattern occurs exactly N patterns later, where N is the depth of the Pipeline. This is a static setting which is programmed on the Config>Data Sequencer A/B>Setting panel by clicking Attributes which brings up this panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setSequencerAttribute
- ARI: AssignPtgSequencerAttribute

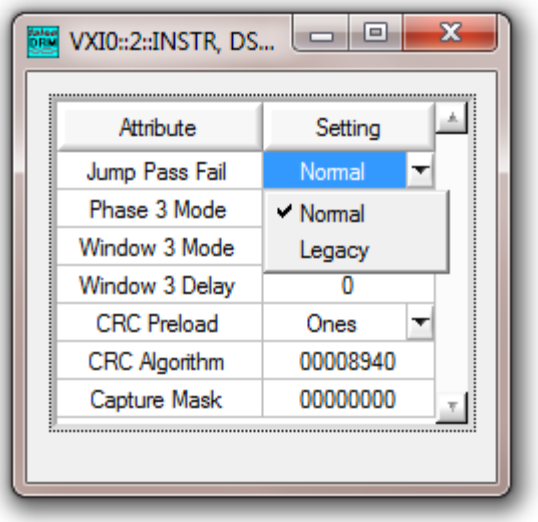


Figure 8-17: Setting the Jump Pass Fail Mode in the DSA Advanced Options Panel

"Normal" is one of the *default* settings included, above. Legacy enables Option #2.

This option is typically used when one is looping a single Pattern, looking for a Pass or Fail. Specifically, one could Jump on NOT Pass or NOT Fail and fall through on a Pass or Fail respectively. Option #1 (i.e., Pass Fail Clear = Mask) must be set on the Seq. Step when using this option. In some applications, this may be known as PATC WAIT.

This option requires that the Pipeline be "preconditioned."

Case 1: Jump on NOT Fail and fall through on a Fail

We want to "precondition" the pipeline with NOT Fail.

There are two options for clearing a pipeline of depth "N" to NOT Fail (not generate an Error):

a. If the Jump Basis is <u>not</u> qualified, use a Seq. Step with a jump to self for a count of "N". For the one Pattern in this step, have an expect condition which is known to NOT Fail (not generate an Error).
b. If the Jump Basis <u>is</u> qualified, use a Seq. Step with a jump to self for a count of "N" and set CONDEN <u>low</u> (e.g., "b" or "n") for the one pattern in this step (this will fill the pipe with NOT Fail).

Note: this case does not require the Pass Valid Mode to be used. But it may be used and will have no effect.

Case 2: Jump on NOT Pass and fall through on a Pass

We want to "precondition" the pipeline with NOT Pass.

There are two options for clearing a pipeline of depth "N" to NOT Pass (generate an error):

a. If the Jump Basis is <u>not</u> qualified, use a Seq. Step with a jump to self for a count of "N". For the one Pattern in this step, have an expect condition which is known to Fail (generate an Error).

b. If the Jump Basis is qualified, use a Seq. Step with a jump to self for a count of "N" and set CONDEN high (e.g., "c" or "a") for the one pattern in this step. For the one Pattern in this step, have an expect condition which is known to Fail (generate an Error).

To generate an Error, there must be at least one channel which has an "expect" which is the complement of the level that is driving that channel. One can, of course, drive one channel and expect the complement if that won't adversely affect the UUT (e.g. it's an unused channel).

But there's more to consider in this case:

Since we're falling through on a Pass, do we want it to be a Valid Pass? As described above, a "Valid Pass" is one where there were no channel Errors but it also says that there was at least one channel with an expect condition. If this additional "qualification" of a Pass is important, then the Pass Valid Mode also needs to be enabled.

Non-Pipelined handling of Pass/Fail with *default* settings:

Since the Error signal (and Pass Valid, if used) are not delayed by the pipeline, these signals will be aligned with the Jump Test made at the end of an individual Sequence Step (or at the end of a Sequence). Thus all the patterns in the Sequence Step (or Sequence) will be accumulated and none outside of the Sequence Step will be included. But there is one option as follows:

Pass/Fail Option 1:

This option allows one to accumulate Pass/Fail across consecutive Sequence Steps.

Pass/Fail Option 2:

Not useful in the non-pipelined case.

Additional Pipeline Information

- With a zero pipeline depth, Raw Error is used for Error. Raw Error comes directly from the channel-in logic. An Error is initially generated at the beginning of a pattern and then reflects the actual Error/non-Error after the final decision point.
- For a non-zero pipeline, Error is captured at the end of the Pattern period and then propagated as a pulse. By using a pulse, higher data rates can be accommodated. For F/W 0.21 and later, the Pulse Width is set by the S/W drivers for optimal operation. For 0.20 F/W and earlier, the Pulse Width is set by the user [PnP: tat964_setErrorPulseWidth; ARI: AssignPatTimeGroup].
- Error and Raw Error can be examined on Aux outputs.
- The pipeline depth needs to be set in the same in the Master and all coupled sequencers.

Valid Pass and Capture Fault

- A Valid Pass for a given pattern occurs if there is at least one channel with an Expect and a Window Capture Mode (an Open Edge, Close Edge or Window) but it does not verify that there is an appropriate window programmed to occur during the period.
- A Capture Fault Event occurs if there was an Expect without an appropriate Capture Mode (i.e. a Capture Mode of “none”) or an Expect and a Capture Mode but without appropriate Window edges within the Pattern period. Capture Faults automatically generate an Error for that Pattern. The channel(s) with a Capture Fault can be queried which may help narrow down where the Capture Fault occurred.

***Note**: Whereas a Valid Pass only requires one channel with an Expect and Capture Mode, a Capture Fault is generated for every channel that has an Expect with neither a Capture Mode nor an appropriate Window edge(s).*

Additional Halt Information

Halt modes are shown on the Execute panel.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setHaltMode
- ARI: AssignPtgHaltMode

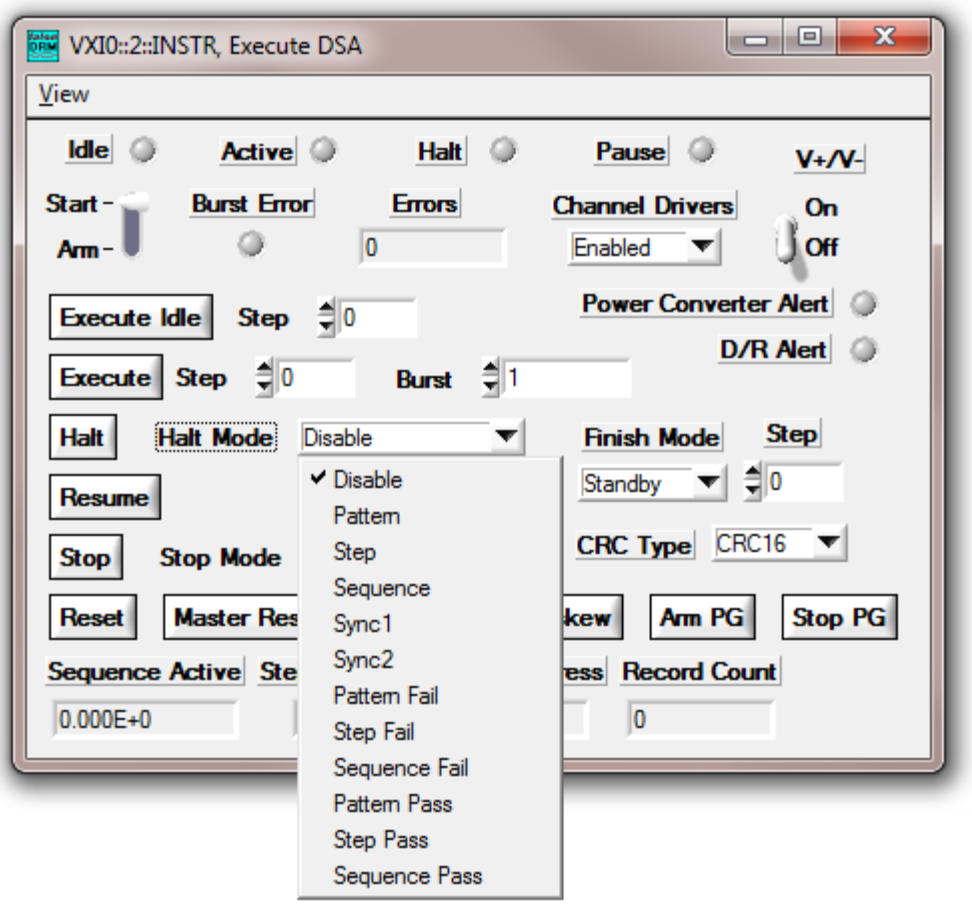


Figure 8-18: Setting the Halt Mode in the Execute DSA Panel

There are different types of Halt Modes. The first five are typically used for single stepping:

- Pattern
- Step
- Sequence
- Sync 1
- Sync 2

These latter two are actually Sync Pulses set on the Execute Panel by clicking “Set Sync”.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_setSyncEvent, tat964_setSyncParameters
- ARI: AssignPtgSyncPulse

Each Sync Pulse, can be set to start from the beginning of the Sequence or a specified Seq. Step and then have an Offset and a Length.

To use these first five, select the desired Halt Mode and then click “Halt” on this Execute panel [PnP: tat964_haltSequence; ARI: currently does not support the Halt command] before clicking “Execute”. Each time “Halt” is subsequently clicked the Halt will re-occur on the next Pattern, Step, etc. One can change the Halt Mode between clicks of “Halt”. For example, one may initially have a Sync Pulse on some desired pattern and then one could single step one pattern at a time, subsequently. If the Length of the Sync Pulse is N, then single pattern stepping will continue until N is exhausted.

Note: there is a max. data rate whereby one can do single stepping without corrupting the counting and/or logging of Errors. This limitation is defined in the Section 12.

When finished doing single stepping, click Resume.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_resumeSequence
- ARI: ResumePtg

The last six types of Halt Modes cover Halt Modes on various types of Pass/Fail conditions. In these modes, set the desired condition and then click “Execute”.

The relevant VXI*plug&play* API and ARI functions are:

- API: tat964_executeSequence
- ARI: ExecutePtg

Do not click “Halt” before “Execute”. Click Resume when you want to proceed to the next conditional Halt, if more are expected. As before, the Halt Mode may be changed between “Resumes”. To finish the Primary Sequence without any further Halts, change the Halt Mode to Disable.

Notes:

1. *The “Pass Fail Basis” applies to conditional Halting. Thus one can Halt on all Pattern Pass or Fail conditions or only those qualified with CONDEN.*
2. *When pipelined, these Halts occur the depth of the pipeline later.*
3. *In non-pipelined mode, there is a max. data rate where that one can do conditional Halting without corrupting the counting and/or logging of Errors as shown in Section 12*

Pipelined Depth Calculation

Capture Delay (CD) is the total time from a beginning of the first pattern to when the data can be captured for Jumping or Halting on Pass/Fail.

CD = (Local/BP delay) + (RO in ns) + (Error Resp. Delay) + (Period) + (11 Master Clocks) + 16ns.

Where:

- Local/BP delay:

	Independent	Linked	DRS
Local	14ns	16ns	
BP			1ns/DRM + 21ns

Pause and Halt Capabilities

Definitions:

- A “Halt” disables the System and Pattern Clocks at the end of the Pattern cycle after all Phases and Windows complete their action.
- A “Pause” disables the System and Pattern Clocks and freezes the Phases and Windows.
- A “Resume” generally de-asserts a Pause or Halt and allows the normal operation to continue….but there are exceptions.

Applications:

- A Halt can be used to:
  - Replicate the function of a System Clutch
  - Halt on Error
  - Halt on a pattern using a Sync pulse or external signal
  - Establish a breakpoint
  - Do single-stepping
  - Do Probe stepping
- A Pause can be used to:
  - Replicate the function of a Pattern Clutch
  - Pause the data output when doing a handshake.
  - Pause on a pattern at a Phase edge or with an external signal.
  - Insert a fixed wait time.
- An external Resume can be used as a handshake resume.

CPU Halt/Single-Stepping/Resume Operations:

- Single-stepping is a Resume/Halt combination.
- CPU Halt/Single Step Test Condition Choices (static selection):
  - None

  - Halt on a Pattern
  - Halt on the last Pattern of the Seq. Step (Branches and Loops are ignored.)
  - Halt on the last Pattern of the Sequence as though there were a Burst of 1
  - Halt on a Pattern where Sync Pulse 1 is Asserted
  - Halt on a Pattern where Sync Pulse 2 is Asserted
  - Halt on Pattern Error or CONDEN qualified Pattern Error
  - Halt on the last Pattern of the Seq. Step if there was a Step Failure or CONDEN qualified Step Failure
  - Halt on the last Pattern of the Sequence if there was a Burst Failure or CONDEN qualified Burst Failure
- Timing requirements for a Halt on Pattern Error, Step Failure or Burst Failure:
  - See the Jumping, Halting, Counting and Logging on Pass/Fail section for the detailed timing requirements and additional information
- The CPU can also perform a Resume at any time which can allow normal operation to proceed. This CPU resume can be used to:
  - Resume after single-stepping
  - Resume other types of Halt conditions
  - Resume any Pause condition

External Halt Operations:

- External Halt Test Sources (static selection):
  - None
  - Any Aux. Input (1 of 12)
  - Any TTLTRG Bus input (1 of 8)
  - Either ECL TRG Bus input (1 of 2)
  - Channel Test 1 (master channel test)
- External Halt Test Conditions (static selection):
  - High
  - Low
  - Rising Edge
  - Falling Edge
- External Halt Timing Considerations:
  - The external signal used to initiate the halt must occur in a timely

manner with respect to the Master Sequencer. To Halt in a pattern period, the “halt” signal must be provided ~10 Master Clocks and 40-60ns before the end of the desired pattern period (to be refined).

- Resume options:
  - CPU Resume
  - CPU Single-Step
  - Probe button
  - Trailing edge of an External Halt (used for System Clutch...see example below).
- Halt Edge Test Clear options (static selection):
  - The Halt Edge test flip-flop is cleared just before the beginning of the Sequence (option #1)
  - The Halt Edge test flip-flop is cleared just before the beginning of the Sequence or just before the beginning of each subsequent Sequence Step (option #2)
  - The Halt Edge test flip-flop is cleared just before the beginning of the Sequence or with a CPU Resume or Single Step (option #3).

Halt Examples:

- Halt on a Pattern Error:
  - Set the Single Step Type to Halt on Pattern Error
- Halt on Pattern 6 in Sequence Step 4 (like a breakpoint):
  - Set the Single Step Type to Halt on Sync1
  - Setup Sync Pulse 1 to begin a Sync Pulse on Pattern 6 in Sequence Step 4 with a duration of 1 pattern.
- Halt at the end of the Sequence
  - Set the Single Step Type to Halt on the last pattern of the Sequence
  - Start the Sequence
- Halt on an external Rising Edge signal occurring on the Aux. 2 Input:
  - Set the Halt Source to Aux. 2
  - Set for a Rising Edge Test Condition
  - Set Event Reset to Event
- Replicate a “System Clutch” function using the Aux. 8 input (an active high clutch):
  - Set the Halt Source to Aux. 8
  - Set a High Test Condition

Note: *A “high” on Aux. 8 causes a halt at the end of the Pattern and a “low”*

resumes (a Resume is not needed in this case). Thus the actual duration of the Halt will most likely be longer than the duration of the System Clutch.

Halt Notes:

- When Halted, the CPU may access the Data, Record and Probe memories.
- A Resume will be ignored while memory access is granted.
- An external Halt can only halt on a Pattern.
- When the timing requirements are not met for completing the capture of the response data prior to the Halt, the response data and related error counting/logging will be corrupted. See the Jumping, Halting, Counting and Logging on Pass/Fail section for the detailed timing requirements and additional information.

Pause Operations:

- A Pause operation is defined within a Sequence Step. Thus it can be constrained to occur only at particular times during the Sequence.
- Pause Test Condition Choices (settable in each Seq. Step):
  - None
  - Always
  - Pause Test 1 True or Not True
  - Pause Test 2 True or Not True
  - Phase 1 Rising Edge (RE)
  - Phase 1 Falling Edge (FE)
  - Phase 2 RE
  - Phase 2 FE
  - Phase 3 RE
  - Phase 3 FE
  - Phase 4 RE
  - Phase 4 FE
- Pause Test 1-2 Sources (static selection):
  - None
  - Any Aux. Input (1 of 12)
  - Any TTLTRG Bus input (1 of 8)
  - Either ECL TRG Bus input (1 of 2)
  - Channel Test 1 (master channel test)
- Pause Test 1-2 Conditions (static selection):

  - High
  - Low
  - Rising Edge
  - Falling Edge
- Pause Test 1-2 Resume Sources (static selection):
  - Any Aux. Input (1 of 12)
  - Any TTLTRG Bus input (1 of 8)
  - Either ECL TRG Bus input (1 of 2)
  - Channel Test 1 (master channel test)
- Phase Test 1-4 Resume Sources (static selection):
  - Any Aux. Input (1 of 12)
  - Any TTLTRG Bus input (1 of 8)
  - Either ECL TRG Bus input (1 of 2)
  - Channel Test 1 (master channel test)
- Pause Test 1-2 or Phase Test 1-4 Resume Conditions (static selection):
  - High
  - Low
  - Rising Edge
  - Falling Edge
- Pause Resume Options (settable in each Seq. Step)
  - None
  - Pattern Delay Timer 1 (used to Resume after a fixed delay)
  - Pattern Delay Timer 2 (used to Resume after a fixed delay)
  - Pattern Timeout Timer
- Pattern Delay/Timeout Timer (static settings):
  - Range: ~20 ns to ~43s
  - Resolution: 10ns
- Pause Timing Considerations:
  - An external signal used to initiate the pause must occur in a timely manner with respect to the Primary Sequencer. The “pause” signal must be provided ~10 Master Clocks and 40-60ns before the desired pausing point (to be refined).
  - Using a Phase edge to pause will have less delay but will still require a few Master Clocks which may vary depending on the placement of the Phase edge (to be refined)
- Pause Edge Test 1-2 Clear options (static selection):

  - Clear both Pause Edge test flip-flops just before the beginning of the Sequence (option #1)
  - Clear both Pause Edge test flip-flops just before the beginning of the Sequence and just before the beginning of each subsequent Sequence Step (option #2)
  - Clear both Pause Edge test flip-flops just before the beginning of the Sequence but only clear the selected Pause Edge Test flip-flops with a CPU Resume, Mated External Resume or the timeout of Pattern Delay Timer. (option #3).

- Phase Edge Test 1-4 Clear operation:
  - Clear all 4 Phase Edge Test flip-flop pairs just before the beginning of each pattern, with each CPU Resume but only clear the selected Phase Edge Test flip-flop pair with a Mated External Phase Resume
- Pause Test 1-2 Resume options:
  - CPU Resume
  - Mated External Resume (there's one for each Pause Test source)
  - Pattern Delay Timer timeout
- Phase Test 1-4 Resume options:
  - CPU Resume
  - Mated External Resume (there's one for each Phase Test source)
  - Pattern Delay Timer timeout

Pause Examples:

- A Handshake example: Pause on Phase 4 FE (right after the output data is formatted and before the input data is to be captured) of Sequence Step 3 (a one pattern Sequence Step) and Resume on the Rising Edge of Aux. 5:
  - In Sequence Step 3, set the Pause Test Condition: Phase 4 FE
  - Select for Resume Phase Test 4: Aux. 5
  - Select for Resume Phase Test 4: Rising Edge Test Condition
- Replicate a "Pattern Clutch" function using the Aux. 6 input (an active high clutch):
  - For all Sequence Steps within the Sequence, set the Pause Test Condition: Pause Test 1 True
  - Select for Pause Test 1: Aux. 6
  - Select for Pause Test 1: High

  Note: a "high" on Aux. 6 pauses and a "low" resumes (a Resume need not be programmed in this case.)
- Insert a 1s delay in one Pattern starting at the FE of Phase 4:

- Isolate the Pattern in one Sequence Step.
- In this Sequence Step, set the Pause Test Condition: Phase 4 FE
- Set Delay Timer 1 for 1s.
- Select the option in the Seq. Step which selects Delay Timer 1 for a Pattern Delay.

Pause Notes:

- Since a Pattern can have multiple Phases (using a Phase Trigger Type=0) and a CCP>1, multiple handshakes can be performed within a pattern.
- Since a Waveform can replace Phases 3 & 4, there can actually be multiple, irregularly spaced Handshakes within a Pattern.
- The Phase used for a Handshake may be output as a Handshake ready signal.
- The timing requirements for a Pause and Resume may preclude certain types of high-speed handshaking.
- The mated edge flip-flops used for Pause Test 1-2 Resume and Phase Test 1-4 Resume are automatically cleared when not paused.
- If the mated Resume is already satisfied (like with a level), the Pause will not occur.
- When Paused, the CPU cannot access the Pattern, Record or Probe memories.
- For 0.23 F/W, a Pause based on a level can only be cleared by removing the level causing the Pause . Changing the Pause Test Condition will not clear a Pause nor will a CPU Resume, a Pattern Delay Timeout or a Sequence Reset.
- For 0.23 F/W, the Phase Pause edge may occur as early as 0ns (T0) but not later than 16ns before the end of the period (using a 500MHz Master Clock).
- For 0.23 F/W, it is possible to record the correct results even when pausing. To do so, the observed Window decision edge must occur no later than 6ns after the Pause decision edge. Aux. outputs may be used to examine the timing relationship of the active Windows with respect to the Phase edge (or external signal) used to trigger a pause.
- For 0.23, the Window decision edge in pattern “n” must occur before any pause in pattern “n+1” by at least the amount of record offset in ns, in order to capture results correctly.
- For 0.23, the delay from a TTL Aux. Pause 1/2 Trigger Input or a Phase 1/2/3/4 Pause to an actual pause ~6-7ns. Likewise, the delay from Pause 1/2 Trigger Resume or a Phase 1/2/3/4 Resume is ~6-7ns.

Sequencer Operation

Introduction

The Pattern data describes both the Stimulus to be applied to the UUT and how the response from the UUT is to be examined (includes expect data if applicable) for each channel.

The “Sequencer” is a Mealy state machine that controls the flow of patterns.

The Sequencer is always running unless “Paused” or “Halted” (these terms are similar to Pattern and System Clutch although they have broader application).

The sequencer memory contains one or more of the following:

- A “Primary Sequence” is composed of one or more “Sequence Steps” and describes in total how all the Patterns will be applied to a UUT for a dynamic Stimulus/Response test.
- A “Standby Sequence” is a special Seq. Step which defines the power-up/reset state of the sequencer. It runs continuously and may output one pattern but response data is ignored.
- An “Idle Sequence” is a special Seq. Step that may be run before and/or after the Primary Sequence. The Idle Sequence run after a Primary Sequence may be different than the one run before a Primary Sequence. An Idle Sequence always runs continuously and may output one or more Patterns, but response data is ignored.

A “Finishing Sequence” is the Seq. Step that is run after the Primary Sequence. It may be an Idle Sequence or a Standby Sequence.

A “Sequence Step” defines a subset of the total number of Patterns to be applied to the UUT and defines the following properties:

- The location of the Data to be output and the number of Patterns to be output.
- The timing to be used for the Stim/Resp Data (T0CLK period, phase and window timing)
- The Clocks per Pattern (CPP) to be used for each Pattern in this Sequence Step the Clocks per Pattern may be from 1 to 256.
- Waveform selection control (4 bits) and Waveform Table to use (1 of 256)
- The Phase Trigger Type for each Phase (Pattern or System Clock) (4 bits). This is applicable when CPP is greater than 1.
- Sequence Flag state (2)
- Pattern Control Instructions

One or more Sequence Steps may be designated as a Subroutine.

The Pattern Control Instructions handle looping, branching, etc.

Pattern Control Instructions

The Pattern Controller defines the following:

- Jump Test conditions (4 bits)
- Jump Sequence Address (12 bits)
- Loop count (16 bits)
- Loop counter to use (4 b
- Control bits (1 bit each):
  - LSTSEQ (Last Seq. Step in the Primary Seq.)
  - CLOOP (Counted Loop)
  - SUBRT (Subroutine Jump) its)
  - RTN (Return...used on the last Seq. Step of a Subroutine)
  - VJ (Vector Jump)
  - Continue accumulating Seq. Timeout Time
- Pause Test Conditions...used for Handshaking and other purposes (4 bits)
- Pause Resume Options...used for Pattern Delay and Pattern Timeout (2bits)
- Record/Capture Type (2 bits)

The first 5 items above are used to control the execution of the Sequence Steps. Here are some examples:

- Unconditional Jumps:
  - Select a Jump Always Test Condition
  - Designate the Jump Sequence Address
- Conditional Jumps:
  - Select a Test Condition
  - Designate the Jump Sequence Address
- Counted Loops:
  - Set a Loop Count >0 (this sets the CLOOP bit).
  - Designate a loop counter to use (0 to 15)
  - Select a Jump Always Test Condition
  - Designate the Jump Sequence Address
- Counted Loop with Termination test:
  - Set a Loop Count >0 (this sets the CLOOP bit).
  - Designate a loop counter to use (0 to 15)
  - Designate the Jump Sequence Address

  - Select a Test Condition (when the condition is no longer true, execution advances to the next Sequence Step)

- Unconditional Subroutine Jump
  - Set SUBRT
  - Select a Jump Always Test Condition
  - Designate the Jump Sequence Address (First Sequence Step of the Subroutine)
- Conditional Subroutine Jump
  - Set SUBRT
  - Select the Test Condition
  - Designate the Jump Sequence Address (First Sequence Step of the Subroutine)
- Set LSTSEQ on the last Sequence Step of the Primary Sequence

Notes and Restrictions:

- Loops can be nested but only one can end on a given Sequence Step.
- Loop Counters can be re-used when exhausted (un-exhausted Loop Counters will continue where they left off when re-used). Note: There are 2 bits associated with each of the 16 loop counters. One bit, the Counter Active (CA) bit, gets set when the loop counter is used. Bit two, the Use Counter Once (UCO) bit, is programmed by the user. If UCO is set, the CA bit will **not** be reset when exiting the loop, thus the counter cannot be re-used once the count is exhausted. If not set, the CA bit is reset when the count is exhausted and the next sequence step begins.
- Loops can be done around one or more Sequence Steps and the group of sequence steps need not be consecutive…i.e. one or more intermediate Jumps could have occurred.
- A Counted Loop command is ignored if the Loop Count is zero.
- A “Jump Always” Jump condition is not recommended for looping a group of Sequence Steps….a Sequence Reset or Stop Looping command would be the only way to stop it.
- Subroutines cannot be nested.
- Subroutines may consist of multiple Sequence Steps which contain Loops and/or Jumps.
- The Sequence Step designated as the LSTSEQ may have Loops or Jumps to a subroutine. Upon completing the Loops or returning from a Subroutine, execution will proceed to the Finishing Sequence.
- All Jumps are to the Jump Sequence Address (JSA) unless a Vectored Jump is requested in which case the Jump will be to the

Sequence Address provided by the Vector Jump Address Memory.

Pattern Control Instruction Details

The following table describes what will happen under various conditions. It's a flow chart in a tabular form. The "Jump" column designates that the Test Condition was "True".

The nomenclature for the table is:

- JSA Jump Sequence Addr
- CA Loop Counter Active
- LC Loop Count from the Sequence Step
- LCD Loop Count Done
- BCD Burst Count Done
- BC Burst Continuous
- UCO Use Counter Once
- LAST A flag used to denote that a LSTSEQ had a jump to a SUBRT (thus the Return needs to be altered)

The general order of precedence is:

- Jump
- Return
- Last Sequence
- Next Sequence

	Jump	LSTSEQ	RTN	SUBRT	CLOOP	Action/Comments
1.	0	0	0	0	0	Proceed to the next Seq. Step
2.	1	0	0	0	0	Jump to JSA
3.	0	0	0	0	1	Proceed to the next Seq. Step
4.	1	0	0	0	1	• If LC=0, proceed to the next Seq. Step. • If LC>0 and CA=0, load the designated Loop Counter, set CA=1 and jump to JSA. • If CA=1 and NOT LCD, decrement the loop counter and Jump to JSA.

	Jump	LSTSEQ	RTN	SUBRT	CLOOP	Action/Comments
						• If CA=1 and LCD, reset CA if UCO=0 and proceed to the next Seq. Step.
5.	0	0	0	1	0	Proceed to the next Seq. Step
6.	1	0	0	1	0	• If NOT IN_SUB, set the IN_SUB flag, save the Return Seq. addr. and jump to JSA • Otherwise proceed to the next Seq. Step (also set a fault flag)
7.	0	0	0	1	1	Proceed to the next Seq. Step
8.	1	0	0	1	1	• If LC=0, proceed to the next Seq. Step. • If LC>0 and CA=0 and NOT IN_SUB, load the designated Loop Counter, set CA=1, set the IN_SUB flag, save the Return Seq. addr. and jump to JSA. • If CA=1 and NOT LCD, decrement the loop counter and jump to JSA. • If CA=1 and LCD, reset CA if UCO=0 and proceed to the next Seq. Step. • Otherwise proceed to the next Seq. Step
9.	0	0	1	0	0	• If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise proceed to the next Seq. Step (also set a fault flag)
10.	1	0	1	0	0	Jump to JSA (also set fault flag)
11.	0	0	1	0	1	• If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise proceed to the next Seq. Step (also set a fault flag)
12.	1	0	1	0	1	• If LC=0 and IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • If LC>0 and CA=0, load the designated Loop Counter, set CA=1 and jump to JSA.

	Jump	LSTSEQ	RTN	SUBRT	CLOOP	Action/Comments
						• If CA=1 and NOT LCD, decrement the loop counter and jump to JSA. • If CA=1 and LCD, reset CA if UCO=0; also if IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise proceed to the next Seq. Step (also set a fault flag)
13.	0	0	1	1	0	• If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise proceed to the next Seq. Step (also set a fault flags)
14.	1	0	1	1	0	• If NOT IN_SUB, set the IN_SUB flag, save the Return Seq. addr. and jump to JSA • If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag (also set a fault flags)
15.	0	0	1	1	1	• If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise proceed to the next Seq. Step (also set a fault flags)
16.	1	0	1	1	1	• If LC=0 and IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • If LC>0 and CA=0 and NOT IN_SUB, load the designated Loop Counter, set CA=1, set the IN_SUB flag, save the Return Seq. addr. and jump to JSA. • If CA=1 and NOT LCD and NOT IN_SUB, set the IN_SUB flag, save the Return Seq. addr., decrement the loop counter and jump to JSA. • If CA=1 and LCD reset CA if UCO=0; also if IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise, if LC>0, CA=0 and INSUB, jump to the return Seq. and clear the INSUB flag.

	Jump	LSTSEQ	RTN	SUBRT	CLOOP	Action/Comments
						• Otherwise proceed to the next Seq. Step (also set a fault flag)
17.	0	1	0	0	0	The Seq. loops or finishes
18.	1	1	0	0	0	Jumps to JSA
19.	0	1	0	0	1	The Seq. loops or finishes
20.	1	1	0	0	1	• If LC=0, the Seq. loops or finishes. • If LC>0 and CA=0, load the designated Loop Counter, set CA=1 and jump to JSA. • If CA=1 and NOT LCD, decrement the loop counter and jump to JSA. • If CA=1 and LCD reset CA if UCO=0; also the Seq. loops or finishes. • Otherwise, the Seq. loops or finishes
21.	0	1	0	1	0	The Seq. loops or finishes
22.	1	1	0	1	0	• If NOT IN_SUB, set the IN_SUB flag, set the LAST flag and jump to JSA • Otherwise, the Seq. loops or finishes. (also set a fault flag)
23.	0	1	0	1	1	The Seq. loops or finishes
24.	1	1	0	1	1	• If LC=0 the Seq. loops or finishes • If LC>0 and CA=0 and NOT IN_SUB, load the designated Loop Counter, set CA=1, set the IN_SUB flag, set the LAST flag and jump to JSA. • If CA=1 and NOT LCD and NOT IN_SUB, set the IN_SUB flag, set the LAST flag, decrement the loop counter and jump to JSA. • If CA=1 and LCD reset CA if UCO=0; also the Seq. loops or finishes. • Otherwise, the Seq. loops or finishes
25.	0	1	1	0	0	• If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag.

	Jump	LSTSEQ	RTN	SUBRT	CLOOP	Action/Comments
						• Otherwise, the Seq. loops or finishes (also set a fault flag)
26.	1	1	1	0	0	Jumps to JSA (also set a fault flag)
27.	0	1	1	0	1	• If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise, the Seq. loops or finishes (also set a fault flag)
28.	1	1	1	0	1	• If LC=0 and IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • If LC>0 and CA=0, load the designated Loop Counter, set CA=1 and jump to JSA. • If CA=1 and NOT LCD, decrement the loop counter and jump to JSA. • If CA=1 and LCD reset CA if UCO=0; also if IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise, the Seq. loops or finishes. (also set a fault flag)
29.	0	1	1	1	0	• If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise, the Seq. loops or finishes (also set a fault flag)
30.	1	1	1	1	0	• If NOT IN_SUB, set the IN_SUB flag, set the LAST flag and jump to JSA • If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag (also set a fault flag)
31.	0	1	1	1	1	• If IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise, the Seq. loops or finishes (also set a fault flag)
32.	1	1	1	1	1	• If LC=0 and IN_SUB, jump to the Return Seq. and clear the IN_SUB flag.

	Jump	LSTSEQ	RTN	SUBRT	CLOOP	Action/Comments
						• If LC>0 and CA=0 and NOT IN_SUB, load the designated Loop Counter, set CA=1, set the IN_SUB flag, set the LAST flag and jump to JSA. • If CA=1 and NOT LCD , decrement the loop counter and jump to JSA. • If CA=1 and LCD reset CA if UCO=0; also if IN_SUB, jump to the Return Seq. and clear the IN_SUB flag. • Otherwise, if LC>0, CA=0 and INSUB, jump to the return Seq. and clear the INSUB flag • Otherwise, the Seq. loops or finishes (also set a fault flag).

T964 VXI Backplane Trigger Bus

Trigger Bus description:

TTLTRG Bus (8 VXI backplane signals): normally active low

ECLTRG Bus (2 VXI backplane signals): normally active high

Trigger Bus Applications:

- Inter-module communications (for Sequencers configured in a Master/Slave configuration):
    - Communicating a Trigger for a Conditional Jump
        - Error (with or w/o Pass Valid)
        - Channel Test
    - Communicating a Synchronization Signal from the Primary Sequencer that all the coupled Synchronizers can check themselves against.
    - Communicating a Sequence Reset to all coupled sequencers: primarily used for re-synchronizing coupled Sequencers
    - Communicating a Master Reset to all coupled sequencers
    - Communicating a Driver Disable to all coupled sequencers that can disable all the channel drivers at once.

- Receive a signal from another instrument in the VXI chassis (needs to go to the T940 Primary Sequencer):
    - External Start and/or Stop
    - External Jump
    - External Halt, Pause or Resume

- Trigger another instrument in the VXI chassis. Possible signal choices within the T940 are:
    - A sync pulse
    - A Seq. Flag
    - An Aux. Input
    - Idle Active
    - Seq. Active
    - A Channel Test

Normal Operation:

- For inter-module communication, the “active high” and “active low” state of the backplane bus is handled automatically.
- For communications with other instruments, the “active high” or “active low” state of the bus must be considered when:
    - Receiving a signal from another instrument
    - Providing a signal to another instrument
- The signals driving out onto these buses or coming in from these buses can be inverted.

Normal Operation Example:

- To do a Jump Test on an Aux. Input located on a Slave Sequencer:
    - Select the TRG Bus to be used and select the Aux. signal to drive it.
    - Invert the output, if the Aux. signal is active low.
    - On the Master, select the same TRG Bus signal and use a “High” or “Rising Edge” test condition.
- To do a Jump Test on an input Channel (Channel Test):
    - Select the Channel Test to be used (1 of 4) on the Master or Slave Sequencer which covers that channel.
    - Pick the desired channel and unmask the channel test for that channel.
    - Set the expect level for the channel to be the level desired for a trigger.
    - Select the TRG Bus to be used and select the Channel Test signal to drive it.
    - On the Master, select the same TRG Bus signal and use a “High” or “Rising Edge” test condition.

Advanced Operation Examples:

- To do a Jump Test on the OR of several Channels:

  - Select the Channel Test to be used (1 of 4) on the Master and/or Slave Sequencer for the channels to be ORed.
  - Unmask Channel Test for these channels.
  - Set the expect level for each channel to be the level desired for a trigger.
  - Select the TRG Bus to be used and select the Channel Test signal to drive it.
  - Do a Jump Test On the Master, select the same TRG bus signal and use a "High" or "Rising Edge" test condition.

- To do a Jump Test on the AND of several Channels:
  - Select the Channel Test to be used (1 of 4) on the Master and/or Slave Sequencer for the channels to be ANDed.
  - Unmask Channel Test for these channels.
  - Set the expect level for each channel to be the complement of the level desired for a trigger.
  - Select the TRG Bus to be used and select the Channel Test signal to drive it.
  - On the Master, select the same TRG bus signal and use a "Low" or "Falling Edge" test condition.

Notes:

1. Local versions of the TRG signals are used when DSA and DSB on the same module are linked. Thus Channel Tests will function as above without using the backplane TRG Bus lines.
2. The TTLTRG Bus has a weak pullup, thus the risetime will be quite slow. As such, the trailing edge of an active low signal will be delayed up to 40ns more than the leading edge. Triggering on a falling edge is recommended when delay is a concern.
3. There is a way to do AND/OR or OR/AND channel tests between groups of channels on different sequencers.
4. Since Aux Inputs can drive TRG Bus lines, they can be ORed. ANDed or even combined with Channel Test signals in various ways. For example, an Aux. input could be a qualifier for a Channel test.
5. When a TRG Bus line is configured to drive out an "ERROR", a "Synchronization Signal", a "Sequence Reset", a "Master Reset" or "Driver Disable" signal, the corresponding input of these signals to the Master will be automatically configured.
6. The combination of up to 4 TRG Bus signals may be used to formulate a 1 of 16 "vector" to the sequencers so one can do a vectored jump to 1 of 16 locations based on the state of these four signals.

Appendix A
Glossary of Terms and Acronyms

This appendix includes a list of many of the terms and acronyms used in this manual.

A16/A24/A32	The VXI address is segmented into three separate areas by a group of VXI signals called the address modifiers (AM0-AM5). These three areas are called A16, A24 and A32. Every VXI module is mapped into 64 bytes of the A16 memory. VXI modules, in addition, may request additional memory map space in the A24 or A32 space. The DRM maps the Sequencers and Driver/Receiver board's registers into the A24/A32 space.
ADE	Application Development Environment
ARGCS	Agile Rapid Global Combat Support
Assert	Rising edge of a Phase
ARI	Application Resource Interface
ATLAS	Abbreviated Test Language for All Systems
AUX	Auxiliary
Bipolar	Sources and sinks current (single-ended)
CAD	Computer Aided Design
CPP	Clocks per Pattern
CH	Channel (signal)
Channel Test	Allows any channel of the installed Driver/Receiver boards to be used as a test input (TEST1 or TEST2). It can also be used with other Channel tests to form a Vector Jump Index. It can even be used to start or stop a sequence.
Close	The falling edge of a Window
Comparator	Compares an input signal with a voltage reference level
Coupled	Used to describe a DRM sequencer that is included in a DRS chain
CMH	Commutating Voltage High
CML	Commutating Voltage Low
CVH	Compare Voltage High
CVL	Compare Voltage Low
DB	Digital Board

Differential	A pair of signals representing a state when one is at a high level the other is at a low level.
DR1	Driver/Receiver Board Type ‘1’ 32 channel LVTTL I/O.
DR2	Driver/Receiver Board Type ‘2’ 32 channel LVDS I/O.
DR3E	Driver/Receiver Board Type ‘3E’ 32 channel programmable I/O.
DR4	Driver/Receiver Board Type ‘4’ 48 channel programmable I/O.
DR7	Driver/Receiver Board Type ‘7’ 32 channel RS-422/485 I/O.
DR8	Driver/Receiver Board Type ‘8’ 32 channel TTL I/O.
DR9	Driver/Receiver Board Type ‘9’ 24 channel programmable I/O.
DRA	Driver/Receiver Board A
DRB	Driver/Receiver Board B
DRM	Digital Resource Module
DRS	Digital Resource Suite. A DRS is two or more adjacent DRMs synchronized together to form a digital test system with more than 64 channels.
DSA	Digital Sequencer A
DSB	Digital Sequencer B
DUT	Device Under Test
DVH	Drive Voltage High
DVL	Drive Voltage Low
ECL	Emitter-Coupled Logic
ECL TRG	VXI ECL trigger
EN	Enable
Error	A channel error is determined by comparing the channel response to the expect/mask conditions of the Pattern data.
GND_REF	Ground reference output from the pin electronics devices
Good “0”	A signal generated when an input signal is less than CVL
Good “1”	A signal generated when an input signal is greater than CVH
Idle	An execution state that outputs the entire pattern set of a specified step after a sequence burst. Pattern and record memory cannot be accessed by the user.
Indeterminate	An “indeterminate” PASS/FAIL condition occurs if there is neither a valid PASS nor a FAIL. This is discussed in more detail in the **Jumping, Halting, Counting and Logging Errors** section in **Chapter 8**.
I/O	Input/Output
Jump	Used to “Jump” out of the normal sequential flow of Sequence Steps to another Sequence Step. The jump occurs at the end of the sequence step after all of the patterns have been output.

JTAG	Joint Test Action Group, IEEE 1149.1: serial interface that allows the serial PROM to be reloaded for in-field system upgrades.
CBUS	An internal Control Bus connecting the VXI Bridge to the Data Sequencers and the Driver/Receiver board's Control Logic
l/s	Liters per second (flow rate measurement)
LED	Light Emitting Diode
Linked Mode	DSA and DSB operating synchronously within a DRM
LVDS	Low-Voltage Differential Signaling
LVTTL	Low-Voltage TTL
MCLK	Master Clock
Open	The rising edge of a Window
PAT_CLK	Pattern Clock
Pass Valid	A signal which conveys a Pass Valid Mode setting. If Pass Valid is enabled for a DRS, then the Pass Valid signal must be coupled between DRMs via the TTL or ECL TRG bus. The ECL TRG Bus is recommended for data rates greater than 10 MHz. This is discussed in more detail in the **Jumping, Halting, Counting and Logging Errors** section of **Chapter 8**. See also "Valid Pass", below.
Pattern	One stimulus applied to and/or one response received from the UUT. Sometimes called a Word or Vector.
Pattern Set	A Pattern Set is one or more consecutive channel patterns
PBUT	Probe button input signal to the Sequencer for support of remote probe operations
PMODE	Control signal from the Sequencer for support of remote probe operations
Primary	Used to describe sequencer A on the DRM that provides all the timing for the sequencers that are part of the DRS chain. Sequencer B can be coupled to the new chain, terminate the previous chain (Primary Terminator) or run independently from the chain. The primary module must be located in the rightmost slot position in the VXI chassis relative to the DRMs that will be coupled.
PWR	Front panel connector for optional external power on the DR3e
Reference	A programmable DC voltage
Return	Falling edge of a Phase
RTCASS	Reconfigurable Transportable Consolidated Automated Support System
Standby	An execution state that outputs the first pattern of a specified step after a sequence burst. Pattern and record memory can be accessed by the user.

Secondary	Used to describe the DRMs located between the primary and terminating modules that pass the timing signals to the DRM in the next higher slot position. Individual sequencers can either be coupled or run independently from the primary module.
Sequence	A sequence is an ordered list of stimulus/response actions consisting of one or more sequence steps.
Sequence Burst	An execution of one or more patterns.
Sequence Step	A sequence step is a single element of a sequence. A sequence step selects a timing set, pattern set, loop count, jump condition and control flags.
Slew Rate	Rate of change of an output transition (typically in V/ns)
Terminator	Used to describe the DRM in the leftmost position of the DRS chain. One or both sequencers can be coupled to the DRS chain.
Timing Set	A timing set is the structure that is created that defines the stimulus/response timing.
TO_CLK	System Clock
TPS	Test Program Set
TTL TRG	VXI TTL Trigger
UR14	Utility Resource Board Probe and 32 channel open collector I/O
UUT	Unit Under Test
V+	Positive supply voltage provided by the Power Converter which is used to power the Pin Electronics devices. In addition, external power may be applied to V+ via an optional front panel power connector.
V-	Negative supply voltage provided by the Power Converter which is used to power the Pin Electronics devices. In addition, external power may be applied to V- via an optional front panel power connector.
Valid Pass	A Valid Pass is one where no channel errors were detected but there must be at least one valid pattern expect code for each pattern in the sequence step. This is discussed in more detail in the **Jumping, Halting, Counting and Logging Errors** section of **Chapter 8**.
VADDR	(VXI Address Bus) The 32 bit backplane address bus
VBB	ECL Input Threshold (~ -1.3V)
VCC	Positive supply voltage for the TTL or LVTTL drivers/receivers
VCTRL	(VXI Control Bus) The backplane control bus
VDATA	(VXI Data Bus) The 32 bit backplane data bus
VIH	Voltage Input High Level (min.)
VIL	Voltage Input Low Level (max.)
VOH	Voltage Output High Level (min.)

VOL	Voltage Output Low Level (max.)
VXI	VME Extensions for Instrumentation
VXI_INT	(VXI Interrupt Signals) The backplane interrupt signals
WCEM	Microsoft Windows CIIL Emulation Module

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Appendix B
DR1 Driver/Receiver Board

DR1 Features

- Channels: 32 single-ended LVTTL
- Relay Isolation on all I/O and AUX channels
- Selectable resistive input load to VCC (+3.3 V), ground or both
- Direct or 50 ohm selectable output impedance
- Auxiliary channels
  - Four LVTTL with selectable output impedance and resistive input load
  - Four LVTTL
  - Four ECL (single ended or differential)

Front Panel Connectors

The front panel of the DR1 Driver/Receiver is shown in Chapter 3.

Block Diagram

This section describes the basic hardware configuration of the DR1 Driver/Receiver (DRA or DRB).

The DR1 is comprised of four major logic sections as shown in Figure B-1.

- Auxiliary Driver & Receiver I/O
- DR1 Driver & Receiver I/O
- Control Logic
- Firmware & NV Data

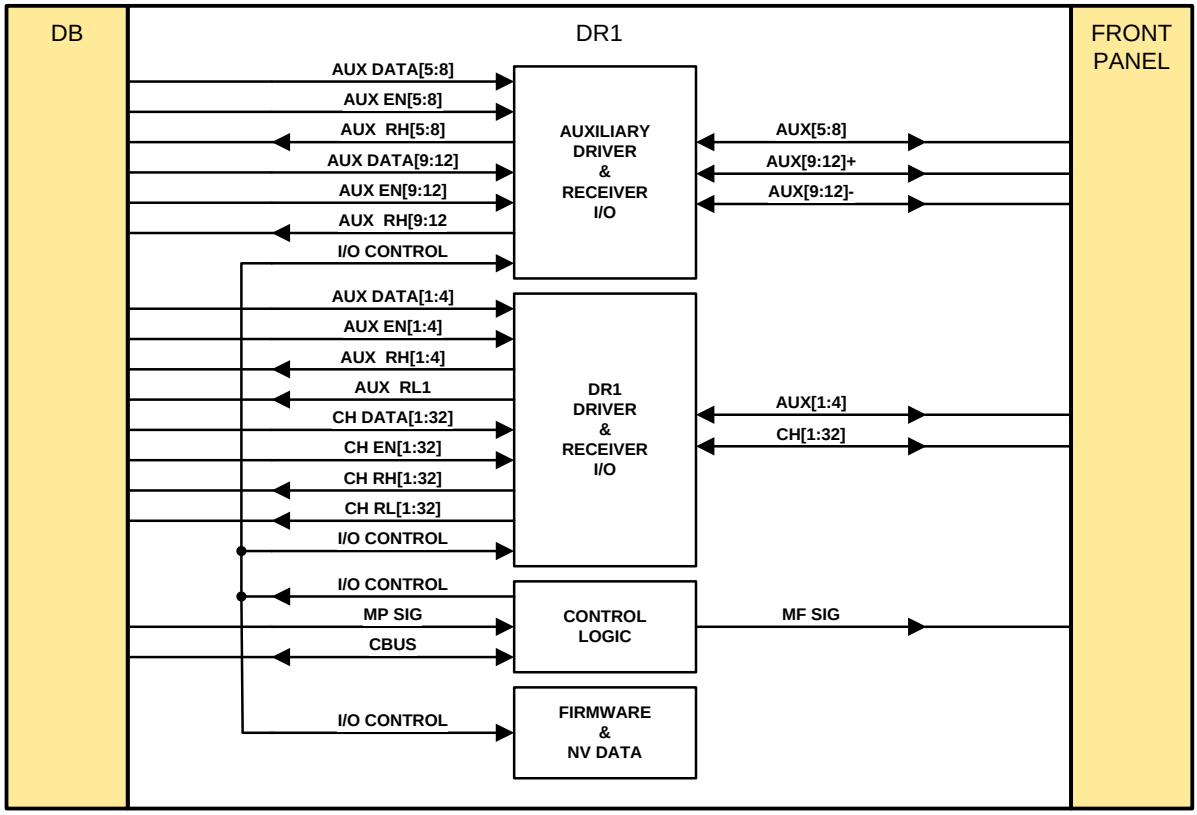


Figure B-1: DR1 Driver/Receiver Block Diagram

Auxiliary Driver & Receiver I/O

Figure B-2 illustrates the configuration and control of AUX5-8 (LVTTL) and AUX9-12 (ECL) Driver & Receiver I/O.

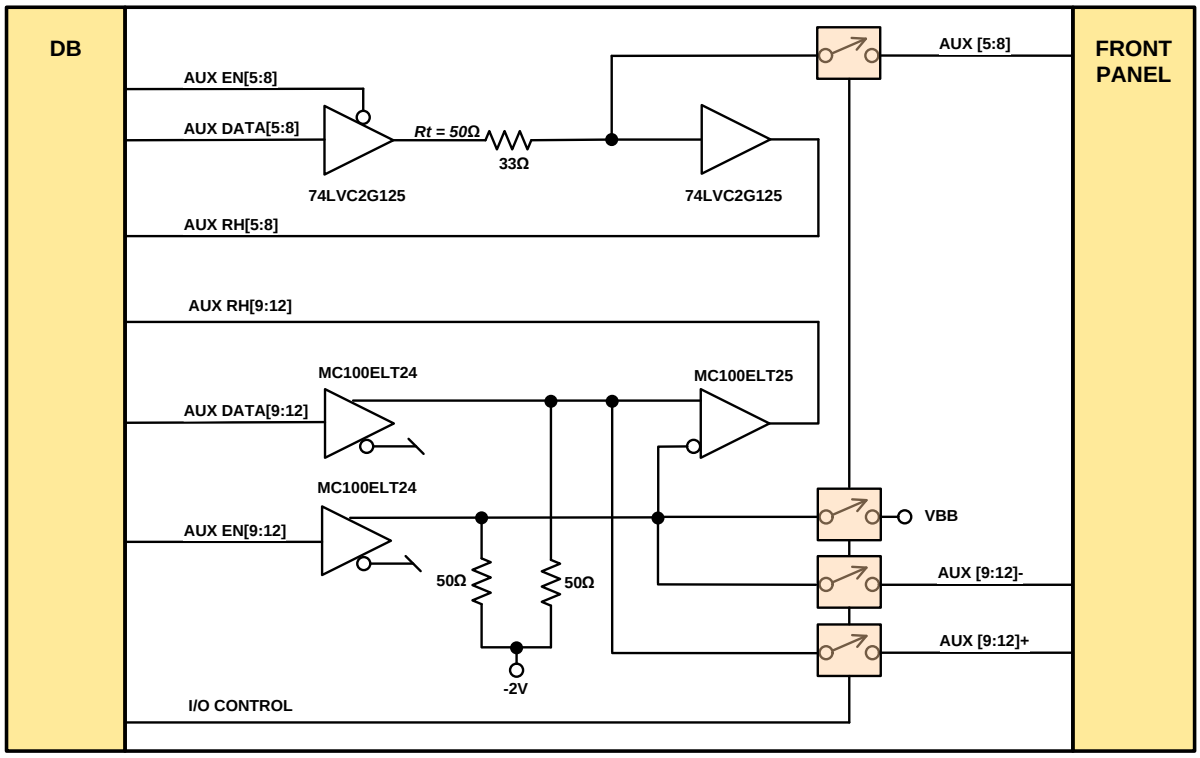


Figure B-2: Auxiliary Driver & Receiver I/O Block Diagram

Signal Descriptions

AUX EN[5:8]	Auxiliary Enable outputs from the Data Sequencer to the LVTTL output buffers.
AUX DATA[5:8]	Auxiliary Data outputs from the Data Sequencer to the LVTTL output buffers.
AUX RH[5:8]	Auxiliary Response High inputs to the Data Sequencer from the LVTTL input buffers.
AUX RH[9:12]	Auxiliary Response High inputs to the Data Sequencer from the ECL input buffers.
AUX DATA[9:12]	Auxiliary active high Data outputs from the Data Sequencer to the ECL output buffers.
AUX EN[9:12]	Auxiliary active low Data outputs from the Data Sequencer to the ECL output buffers.
EN 9-12	Auxiliary Enable outputs from the Data Sequencer to the ECL output buffers.
I/O CONTROL	Signals used to control isolation relays and ECL bipolar/differential mode.
AUX [5:8]	Four LVTTL signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
VBB	ECL input threshold (~ -1.3V).
AUX [9:12]-	Four negative differential signals used to input or output test signals. See **Configuring the AUX Channels** in

Chapter 5.

AUX [9:12]+ Four bipolar/positive differential signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.

DR1 Driver & Receiver I/O

Figure B-3 illustrates the configuration and control of the DR1 Driver & Receiver I/O (LVTTL).

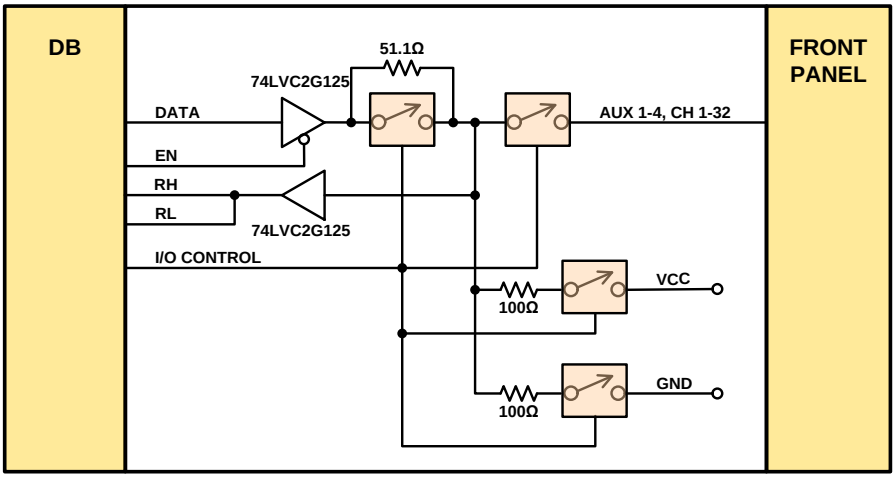


Figure B-3: DR1 Driver & Receiver I/O Block Diagram

Signal Descriptions

DATA	Channel and auxiliary data output signals from the Data Sequencer to the LVTTL output drivers.
EN	Channel and auxiliary enable output signals from the Data Sequencer to the LVTTL output drivers.
RH	Response High input signals to the Data Sequencer from the LVTTL input receivers. 1 = good 1, 0 = good 0.
RL	Response Low input signals to the Data Sequencer from the LVTTL input receivers. 0 = good 0, 1 = good 1.
AUX 1-4	Four LVTTL signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
CH 1-32	These are UUT Bi-directional LVTTL I/O channels from the DR1 Drivers and Receivers
VCC	LVTTL Power (~3.3V).

Control Logic

The control logic contains the registers, memory and logic that allow the digital board to interface and configure the hardware.

Signal Descriptions

I/O CONTROL	Signals used to control isolation, termination, NV data and load relays
MP SIG	Multi-Purpose signal from the data sequencer.
CBUS	An internal Control Bus connecting the digital board to the Driver/Receiver board.
MF SIG	Multi-Function signal output to the PWR connector.

Firmware & NV Data

The Control Logic firmware is loaded via a serial PROM on power up or VXI Reset. The firmware is field-upgradeable using our supplied loader utility. Nonvolatile data (serial number, assembly revision is stored in an on-board EEPROM.

Signal Descriptions

I/O CONTROL	Signals used to program firmware and NV DATA.

DR1 Characteristics

Table B-1: DR1 Characteristics

Description	Characteristics
Digital I/O Type	LVTTL (74LVC2G125)
Channels	32 single-ended (SE) per I/O board Per channel relay isolation
Output Voltage	V_{OL}: 0.55 V (max) V_{OH}: 2.4 V (min)
Output Drive Current (typical)	Source/Sink: 24 mA
Output Impedance (Program selectable per pin)	Direct or 100 Ω Series (-001) Direct or 50 Ω Series (-002)
Input Voltage	V_{IL}: 0.8 V (max) V_{IH}: 2.0 V (min)
Input Impedance (Program selectable per pin)	100 Ω pull-up to VCC (+3.3 V) 100 Ω pull-down to ground (Ch1-32, Aux1-4 only)
Skew (Channel-to-Channel)	< 3 ns (drive and compare)
Auxiliary I/O Channels (per I/O board)	LVTTL (Aux 1-4) Like the channels with optional pull-up and pull-down LVTTL (Aux 5-8) ECL (Aux 9-12) Single-ended or Differential AUX I/O is bi-directional Per channel relay isolation
Data Rate (max)	50 MHz (input and output)

Power Requirements

Table B-2: DR1 Power Requirements

Voltage	Peak Current	Dynamic Current
+5 V	4.3 A	25 mA
-5.2 V	2.5 A	1 mA
-2 V	608 mA	7.4 mA
+12 V	0	0
-12 V	0	0
+24 V	0	0
-24 V	0	0

Environmental

Temperature	Operating: 0° C to 45° C Storage: -40° C to 70° C
Humidity (non-condensing)	0° C to 10° C: Not controlled 10° C to 30° C: 5% to 95% ±5% RH 30° C to 40° C: 5% to 75% ±5% RH 40° C to 50° C: 5% to 55% ±5% RH
Altitude	10,000 ft
Cooling Required (10°C Rise; 2 DR1s)	Max: 4.68 lps @ 8.9 mmH^{2}0 Typ.: 4.60 lps @ 4.5 mmH^{2}0
Front Panel Current Requirements	NA
MTBF (ground benign)	DR1: 257,335 hours T940: 180,885 hours T940-DR1: 106,220 hours T940-DR1-DR1: 66,922 hours
Dimensions	20 x 114 x 305 mm
EMC (Council Directive 89/336/EEC)	Emission: EN61326-1: 2006, Class A Immunity: EN61326-1: 2006, Table 1 ***Designed to Meet – Testing in Progress***
Safety (Low Voltage Directive 73/23/EEC)	BS EN61010-1: 2010 ***Designed to Meet – Testing in Progress***

DR1 Signal Description

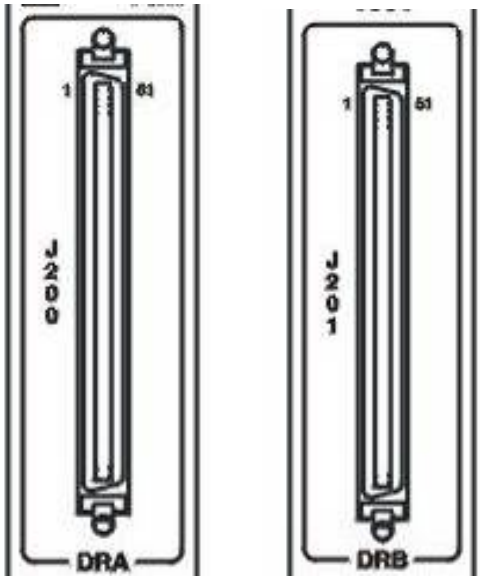


Figure B-4: J200 and J201 Connectors

DRA I/O Channels (J200)

Table B-3: DR1, DRA I/O Channels (J200)

Name	Pin No.	Description
CH1-CH32	Various	(Bi-directional) High speed LVTTL channels
SIG_GND	Various	Signal Ground reference
AUX1 A	34	(Bi-directional) General Purpose I/O pin
AUX2 A	36	(Bi-directional) General Purpose LVTTL I/O pin
AUX3 A	38	(Bi-directional) General Purpose LVTTL I/O pin
AUX4 A	40	(Bi-directional) General Purpose LVTTL I/O pin
AUX5 A	42	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX6 A	44	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX7 A	84	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX8 A	86	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX9+ A	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2V
AUX9- A	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2V
AUX10+ A	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2V
AUX10- A	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2V
AUX11+ A	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2V
AUX11- A	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2V
AUX12+ A	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2V

Name	Pin No.	Description
AUX12- A	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2V
PBUT A	46	(Bi-directional) Probe Button Input
PMODE A	47	(Output) Probe Support Output
BCLK-A	96	(Output) Reserved

Table B-4: DR1 Pinout by Pin Number (DRA)

Pin No.	Signal	Pin No.	Signal
1	SIG_GND	51	SIG_GND
2	CH1	52	CH17
3	SIG_GND	53	SIG_GND
4	CH2	54	CH18
5	SIG_GND	55	SIG_GND
6	CH3	56	CH19
7	SIG_GND	57	SIG_GND
8	CH4	58	CH20
9	SIG_GND	59	SIG_GND
10	CH5	60	CH21
11	SIG_GND	61	SIG_GND
12	CH6	62	CH22
13	SIG_GND	63	SIG_GND
14	CH7	64	CH23
15	SIG_GND	65	SIG_GND
16	CH8	66	CH24
17	SIG_GND	67	SIG_GND
18	CH9	68	CH25
19	SIG_GND	69	SIG_GND
20	CH10	70	CH26
21	SIG_GND	71	SIG_GND
22	CH11	72	CH27
23	SIG_GND	73	SIG_GND
24	CH12	74	CH28
25	SIG_GND	75	SIG_GND
26	CH13	76	CH29
27	SIG_GND	77	SIG_GND
28	CH14	78	CH30
29	SIG_GND	79	SIG_GND
30	CH15	80	CH31
31	SIG_GND	81	SIG_GND
32	CH16	82	CH32
33	SIG_GND	83	SIG_GND

Pin No.	Signal
34	AUX1 A
35	SIG_GND
36	AUX2 A
37	SIG_GND
38	AUX3 A
39	SIG_GND
40	AUX4 A
41	SIG_GND
42	AUX5 A
43	SIG_GND
44	AUX6 A
45	SIG_GND
46	PBUT_A
47	PMODE_A
48	SIG_GND
49	NC
50	NC

Pin No.	Signal
84	AUX7 A
85	SIG_GND
86	AUX8 A
87	SIG_GND
88	AUX9+ A
89	AUX9- A
90	AUX10+ A
91	AUX10- A
92	AUX11+ A
93	AUX11- A
94	AUX12+ A
95	AUX12- A
96	BCLK-A
97	SIG_GND
98	NC
99	SIG_GND
100	NC

DRB I/O Channels (J201)

Table B-5: DR1, DRB I/O Channels (J201)

Name	Pin No.	Description
CH33-CH64	Various	(Bi-directional) High speed LVTTL channels
SIG_GND	Various	Signal Ground reference
AUX1 B	34	(Bi-directional) General Purpose LVTTL I/O pin
AUX2 B	36	(Bi-directional) General Purpose LVTTL I/O pin
AUX3 B	38	(Bi-directional) General Purpose LVTTL I/O pin
AUX4 B	40	(Bi-directional) General Purpose LVTTL I/O pin
AUX5 B	42	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX6 B	44	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX7 B	84	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX8 B	86	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX9+ B	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX9- B	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10+ B	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10- B	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11+ B	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V

Name	Pin No.	Description
AUX11- B	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12+ B	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12- B	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
PBUT B	46	(Bi-directional) Probe Button Input
PMODE B	47	(Output) Probe Support Output
BCLK B	96	(Output) Reserved

Table B-6: DR1 Pinout by Pin Number (DRB)

Pin No.	Signal	Pin No.	Signal
1	SIG_GND	51	SIG_GND
2	CH33	52	CH49
3	SIG_GND	53	SIG_GND
4	CH34	54	CH50
5	SIG_GND	55	SIG_GND
6	CH35	56	CH51
7	SIG_GND	57	SIG_GND
8	CH36	58	CH52
9	SIG_GND	59	SIG_GND
10	CH37	60	CH53
11	SIG_GND	61	SIG_GND
12	CH38	62	CH54
13	SIG_GND	63	SIG_GND
14	CH39	64	CH55
15	SIG_GND	65	SIG_GND
16	CH40	66	CH56
17	SIG_GND	67	SIG_GND
18	CH41	68	CH57
19	SIG_GND	69	SIG_GND
20	CH42	70	CH58
21	SIG_GND	71	SIG_GND
22	CH43	72	CH59
23	SIG_GND	73	SIG_GND
24	CH44	74	CH60
25	SIG_GND	75	SIG_GND
26	CH45	76	CH61
27	SIG_GND	77	SIG_GND
28	CH46	78	CH62
29	SIG_GND	79	SIG_GND
30	CH47	80	CH63
31	SIG_GND	81	SIG_GND

Pin No.	Signal
32	CH48
33	SIG_GND
34	AUX1 B
35	SIG_GND
36	AUX2 B
37	SIG_GND
38	AUX3 B
39	SIG_GND
40	AUX4 B
41	SIG_GND
42	AUX5 B
43	SIG_GND
44	AUX6 B
45	SIG_GND
46	PBUT_B
47	PMODE_B
48	SIG_GND
49	NC
50	NC

Pin No.	Signal
82	CH64
83	SIG_GND
84	AUX7 B
85	SIG_GND
86	AUX8 B
87	SIG_GND
88	AUX9+ B
89	AUX9- B
90	AUX10+ B
91	AUX10- B
92	AUX11+ B
93	AUX11- B
94	AUX12+ B
95	AUX12- B
96	BCLK
97	SIG_GND
98	NC
99	SIG_GND
100	NC

PWR Connector

When connected to an installed DR1 board, the PWR connector (Figure B-5) only utilizes the pins for the multi-function signal (MFSIG) and signal ground (GND). The power pins are not connected to the board.

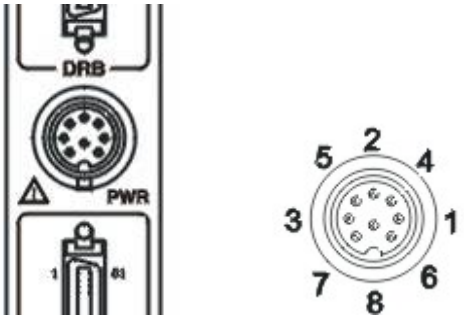


Figure B-5: Front Panel PWR Connector

When installing the Driver/Receiver Board, be sure that the correctly marked PWR cable (inside the module) is connected to its specific board – the cable marked DRA for the DRA board and marked DRB for the DRB board. Incorrect installation may cause you to be connected to the wrong MFSIG.

Table B-7 shows the connection names, pins, and descriptions for the PWR connector.

Table B-7: PWR Connector

Name	Pin No.	Description
DRB MFSIG	2	(Output) Multi-function signal DRB
DRB GND	4	Power supply signal return DRB
DRA MFSIG	6	(Output) Multi-function signal DRA
DRA GND	7	Power supply signal return DRA

Calibration

Table B-8: Calibration Settings

Inter-module timing deskew	Static
End-of-cable deskew	Static

Appendix C
DR2 Driver/Receiver Board

DR2 Features

- Channels: 32 differential LVDS
- Auxiliary channels:
  - Four LVDS
  - Four LVTTL
  - Four ECL (single ended or differential)

Front Panel Connectors

The front panel of the DR2 Driver/Receiver is shown in Chapter 3.

Block Diagram

This section describes the basic hardware configuration of the DR2 Driver/Receiver (DRA or DRB).

The DR2 is comprised of four major logic sections as shown in Figure C-1.

- Auxiliary Driver & Receiver I/O
- DR2 Driver & Receiver I/O
- Control Logic
- Firmware & NV Data

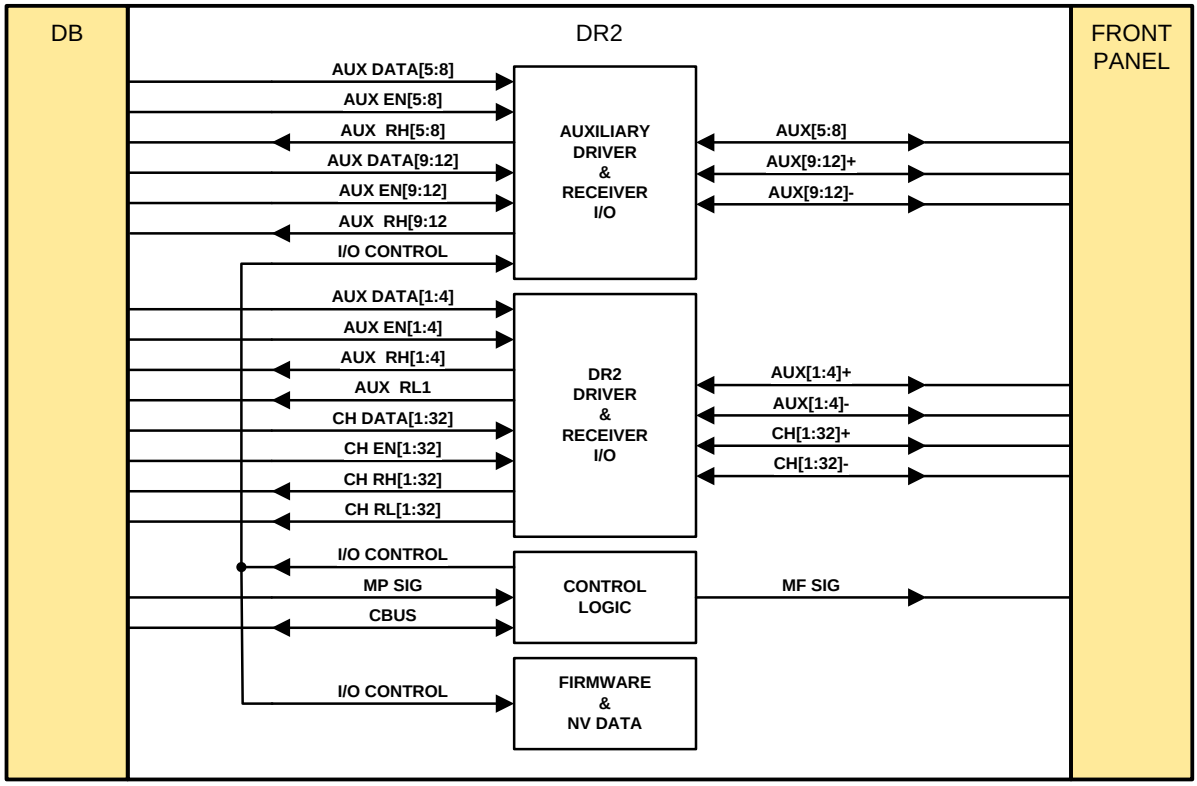


Figure C-1: DR2 Driver/Receiver Block Diagram

Auxilliary Driver & Receiver I/O

Figure C-2 illustrates the configuration and control of AUX5-8 (LVTTL) and AUX9-12 (ECL) Driver & Receiver I/O.

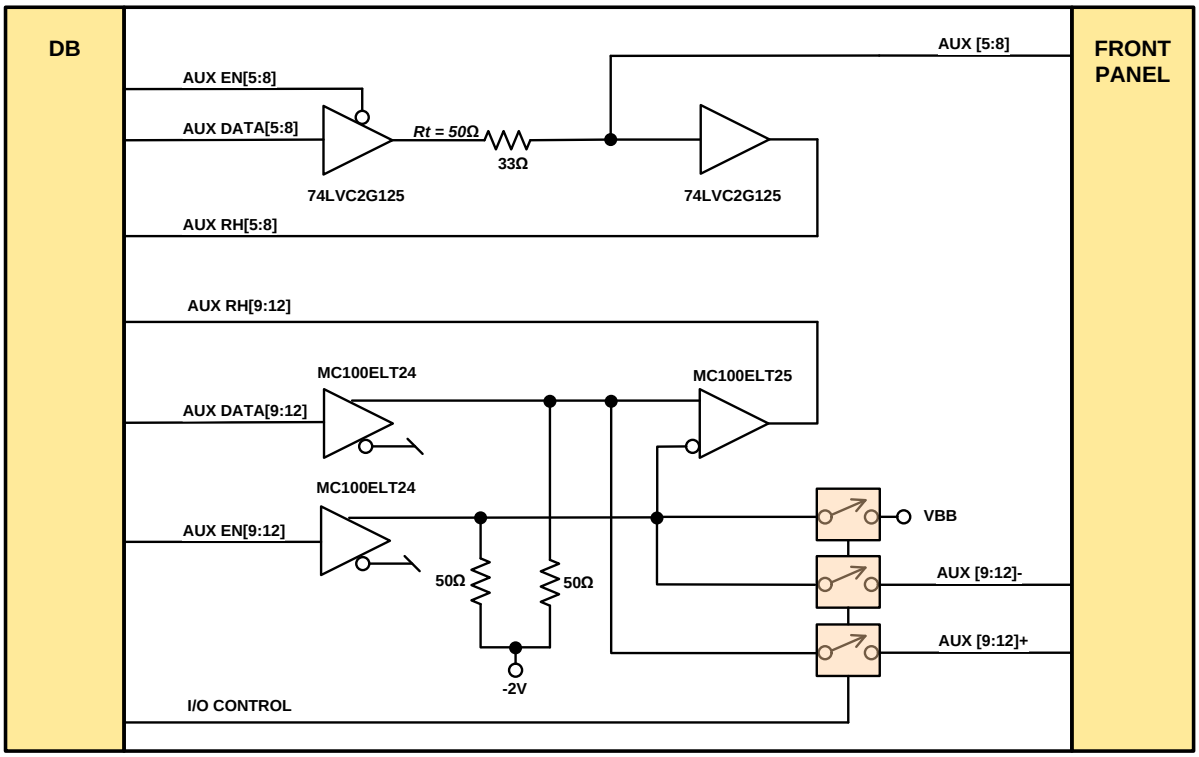


Figure C-2: Auxiliary Driver & Receiver I/O Block Diagram

Signal Descriptions

AUX EN[5:8]	Auxiliary Enable outputs from the Data Sequencer to the LVTTL output buffers.
AUX DATA[5:8]	Auxiliary Data outputs from the Data Sequencer to the LVTTL output buffers.
AUX RH[5:8]	Auxiliary Response High inputs to the Data Sequencer from the LVTTL input buffers.
AUX RH[9:12]	Auxiliary Response High inputs to the Data Sequencer from the ECL input buffers.
AUX DATA[9:12]	Auxiliary active high Data outputs from the Data Sequencer to the ECL output buffers.
AUX EN[9:12]	Auxiliary active low Data outputs from the Data Sequencer to the ECL output buffers.
EN 9-12	Auxiliary Enable outputs from the Data Sequencer to the ECL output buffers.
I/O CONTROL	Signals used to control isolation relays and ECL bipolar/differential mode.
AUX [5:8]	Four LVTTL signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
VBB	ECL input threshold (~ -1.3V).
AUX [9:12]-	Four negative differential signals used to input or output test signals. See **Configuring the AUX Channels** in

Chapter 5.

AUX [9:12]+ Four bipolar/positive differential signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.

DR2 Driver & Receiver I/O

Figure C-3 illustrates the configuration and control of the DR2 Driver & Receiver I/O (LVDS).

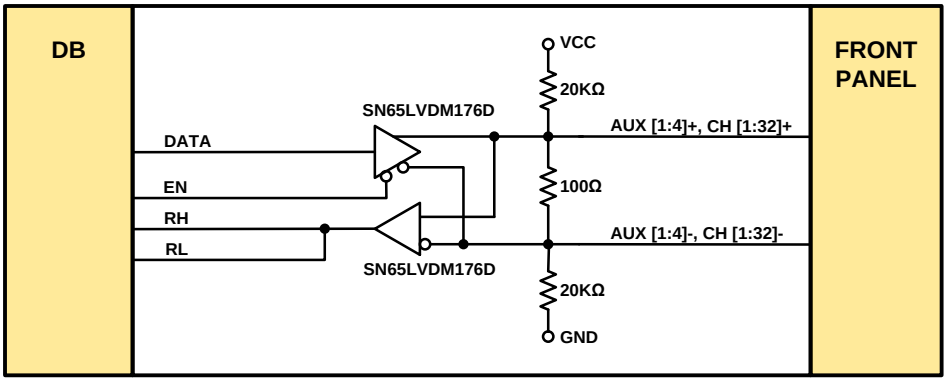


Figure C-3: DR2 Driver & Receiver I/O Block Diagram

Signal Descriptions

DATA Channel and auxiliary data output signals from the Data Sequencer to the LVDS output drivers.

EN Channel and auxiliary enable output signals from the Data Sequencer to the LVDS output drivers.

RH Response High input signals to the Data Sequencer from the LVDS input receivers. 1 = good 1, 0 = good 0.

RL Response Low input signals to the Data Sequencer from the LVDS input receivers. 0 = good 0, 1 = good 1.

AUX [1:4]+ Four positive differential LVDS signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.

AUX [1:4]- Four negative differential LVDS signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.

CH [1:32]+ These are UUT Bi-directional positive differential LVDS I/O channels from the DR2 Drivers and Receivers

CH [1:32]- These are UUT Bi-directional negative differential LVDS I/O channels from the DR2 Drivers and Receivers

Control Logic

The control logic contains the registers, memory and logic that allow the

digital board to interface and configure the hardware.

Signal Descriptions

I/O CONTROL	Signals used to control isolation, ECL mode and NV data.
MP SIG	Multi-Purpose signal from the data sequencer.
MF SIG	Multi-Function signal output to the PWR connector.
CBUS	An internal Control Bus connecting the digital board to the Driver/Receiver board.

Firmware & NV Data

The Control Logic firmware is loaded via a serial PROM on power up or VXI Reset. The firmware is field upgradeable using our supplied loader utility. Nonvolatile data (serial number, assembly revision is stored in an on-board EEPROM.

Signal Descriptions

I/O CONTROL	Signals used to program firmware and NV DATA.

DR2 Characteristics

Table C-1: DR2 Characteristics

Description	Characteristics
Digital I/O Type	LVDS (SN65LVDM176D)
Channels	32 differential per Driver/Receiver board
Output Voltage	VOL: 454 mV (max) VOH: 247 mV (min)
Differential Input Voltage	200 mV min
Output Drive Current (typical)	Source/Sink: ±8 mA
I/O Impedance	100 Ω in parallel with 20K pull-up/pull-down bias resistors to establish a True level if unconnected
Skew (Channel-to-Channel)	< 3 ns (drive and compare)
Auxiliary I/O Channels (per Driver/Receiver board)	LVDS (4), Differential (with 20K bias resistors) LVTTL (4), Single-ended ECL (4), Single-ended or Differential AUX I/O is bi-directional Per channel relay isolation on ECL I/O
Data Rate (max)	50 MHz (input and output)

Power Requirements

Table C-2: DR2 Power Requirements

Voltage	Peak Current	Dynamic Current
+5 V	500 mA	25 mA
-5.2 V	355 mA	25 mA
-2 V	350 mA	8.5 mA
+12 V	0	0
-12 V	0	0
+24 V	0	0
-24 V	0	0

Environmental

Temperature	Operating: 0° C to 45° C Storage: -40° C to 70° C
Humidity (non-condensing)	0° C to 10° C: Not controlled 10° C to 30° C: 5% to 95% ±5% RH 30° C to 40° C: 5% to 75% ±5% RH 40° C to 50° C: 5% to 55% ±5% RH
Altitude	10,000 ft
Cooling Required (10°C Rise; 2 DR2s)	Max: 2.4 lps @ 8.9 mmH^{2}0 Typ.: 2.4 lps @ 4.5 mmH^{2}0
Front Panel Current Requirements	NA
MTBF (ground benign)	DR2: 305,905 hours T940: 180,885 hours T940-DR2: 113,670 hours T940-DR2-DR2: 69,804 hours
Dimensions	20 x 114 x 305 mm
EMC (Council Directive 89/336/EEC)	Emission: EN61326-1: 2006, Class A Immunity: EN61326-1: 2006, Table 1 ***Designed to Meet – Testing in Progress***
Safety (Low Voltage Directive 73/23/EEC)	BS EN61010-1: 2010 ***Designed to Meet – Testing in Progress***

DR2 Signal Description

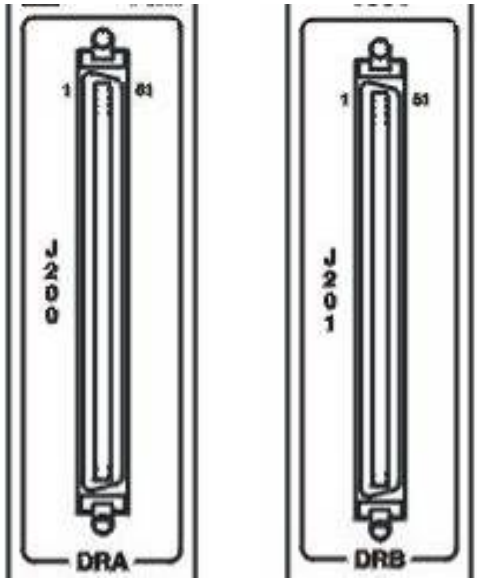


Figure C-4: J200 and J201 Connectors

DRA I/O Channels (J200)

Table C-3: DR2, DRA I/O Channels (J200)

Name	Pin No.	Description
CH1+ to CH32+	Various	(Bi-directional) LVDS Positive High speed channels
CH1- to CH32-	Various	(Bi-directional) LVDS Negative High speed channels
SIG_GND	Various	Signal Ground reference
AUX1+ A	34	(Bi-directional) General Purpose LVDS Positive I/O pin
AUX1- A	35	(Bi-directional) General Purpose LVDS Negative I/O pin
AUX2+ A	36	(Bi-directional) General Purpose LVDS Positive I/O pin
AUX2- A	37	(Bi-directional) General Purpose LVDS Negative I/O pin
AUX3+ A	38	(Bi-directional) General Purpose LVDS Positive I/O pin
AUX3- A	39	(Bi-directional) General Purpose LVDS Negative I/O pin
AUX4+ A	40	(Bi-directional) General Purpose LVDS Positive I/O pin
AUX4- A	41	(Bi-directional) General Purpose LVDS Negative I/O pin
AUX5 A	42	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX6 A	44	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX7 A	84	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX8 A	86	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series

Name	Pin No.	Description
AUX9+ A	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX9- A	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10+ A	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10- A	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11+ A	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11- A	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12+ A	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12- A	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
PBUT A	46	(Bi-directional) Probe Button Input
PMODE A	47	(Output) Probe Support Output
BCLK-A	96	(Output) Reserved

Table C-4: DR2 Pinout by Pin Number (DRA)

Pin No.	Signal	Pin No.	Signal
1	SIG_GND	51	SIG_GND
2	CH1+	52	CH17+
3	CH1-	53	CH17-
4	CH2+	54	CH18+
5	CH2-	55	CH18-
6	CH3+	56	CH19+
7	CH3-	57	CH19-
8	CH4+	58	CH20+
9	CH4-	59	CH20-
10	CH5+	60	CH21+
11	CH5-	61	CH21-
12	CH6+	62	CH22+
13	CH6-	63	CH22-
14	CH7+	64	CH23+
15	CH7-	65	CH23-
16	CH8+	66	CH24+
17	CH8-	67	CH24-
18	CH9+	68	CH25+
19	CH9-	69	CH25-
20	CH10+	70	CH26+
21	CH10-	71	CH26-
22	CH11+	72	CH27+
23	CH11-	73	CH27-
24	CH12+	74	CH28+
25	CH12-	75	CH28-

Pin No.	Signal
26	CH13+
27	CH13-
28	CH14+
29	CH14-
30	CH15+
31	CH15-
32	CH16+
33	CH16-
34	AUX1+ A
35	AUX1- A
36	AUX2+ A
37	AUX2- A
38	AUX3+ A
39	AUX3- A
40	AUX4+ A
41	AUX4- A
42	AUX5 A
43	SIG_GND
44	AUX6 A
45	SIG_GND
46	PBUT_A
47	PMODE_A
48	SIG_GND
49	NU
50	NU

Pin No.	Signal
76	CH29+
77	CH29-
78	CH30+
79	CH30-
80	CH31+
81	CH31-
82	CH32+
83	CH32-
84	AUX7 A
85	SIG_GND
86	AUX8 A
87	SIG_GND
88	AUX9+ A
89	AUX9- A
90	AUX10+ A
91	AUX10- A
92	AUX11+ A
93	AUX11- A
94	AUX12+ A
95	AUX12- A
96	BCLK-A
97	SIG_GND
98	NU
99	SIG_GND
100	NU

DRB I/O Channels (J201)

Table C-5: DR2, DRB I/O Channels (J201)

Name	Pin No.	Description
CH33+ to CH64+	Various	(Bi-directional) LVDS Positive High speed channels
CH33- to CH64-	Various	(Bi-directional) LVDS Negative High speed channels
SIG_GND	Various	Signal Ground reference
AUX1+ B	34	(Bi-directional) General Purpose LVDS Positive I/O pin
AUX1- B	35	(Bi-directional) General Purpose LVDS Negative I/O pin
AUX2+ B	36	(Bi-directional) General Purpose LVDS Positive I/O pin
AUX2- B	37	(Bi-directional) General Purpose LVDS Negative I/O pin
AUX3+ B	38	(Bi-directional) General Purpose LVDS Positive I/O pin
AUX3- B	39	(Bi-directional) General Purpose LVDS Negative I/O pin
AUX4+ B	40	(Bi-directional) General Purpose LVDS Positive I/O pin
AUX4- B	41	(Bi-directional) General Purpose LVDS Negative I/O pin
AUX5 B	42	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX6 B	44	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX7 B	84	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX8 B	86	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX9+ B	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX9- B	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10+ B	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10- B	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11+ B	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11- B	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12+ B	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12- B	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
PBUT B	46	(Bi-directional) Probe Button Input
PMODE B	47	(Output) Probe Support Output
BCLK B	96	(Output) Reserved

Table C-6: DR2 Pinout by Pin Number (DRB)

Pin No.	Signal	Pin No.	Signal
1	SIG_GND	51	SIG_GND
2	CH33+	52	CH49+
3	CH33-	53	CH49-
4	CH34+	54	CH50+
5	CH34-	55	CH50-
6	CH35+	56	CH51+
7	CH35-	57	CH51-
8	CH36+	58	CH52+
9	CH36-	59	CH52-
10	CH37+	60	CH53+
11	CH37-	61	CH53-
12	CH38+	62	CH54+
13	CH38-	63	CH54-
14	CH39+	64	CH55+
15	CH39-	65	CH55-
16	CH40+	66	CH56+
17	CH40-	67	CH56-
18	CH41+	68	CH57+
19	CH41-	69	CH57-
20	CH42+	70	CH58+
21	CH42-	71	CH58-
22	CH43+	72	CH59+
23	CH43-	73	CH59-
24	CH44+	74	CH60+
25	CH44-	75	CH60-
26	CH45+	76	CH61+
27	CH45-	77	CH61-
28	CH46+	78	CH62+
29	CH46-	79	CH62-
30	CH47+	80	CH63+
31	CH47-	81	CH63-
32	CH48+	82	CH64+
33	CH48-	83	CH64-
34	AUX1+ B	84	AUX7 B
35	AUX1- B	85	SIG_GND
36	AUX2+ B	86	AUX8 B
37	AUX2- B	87	SIG_GND
38	AUX3+ B	88	AUX9+ B
39	AUX3- B	89	AUX9- B
40	AUX4+ B	90	AUX10+ B

Pin No.	Signal
41	AUX4- B
42	AUX5 B
43	SIG_GND
44	AUX6 B
45	SIG_GND
46	PBUT_B
47	PMODE_B
48	SIG_GND
49	NU
50	NU

Pin No.	Signal
91	AUX10- B
92	AUX11+ B
93	AUX11- B
94	AUX12+ B
95	AUX12- B
96	BCLK
97	SIG_GND
98	NU
99	SIG_GND
100	NU

PWR Connector

When connected to an installed DR2 board, the PWR connector (Figure C-5) only utilizes the pins for the multi-function signal (MFSIG) and signal ground (GND). The power pins are not connected to the board.

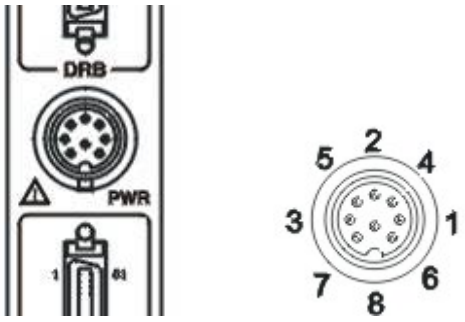


Figure C-5: Front Panel PWR Connector

When installing the Driver/Receiver Board, be sure that the correctly marked PWR cable (inside the module) is connected to its specific board – the cable marked DRA for the DRA board and marked DRB for the DRB board. Incorrect installation may cause you to be connected to the wrong MFSIG.

If the board is preinstalled by the factory, the cables have already been installed.

Table C-7 shows the connection names, pins, and descriptions for the PWR connector.

Table C-7: PWR Connector

Name	Pin No.	Description
DRB MFSIG	2	(Output) Multi-function signal DRB
DRB GND	4	Power supply signal return DRB
DRA MFSIG	6	(Output) Multi-function signal DRA
DRA GND	7	Power supply signal return DRA

Calibration

Table C-8: Calibration Settings

Inter-module timing deskew	Static
End-of-cable deskew	Static

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Appendix D
DR3e Driver/Receiver Board

DR3e Features

- Channels: 32 single-ended variable voltage or 16 differential channels
- Voltage range: -15 V to +24 V with an output swing of up to 24 V
- Relay Isolation on all I/O and AUX channels
- Provides full drive current on all channels simultaneously
- Programmable current load with dual commutating voltages
- Selectable resistive input load (8 choices) to a programmed voltage
- Selectable slew rate (0.25 V/ns to 1.3 V/ns)
- 12/50 ohm selectable output impedance
- Over-current detection
- Over-voltage detection/protection
- Auxiliary channels:
  - Four variable voltage
  - Four LVTTL
  - Four ECL (single-ended or differential)

Front Panel Connectors

The front panel of the DR3e Driver/Receiver is shown in Chapter 3.

Block Diagram

This section describes the basic hardware configuration of the DR3e Driver/Receiver (DRA or DRB).

The DR3e is comprised of four major logic sections as shown in Figure D-1.

- Auxiliary Driver & Receiver I/O
- DR3e Driver & Receiver I/O
- Control Logic
- Firmware & NV Data

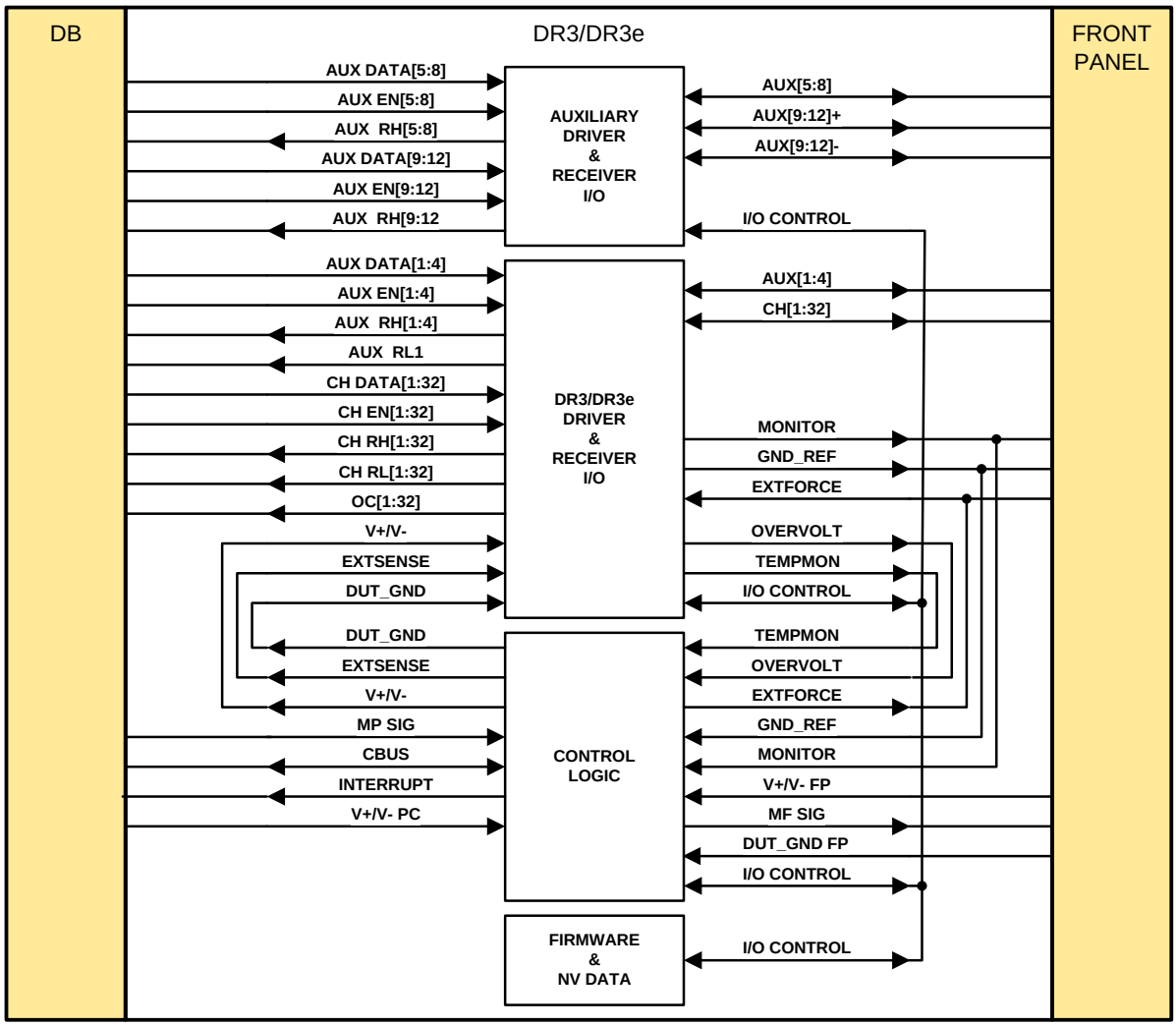


Figure D-1: DR3e Driver/Receiver Block Diagram

Auxiliary Driver & Receiver I/O

Figure D-2 illustrates the configuration and control of AUX5-8 (LVTTL) and AUX9-12 (ECL) Driver & Receiver I/O.

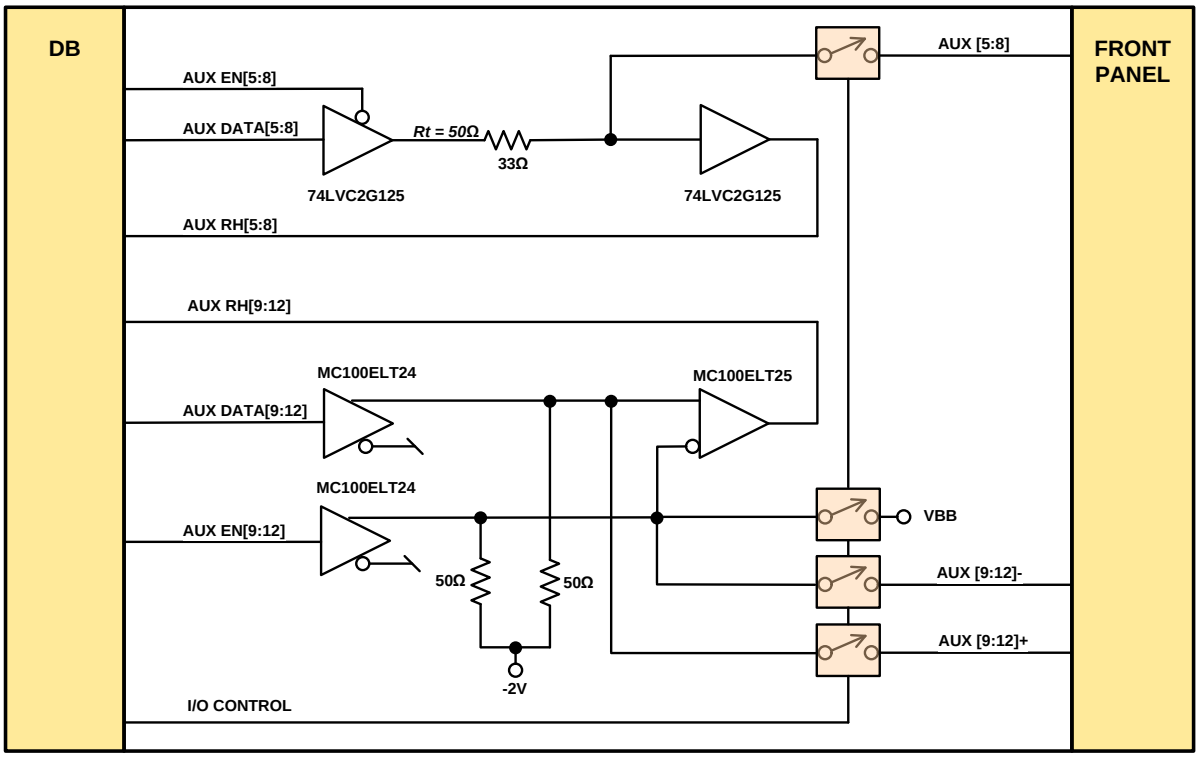


Figure D-2: Auxiliary Driver & Receiver I/O Block Diagram

Signal Descriptions

AUX EN[5:8]	Auxiliary Enable outputs from the Data Sequencer to the LVTTL output buffers.
AUX DATA[5:8]	Auxiliary Data outputs from the Data Sequencer to the LVTTL output buffers.
AUX RH[5:8]	Auxiliary Response High inputs to the Data Sequencer from the LVTTL input buffers.
AUX RH[9:12]	Auxiliary Response High inputs to the Data Sequencer from the ECL input buffers.
AUX DATA[9:12]	Auxiliary active high Data outputs from the Data Sequencer to the ECL output buffers.
AUX EN[9:12]	Auxiliary active low Data outputs from the Data Sequencer to the ECL output buffers.
EN 9-12	Auxiliary Enable outputs from the Data Sequencer to the ECL output buffers.
I/O CONTROL	Signals used to control isolation relays and ECL bipolar/differential mode.
AUX [5:8]	Four LVTTL signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
VBB	ECL input threshold (~ -1.3V).
AUX [9:12]-	Four negative differential signals used to input or output test signals. See **Configuring the AUX Channels** in

Chapter 5.

AUX [9:12]+ Four bipolar/positive differential signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.

DR3e Driver & Receiver I/O

Figure D-3 illustrates the configuration and control of the DR3e Driver & Receiver I/O.

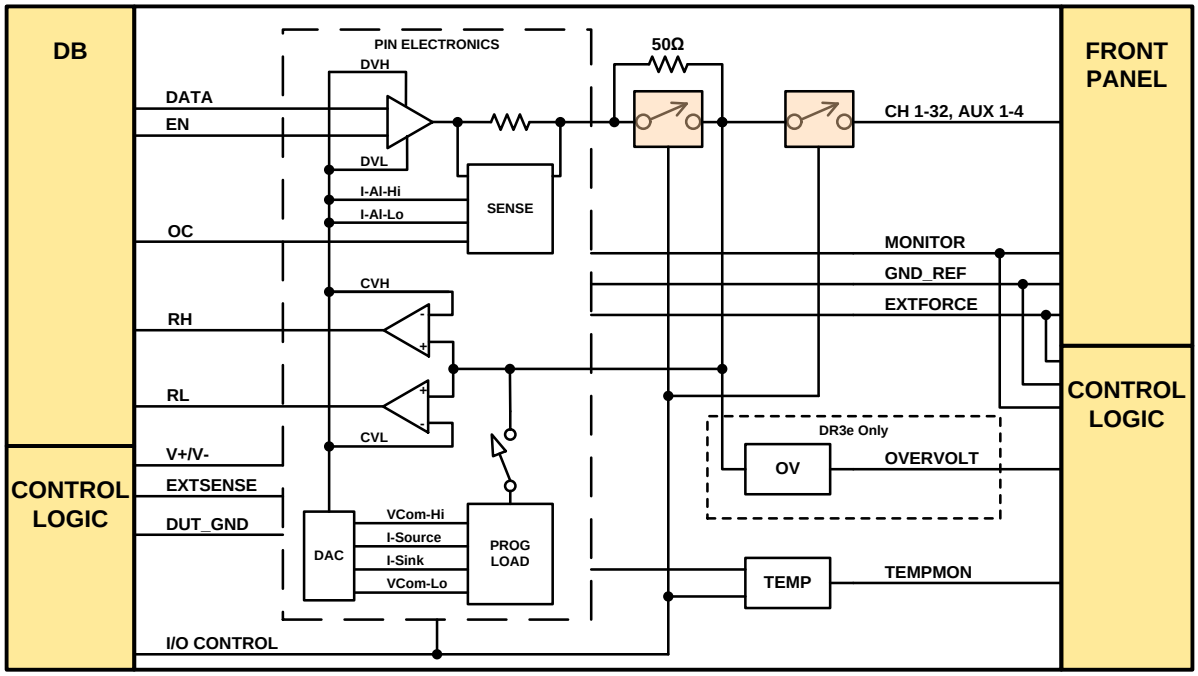


Figure D-3: DR3e Driver & Receiver I/O Block Diagram

Signal Descriptions

DATA	Channel and auxiliary data output signals from the Data Sequencer to the programmable output drivers.
EN	Channel and auxiliary enable output signals from the Data Sequencer to the programmable output drivers.
OC	Over-Current detect from the programmable Driver and Receiver channels.
RH	Response High input signals to the Data Sequencer from the programmable input receivers. 1 = good 1, 0 = good 0.
RL	Response Low input signals to the Data Sequencer from the programmable input receivers. 0 = good 0, 1 = good 1.
V+/V-	Bias Power required for operation of the Pin Electronics devices.
EXTSENSE	Pin electronics signal used for calibration.

DUT_GND	This signal comes from the UUT and can be used to offset the reference levels up to ±3V. Excursions of DUT_GND beyond ±390 mV with respect to signal ground yield a GND FAULT signal.
I/O CONTROL	Control Logic signals to control isolation relays, termination, pin electronics and temperature thresholds.
AUX 1-4	Four programmable signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
CH 1-32	These are UUT Bi-directional programmable I/O channels from the DR3e Drivers and Receivers
MONITOR	This is an analog output signal from the Pin Electronics devices which can be used to monitor DAC levels even the Channel I/O levels. This signal is used with the internal ADC but a buffered version also comes out the Front Panel.
GND_REF	This is the ground reference output signal from the Pin Electronics devices. It is used with MONITOR to make accurate ADC measurements. A buffered version also comes out the Front Panel.
EXTFORCE	External Force is an analog I/O signal which is connected to all of the Pin Electronics devices and can be used to force a level on the output of the driver. It may also be used to monitor a channel's state. EXTFORCE is also used for calibration.
OVERVOLT	Real-time over-voltage detector circuit monitors Driver and Receivers to protect the pin electronics. Also clamps the inputs to the V+/- rails (DR3e only).
TEMPMON	Real-time temperature monitors for the pin electronics.

Control Logic

The control logic contains the registers, memory and logic that allow the digital board to interface and configure the hardware. See Figure D-4.

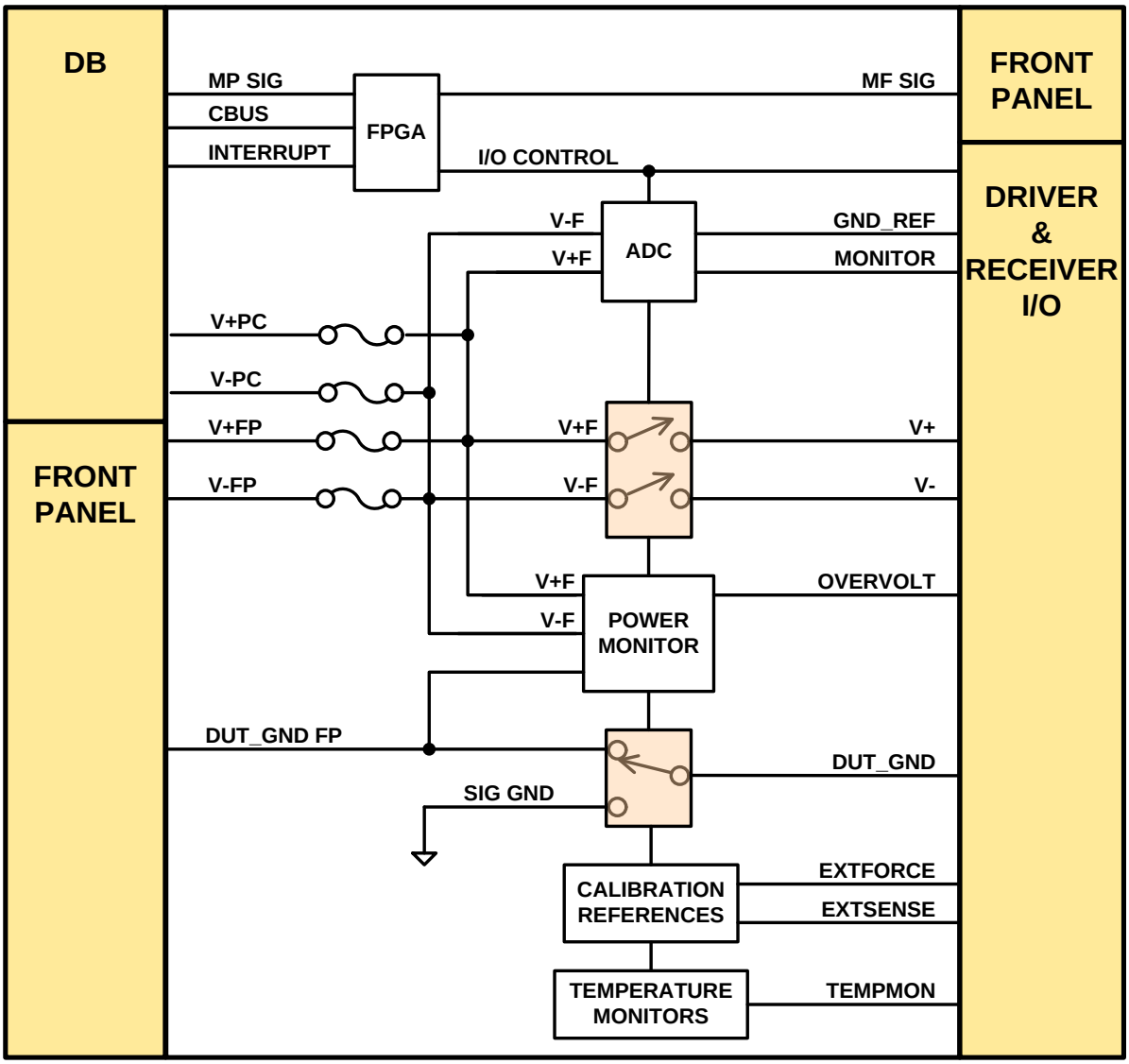


Figure D-4: DR3e Control Logic Block Diagram

Signal Descriptions

MP SIG	Multi-Purpose signal from the data sequencer.
CBUS	An internal Control Bus connecting the digital board to the Driver/Receiver board.
INTERRUPT	Real time signal generated from the power and temperature monitor data.
V+PC	Positive bias power required for operation of the Pin Electronics devices from the T940 power converter.
V-PC	Negative bias power required for operation of the Pin Electronics devices from the T940 power converter.
V+FP	Positive bias power required for operation of the Pin Electronics devices comes from the T964 Front Panel

	PWR connector provided by external power supplies.
V-FP	Negative bias power required for operation of the Pin Electronics devices comes from the T964 Front Panel PWR connector provided by external power supplies.
DUT_GND FP	This signal comes from the UUT and can be used to offset the reference levels up to ±3 V. Excursions of DUT_GND beyond ±390 mV with respect to signal ground yields a GND FAULT signal.
MF SIG	Multi-Function signal output to the PWR connector.
I/O CONTROL	Signals used to program the features of the DR3e Driver/Receiver board.
GND_REF	This is the ground reference output signal from the Pin Electronics devices. It is used with MONITOR to make accurate ADC measurements.
V+	Fused and switched positive bias power required for operation of the Pin Electronics devices.
V-	Fused and switched negative bias power required for operation of the Pin Electronics devices.
OVERVOLT	Real-time over-voltage detector circuit monitors Driver and Receivers to protect the pin electronics. Also clamps the inputs to the V+/- rails.
DUT_GND	Either the front panel DUT_GND signal or SIG GND.
EXTFORCE	Pin electronics signal used for calibration.
EXTSENSE	Pin electronics signal used for calibration.
TEMPMON	Real-time temperature monitors for the pin electronics

Firmware & NV Data

The Control Logic firmware is loaded via a serial PROM on power up or VXI Reset. The firmware is field upgradeable using our supplied loader utility. Nonvolatile data (serial number, assembly revision is stored in an on-board EEPROM.

Signal Descriptions

I/O CONTROL	Signals used to program firmware and NV DATA.

DR3e Characteristics

Table D-1: DR3e Characteristics

Description	Characteristics
Digital I/O Type	Variable Voltage
Channels	32 SE or 16 DIFF per Driver/Receiver board 64 per VXI slot Per channel relay isolation
Output Voltage Ranges* (Selectable/Sequencer)	-15 V to +17 V (VM0) -7 V to +24 V (VM1)
Output Voltage Swing	500 mV [1] to 24 V
Output Resolution	< 5 mV
Output Accuracy (DVH and DVL)	± (50mV + 1% of PV) Slow, Default, Medium slew settings ± (75mV + 1% of PV) Fast slew setting
Output Drive Current	± 85 mA typical (Source/Sink)
Output Impedance (Selectable/Channel)	Direct (12 Ω) or Series (50 Ω), ± 4 Ω
Slew Rate (Selectable/Channel or custom)	0.25 V/ns 0.7 V/ns, 1.0 V/ns or 1.3 V/ns: typical
Input Threshold Ranges*	-14.75 V to +14 V (VM0) -6.75 V to +21 V (VM1)
Input Threshold Resolution	< 5 mV
Input Threshold Accuracy (CVH and CVL)	± (50mV + 1% of PV)
Skew (Chan. to Chan.)	< 3 ns (drive and compare)
Current Source/Sink (Programmable/Channel)	Range: ±0.4 mA to ±20 mA (usable to 24 mA) Resolution: < 10 µA Accuracy: 3% of PV + 120uA
Commutating Voltage: V_{com} (CMH and CML)	Range: same as driver Resolution: < 5 mV Accuracy: ± (50mV + 1% of PV)
Over Current Alarm (IAH and IAL)	Range: ±800 mA Resolution: < 30 µA Accuracy: ± (50mA + 1% of PV)
Resistive Loads (Selectable/Channel)	140 Ω to ~1 KΩ (8 selections) to Vcom Accuracy: 30%
PMU capability	Voltage Range/Resolution/Accuracy: same as driver
DUT_GND Reference Input (per Driver/Receiver board)	Offset range: ±3 V Interrupt Voltage: 390 mV Resistive load: 100 kΩ Bypass Relay: On or Off

Description	Characteristics
Power Input Using Optional Front Panel Power Input Connector (for Pin Electronics devices)	V+: 10 to 28 V V-: -4 to -19 V V+ to V- delta: <32 V
Pin Electronics Monitoring (per channel)	All programmed levels Output and Input levels Temperature
Channel Over-voltage Protection	Clamped to 0.4 V beyond V+ or V- • Max current 200mA for < 10ms Auto Shutdown: • DC level within 1 V of V+ or V- • A 5 µs spike exceeding V+ or V-
Channel Capacitance	<120 pF
Channel Crosstalk	<250 mV_{pk-pk}
Voltage Monitoring (per Driver/Receiver board)	V+, V- and Front Panel DUT_GND
Hybrid Connection (per Driver/Receiver board)	Connects Front Panel pin to any channel via the Pin Driver electronics. (User must disable the drive enabled to the channel.) ~40 Ω series impedance, ~3 MHz bandwidth
Auxiliary I/O Channels (per Driver/Receiver board)	Programmable Level (4) LVTTL (4) ECL (4)...Single Ended or Differential AUX I/O is bi-directional Relay isolation

* This range is limited by the V+ and V- levels.

[1] 700 mV at the fastest slew rate

I/O Min/Max Levels

The I/O level minimum and maximum values are determined by the V+ an V- bias voltage levels. The following table lists the min and max levels based on the V+ and V- level:

Table D-2: DR3e I/O Min/Max Levels Front Panel

Level	Min	Max	Units
DVH	V- + 5	V+ - 3	V
DVL	V- + 4	V+ - 7	V
CVH	V- + 2	V+ - 7	V
CVL	V- + 2	V+ - 7	V
Vcom High (CMH)	V- + 2	V+ - 7	V
Vcom Low (CML)	V- + 2	V+ - 7	V

The following table lists the min and max levels based on the power converter type 1 or 3 setting:

Table D-3: DR3e I/O Min/Max Levels Power Converter Type 1 or 3

Level	Power Converter Setting							Units
	-12 to +12	-15 to +5	-10 to +10	-5 to +7	-5 to +15	0 to +24	-2 to +22	
DVH max	12	5	10	7	15	24	22	V
DVH min	-10	-13.5	-8.5	-4	-4	1	-0.5	V
DVL max	8.5	2	8.5	4.5	11.6	21	18.8	V
DVL min	-11.6	-15	-10	-5	-5	0	-2	V
CVH max	9	2.6	9	5	12.2	21.8	19.4	V
CVH min	-12	-15	-10	-5	-5	0	-2	V
CVL max	9	2.6	9	5	12.2	21.8	19.4	V
CVL min	-12	-15	-10	-5	-5	0	-2	V
CMH max	9	2.6	9	5	12.2	21.8	19.4	V
CMH min	-12	-15	-10	-5	-5	0	-2	V
CML max	9	2.6	9	5	12.2	21.8	19.4	V
CML min	-12	-15	-10	-5	-5	0	-2	V

Power Requirements

Table D-4: VXI Power Requirements with Front Panel Power

Voltage	Peak Current	Dynamic Current
+5 V	3.3 A	330 mA
-5.2 V	2.50 A	25 mA
-2 V	110 mA	10 mA
+12 V	21 mA	7 mA
-12 V	18.1 mA	17 mA
+24 V	9.9 mA	9.8 mA
-24 V	0	0

Table D-5: VXI Power Requirements (not including Power Converter power consumption)

Voltage	Peak Current	Dynamic Current
+5 V	3.3 A	330 mA
-5.2 V	2.50 A	25 mA
-2 V	110 mA	10 mA
+12 V	21 mA	7 mA

Voltage	Peak Current	Dynamic Current
-12 V	18.1 mA	17 mA
+24 V	9.9 mA	9.8 mA
-24 V	0	0

Note: *Use the DR3e Current Estimator calculation tool to estimate the power converter power consumption from the ±12V and ±24V power rails. This tool is available upon request from Astronics Test Systems at atssales@astronics.com.*

Environmental

Temperature	Operating: 0° C to 45° C * Storage: -40° C to 70° C
Humidity	0° C to 10° C: Not controlled 10° C to 30° C: 5% to 95% ±5% RH 30° C to 40° C: 5% to 75% ±5% RH 40° C to 50° C: 5% to 55% ±5% RH
Altitude	10,000 ft
Cooling Required (10°C Rise; 2 DR3s)	Max: 27.4 lps @ 8.9 mmH^{2}0 Typ.: 18.9 lps @ 4.5 mmH^{2}0
Front Panel Current Requirements (channels unloaded)	V+: 3.8 A max.; 2.9 A typ. @ 21.5 V V-: 4.3 A max.; 3.4 A typ. @ -10.5 V
MTBF (ground benign)	DR3e: 131,656 hours T940: 180,885 hours Power Converter: 540,040 hours T940-DR3e: 66,775 hours T940-DR3e-DR3e: 44,304 hours
Dimensions	20 x 114 x 305 mm
EMC (Council Directive 89/336/EEC)	Emission: EN61326-1: 2006, Class A Immunity: EN61326-1: 2006, Table 1 ***Designed to Meet – Testing in Progress***
Safety (Low Voltage Directive 73/23/EEC)	BS EN61010-1: 2010 ***Designed to Meet – Testing in Progress***

***** For a DRM with 2 DR3s, the 1263 chassis has sufficient airflow for ~25 ºC max. inlet air temperature at <~2000 ft.

DR3e Signal Description

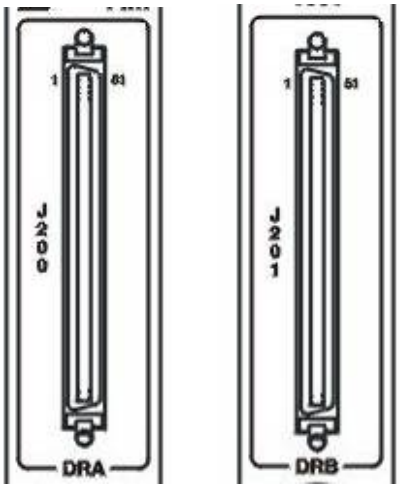


Figure D-5: J200 and J201 Connectors

DRA I/O Channels (J200)

Table D-6: DR3e, DRA I/O Channels (J200)

Name	Pin No.	Description
CH1-CH32	Various	(Bi-directional) High speed channels
DUT_GND A	100	(Input) DUT/UUT ground reference. All of the Pin Electronics devices have a UUT ground reference input that can be selected to be this signal or signal ground.
SIG_GND	Various	Signal Ground reference
AUX1 A	34	(Bi-directional) General Purpose Programmable I/O pin. Also used as the probe input data channel.
AUX2 A	36	(Bi-directional) General Purpose Programmable I/O pin
AUX3 A	38	(Bi-directional) General Purpose Programmable I/O pin
AUX4 A	40	(Bi-directional) General Purpose Programmable I/O pin
AUX5 A	42	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX6 A	44	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX7 A	84	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX8 A	86	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX9+ A	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX9- A	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10+ A	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10- A	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11+ A	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11- A	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12+ A	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12- A	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
PBUT A	46	(Bi-directional) Probe Button Input
PMODE A	47	(Output) Probe Support Output
GNDREF A	49	(Output) Ground Reference output from the Pin Electronics devices
MONITOR A	50	(Output) Monitor signal from the Pin Electronics devices ***Note:*** *Only one channel can be selected at a time.*
BCLK-A	96	(Output) Reserved
EXTFORCEA	98	(Input) External Force routed to all of the Pin Electronics devices

Table D-7: DR3e Pinout by Pin Number (DRA)

Pin No.	Signal
1	SIG_GND
2	CH1
3	SIG_GND
4	CH2
5	SIG_GND
6	CH3
7	SIG_GND
8	CH4
9	SIG_GND
10	CH5
11	SIG_GND
12	CH6
13	SIG_GND
14	CH7
15	SIG_GND
16	CH8
17	SIG_GND
18	CH9
19	SIG_GND
20	CH10
21	SIG_GND
22	CH11
23	SIG_GND
24	CH12
25	SIG_GND
26	CH13
27	SIG_GND
28	CH14
29	SIG_GND
30	CH15
31	SIG_GND
32	CH16
33	SIG_GND
34	AUX1 A
35	SIG_GND
36	AUX2 A
37	SIG_GND
38	AUX3 A
39	SIG_GND
40	AUX4 A

Pin No.	Signal
51	SIG_GND
52	CH17
53	SIG_GND
54	CH18
55	SIG_GND
56	CH19
57	SIG_GND
58	CH20
59	SIG_GND
60	CH21
61	SIG_GND
62	CH22
63	SIG_GND
64	CH23
65	SIG_GND
66	CH24
67	SIG_GND
68	CH25
69	SIG_GND
70	CH26
71	SIG_GND
72	CH27
73	SIG_GND
74	CH28
75	SIG_GND
76	CH29
77	SIG_GND
78	CH30
79	SIG_GND
80	CH31
81	SIG_GND
82	CH32
83	SIG_GND
84	AUX7 A
85	SIG_GND
86	AUX8 A
87	SIG_GND
88	AUX9+ A
89	AUX9- A
90	AUX10+ A

Pin No.	Signal
41	SIG_GND
42	AUX5 A
43	SIG_GND
44	AUX6 A
45	SIG_GND
46	PBUT_A
47	PMODE_A
48	SIG_GND
49	GNDREF A
50	MONITOR A

Pin No.	Signal
91	AUX10- A
92	AUX11+ A
93	AUX11- A
94	AUX12+ A
95	AUX12- A
96	BCLK-A
97	SIG_GND
98	EXTFORCE A
99	SIG_GND
100	DUT_GND A

DRB I/O Channels (J201)

Table D-8: DR3e, DRB I/O Channels (J201)

Name	Pin No.	Description
CH33-CH64	Various	(Bi-directional) High speed channels
DUT_GND B	100	(Input) DUT/UUT ground reference. All of the Pin Electronics devices have a UUT ground reference input that can be selected to be this signal or signal ground.
SIG_GND	Various	Signal Ground reference
AUX1 B	34	(Bi-directional) General Purpose I/O pin. Also used as the probe input data channel.
AUX2 B	36	(Bi-directional) General Purpose I/O pin
AUX3 B	38	(Bi-directional) General Purpose I/O pin
AUX4 B	40	(Bi-directional) General Purpose I/O pin
AUX5 B	42	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX6 B	44	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX7 B	84	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX8 B	86	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX9+ B	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX9- B	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10+ B	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10- B	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11+ B	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11- B	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12+ B	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12- B	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
PBUT B	46	(Bi-directional) Probe Button Input

Name	Pin No.	Description
PMODE B	47	(Output) Probe Support Output
GNDREF B	49	(Output) Ground Reference output from driver/receiver logic
MONITOR B	50	(Output) Monitor signal from the Pin Electronics devices ***Note:*** *Only one channel can be selected at a time.*
BCLK B	96	(Output) Reserved
EXTFORCEB	98	(Input) External Force routed to all of the Pin Electronics devices

Table D-9: DR3e Pinout by Pin Number (DRB)

Pin No.	Signal	Pin No.	Signal
1	SIG_GND	51	SIG_GND
2	CH33	52	CH49
3	SIG_GND	53	SIG_GND
4	CH34	54	CH50
5	SIG_GND	55	SIG_GND
6	CH35	56	CH51
7	SIG_GND	57	SIG_GND
8	CH36	58	CH52
9	SIG_GND	59	SIG_GND
10	CH37	60	CH53
11	SIG_GND	61	SIG_GND
12	CH38	62	CH54
13	SIG_GND	63	SIG_GND
14	CH39	64	CH55
15	SIG_GND	65	SIG_GND
16	CH40	66	CH56
17	SIG_GND	67	SIG_GND
18	CH41	68	CH57
19	SIG_GND	69	SIG_GND
20	CH42	70	CH58
21	SIG_GND	71	SIG_GND
22	CH43	72	CH59
23	SIG_GND	73	SIG_GND
24	CH44	74	CH60
25	SIG_GND	75	SIG_GND
26	CH45	76	CH61
27	SIG_GND	77	SIG_GND
28	CH46	78	CH62
29	SIG_GND	79	SIG_GND
30	CH47	80	CH63
31	SIG_GND	81	SIG_GND

Pin No.	Signal
32	CH48
33	SIG_GND
34	AUX1 B
35	SIG_GND
36	AUX2 B
37	SIG_GND
38	AUX3 B
39	SIG_GND
40	AUX4 B
41	SIG_GND
42	AUX5 B
43	SIG_GND
44	AUX6 B
45	SIG_GND
46	PBUT_B
47	PMODE_B
48	SIG_GND
49	GNDREF B
50	MONITOR B

Pin No.	Signal
82	CH64
83	SIG_GND
84	AUX7 B
85	SIG_GND
86	AUX8 B
87	SIG_GND
88	AUX9+ B
89	AUX9- B
90	AUX10+ B
91	AUX10- B
92	AUX11+ B
93	AUX11- B
94	AUX12+ B
95	AUX12- B
96	BCLK
97	SIG_GND
98	EXTFORCE B
99	SIG_GND
100	DUT_GND B

PWR Connector

The PWR connector (Figure D-6) supplies both positive and negative bias power as well as multi-function signals to the DR3e Driver/Receiver Board if the external front power option is purchased. The DR3e does not require front panel power.

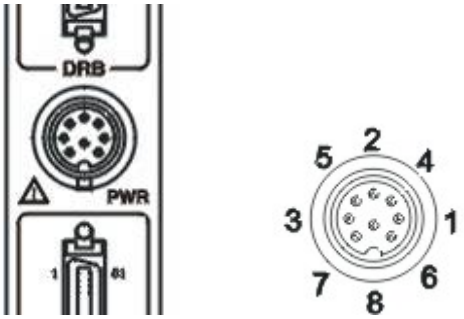


Figure D-6: Front Panel Optional DR3e PWR Connector

When installing the DR3e Driver/Receiver Board with the front panel power option, be sure that the correctly marked power cable (inside the module) is connected to its specific board – the cable marked DRA for the DRA board and marked DRB for the DRB board.

Table D-8 shows the connection names, pins, and descriptions for the power connector.

Table D-10: PWR Connector

Name	Pin No.	Description
DRB V+	1	Positive supply for the DRB Board Pin Electronics devices
DRB MFSIG	2	(Output) Multi-function signal DRB
DRA V+	3	Positive supply for the DRA Board Pin Electronics devices
DRB GND	4	Power supply signal return DRB
DRB V-	5	Negative supply for the DRB Board Pin Electronics devices
DRA MFSIG	6	(Output) Multi-function signal DRA
DRA GND	7	Power supply signal return DRA
DRA V-	8	Negative supply for the DRA Board Pin Electronics devices

Calibration

Driver/Receiver boards are calibrated using the following settings prior to shipment:

- -15 V to +17 V Voltage Mode

  Power Converter -12 to +12
- -7 V to +24 V Voltage Mode

  Power Converter -5 to +15

Table D-11: Calibration Settings

DAC Basic	Factory stored in EEPROM
Driver channel deskew	Factory stored in EEPROM
ADC/Monitor	Field upgradable stored in EEPROM
DVH/DVL	Field upgradable stored in EEPROM
CVH/CVL	Field upgradable stored in EEPROM
Vcom High/Vcom Low	Field upgradable stored in EEPROM
Isource//Isink	Field upgradable stored in EEPROM
IAL/IAH	Field upgradable stored in EEPROM
Inter-module timing deskew	Static
End-of-cable deskew	Static

Appendix E
DR4 Driver/Receiver Board

DR4 Features

- Channels: 48 single-ended variable voltage or 24 differential channels
- Voltage range: -31 V to +31 V with an output swing of up to 31 V
- Relay Isolation on all channel I/O
- Selectable drive current
- 5 Ω, 50 Ω selectable output impedance
- Over-current detection
- Temperature Monitoring
- 16 TTL auxiliary channels

Front Panel Connectors

The front panel of the DR4 Driver/Receiver is shown in Chapter 3 (no external power connector).

Block Diagram

The DR4 I/O Block Diagram (Figure E-1) describes the distribution of resources of the DR4.

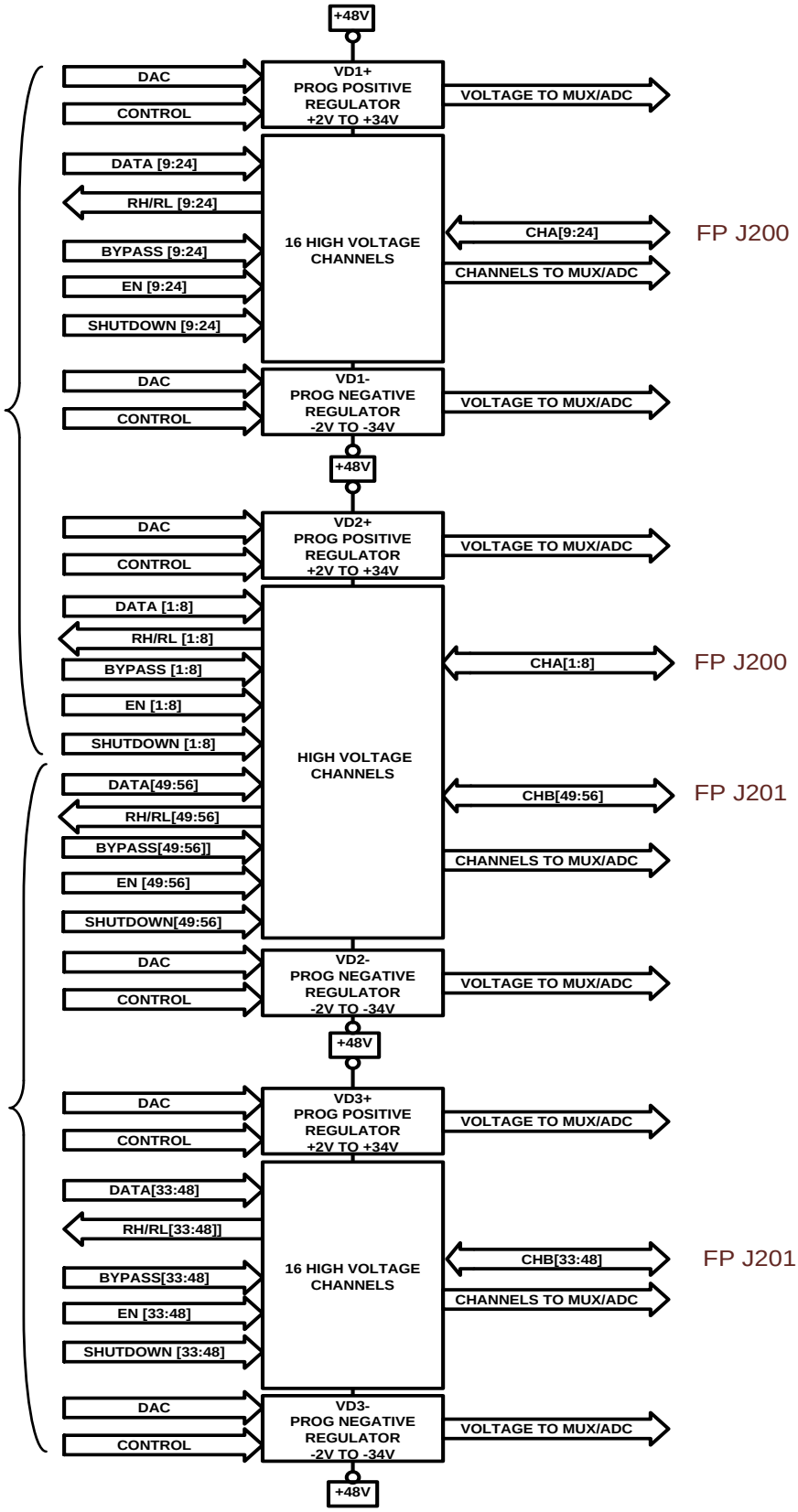


Figure E-1: DR4 I/O Block Diagram

Signal Descriptions

DATA	Channel data output signals from the Data Sequencer to the programmable output drivers.
EN	Channel enable output signals from the Data Sequencer to the programmable output drivers.
OC	Over-Current detect from the programmable Driver and Receiver channels.
RH/RL	Response High input signals to the Data Sequencer from the programmable input receivers. 1 = good 1, 0 = good 0.
	Response Low input signals to the Data Sequencer from the programmable input receivers. 0 = good 0, 1 = good 1.
CONTROL	Control Logic signals to control isolation relays, termination, pin electronics and temperature thresholds.
CHA [1:24]	These are Bi-directional programmable I/O channels from
CHB [33:56]	the DR4 Drivers and Receivers connected to the UUT
TEMPMON	Real-time temperature monitors the PCB junction plane.
SHUTDOWN	These are signals that control the driver output used in Direct Drive mode.
SEQUENCER A	T940 Digital Board Sequencer logic that provides the Stimulus and captures Response data.
SEQUENCER B	T940 Digital Board Sequencer logic that provides the Stimulus and captures Response data.
+48V	This is the common power bus from used by the Prog Positive and Prog Negative regulators.
DAC	Provides the reference used to generate the programmable Positive and Negative Regulator Voltages.
CHANNELS TO MUX/ADC	
	DC levels of the High Voltage Channels is measured using these signals for Field Calibration.
PROG POSITIVE/NEGATIVE REGULATORS	
	These programmable regulators provide the bias power for the High Voltage channels. There are three GROUP power regulators.
CHANNELS TO MUX/ADC	
	DC levels of the High Voltage Channels is measured using these signals for Field Calibration. The ADC can also be used to monitor other board voltages including the Power Regulators.

Channel Driver & Receiver I/O

Figure E-2 illustrates Driver & Receiver I/O for a single channel.

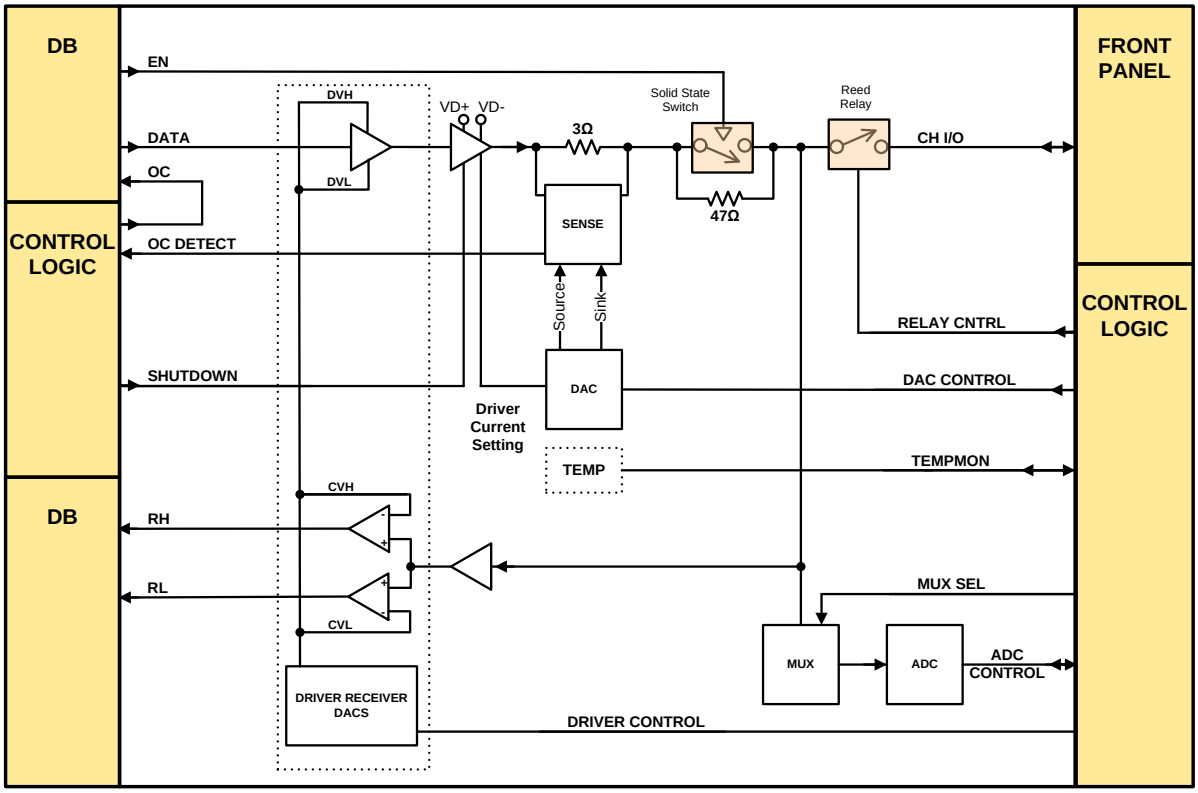


Figure E-2: DR4 Driver/Receiver Block Diagram

Signal Descriptions

DATA	Channel data output signal from the Data Sequencer to the programmable output driver.
EN	Channel enable output signal from the Data Sequencer to the solid state switch (for tristate).
OC	Over Current signal from the Control logic to the Digital Board. Detection of an OC event will disable the channel output in the Series mode.
OC DETECT	Over-Current detect from the programmable Driver sense comparator. Detection is controlled by Source Sink DAC levels. Drives the OC line to the Digital board. In Direct mode an OC DETECT will set SHUTDOWN for the driver (two adjacent channels).
DVH, DVL	Drive High level, Drive Low Level per channel
CVH, CVL	Compare High Level, Compare Low Level shared between two adjacent channels (CH1 and CH2, CH3 and CH4 etc.)
RH	Response High input signals to the Data Sequencer from the programmable input receivers. 1 = Good '1',

	0 = Good ‘0’.
RL	Response Low input signals to the Data Sequencer from the programmable input receivers. 0 = Good ‘1’, 1 = Good ‘0’.
RELAY CNTRL	Controls isolation relays,
CH I/O	This is the Bi-directional programmable I/O channel from the DR4 Drivers and Receivers to the UUT
TEMPMON	Real-time temperature monitors the PCB junction plane.
VD+, VD-	Driver Bias Power from the Programmable Regulators.

Auxiliary Driver & Receiver I/O

Figure E-3 illustrates the configuration and control of the AUXA 1-8 and the AUXB 1-8 Driver & Receiver I/Os.

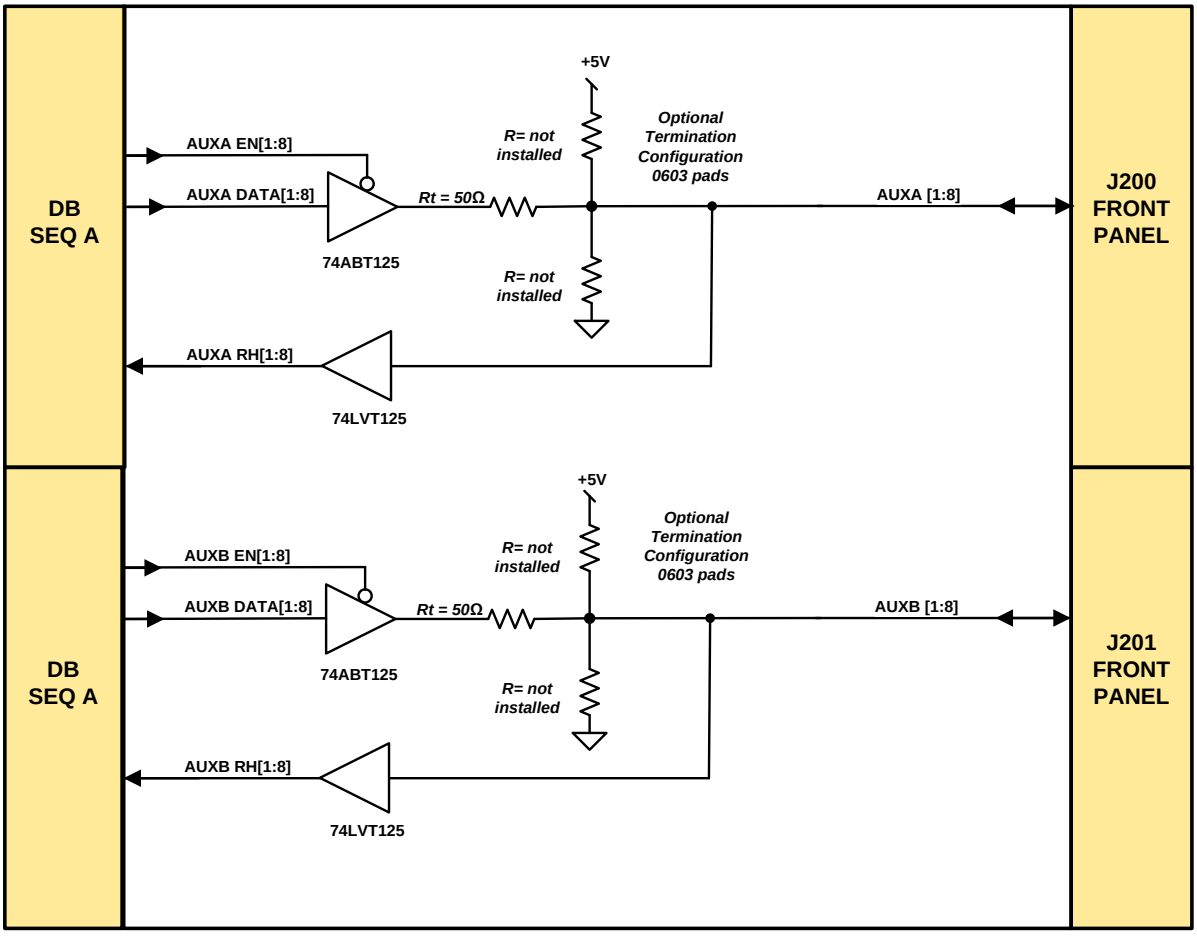


Figure E-3: Auxiliary Driver & Receiver I/O Block Diagram

Signal Descriptions

AUXA EN[5:8]	Auxiliary Enable outputs from the Data Sequencer to the TTL output buffers.
AUXA DATA[1:8]	Auxiliary Data outputs from the Data Sequencer to the TTL output buffers.
AUXA RH[1:8]	Auxiliary Response High inputs to the Data Sequencer from the TTL input buffers.
AUXA [1:8]	Eight TTL signals used to input or output test signals.
AUXB EN[1:8]	Auxiliary Enable outputs from the Data Sequencer to the TTL output buffers.
AUXB DATA[1:8]	Auxiliary Data outputs from the Data Sequencer to the TTL output buffers.
AUXB RH[1:8]	Auxiliary Response High inputs to the Data Sequencer from the TTL input buffers.
AUXB [1:8]	Eight TTL signals used to input or output test signals. DR4Driver & Receiver I/O

OPTIONAL TERMINATION CONFIGURATION;

The default termination of the TTL AUX I/O is a series 50 ohms. The pull-up and pulldown positions are unpopulated. Optional termination configurations can be specified as a Special by contacting the factory.

Power Configuration

The DR4 Power is supplied by VXI Backplane power. Figure E-4 illustrates the distribution of power to the channel groups.

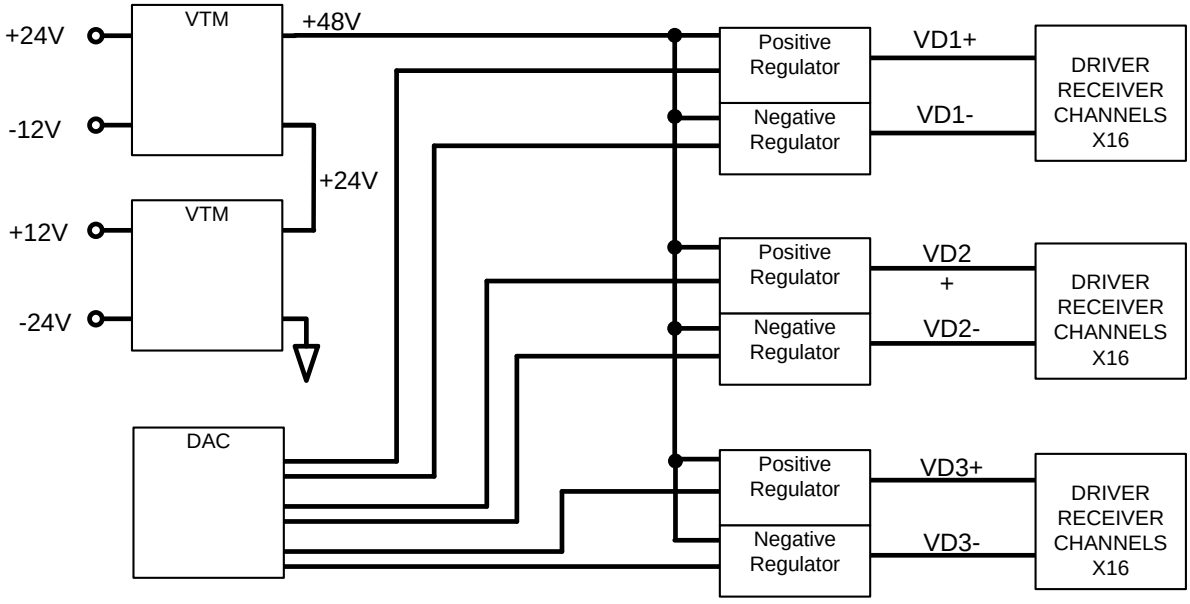


Figure E-4: DR4 Power Configuration

DR4 Characteristics

Table E-1: DR4 Characteristics

Description	Characteristics
Digital I/O Type	Variable Voltage
Channels	48 SE or 24 DIFF per Driver/Receiver board 64 per VXI slot Per channel relay isolation
Output Voltage Ranges	0 V to + 31 V -15.5 V to +15.5 V -31 V to 0 V
Output Level Granularity	Per channel (Drive High and Drive Low)
Output Voltage Swing	31 V max.
Output Resolution	< 10 mV
Output Accuracy	< ± 2% ± 100 mV
Output Drive Current	31V range ± 50 mA typical (Source/Sink) 20V range ± 65 mA typical (Source/Sink)
Output Impedance (Selectable/Channel)	5 Ω; 50 Ω ±20%
Programmable Drive Current	Programmable per group (16 Channel)
Input Threshold Ranges	0 V to + 31 V -15.5 V to +15.5 V -31 V to 0 V
Input Threshold levels	Dual Threshold
Input Threshold granularity	Per 2 channels (CVH and CVL shared)
Input Threshold Resolution	< 20 mV
Input Threshold Accuracy	< ±2% ±200 mV
Skew (Chan. to Chan.)	< 5 ns
Pin Electronics Monitoring (per channel)	All programmed levels Output and Input levels
Temperature Monitoring	Per 16 channel group junction plane monitors.
Voltage Monitoring	Real time alarms for driver voltages. Internal voltage measurements using internal ADC
Auxiliary I/O Channels	16 TTL

Power Requirements

Table E-2: VXI Power Requirements

Voltage	Peak Current	Dynamic Current
+5 V	tbd	tbd
-5.2 V	tbd	tbd
-2 V	tbd	tbd
+12 V	tbd	tbd
-12 V	tbd	tbd
+24 V	tbd	tbd
-24 V	tbd	tbd

Environmental

Temperature	Operating: 0° C to 45° C * Storage: -40° C to 70° C
Humidity	0° C to 10° C: Not controlled 10° C to 30° C: 5% to 95% ±5% RH 30° C to 40° C: 5% to 75% ±5% RH 40° C to 50° C: 5% to 55% ±5% RH
Altitude	10,000 ft
Cooling Required (10°C Rise; 2 DR4s)	Max: tbd lps @ tbd mmH^20 Typ.: tbd lps @ 4.5 mmH^20
MTBF (ground benign)	DR4: 57,630 hours T940: 180,885 hours T940-DR4: 43,705 hours
EMC (Council Directive 89/336/EEC)	Emission: EN61326-1: 2006, Class A Immunity: EN61326-1: 2006, Table 1 ***Designed to Meet***
Safety (Low Voltage Directive 73/23/EEC)	BS EN61010-1: 2010 ***Designed to Meet***

* For a DRM with 1 DR4, the 1263HPf chassis has sufficient airflow for ~25 ºC max. inlet air temperature at <~2000 ft.

DR4 Signal Description

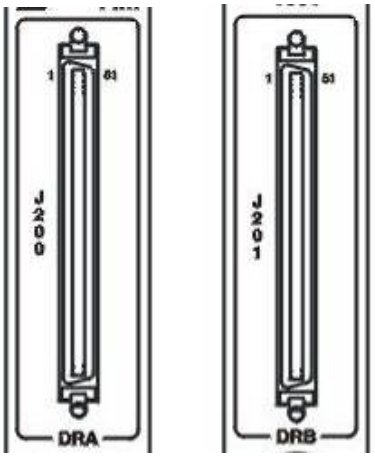


Figure E-5: J200 and J201 Connectors

DRA I/O Channels (J200)

Table E-3: DR4, DRA I/O Channels (J200)

Name	Pin No.	Description
CH1-CH24	Various	(Bi-directional) High speed channels
AUX1 A	34	(Bi-directional) General Purpose TTL I/O pin
AUX2 A	36	(Bi-directional) General Purpose TTL I/O pin
AUX3 A	38	(Bi-directional) General Purpose TTL I/O pin
AUX4 A	40	(Bi-directional) General Purpose TTL I/O pin
AUX5 A	42	(Bi-directional) General Purpose TTL I/O pin
AUX6 A	44	(Bi-directional) General Purpose TTL I/O pin
AUX7 A	84	(Bi-directional) General Purpose TTL I/O pin
AUX8 A	86	(Bi-directional) General Purpose TTL I/O pin

Table E-4: DR4 Pinout by Pin Number (DRA)

Pin No.	Signal
1	SIG_GND
2	CH1
3	SIG_GND
4	CH2
5	SIG_GND
6	CH3
7	SIG_GND
8	CH4
9	SIG_GND

Pin No.	Signal
51	SIG_GND
52	CH17
53	SIG_GND
54	CH18
55	SIG_GND
56	CH19
57	SIG_GND
58	CH20
59	SIG_GND

Pin No.	Signal
10	CH5
11	SIG_GND
12	CH6
13	SIG_GND
14	CH7
15	SIG_GND
16	CH8
17	SIG_GND
18	CH9
19	SIG_GND
20	CH10
21	SIG_GND
22	CH11
23	SIG_GND
24	CH12
25	SIG_GND
26	CH13
27	SIG_GND
28	CH14
29	SIG_GND
30	CH15
31	SIG_GND
32	CH16
33	SIG_GND
34	AUX1 A
35	SIG_GND
36	AUX2 A
37	SIG_GND
38	AUX3 A
39	SIG_GND
40	AUX4 A
41	SIG_GND
42	AUX5 A
43	SIG_GND
44	AUX6 A
45	SIG_GND
46	PBUT_A
47	PMODE_A
48	SIG_GND
49	NC
50	MONITOR A

Pin No.	Signal
60	CH21
61	SIG_GND
62	CH22
63	SIG_GND
64	CH23
65	SIG_GND
66	CH24
67	SIG_GND
68	NC
69	SIG_GND
70	NC
71	SIG_GND
72	NC
73	SIG_GND
74	NC
75	SIG_GND
76	NC
77	SIG_GND
78	NC
79	SIG_GND
80	NC
81	SIG_GND
82	NC
83	SIG_GND
84	AUX7 A
85	SIG_GND
86	AUX8 A
87	SIG_GND
88	NC
89	NC
90	NC
91	NC
92	NC
93	NC
94	NC
95	MPSIGA
96	BCLK-A
97	SIG_GND
98	EXTFORCE A
99	SIG_GND
100	NC

DRB I/O Channels (J201)

Table E-5: DR4, DRB I/O Channels (J201)

Name	Pin No.	Description
CH33-CH48	Various	(Bi-directional) High speed channels
SIG_GND	Various	Signal Ground reference
AUX1 B	34	(Bi-directional) General Purpose TTL I/O pin
AUX2 B	36	(Bi-directional) General Purpose TTL I/O pin
AUX3 B	38	(Bi-directional) General Purpose TTL I/O pin
AUX4 B	40	(Bi-directional) General Purpose TTL I/O pin
AUX5 B	42	(Bi-directional) General Purpose TTL I/O pin
AUX6 B	44	(Bi-directional) General Purpose TTL I/O pin
AUX7 B	84	(Bi-directional) General Purpose TTL I/O pin
AUX8 B	86	(Bi-directional) General Purpose TTL I/O pin

Table E-6: DR4 Pinout by Pin Number (DRB)

Pin No.	Signal	Pin No.	Signal
1	SIG_GND	51	SIG_GND
2	CH33	52	CH49
3	SIG_GND	53	SIG_GND
4	CH34	54	CH50
5	SIG_GND	55	SIG_GND
6	CH35	56	CH51
7	SIG_GND	57	SIG_GND
8	CH36	58	CH52
9	SIG_GND	59	SIG_GND
10	CH37	60	CH53
11	SIG_GND	61	SIG_GND
12	CH38	62	CH54
13	SIG_GND	63	SIG_GND
14	CH39	64	CH55
15	SIG_GND	65	SIG_GND
16	CH40	66	CH56
17	SIG_GND	67	SIG_GND
18	CH41	68	NC
19	SIG_GND	69	SIG_GND
20	CH42	70	NC
21	SIG_GND	71	SIG_GND
22	CH43	72	NC
23	SIG_GND	73	SIG_GND
24	CH44	74	NC

Pin No.	Signal
25	SIG_GND
26	CH45
27	SIG_GND
28	CH46
29	SIG_GND
30	CH47
31	SIG_GND
32	CH48
33	SIG_GND
34	AUX1 B
35	SIG_GND
36	AUX2 B
37	SIG_GND
38	AUX3 B
39	SIG_GND
40	AUX4 B
41	SIG_GND
42	AUX5 B
43	SIG_GND
44	AUX6 B
45	SIG_GND
46	PBUT_B
47	PMODE_B
48	SIG_GND
49	NC
50	MONITOR B

Pin No.	Signal
75	SIG_GND
76	NC
77	SIG_GND
78	NC
79	SIG_GND
80	NC
81	SIG_GND
82	NC
83	SIG_GND
84	AUX7 B
85	SIG_GND
86	AUX8 B
87	SIG_GND
88	NC
89	NC
90	NC
91	NC
92	NC
93	NC
94	NC
95	MPSIGB
96	BCLK
97	SIG_GND
98	EXTFORCE B
99	SIG_GND
100	NC

Calibration

Driver/Receiver boards are calibrated for each range before shipment. Field calibration can be performed using Soft Front Panel or API call.

Table E-7: Calibration Settings

ADC/Monitor	Factory calibrated stored in EEPROM
CHANNEL Measure	Factory calibrated stored in EEPROM
DVH/DVL	Field upgradable stored in EEPROM
CVH/CVL	Field upgradable stored in EEPROM

Appendix F
DR7 Driver/Receiver Board

DR7 Features

- Channels: 32 differential RS-422/485
- Auxiliary channels:
  - Four Differential RS-422/485
  - Four TTL
  - Four ECL (single ended or differential)

Front Panel Connectors

The front panel of the DR7 Driver/Receiver is shown in Chapter 3.

Block Diagram

This section describes the basic hardware configuration of the DR7 Driver/Receiver (DRA or DRB).

The DR7 is comprised of four major logic sections as shown in Figure F-1.

- Auxiliary Driver & Receiver I/O
- DR7 Driver & Receiver I/O
- Control Logic
- Firmware & NV Data

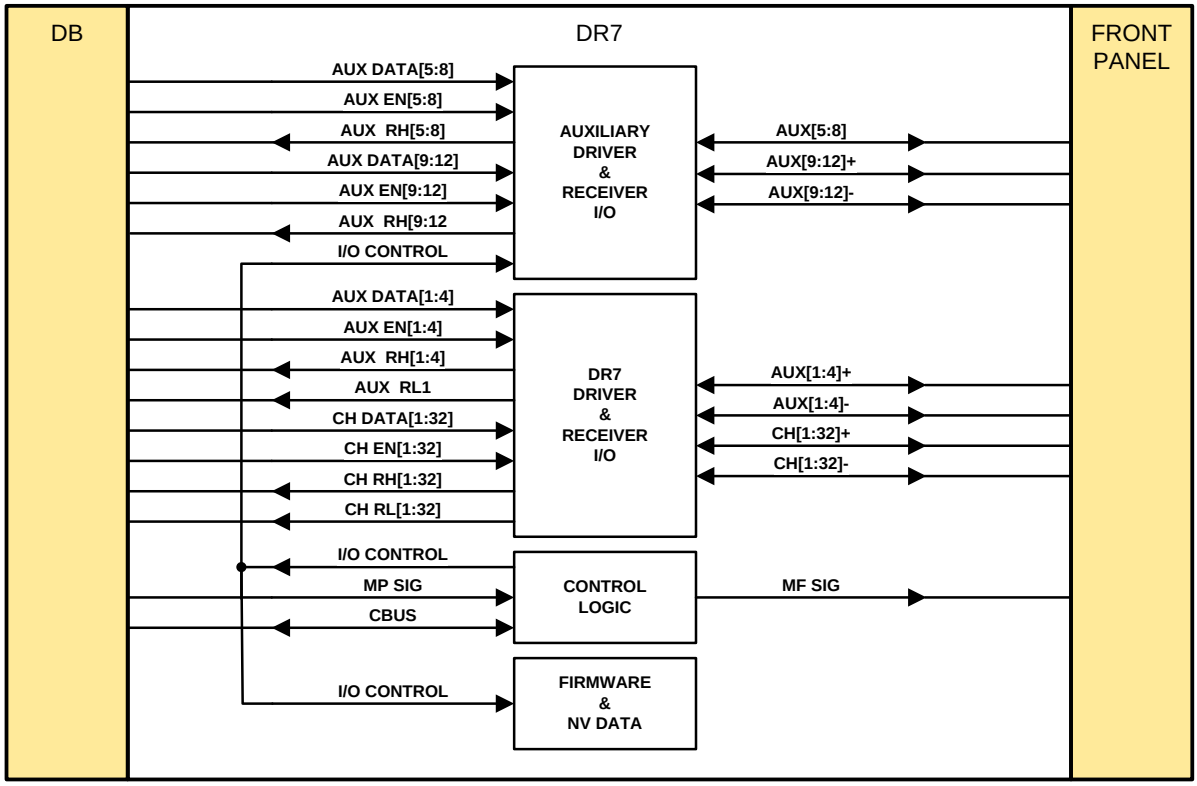


Figure F-1: DR7 Driver/Receiver Block Diagram

Auxiliary Driver & Receiver I/O

Figure F-2 illustrates the configuration and control of AUX5-8 (LVTTL) and AUX9-12 (ECL) Driver & Receiver I/O.

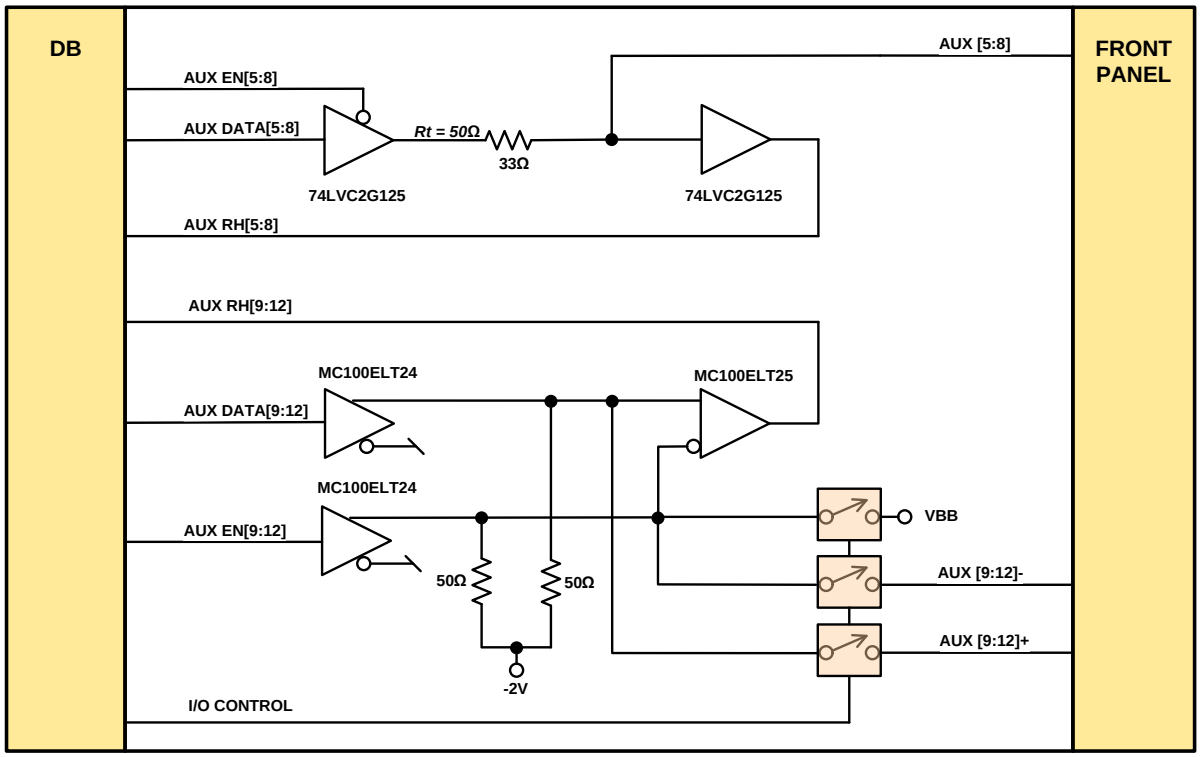


Figure F-2: Auxiliary Driver & Receiver I/O Block Diagram

Signal Descriptions

AUX EN[5:8]	Auxiliary Enable outputs from the Data Sequencer to the LVTTL output buffers.
AUX DATA[5:8]	Auxiliary Data outputs from the Data Sequencer to the LVTTL output buffers.
AUX RH[5:8]	Auxiliary Response High inputs to the Data Sequencer from the LVTTL input buffers.
AUX RH[9:12]	Auxiliary Response High inputs to the Data Sequencer from the ECL input buffers.
AUX DATA[9:12]	Auxiliary active high Data outputs from the Data Sequencer to the ECL output buffers.
AUX EN[9:12]	Auxiliary active low Data outputs from the Data Sequencer to the ECL output buffers.
EN 9-12	Auxiliary Enable outputs from the Data Sequencer to the ECL output buffers.
I/O CONTROL	Signals used to control isolation relays and ECL bipolar/differential mode.
AUX [5:8]	Four LVTTL signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
VBB	ECL input threshold (~ -1.3V).
AUX [9:12]-	Four negative differential signals used to input or output test signals. See **Configuring the AUX Channels** in

Chapter 5.

AUX [9:12]+ Four bipolar/positive differential signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.

DR7 Driver & Receiver I/O

Figure F-3 illustrates the configuration and control of the DR7 Driver & Receiver I/O (RS422/RS485).

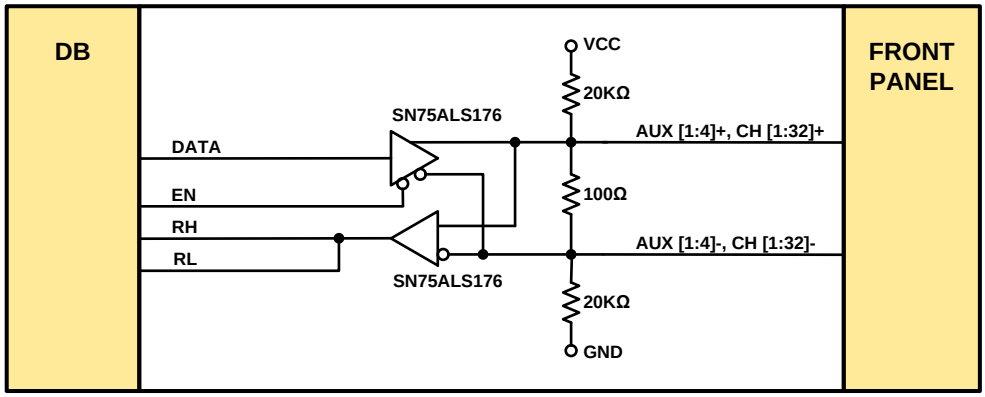


Figure F-3: DR7 Driver & Receiver I/O Block Diagram

Signal Descriptions

DATA Channel and auxiliary data output signals from the Data Sequencer to the RS422/RS485 output drivers.

EN Channel and auxiliary enable output signals from the Data Sequencer to the RS422/RS485 output drivers.

RH Response High input signals to the Data Sequencer from the RS422/RS485 input receivers. 1 = good 1, 0 = good 0.

RL Response Low input signals to the Data Sequencer from the RS422/RS485 input receivers. 0 = good 0, 1 = good 1.

AUX [1:4]+ Four positive differential RS422/RS485 signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.

AUX [1:4]- Four negative differential RS422/RS485 signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.

CH [1:32]+ These are UUT Bi-directional positive differential RS422/RS485 I/O channels from the DR7 Drivers and Receivers

CH [1:32]- These are UUT Bi-directional negative differential RS422/RS485 I/O channels from the DR7 Drivers and Receivers

Control Logic

The control logic contains the registers, memory and logic that allow the digital board to interface and configure the hardware.

Signal Descriptions

I/O CONTROL	Signals used to control isolation, termination, NV data and load relays
MP SIG	Multi-Purpose signal from the data sequencer.
CBUS	An internal Control Bus connecting the digital board to the Driver/Receiver board.
MF SIG	Multi-Function signal output to the PWR connector.

Firmware & NV Data

The Control Logic firmware is loaded via a serial PROM on power up or VXI Reset. The firmware is field upgradeable using our supplied loader utility. Nonvolatile data (serial number, assembly revision is stored in an on-board EEPROM.

Signal Descriptions

I/O CONTROL	Signals used to program firmware and NV DATA.

DR7 Characteristics

Table F-1: DR7 Characteristics

Description	Characteristics
Digital I/O Type	RS-422/485 (SN75ALS176)
Channels	32 differential per Driver/Receiver board
Output Voltage	V_{OL}: 3.0 V (max) V_{OH}: 2.0 V (min)
Differential Input Voltage	200 mV min.±6 V max.
Hysteresis	60 mV
Output Drive Current (typical)	Source/Sink: ± 60 mA
I/O Impedance	100 Ω in parallel with 20K pull-up/pull-down bias resistors to establish a True level if unconnected.
Output Skew (Channel-to-Channel)	< 3 ns (drive and compare)
Input Skew (Channel-to-Channel)	< 3 ns (drive and compare)
Auxiliary I/O Channels (per Driver/Receiver board)	RS-422/485 (4), Differential (with 20K bias resistors) TTL (4), Single-ended ECL (4), Single-ended or Differential AUX I/O is bi-directional

Description	Characteristics
	Per channel relay isolation on ECL I/O
Data Rate (max)	10 MHz (input and output)

Power Requirements

Table F-2: DR7 Power Requirements

Voltage	Peak Current	Dynamic Current
+5 V	620 mA	25 mA
-5.2 V	355 mA	25 mA
-2 V	350 mA	8.5 mA
+12 V	0	0
-12 V	0	0
+24 V	0	0
-24 V	0	0

Environmental

Temperature	Operating: 0° C to 45° C Storage: -40° C to 70° C
Humidity (non-condensing)	0° C to 10° C: Not controlled 10° C to 30° C: 5% to 95% ±5% RH 30° C to 40° C: 5% to 75% ±5% RH 40° C to 50° C: 5% to 55% ±5% RH
Altitude	10,000 ft
Cooling Required (10°C Rise; 1 DR7)	Max: 1.9 lps @ 1 mmH^20
Cooling Required (10°C Rise; 2 DR7s)	Max: 2.4 lps @ 1 mmH^20
MTBF (ground benign)	DR7: 305,905 hours T940: 180,885 hours T940-DR7: 113,670 hours T940-DR7-DR7: 69,804 hours
Dimensions	20 x 114 x 305 mm
EMC (Council Directive 89/336/EEC)	Emission: EN61326-1: 2006, Class A Immunity: EN61326-1: 2006, Table 1 ***Designed to Meet – Testing in Progress***
Safety (Low Voltage Directive 73/23/EEC)	BS EN61010-1: 2010 ***Designed to Meet – Testing in Progress***

DR7 Signal Description

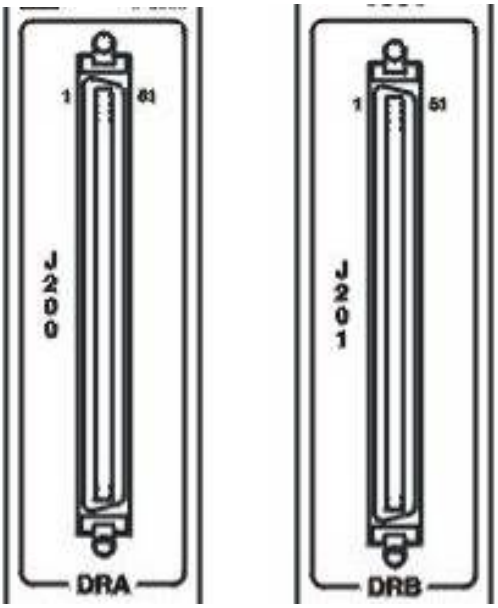


Figure F-4: J200 and J201 Connectors

DRA I/O Channels (J200)

Table F-3: DR7, DRA I/O Channels (J200)

Name	Pin No.	Description
CH1+ to CH32+	Various	(Bi-directional) RS-422/485 Positive High speed channels
CH1- to CH32-	Various	(Bi-directional) RS-422/485 Negative High speed channels
SIG_GND	Various	Signal Ground reference
AUX1+ A	34	(Bi-directional) General Purpose RS-422/485 Positive I/O pin
AUX1- A	35	(Bi-directional) General Purpose RS-422/485 Negative I/O pin
AUX2+ A	36	(Bi-directional) General Purpose RS-422/485 Positive I/O pin
AUX2- A	37	(Bi-directional) General Purpose RS-422/485 Negative I/O pin
AUX3+ A	38	(Bi-directional) General Purpose RS-422/485 Positive I/O pin
AUX3- A	39	(Bi-directional) General Purpose RS-422/485 Negative I/O pin
AUX4+ A	40	(Bi-directional) General Purpose RS-422/485 Positive I/O pin
AUX4- A	41	(Bi-directional) General Purpose RS-422/485 Negative I/O pin
AUX5 A	42	(Bi-directional) General Purpose TTL I/O pin, 51.1 Ohm series
AUX6 A	44	(Bi-directional) General Purpose TTL I/O pin, 51.1 Ohm series
AUX7 A	84	(Bi-directional) General Purpose TTL I/O pin, 51.1 Ohm series
AUX8 A	86	(Bi-directional) General Purpose TTL I/O pin, 51.1 Ohm series
AUX9+ A	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX9- A	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V

Name	Pin No.	Description
AUX10+ A	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10- A	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11+ A	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11- A	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12+ A	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12- A	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
PBUT A	46	(Bi-directional) Probe Button Input
PMODE A	47	(Output) Probe Support Output
BCLK-A	96	(Output) Reserved

Table F-4: DR7 Pinout by Pin Number (DRA)

Pin No.	Signal	Pin No.	Signal
1	SIG_GND	51	SIG_GND
2	CH1+	52	CH17+
3	CH1-	53	CH17-
4	CH2+	54	CH18+
5	CH2-	55	CH18-
6	CH3+	56	CH19+
7	CH3-	57	CH19-
8	CH4+	58	CH20+
9	CH4-	59	CH20-
10	CH5+	60	CH21+
11	CH5-	61	CH21-
12	CH6+	62	CH22+
13	CH6-	63	CH22-
14	CH7+	64	CH23+
15	CH7-	65	CH23-
16	CH8+	66	CH24+
17	CH8-	67	CH24-
18	CH9+	68	CH25+
19	CH9-	69	CH25-
20	CH10+	70	CH26+
21	CH10-	71	CH26-
22	CH11+	72	CH27+
23	CH11-	73	CH27-
24	CH12+	74	CH28+
25	CH12-	75	CH28-
26	CH13+	76	CH29+
27	CH13-	77	CH29-
28	CH14+	78	CH30+

Pin No.	Signal
29	CH14-
30	CH15+
31	CH15-
32	CH16+
33	CH16-
34	AUX1+ A
35	AUX1- A
36	AUX2+ A
37	AUX2- A
38	AUX3+ A
39	AUX3- A
40	AUX4+ A
41	AUX4- A
42	AUX5 A
43	SIG_GND
44	AUX6 A
45	SIG_GND
46	PBUT_A
47	PMODE_A
48	SIG_GND
49	NU
50	NU

Pin No.	Signal
79	CH30-
80	CH31+
81	CH31-
82	CH32+
83	CH32-
84	AUX7 A
85	SIG_GND
86	AUX8 A
87	SIG_GND
88	AUX9+ A
89	AUX9- A
90	AUX10+ A
91	AUX10- A
92	AUX11+ A
93	AUX11- A
94	AUX12+ A
95	AUX12- A
96	BCLK-A
97	SIG_GND
98	NU
99	SIG_GND
100	NU

DRB I/O Channels (J201)

Table F-5: DR7, DRB I/O Channels (J201)

Name	Pin No.	Description
CH33+ to CH64+	Various	(Bi-directional) RS-422/485 Positive High speed channels
CH33- to CH64-	Various	(Bi-directional) RS-422/485 Negative High speed channels
SIG_GND	Various	Signal Ground reference
AUX1+ B	34	(Bi-directional) General Purpose RS-422/485 Positive I/O pin
AUX1- B	35	(Bi-directional) General Purpose RS-422/485 Negative I/O pin
AUX2+ B	36	(Bi-directional) General Purpose RS-422/485 Positive I/O pin
AUX2- B	37	(Bi-directional) General Purpose RS-422/485 Negative I/O pin
AUX3+ B	38	(Bi-directional) General Purpose RS-422/485 Positive I/O pin
AUX3- B	39	(Bi-directional) General Purpose RS-422/485 Negative I/O pin
AUX4+ B	40	(Bi-directional) General Purpose RS-422/485 Positive I/O pin
AUX4- B	41	(Bi-directional) General Purpose RS-422/485 Negative I/O pin
AUX5 B	42	(Bi-directional) General Purpose TTL I/O pin, 51.1 Ohm series
AUX6 B	44	(Bi-directional) General Purpose TTL I/O pin, 51.1 Ohm series
AUX7 B	84	(Bi-directional) General Purpose TTL I/O pin, 51.1 Ohm series
AUX8 B	86	(Bi-directional) General Purpose TTL I/O pin, 51.1 Ohm series
AUX9+ B	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX9- B	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10+ B	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10- B	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11+ B	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11- B	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12+ B	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12- B	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
PBUT B	46	(Bi-directional) Probe Button Input
PMODE B	47	(Output) Probe Support Output
BCLK B	96	(Output) Reserved

Calibration

Table F-6: Calibration Settings

Inter-module timing deskew	Static
End-of-cable deskew	Static

Appendix G
DR8 Driver/Receiver Board

DR8 Features

- Channels: 32 single-ended TTL
- Relay Isolation on all I/O and AUX channels
- Selectable resistive input load to VCC (+5.0 V), ground or both
- Direct or 50/100 ohm selectable output impedance
- Auxiliary channels
  - Four TTL with selectable output impedance and resistive input load
  - Four TTL
  - Four ECL (single ended or differential)

Front Panel Connectors

The front panel of the DR8 Driver/Receiver is shown in Chapter 3.

Block Diagram

This section describes the basic hardware configuration of the DR8 Driver/Receiver (DRA or DRB).

The DR8 is comprised of four major logic sections as shown in Figure G-1.

- Auxiliary Driver & Receiver I/O
- Channels Driver & Receiver I/O
- Control Logic
- Firmware & NV Data

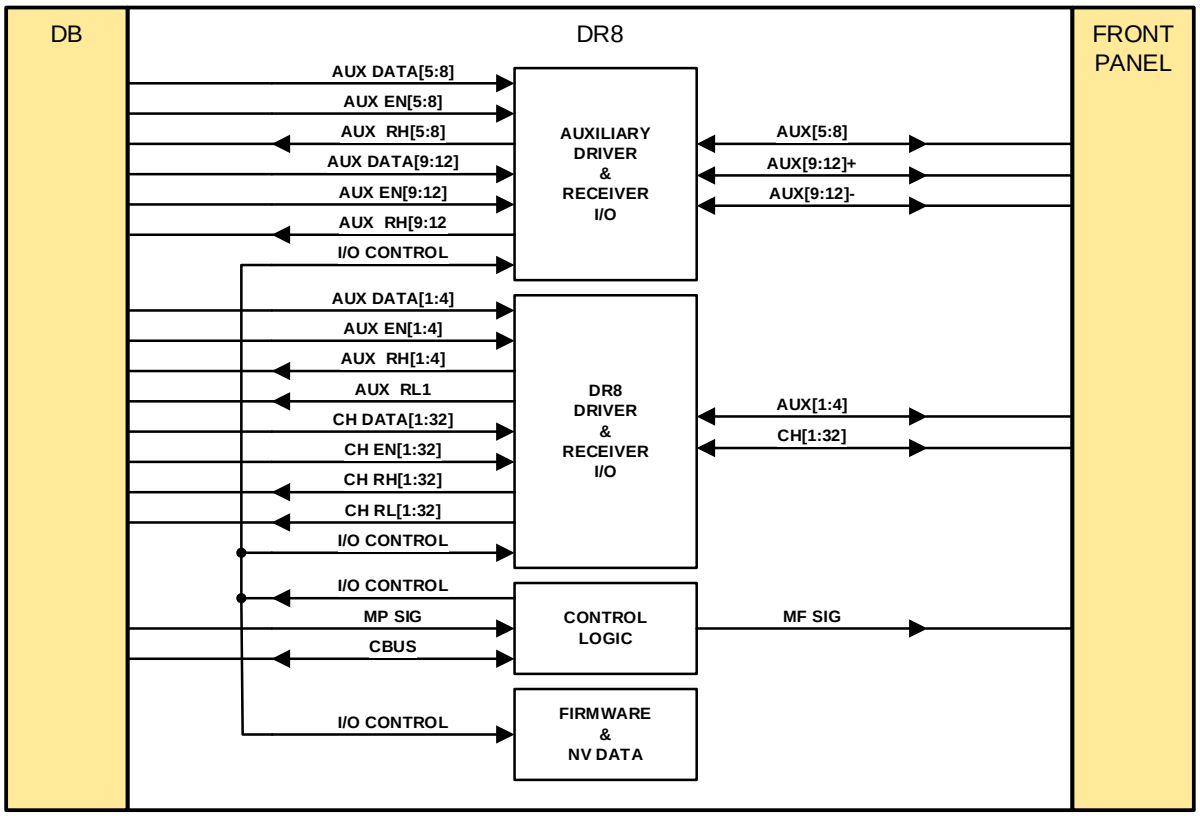


Figure G-1: DR8 Driver/Receiver Block Diagram

Auxiliary Driver & Receiver I/O

Figure G-2 illustrates the configuration and control of AUX5-8 (TTL) and AUX9-12 (ECL) Driver & Receiver I/O.

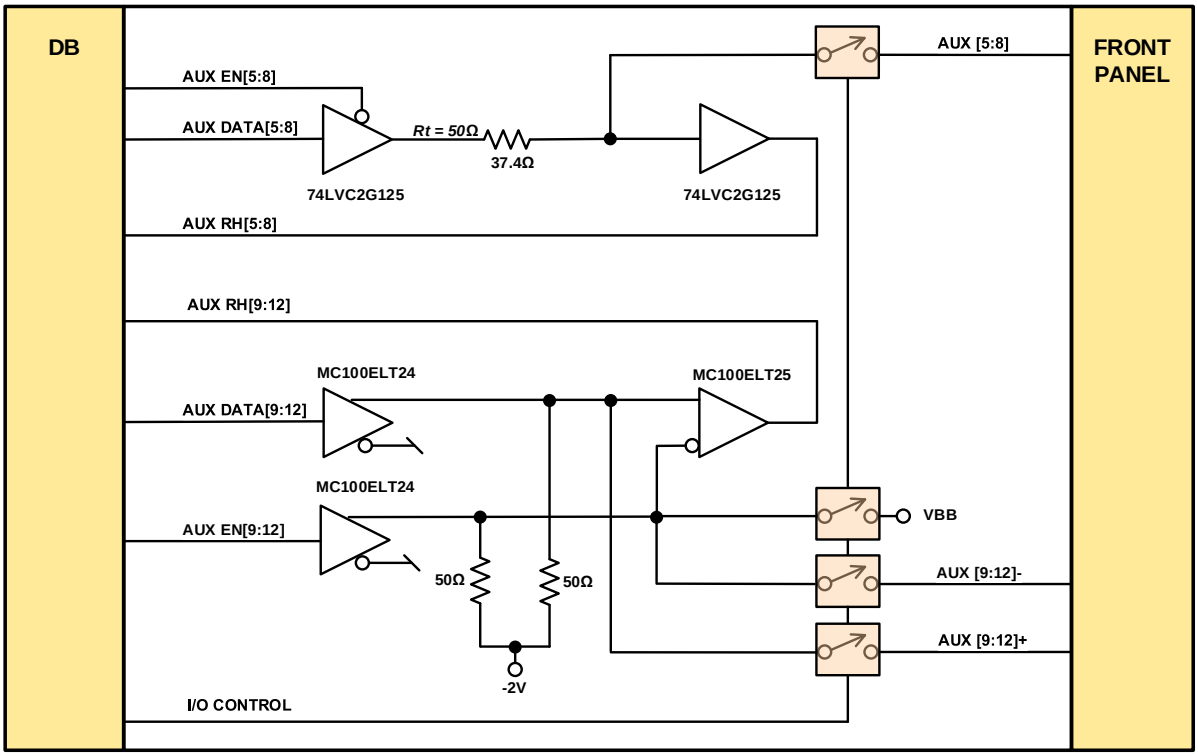


Figure G-2: Auxiliary Driver & Receiver I/O Block Diagram

Signal Descriptions

AUX EN[5:8]	Auxiliary Enable outputs from the Data Sequencer to the TTL output buffers.
AUX DATA[5:8]	Auxiliary Data outputs from the Data Sequencer to the TTL output buffers.
AUX RH[5:8]	Auxiliary Response High inputs to the Data Sequencer from the TTL input buffers.
AUX RH[9:12]	Auxiliary Response High inputs to the Data Sequencer from the ECL input buffers.
AUX DATA[9:12]	Auxiliary active high Data outputs from the Data Sequencer to the ECL output buffers.
AUX EN[9:12]	Auxiliary active low Data outputs from the Data Sequencer to the ECL output buffers.
I/O CONTROL	Signals used to control isolation relays and ECL bipolar/differential mode.
AUX [5:8]	Four TTL signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
VBB	ECL input threshold (~ -1.3V).
AUX [9:12]-	Four negative differential signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
AUX [9:12]+	Four bipolar/positive differential signals used to input or output test signals. See **Configuring the AUX Channels**

in **Chapter 5**.

DR8 Driver & Receiver I/O

Figure G-3 illustrates the configuration and control of the DR8 Driver & Receiver I/O (TTL).

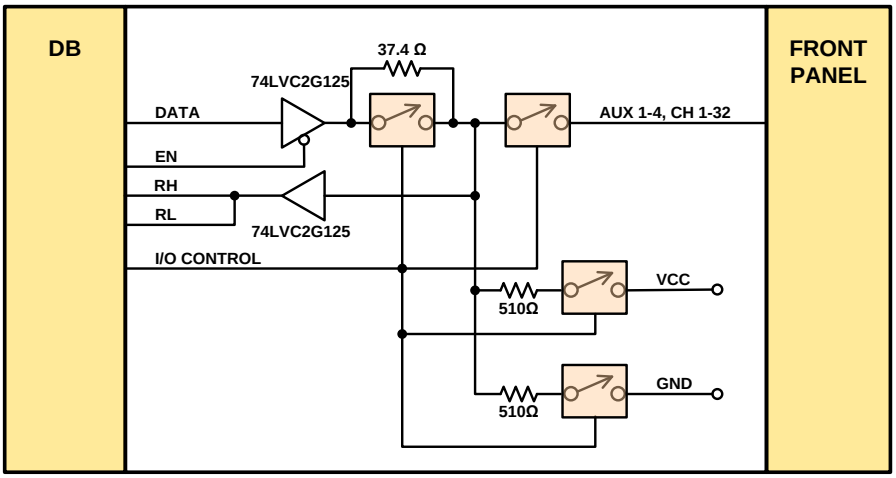


Figure G-3: DR8 Driver & Receiver I/O Block Diagram

Signal Descriptions

DATA	Channel and auxiliary data output signals from the Data Sequencer to the TTL output drivers.
EN	Channel and auxiliary enable output signals from the Data Sequencer to the TTL output drivers.
RH	Response High input signals to the Data Sequencer from the TTL input receivers. 1 = good 1, 0 = good 0.
RL	Response Low input signals to the Data Sequencer from the TTL input receivers. 0 = good 0, 1 = good 1.
AUX 1-4	Four TTL signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
CH 1-32	These are UUT Bi-directional TTL I/O channels from the DR8 Drivers and Receivers.
VCC	TTL Power (~5.0V).

Control Logic

The control logic contains the registers, memory and logic that allow the digital board to interface and configure the hardware.

Signal Descriptions

I/O CONTROL	Signals used to control isolation, termination, NV data and load relays

MP SIG	Multi-Purpose signal from the data sequencer.
CBUS	An internal Control Bus connecting the digital board to the Driver/Receiver board.
MF SIG	Multi-Function signal output to the PWR connector.

Firmware & NV Data

The Control Logic firmware is loaded via a serial PROM on power up or VXI Reset. The firmware is field-upgradeable using our supplied loader utility. Nonvolatile data (serial number, assembly revision is stored in an on-board EEPROM.

Signal Descriptions

I/O CONTROL	Signals used to program firmware and NV DATA.

DR8 Characteristics

Table G-1: DR8 Characteristics

Description	Characteristics
Digital I/O Type	TTL (74LVC2G125)
Channels	32 single-ended (SE) per I/O board Per channel relay isolation
Output Voltage	V_{OL}: 0.55 V (max) V_{OH}: 3.8 V (min)
Output Drive Current (typical)	Source/Sink: 32 mA
Output Impedance (Program selectable per pin)	Direct or 100 Ω Series (-101) Direct or 50 Ω Series (-102)
Input Voltage	V_{IL}: 0.8 V (max) V_{IH}: 2.0 V (min)
Input Impedance (Program selectable per pin)	~600 Ω[1] pull-up to VCC (+5.0 V) 510 Ω pull-down to ground (Ch1-32, Aux1-4 only)
Skew (Channel-to-Channel)	< 3 ns (drive and compare)
Auxiliary I/O Channels (per I/O board)	TTL (Aux 1-4) Like the channels with optional pull-up and pull-down TTL (Aux 5-8) ECL (Aux 9-12) Single-ended or Differential AUX I/O is bi-directional Per channel relay isolation
Data Rate (max)	50 MHz (input and output)

Note 1: Includes switch impedance of ~90 ohms

Power Requirements

Table G-2: DR8 Power Requirements

Voltage	Peak Current	Dynamic Current
+5 V	4.3 A	25 mA
-5.2 V	2.5 A	1 mA
-2 V	608 mA	7.4 mA
+12 V	0	0
-12 V	0	0
+24 V	0	0
-24 V	0	0

Environmental

Temperature	Operating: 0° C to 45° C Storage: -40° C to 70° C
Humidity (non-condensing)	0° C to 10° C: Not controlled 10° C to 30° C: 5% to 95% ±5% RH 30° C to 40° C: 5% to 75% ±5% RH 40° C to 50° C: 5% to 55% ±5% RH
Altitude	10,000 ft
Cooling Required (10°C Rise; 2 DR8s)	Max: 4.68 lps @ 8.9 mmH^{2}0 Typ.: 4.60 lps @ 4.5 mmH^{2}0
Front Panel Current Requirements	NA
MTBF (ground benign)	DR8: 257,335 hours T940: 180,885 hours T940-DR8: 106,220 hours T940-DR8-DR8: 66,922 hours
Dimensions	20 x 114 x 305 mm
EMC (Council Directive 89/336/EEC)	Emission: EN61326-1: 2006, Class A Immunity: EN61326-1: 2006, Table 1 ***Designed to Meet – Testing in Progress***
Safety (Low Voltage Directive 73/23/EEC)	BS EN61010-1: 2010 ***Designed to Meet – Testing in Progress***

DR8 Signal Description

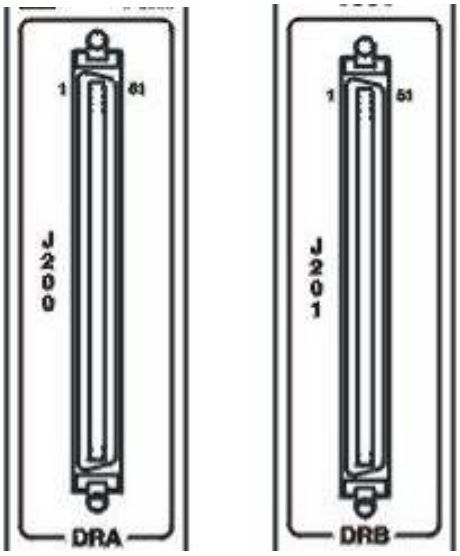


Figure G-4: J200 and J201 Connectors

DRA I/O Channels (J200)

Table G-3: DR8, DRA I/O Channels (J200)

Name	Pin No.	Description
CH1-CH32	Various	(Bi-directional) High speed TTL channels
SIG_GND	Various	Signal Ground reference
AUX1 A	34	(Bi-directional) General Purpose I/O pin
AUX2 A	36	(Bi-directional) General Purpose TTL I/O pin
AUX3 A	38	(Bi-directional) General Purpose TTL I/O pin
AUX4 A	40	(Bi-directional) General Purpose TTL I/O pin
AUX5 A	42	(Bi-directional) General Purpose TTL I/O pin, 50 Ω series
AUX6 A	44	(Bi-directional) General Purpose TTL I/O pin, 50 Ω series
AUX7 A	84	(Bi-directional) General Purpose TTL I/O pin, 50 Ω series
AUX8 A	86	(Bi-directional) General Purpose TTL I/O pin, 50 Ω series
AUX9+ A	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ω to -2V
AUX9- A	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ω to -2V
AUX10+ A	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ω to -2V
AUX10- A	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ω to -2V
AUX11+ A	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ω to -2V
AUX11- A	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ω to -2V
AUX12+ A	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ω to -2V
AUX12- A	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ω to -2V
PBUT A	46	(Bi-directional) Probe Button Input
PMODE A	47	(Output) Probe Support Output
BCLK-A	96	(Output) Reserved

Table G-4: DR8 Pin out by Pin Number (DRA)

Pin No.	Signal	Pin No.	Signal
1	SIG_GND	51	SIG_GND
2	CH1	52	CH17
3	SIG_GND	53	SIG_GND
4	CH2	54	CH18
5	SIG_GND	55	SIG_GND
6	CH3	56	CH19
7	SIG_GND	57	SIG_GND
8	CH4	58	CH20
9	SIG_GND	59	SIG_GND
10	CH5	60	CH21
11	SIG_GND	61	SIG_GND
12	CH6	62	CH22
13	SIG_GND	63	SIG_GND
14	CH7	64	CH23
15	SIG_GND	65	SIG_GND
16	CH8	66	CH24
17	SIG_GND	67	SIG_GND
18	CH9	68	CH25
19	SIG_GND	69	SIG_GND
20	CH10	70	CH26
21	SIG_GND	71	SIG_GND
22	CH11	72	CH27
23	SIG_GND	73	SIG_GND
24	CH12	74	CH28
25	SIG_GND	75	SIG_GND
26	CH13	76	CH29
27	SIG_GND	77	SIG_GND
28	CH14	78	CH30
29	SIG_GND	79	SIG_GND
30	CH15	80	CH31
31	SIG_GND	81	SIG_GND
32	CH16	82	CH32
33	SIG_GND	83	SIG_GND
34	AUX1 A	84	AUX7 A
35	SIG_GND	85	SIG_GND
36	AUX2 A	86	AUX8 A
37	SIG_GND	87	SIG_GND
38	AUX3 A	88	AUX9+ A

Pin No.	Signal
39	SIG_GND
40	AUX4 A
41	SIG_GND
42	AUX5 A
43	SIG_GND
44	AUX6 A
45	SIG_GND
46	PBUT_A
47	PMODE_A
48	SIG_GND
49	NC
50	NC

Pin No.	Signal
89	AUX9- A
90	AUX10+ A
91	AUX10- A
92	AUX11+ A
93	AUX11- A
94	AUX12+ A
95	AUX12- A
96	BCLK-A
97	SIG_GND
98	NC
99	SIG_GND
100	NC

DRB I/O Channels (J201)

Table G-5: DR8, DRB I/O Channels (J201)

Name	Pin No.	Description
CH33-CH64	Various	(Bi-directional) High speed TTL channels
SIG_GND	Various	Signal Ground reference
AUX1 B	34	(Bi-directional) General Purpose TTL I/O pin
AUX2 B	36	(Bi-directional) General Purpose TTL I/O pin
AUX3 B	38	(Bi-directional) General Purpose TTL I/O pin
AUX4 B	40	(Bi-directional) General Purpose TTL I/O pin
AUX5 B	42	(Bi-directional) General Purpose TTL I/O pin, 50 Ohm series
AUX6 B	44	(Bi-directional) General Purpose TTL I/O pin, 50 Ohm series
AUX7 B	84	(Bi-directional) General Purpose TTL I/O pin, 50 Ohm series
AUX8 B	86	(Bi-directional) General Purpose TTL I/O pin, 50 Ohm series
AUX9+ B	88	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX9- B	89	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10+ B	90	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX10- B	91	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11+ B	92	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX11- B	93	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12+ B	94	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
AUX12- B	95	(Bi-directional) General Purpose ECL I/O pin, 51.1 Ohm to -2 V
PBUT B	46	(Bi-directional) Probe Button Input
PMODE B	47	(Output) Probe Support Output
BCLK B	96	(Output) Reserved

Table G-6: DR8 Pin out by Pin Number (DRB)

Pin No.	Signal	Pin No.	Signal
1	SIG_GND	51	SIG_GND
2	CH33	52	CH49
3	SIG_GND	53	SIG_GND
4	CH34	54	CH50
5	SIG_GND	55	SIG_GND
6	CH35	56	CH51
7	SIG_GND	57	SIG_GND
8	CH36	58	CH52
9	SIG_GND	59	SIG_GND
10	CH37	60	CH53
11	SIG_GND	61	SIG_GND
12	CH38	62	CH54
13	SIG_GND	63	SIG_GND
14	CH39	64	CH55
15	SIG_GND	65	SIG_GND
16	CH40	66	CH56
17	SIG_GND	67	SIG_GND
18	CH41	68	CH57
19	SIG_GND	69	SIG_GND
20	CH42	70	CH58
21	SIG_GND	71	SIG_GND
22	CH43	72	CH59
23	SIG_GND	73	SIG_GND
24	CH44	74	CH60
25	SIG_GND	75	SIG_GND
26	CH45	76	CH61
27	SIG_GND	77	SIG_GND
28	CH46	78	CH62
29	SIG_GND	79	SIG_GND
30	CH47	80	CH63
31	SIG_GND	81	SIG_GND
32	CH48	82	CH64
33	SIG_GND	83	SIG_GND
34	AUX1 B	84	AUX7 B
35	SIG_GND	85	SIG_GND
36	AUX2 B	86	AUX8 B
37	SIG_GND	87	SIG_GND
38	AUX3 B	88	AUX9+ B
39	SIG_GND	89	AUX9- B
40	AUX4 B	90	AUX10+ B

Pin No.	Signal
41	SIG_GND
42	AUX5 B
43	SIG_GND
44	AUX6 B
45	SIG_GND
46	PBUT_B
47	PMODE_B
48	SIG_GND
49	NC
50	NC

Pin No.	Signal
91	AUX10- B
92	AUX11+ B
93	AUX11- B
94	AUX12+ B
95	AUX12- B
96	BCLK
97	SIG_GND
98	NC
99	SIG_GND
100	NC

PWR Connector

When connected to an installed DR8 board, the PWR connector (Figure G-5) only utilizes the pins for the multi-function signal (MFSIG) and signal ground (GND). The power pins are not connected to the board.

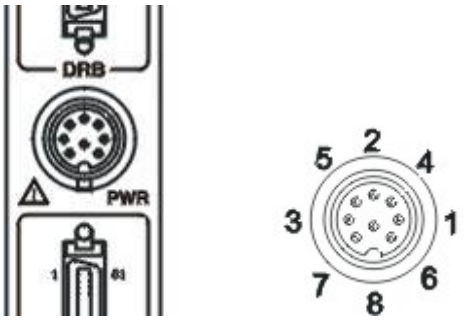


Figure G-5: Front Panel PWR Connector

When installing the Driver/Receiver Board, be sure that the correctly marked PWR cable (inside the module) is connected to its specific board – the cable marked DRA for the DRA board and marked DRB for the DRB board. Incorrect installation may cause you to be connected to the wrong MFSIG.

Table G-7 shows the connection names, pins, and descriptions for the PWR connector.

Table G-7: PWR Connector

Name	Pin No.	Description
DRB MFSIG	2	(Output) Multi-function signal DRB
DRB GND	4	Power supply signal return DRB
DRA MFSIG	6	(Output) Multi-function signal DRA
DRA GND	7	Power supply signal return DRA

Calibration

Table G-8: Calibration Settings

Inter-module timing deskew	Static
End-of-cable deskew	Static

Appendix H
DR9 Driver/Receiver Board

DR9 Features

- Channels: 24 single-ended variable voltage or 12 differential channels
- Voltage range: -15 V to +24 V with an output swing of up to 24 V
- Relay Isolation on all I/O channels.
- 24 Analog connection relays, one per I/O channel
- Provides full drive current on all channels simultaneously
- Programmable current load with dual commutating voltages
- Selectable resistive input load (8 choices) to a programmed voltage
- Selectable slew rate (0.25 V/ns to 1.5 V/ns)
- 12/50 ohm selectable output impedance
- Over-current detection
- Over-voltage detection
- Auxiliary channels:
  - Four LVTTL (no relay isolation)

Front Panel Connectors

The front panel of the DR9 Driver/Receiver board is shown in Figure H-1.

Note: *The orientations of Pin 1 in J1A and J1B are different than the orientations of the other connectors.*

Note: *J9A and J9B are auxiliary channel connectors used for calibration purposes and for access to LVTTL AUX lines for test purposes or to access them for their functionality.*

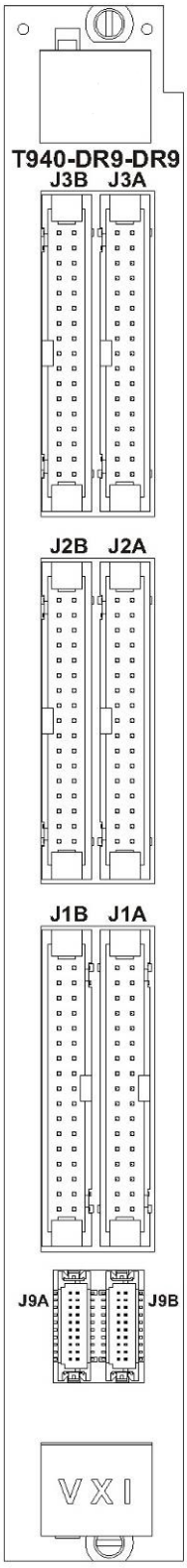


Figure H-1: DR9 Front Panel Connectors

Block Diagram

This section describes the basic hardware configuration of the DR9 Driver/Receiver (DRA or DRB).

The DR9 is comprised of four major logic sections as shown in Figure H-2.

- Auxiliary Driver & Receiver I/O
- DR9 Driver & Receiver I/O
- Control Logic
- Firmware & NV Data

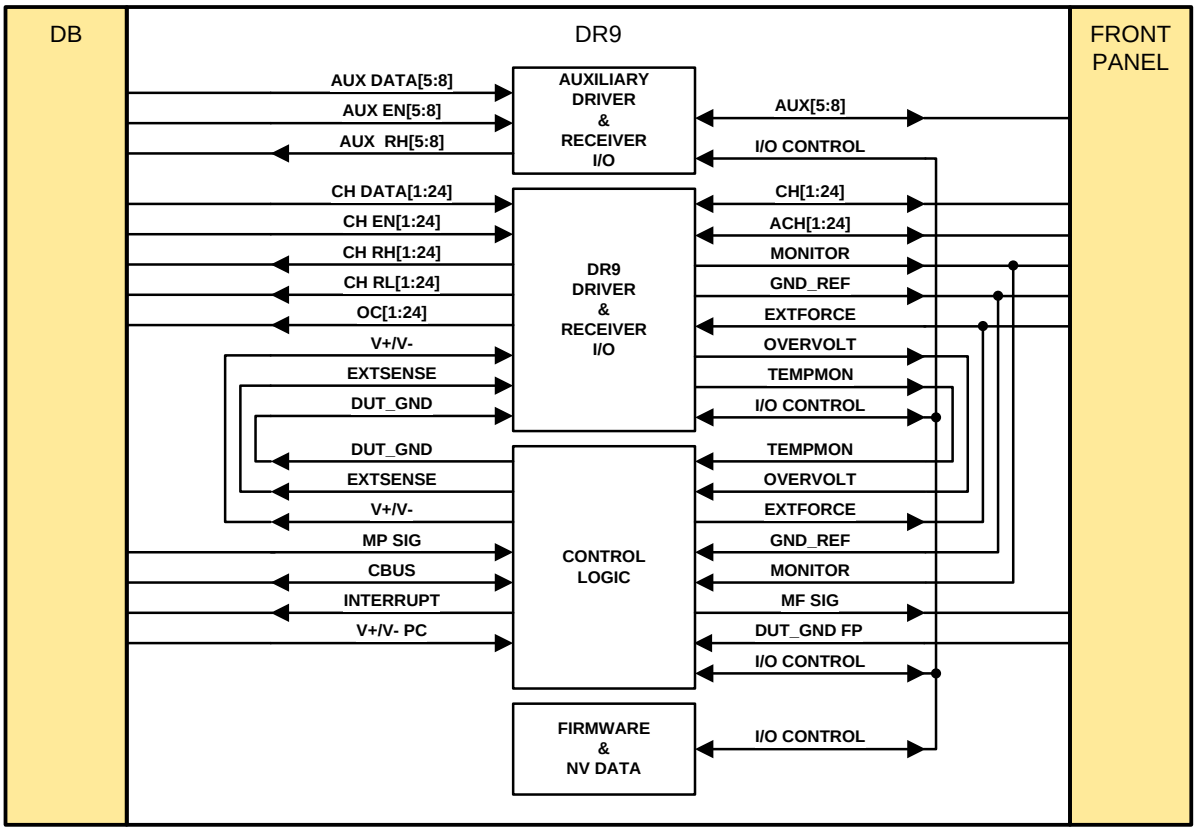


Figure H-2: DR9 Driver/Receiver Block Diagram

Auxiliary Driver & Receiver I/O

Figure H-3 illustrates the configuration and control of AUX5-8 (LVTTL) Driver & Receiver I/O.

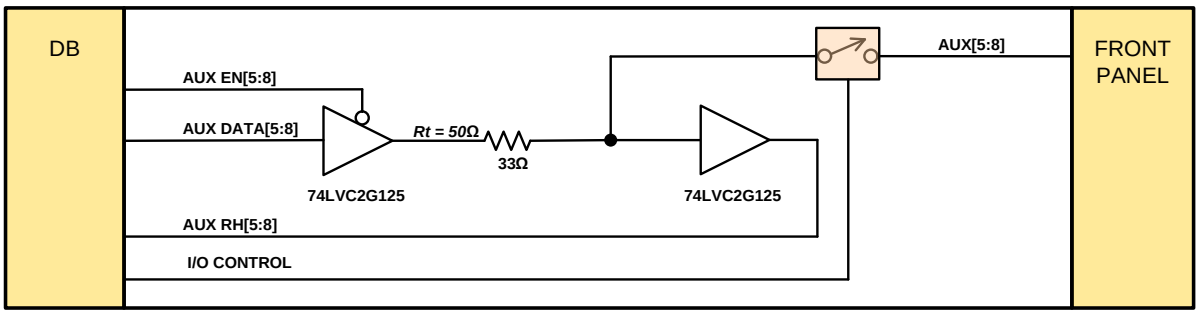


Figure H-3: Auxiliary Driver & Receiver I/O Block Diagram

Signal Descriptions

AUX EN[5:8]	Auxiliary Enable outputs from the Data Sequencer to the LVTTL output buffers.
AUX DATA[5:8]	Auxiliary Data outputs from the Data Sequencer to the LVTTL output buffers.
AUX RH[5:8]	Auxiliary Response High inputs to the Data Sequencer from the LVTTL input buffers.
I/O CONTROL	Signals used to control isolation relays.
AUX[5:8]	Four LVTTL signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.

DR9 Driver & Receiver I/O

Figure H-4 illustrates the configuration and control of the DR9 Driver & Receiver I/O.

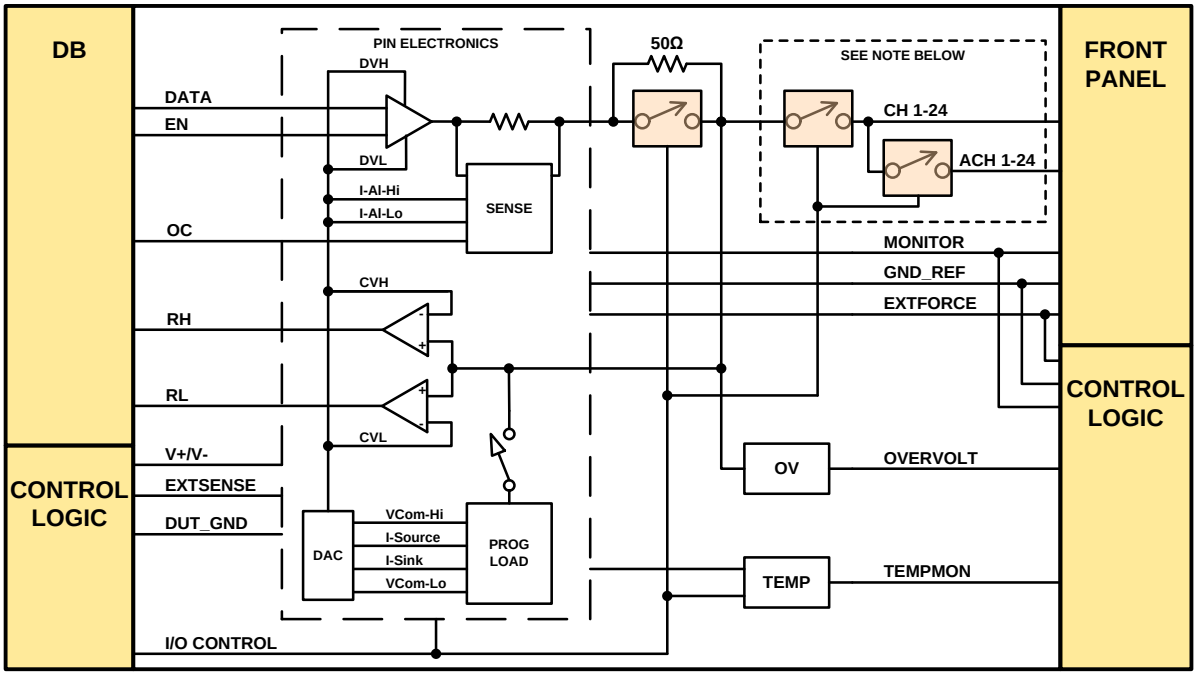


Figure H-4: DR9 Driver & Receiver I/O Block Diagram

Note: *There are two important features associated with the Analog Channel and Digital Channel relay control logic. First, these relay connections are exclusive; if the CH1 connection relay is CLOSED the ACH1 relay cannot be closed. Second, the control logic is implemented to provide a "Break-Before-Make" connection to protect the Pin Electronics from potential damage. Analog Channel connections have voltage specifications that are far beyond the ability of the DR9 overvoltage detection and protection circuitry to reliably operate. Programming an Analog Channel relay opens the associated Digital Channel relay if it is closed. There is a 5 ms latency after making the Analog Channel relay connection to ensure that the Digital Channel relay has had time to open.*

Signal Descriptions

DATA	Channel and auxiliary data output signals from the Data Sequencer to the programmable output drivers.
EN	Channel and auxiliary enable output signals from the Data Sequencer to the programmable output drivers.
OC	Over-Current detect from the programmable Driver and Receiver channels.
RH	Response High input signals to the Data Sequencer from the programmable input receivers. 1 = good 1, 0 = good 0.
RL	Response Low input signals to the Data Sequencer from the programmable input receivers. 0 = good 0,

	1 = good 1.
V+/V-	Bias Power required for operation of the Pin Electronics devices.
EXTSENSE	Pin electronics signal used for calibration.
DUT_GND	This signal comes from the UUT and can be used to offset the reference levels up to ±3V. Excursions of DUT_GND beyond ±390 mV with respect to signal ground yield a GND FAULT signal.
I/O CONTROL	Control Logic signals to control isolation relays, termination, pin electronics and temperature thresholds.
CH 1-24	UUT Bi-directional programmable I/O channels from the DR9 Drivers and Receivers
ACH 1-24	These provide a means to connect to the DR9 DIGITAL CHANNELS to ANALOG TEST resources. The DIGITAL CHANNEL isolation relay is opened before the ANALOG CHANNEL relay is closed to avoid damage to the Pin Electronics (Break-Before-Make).
MONITOR	This is an analog output signal from the Pin Electronics devices which can be used to monitor DAC levels even the Channel I/O levels. This signal is used with the internal ADC but a buffered version also comes out the Front Panel.
GND_REF	This is the ground reference output signal from the Pin Electronics devices. It is used with MONITOR to make accurate ADC measurements. A buffered version also comes out the Front Panel.
EXTFORCE	External Force is an analog I/O signal which is connected to all of the Pin Electronics devices and can be used to force a level on the output of the driver. It may also be used to monitor a channel's state. EXTFORCE is also used for calibration.
OVERVOLT	Real-time over-voltage detector circuit monitors Driver and Receivers to protect the pin electronics. Also clamps the inputs to the V± rails.
TEMPMON	Real-time temperature monitors for the pin electronics.

Control Logic

The control logic contains the registers, memory and logic that allow the digital board to interface and configure the hardware. See Figure H-5.

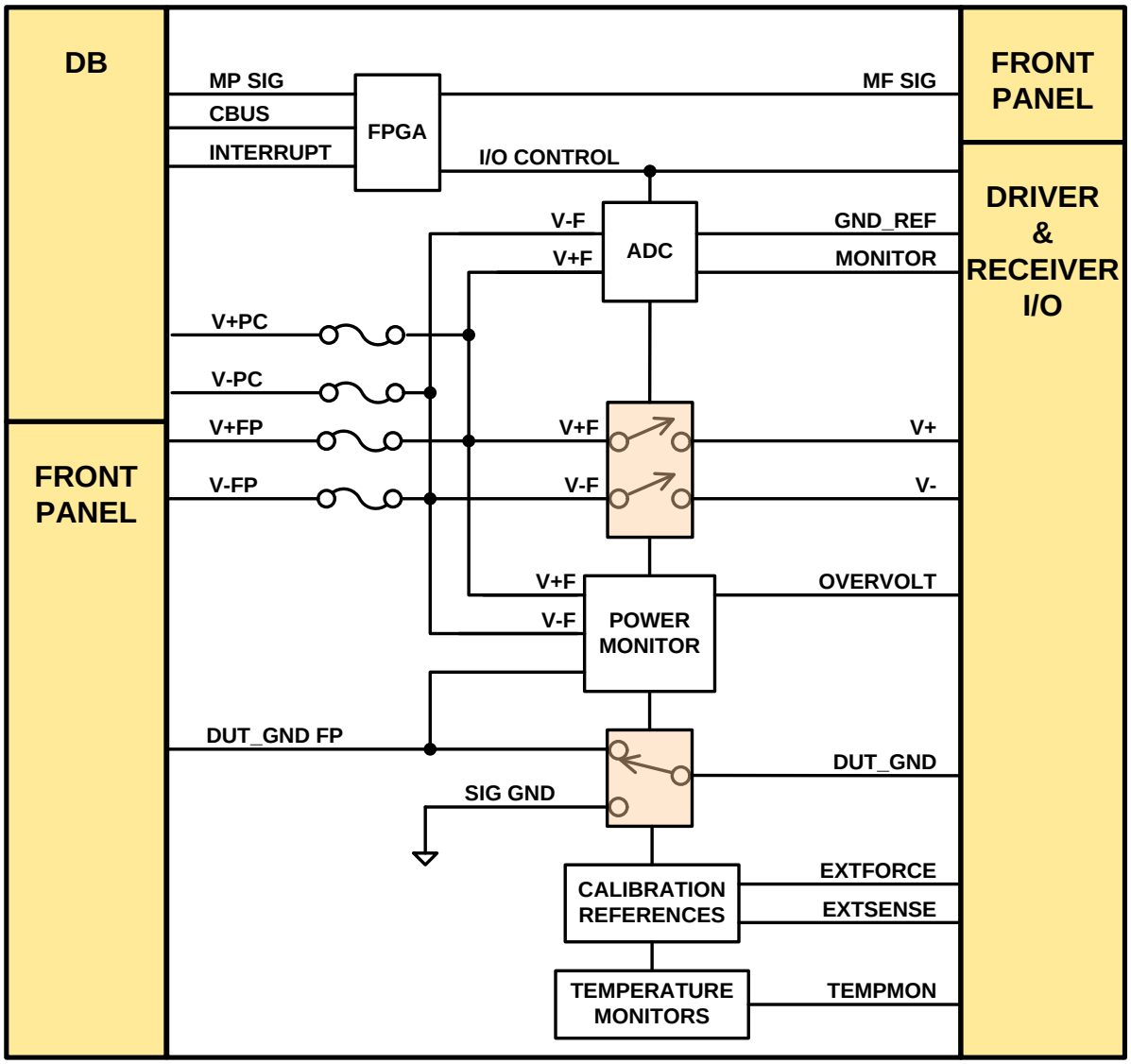


Figure H-5: DR9 Control Logic Block Diagram

Signal Descriptions

MP SIG	Multi-Purpose signal from the data sequencer.
CBUS	An internal Control Bus connecting the digital board to the Driver/Receiver board.
INTERRUPT	Real time signal generated from the power and temperature monitor data.
V+PC	Positive bias power required for operation of the Pin Electronics devices from the T940 power converter.
V-PC	Negative bias power required for operation of the Pin Electronics devices from the T940 power converter.
DUT_GND FP	This signal comes from the UUT and can be used to offset the reference levels up to ±3 V. Excursions of DUT_GND

	beyond ±390 mV with respect to signal ground yields a GND FAULT signal.
MF SIG	Multi-Function signal output to the PWR connector.
I/O CONTROL	Signals used to program the features of the DR9 Driver/Receiver board.
GND_REF	This is the ground reference output signal from the Pin Electronics devices. It is used with MONITOR to make accurate ADC measurements.
V+	Fused and switched positive bias power required for operation of the Pin Electronics devices.
V-	Fused and switched negative bias power required for operation of the Pin Electronics devices.
OVERVOLT	Real-time over-voltage detector circuit monitors Driver and Receivers to protect the pin electronics. Also clamps the inputs to the V+/- rails.
DUT_GND	Either the front panel DUT_GND signal or SIG GND.
EXTFORCE	Pin electronics signal used for calibration.
EXTSENSE	Pin electronics signal used for calibration.
TEMPMON	Real-time temperature monitors for the pin electronics

Firmware & NV Data

The Control Logic firmware is loaded via a serial PROM on power up or VXI Reset. The firmware is field upgradeable using our supplied loader utility. Nonvolatile data (serial number, assembly revision is stored in an on-board EEPROM.

Signal Descriptions

I/O CONTROL	Signals used to program firmware and NV DATA.

DR9 Characteristics

Table H-1: DR9 Characteristics

Description	Characteristics
Digital I/O Type	Variable Voltage
Digital Channels	24 SE or 12 DIFF per Driver/Receiver board 48 per VXI slot Per channel relay isolation
Analog Channels	24 Analog Connections per Driver/Receiver Board 48 per VXI slot
Output Voltage Ranges* (Selectable/Sequencer)	-15 V to +17 V (VM0) -7 V to +24 V (VM1)
Output Voltage Swing	500 mV [1] to 24 V

Description	Characteristics
Output Resolution	< 5 mV
Output Accuracy (DVH and DVL)	± (50mV + 1% of PV) Slow, Default, Medium slew settings ± (75mV + 1% of PV) Fast slew setting
Output Drive Current	± 85 mA typical (Source/Sink)
Output Impedance (Selectable/Channel)	Direct (12 Ω) or Series (50 Ω), ± 4 Ω
Slew Rate (Selectable/Channel or custom)	0.25 V/ns 0.7 V/ns, 1.0 V/ns or 1.3 V/ns: typical
Input Threshold Ranges*	-14.75 V to +14 V (VM0) -6.75 V to +21 V (VM1)
Input Threshold Resolution	< 5 mV
Input Threshold Accuracy (CVH and CVL)	± (50mV + 1% of PV)
Skew (Chan. to Chan.)	< 3 ns (drive and compare)
Current Source/Sink (Programmable/Channel)	Range: ±0.4 mA to ±20 mA (usable to 24 mA) Resolution: < 10 µA Accuracy: 3% of PV + 120uA
Commutating Voltage: V_{com} (CMH and CML)	Range: same as driver Resolution: < 5 mV Accuracy: ± (50mV + 1% of PV)
Over Current Alarm (IAH and IAL)	Range: ±800 mA Resolution: < 30 µA Accuracy: ± (50mA + 1% of PV)
Resistive Loads (Selectable/Channel)	140 Ω to ~1 KΩ (8 selections) to Vcom Accuracy: 30%
PMU capability	Voltage Range/Resolution/Accuracy: same as driver
DUT_GND Reference Input (per Driver/Receiver board)	Offset range: ±3 V Interrupt Voltage: 390 mV Resistive load: 100 kΩ Bypass Relay: On or Off
Power Input Using Optional Front Panel Power Input Conncector (for Pin Electronics devices)	V+: 10 to 28 V V-: -4 to -19 V V+ to V- delta: <32 V
DR9 Channel Over-voltage Protection	Clamped to 0.4 V beyond V+ or V- • Max current 200mA for < 10ms Auto Shutdown: • DC level within 1 V of V+ or V- • A 5 µs spike exceeding V+ or V-
Channel Capacitance	<120 pF
Channel Crosstalk	<250 mV pk-pk

Description	Characteristics
Pin Electronics Monitoring (per channel)	All programmed levels Output and Input levels Temperature
Voltage Monitoring (per Driver/Receiver board)	V+, V- and Front Panel DUT_GND
Hybrid Connection (per Driver/Receiver board)	Connects Front Panel pin to any channel via the Pin Driver electronics. (User must disable the drive enabled to the channel.) ~40 Ω series impedance, ~3 MHz bandwidth
Hybrid Channel Relay Connection (per channel)	Connects I/O pin to the Hybrid channel pin (5 ms connection latency for Break Before Make operation)
Hybrid Channel Relay Connection (per channel)	± 200 V Adjacent Channels must be >= 0 V for +200 V, or <= 0 V or below for -200 V
Hybrid Channel Relay Isolation	-32 db @ 200 MHz -29 db @ 100 MHz
Hybrid Channel Relay Insertion Loss	Insertion loss -0.40 db @ 200 MHz Insertion loss -0.15 db @ 100 MHz
Auxiliary I/O Channels (per Driver/Receiver board)	LVTTL (4) fixed 50 Ω series terminations (for calibration support)

* This range is limited by the Power Converter range selected.
[1] 700 mV at the fastest slew rate

I/O Min/Max Levels

The I/O level minimum and maximum values are determined by the V+ and V- bias voltage levels. The following table lists the min and max levels based on the V+ and V- level:

Table H-2: DR9 I/O Min/Max Levels Front Panel

Level	Min	Max	Units
DVH	V- + 5	V+ - 3	V
DVL	V- + 4	V+ - 7	V
CVH	V- + 2	V+ - 7	V
CVL	V- + 2	V+ - 7	V
Vcom High (CMH)	V- + 2	V+ - 7	V
Vcom Low (CML)	V- + 2	V+ - 7	V

Table D-1 lists the min and max levels based on the power converter type 1 or 3 setting:

Table H-3: DR9 I/O Min/Max Levels Power Converter Type 1 or 3

Level	Power Converter Setting							Units
	-12 to +12	-15 to +5	-10 to +10	-5 to +7	-5 to +15	0 to +24	-2 to +22	
DVH max	12	5	10	7	15	24	22	V
DVH min	-10	-13.5	-8.5	-4	-4	1	-0.5	V
DVL max	8.5	2	8.5	4.5	11.6	21	18.8	V
DVL min	-11.6	-15	-10	-5	-5	0	-2	V
CVH max	9	2.6	9	5	12.2	21.8	19.4	V
CVH min	-12	-15	-10	-5	-5	0	-2	V
CVL max	9	2.6	9	5	12.2	21.8	19.4	V
CVL min	-12	-15	-10	-5	-5	0	-2	V
CMH max	9	2.6	9	5	12.2	21.8	19.4	V
CMH min	-12	-15	-10	-5	-5	0	-2	V
CML max	9	2.6	9	5	12.2	21.8	19.4	V
CML min	-12	-15	-10	-5	-5	0	-2	V

Power Requirements

Table H-4: DR9 Power Requirements (not including Power Converter power consumption)

Voltage	Peak Current	Dynamic Current
+12V	16.9 mA	15 mA
-12V	18.1 mA	17 mA
+5V	2200 mA	1,240 mA
-2V	0	0
-5.2V	0	0
+24V	11.4 mA	20 mA
-24V	0	0

Note: *Use the DR9 Current Estimator calculation tool to estimate the power converter power consumption from the ±12V and ±24V power rails. This tool is available upon request from Astronics Test Systems at atssales@astronics.com.*

Environmental

Temperature	Operating: 0° C to 45° C Storage: -40° C to 70° C
Humidity	0° C to 10° C: Not controlled 10° C to 30° C: 5% to 95% ±5% RH 30° C to 40° C: 5% to 75% ±5% RH 40° C to 50° C: 5% to 55% ±5% RH
Altitude	10,000 ft
Cooling Required (10°C Rise; 1 DR9)	Max: 10.3 lps @ 1.5 mmH^20 Typ.: 8.0 lps @ 1.1 mmH^20
Cooling Required (10°C Rise; 2 DR9s)	Max: 19.5 lps @ 4.6 mmH^20 Typ.: 13 lps @ 2.2 mmH^20
Front Panel Current Requirements (channels unloaded) (per DR3)	V+: 3.8 A max.; 2.9 A typ. @ 21.5 V V-: 4.3 A max.; 3.4 A typ. @ -10.5 V
MTBF (ground benign)	DR9: 145,933 hours T940: 180,885 hours Power Converter: 540,040 hours T940-DR9: 70,261 hours T940-DR9-DR9: 47,427 hours
Dimensions	23 x 114 x 294 mm
EMC (Council Directive 89/336/EEC)	Emission: EN61326-1: 2006, Class A Immunity: EN61326-1: 2006, Table 1 ***Designed to Meet – Testing in Progress***
Safety (Low Voltage Directive 73/23/EEC)	BS EN61010-1: 2010 ***Designed to Meet – Testing in Progress***

DR9 Signal Description

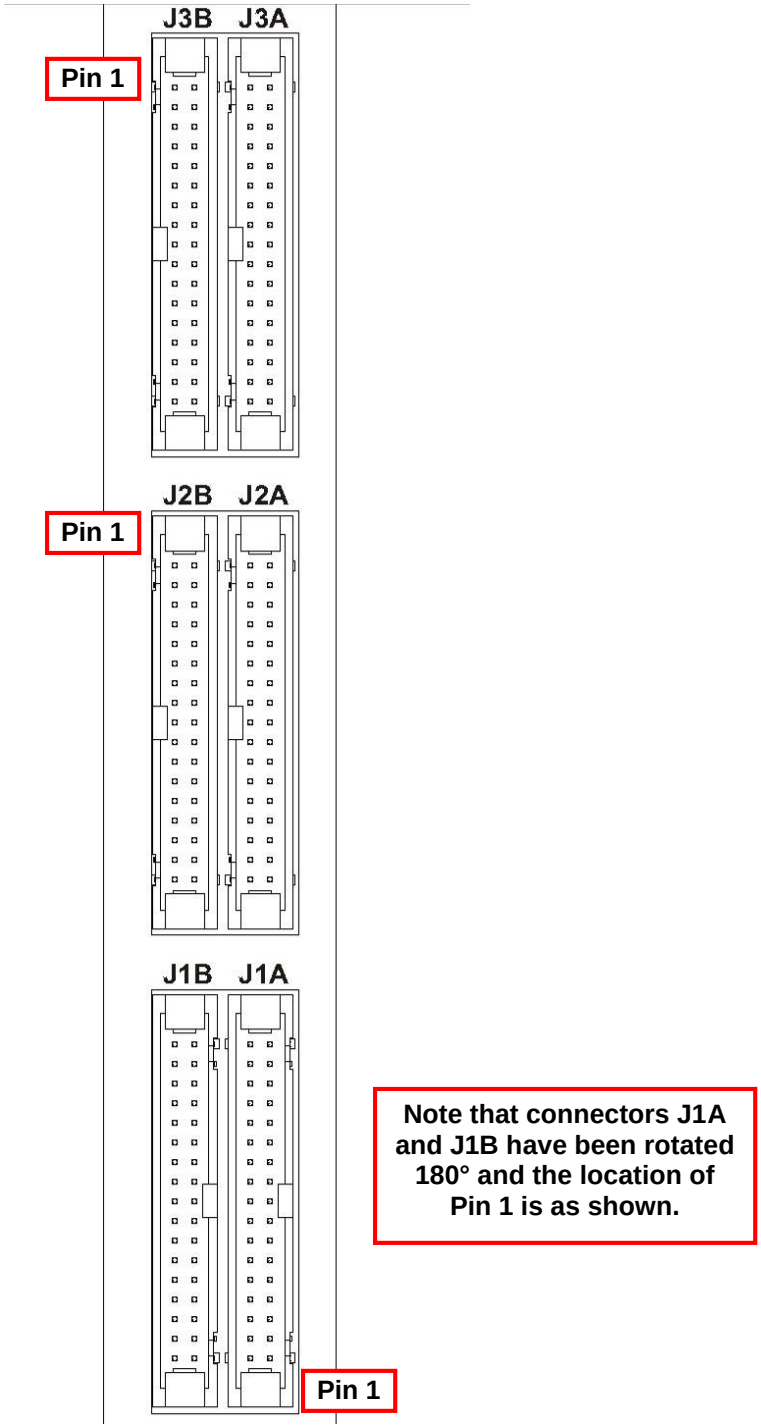


Figure H-6: DR9 J1A, J1B, J2A, J2B, J3A and J3B Signal Connectors

DRA Resources

Table H-5: DRA Resources

Name	Pin No.	Description
CH+1 - CH+24	Various	(Bi-directional) High speed channels
ACH 1 – ACH 24	Various	Analog test connection
DUTGNDA	J1B-34	(Input) DUT/UUT ground reference. All of the Pin Electronics devices have a UUT ground reference input that can be selected to be this signal or signal ground.
SIG_GND	Various	Signal Ground reference

Refer to Figure H-6 and Tables H-6 through H-8.

Table H-6: J3A Connector Pinout by Pin Number

Connector Pin	Signal	Connector Pin	Signal	Resource A or B
1	GND	2	ACH 33	B
3	GND	4	ACH 34	B
5	GND	6	ACH 35	B
7	GND	8	ACH 36	B
9	GND	10	ACH 37	B
11	GND	12	ACH 38	B
13	GND	14	ACH 39	B
15	GND	16	ACH 40	B
17	GND	18	ACH 41	B
19	GND	20	ACH 42	B
21	GND	22	ACH 43	B
23	GND	24	ACH 44	B
25	GND	26	ACH 45	B
27	GND	28	ACH 46	B
29	GND	30	ACH 47	B
31	GND	32	ACH 48	B
33	NC	34	NC	

Table H-7: J2A Connector Pinout by Pin Number

Connector Pin	Signal	Connector Pin	Signal	Resource A or B
1	GND	2	ACH 49	B
3	GND	4	ACH 50	B

Connector Pin	Signal
5	GND
7	GND
9	GND
11	GND
13	GND
15	GND
17	GND
19	GND
21	GND
23	GND
25	GND
27	GND
29	GND
31	GND
33	NC

Connector Pin	Signal	Resource A or B
6	ACH 51	B
8	ACH 52	B
10	ACH 53	B
12	ACH 54	B
14	ACH 55	B
16	ACH 56	B
18	ACH 1	A
20	ACH 2	A
22	ACH 3	A
24	ACH 4	A
26	ACH 5	A
28	ACH 6	A
30	ACH 7	A
32	ACH 8	A
34	NC	

Table H-8: J1A Connector Pinout by Pin Number

Connector Pin	Signal
1	GND
3	GND
5	GND
7	GND
9	GND
11	GND
13	GND
15	GND
17	GND
19	GND
21	GND
23	GND
25	GND
27	GND
29	GND
31	GND
33	NC

Connector Pin	Signal	Resource A or B
2	ACH 24	A
4	ACH 23	A
6	ACH 22	A
8	ACH 21	A
10	ACH 20	A
12	ACH 19	A
14	ACH 18	A
16	ACH 17	A
18	ACH 16	A
20	ACH 15	A
22	ACH 14	A
24	ACH 13	A
26	ACH 12	A
28	ACH 11	A
30	ACH 10	A
32	ACH 09	A
34	NC	

DRB Resources

Table H-9: DRB Resources

Name	Pin No.	Description
CH+33 – CH+48	Various	(Bi-directional) High speed channels
ACH 33 – ACH 48	Various	Analog test connection
DUTGNDB	J1B-34	(Input) DUT/UUT ground reference. All of the Pin Electronics devices have a UUT ground reference input that can be selected to be this signal or signal ground.
SIG_GND	Various	Signal Ground reference

Refer to Figure H-6 and Tables H-10 through H-12.

Table H-10: J3B Connector Pinout by Pin Number

Connector Pin	Signal	Connector Pin	Signal	Resource A or B
1	GND	2	CH+33	B
3	GND	4	CH+34	B
5	GND	6	CH+35	B
7	GND	8	CH+36	B
9	GND	10	CH+37	B
11	GND	12	CH+38	B
13	GND	14	CH+39	B
15	GND	16	CH+40	B
17	GND	18	CH+41	B
19	GND	20	CH+42	B
21	GND	22	CH+43	B
23	GND	24	CH+44	B
25	GND	26	CH+45	B
27	GND	28	CH+46	B
29	GND	30	CH+47	B
31	GND	32	CH+48	B
33	NC	34	NC	

Table H-11: 2B Connector Pinout by Pin Number

Connector Pin	Signal	Connector Pin	Signal	Resource A or B
1	GND	2	CH+49	B

Connector Pin	Signal
3	GND
5	GND
7	GND
9	GND
11	GND
13	GND
15	GND
17	GND
19	GND
21	GND
23	GND
25	GND
27	GND
29	GND
31	GND
33	NC

Connector Pin	Signal	Resource A or B
4	CH+50	B
6	CH+51	B
8	CH+52	B
10	CH+53	B
12	CH+54	B
14	CH+55	B
16	CH+56	B
18	CH+1	A
20	CH+2	A
22	CH+3	A
24	CH+4	A
26	CH+5	A
28	CH+6	A
30	CH+7	A
32	CH+8	A
34	NC	

Table H-12: J1B Connector Pinout by Pin Number

Connector Pin	Signal
1	GND
3	GND
5	GND
7	GND
9	GND
11	GND
13	GND
15	GND
17	GND
19	GND
21	GND
23	GND
25	GND
27	GND
29	GND
31	GND
33	GND

Connector Pin	Signal	Resource A or B
2	CH+24	A
4	CH+23	A
6	CH+22	A
8	CH+21	A
10	CH+20	A
12	CH+19	A
14	CH+18	A
16	CH+17	A
18	CH+16	A
20	CH+15	A
22	CH+14	A
24	CH+13	A
26	CH+12	A
28	CH+11	A
30	CH+10	A
32	CH+09	A
34	DUTGND(A&B)	A&B

J9 Connectors

The J9 connectors are used for calibration and for access to the auxiliary and probe signals.

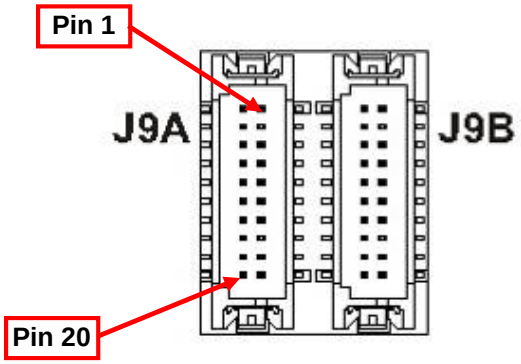


Figure H-7: DR9 J9 Calibration and Auxiliary Connectors

Table H-13: J9A Pinout

Name	Pin No.	Description
AUX5 A	1	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
AUX6 A	3	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
AUX7 A	5	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
AUX8 A	7	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
PROBE MODE A	9	(Output) Probe Support Output
BCLK A	11	(Output) Serial Clock
PBUT A	13	(Bi-directional) Probe Button Input
MPSIG A	15	(Output) Multi-purpose Signal
MONITOR A	17	(Output) Monitor signal from the Pin Electronics devices ***Note**: Only one channel can be selected at a time.*
EXTFORCE A	19	(Input) External Force routed to all of the Pin Electronics devices; used to calibrate the instrument to an external standard.
GND	2-20 (Even)	Ground

Table H-14: J9B Pinout

Name	Pin No.	Description
AUX5 B	1	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
AUX6 B	3	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
AUX7 B	5	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series

Name	Pin No.	Description
AUX8 B	7	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
PROBE MODE B	9	(Output) Probe Support Output
BCLK B	11	(Output) Serial Clock
PBUT B	13	(Bi-directional) Probe Button Input
MPSIG B	15	(Output) Multi-purpose Signal
MONITOR B	17	(Output) Monitor signal from the Pin Electronics devices ***Note**: Only one channel can be selected at a time.*
EXTFORCE B	19	(Input) External Force routed to all of the Pin Electronics devices; used to calibrate the instrument to an external standard.
GND	2-20 (Even)	Ground

Calibration

Driver/Receiver boards are calibrated using the following settings prior to shipment:

- -15 V to +17 V Voltage Mode
  - Power Converter -12 to +12
- -7 V to +24 V Voltage Mode
  - Power Converter -5 to +15

DAC Basic	Factory stored in EEPROM
Driver channel deskew	Factory stored in EEPROM
ADC/Monitor	Field upgradable stored in EEPROM
DVH/DVL	Field upgradable stored in EEPROM
CVH/CVL	Field upgradable stored in EEPROM
Vcom High/Vcom Low	Field upgradable stored in EEPROM
Isource//Isink	Field upgradable stored in EEPROM
IAL/IAH	Field upgradable stored in EEPROM
Inter-module timing deskew	Static
End-of-cable deskew	Static

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Appendix I
UR14 Driver/Receiver Board

UR14 Features

- Channels: 32 Low Speed single-ended Open Collector Utility Pins
- Voltage range: 0 to +30 V
- Suitable for Inductive loads, internal clamping to ~42 V
- +5V Pull-up allowing each channel to operate as low speed TTL.
- Programmable input level detection (per byte) 0-20V
- Programmable Over-current detection (per byte) 0-1A
- External Probe Support
- Auxiliary I/O channels:
  - Six programmable (Two are dedicated for the external probe when used)
  - Two LVTTL (One is dedicated for the external probe when used)
  - Three ECL (single ended or differential)
  - Four LVTTL or SE ECL
  - Four LVTTL or ECL (single-ended or differential)

See Figure I-1 for a front panel illustration of the UR14.

Block Diagram

The top level block diagram for the UR14 Driver/Receiver board is shown in Figure I-2. More detailed diagrams of these blocks are featured in Figures I-3 thru I-5.

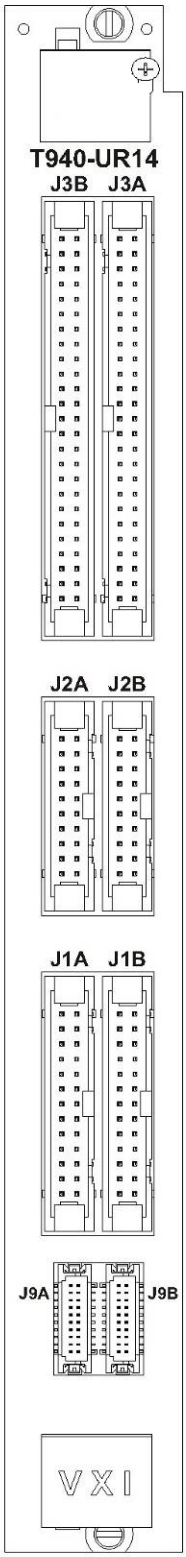


Figure I-1: UR14 Front Panel

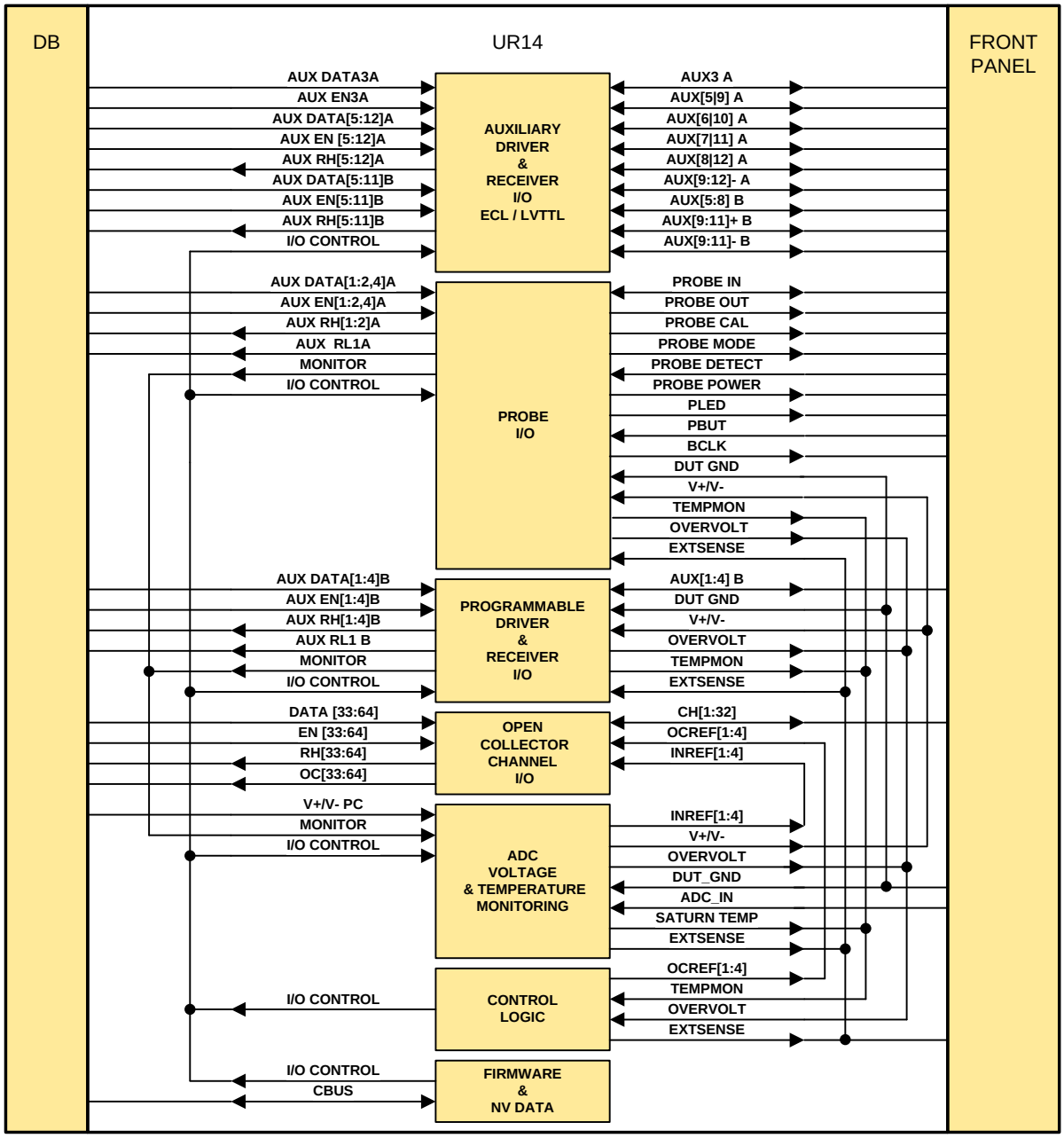


Figure I-2: UR14 Driver/Receiver Block Diagram

- AUXILIARY DRIVER & RECEIVER I/O ECL/LVTTL Block diagram illustrates the configuration and control of Auxiliary ECL & LVTTL Driver & Receivers on the UR14.
- PROBE I/O Block illustrates the configuration and control of the External Probe Support Signals on the UR14.
- PROGRAMMABLE DRIVER & RECEIVER I/O Block diagram illustrates the major Driver & Receiver internal and external features for the PROGRAMMABLE AUX Channels.
- OPEN COLLECTOR CHANNEL I/O block diagram illustrates the

configuration and control of the OPEN COLLECTOR “utility channel” I/O on the UR14.

- ADC VOLTAGE & TEMPERATURE MONITORING block diagram illustrates the Power and Temperature & control features for the PROGRAMMABLE AUX Channels as well as the voltage reference generation used for the OPEN COLLECTOR I/O.
- CONTROL LOGIC This control logic provides facilitates UR14 functions including; access to the Pin Electronics devices, Temperature Monitoring programming, Voltage, Over-voltage and Over Temperature detection.
- FIRMWARE & NV DATA The UR14 Control Logic FPGA firmware is loaded via a serial PROM on power up or VXI Reset. The firmware is field upgradeable using our supplied loader utility. UR14 calibration data is stored in an on-board EEPROM and is loaded initialization of the T940 unit. UR14 power on time is stored for reference using an on-board timer.

Auxiliary Driver and Receiver I/O ECL/LVTTL

The Auxiliary Driver and Receiver I/O ECL/LVTTL block diagram (Figure H-3) illustrates the configuration and control of Auxiliary ECL & LVTTL Driver & Receivers on the UR14.

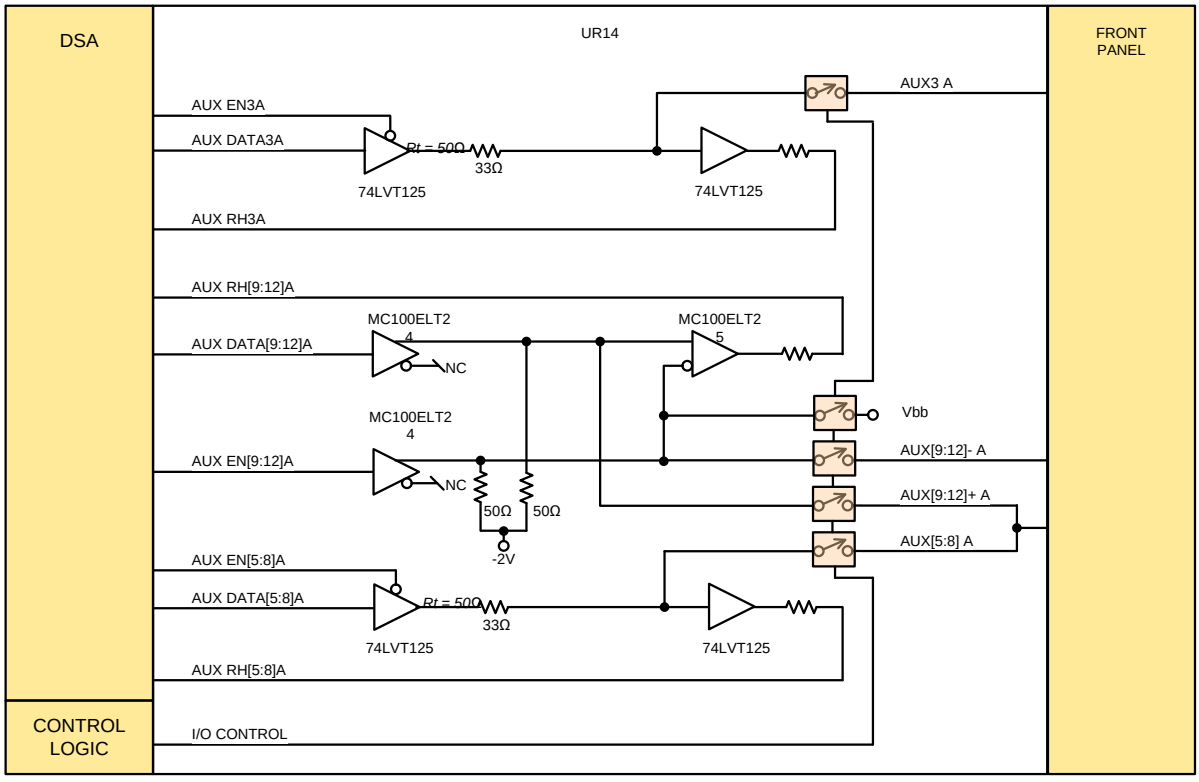


Figure I-3: Auxiliary AUX3 A & AUX[5:12] A LVTTL & DIFF ECL I/O

It is important to note that the positive side of the ECL and the LVTTL selections share a pin. Changing a pin from ECL to LVTTL requires changing the Sequencer assignment of the function as well. For example if External

Clock is assigned to the LVTTL AUX A 5 then subsequently changing that that pin to ECL it would require assigning the External Clock to AUX A 9 as well.

Signal Descriptions (Figure I-3)

AUX DATA3A	Auxiliary Data output from the Data Sequencer to the LVTTL output buffer
AUX EN3A	Auxiliary Enable output from the Data Sequencer to the LVTTL output buffer.
AUX RH3A	Auxiliary Response Input to the Data Sequencer from the LVTTL input buffer.
AUX H[9:12]A	Auxiliary Response Inputs to the Data Sequencer from the ECL input buffers.
AUX DATA[9:12]A	Auxiliary Data outputs from the Data Sequencer to the positive side ECL output buffers.
AUX EN[9:12]A	Auxiliary Data outputs from the Data Sequencer to the negative side ECL output buffers.
AUX DATA[5:8]A	Auxiliary Data outputs from the Data Sequencer to the LVTTL output buffers
AUX EN[5:8]A	Auxiliary Enable outputs from the Data Sequencer to the LVTTL output buffer.
AUX RH[5:8]A	Auxiliary Response Input to the Data Sequencer from the LVTTL input buffers.
I/O CONTROL	Control Logic signals to control isolation, termination and configuration relays
AUX3 A	Front Panel AUX I/O 3A.
AUX[9:12]- A	Front Panel I/O for the minus side of the ECL buffers for AUX I/O 9A through 12A.
AUX[9:12]+ A	Front Panel I/O for the positive side of the ECL buffers for AUX I/O 9A through 12A. These I/O pins are connected to AUX[5:8]A. (5 to 9, 6 to 10, 7 to 11, 8 to 12)
AUX[5:8] A	Front Panel I/O for the LVTTL buffers for AUX I/O 5A through 8A. These I/O pins are connected to AUX[9:12]A+. (5 to 9, 6 to 10, 7 to 11, 8 to 12)

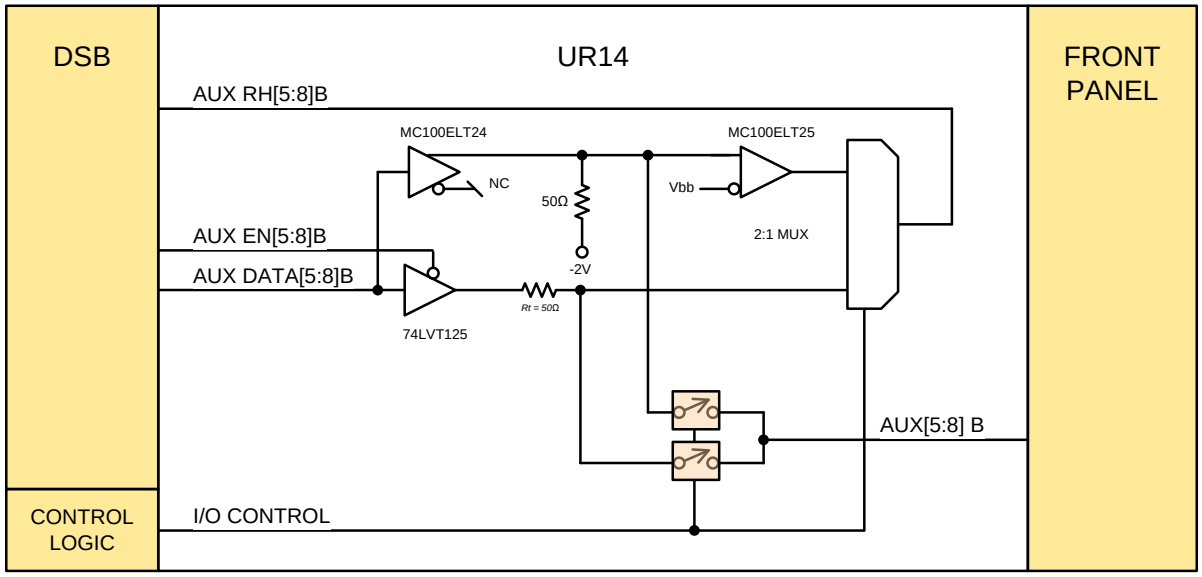


Figure I-4: Auxiliary AUX[5:8] B LVTTL | SE ECL I/O

For these Auxiliary signals, an I/O pin assignment of either ECL or LVTTL requires no Sequencer assignment changes.

Signal Descriptions (Figure I-4)

AUX RH[5:8]B	Auxiliary Response Inputs to the Data Sequencer from the LVTTL or ECL input buffers.
AUX EN[5:8]B	Auxiliary Enable outputs from the Data Sequencer to the LVTTL output buffers.
AUX DATA[5:8]B	Auxiliary Data outputs from the Data Sequencer to the ECL and LVTTL output buffers.
I/O CONTROL	Control Logic signals to control isolation, termination and configuration relays
AUX[5:8] B	Auxiliary I/O 5B through 8B programmable selection between SE ECL or LVTTL I/O
Vbb	ECL Switching threshold typically –1.29 V

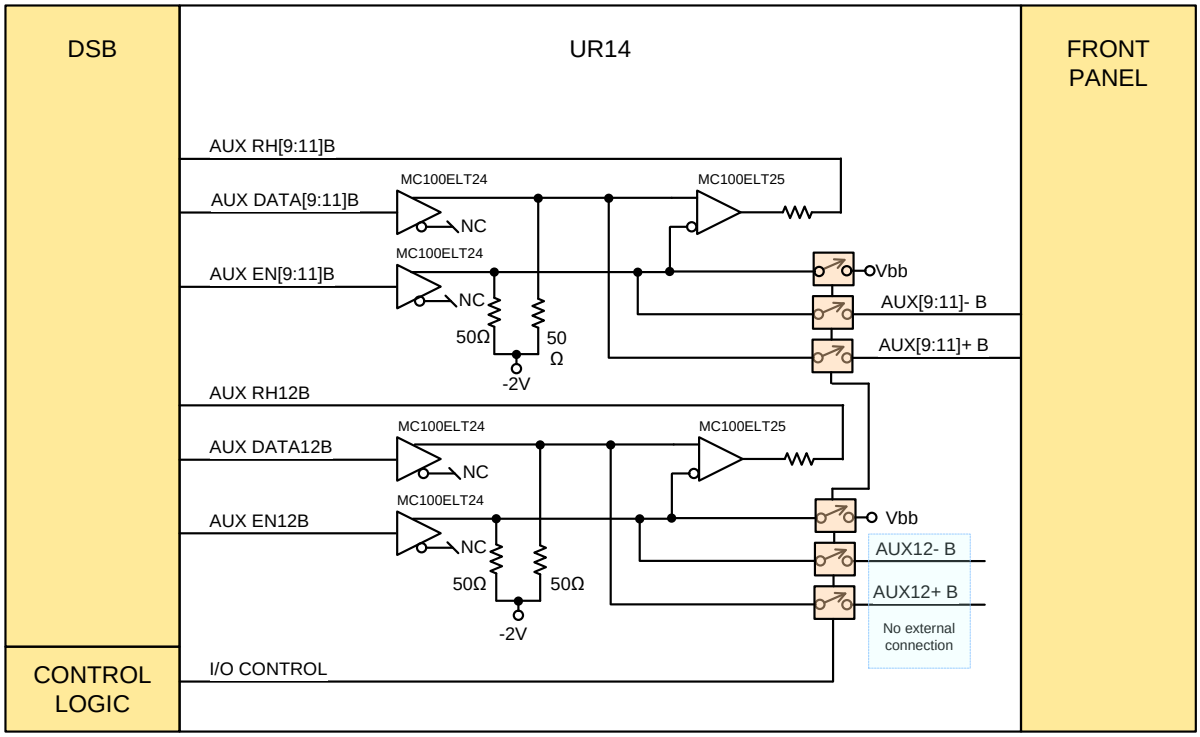


Figure I-5: Auxiliary AUX[9:12] B SE | DIFF ECL I/O

For these Auxiliary signals, I/O pin assignment can be either SE ECL or Differential ECL.

Signal Descriptions (Figure H-5)

AUX RH[9:11]B	Auxiliary Response Inputs to the Data Sequencer from the ECL input buffers.
AUX DATA[9:11]B	Auxiliary Data outputs from the Data Sequencer to the positive side ECL output buffers.
AUX EN[9:11]B	Auxiliary Data outputs from the Data Sequencer to the negative side ECL output buffers.
AUX RH12B	Auxiliary Response Input to the Data Sequencer from the AUX12 B ECL input buffers.
AUX DATA12B	Auxiliary Data output from the Data Sequencer to the positive side AUX12 B ECL output buffers.
AUX EN12B	Auxiliary Data outputs from the Data Sequencer to the negative side AUX12 B ECL output buffers.
I/O CONTROL	Control Logic signals to control isolation, termination and configuration relays
AUX[9:11]+ B	Front Panel I/O for the positive side of the ECL buffers
AUX[9:11]- B	Front Panel I/O for the minus side of the ECL buffers

Probe I/O

The Probe I/O Block Diagram (Figure I-6) illustrates the configuration and control of the External Probe Support Signals on the UR14. The external probe connection is described in more detail in a subsequent section. It is useful to note that AUX1 A, AUX2 A and AUX4 A are general purpose I/O until they are assigned to the external probe.

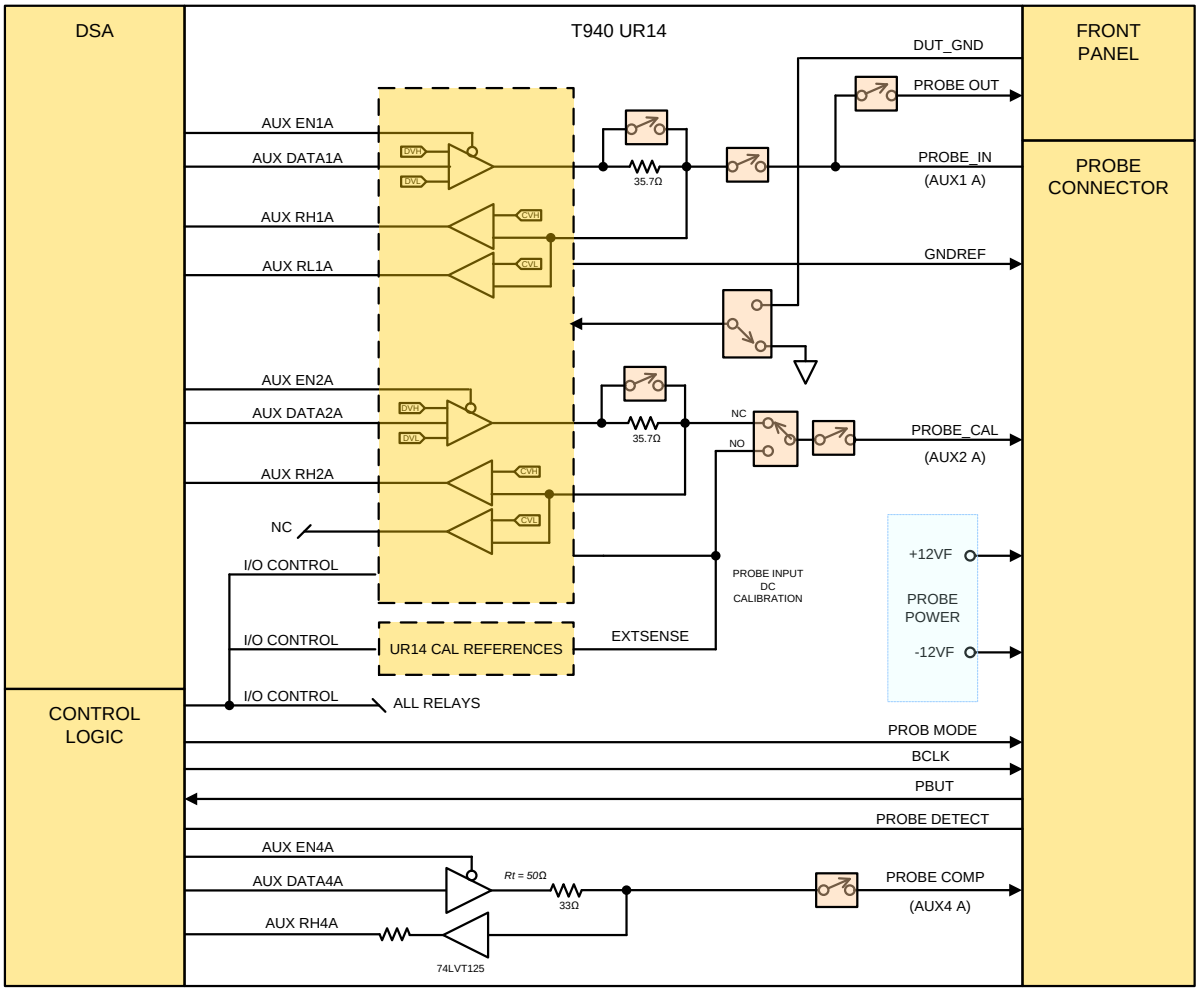


Figure I-6: Probe I/O Block Diagram

Signal Descriptions (Figure I-6)

AUX EN1A	Channel Data Enable from the Data Sequencer to the AUX1 A output driver. AUX1 A is the PROBE IN signal on the UR14 and is input only.
AUX DATA1A	Channel Data output from the Data Sequencer to the AUX1 A output driver. AUX1 A is the PROBE IN signal on the UR14 and is input only.
AUX RH1A	Channel Response High input to the Data Sequencer from the AUX1 A (PROBE IN) input receiver.

AUX RL1A	Channel Response Low input to the Data Sequencer from the AUX1 A (PROBE IN) input receiver.
AUX EN2A	Channel Data Enable from the Data Sequencer to the AUX2 A output driver. AUX2 A is the PROBE CAL signal on the UR14 and is output only.
AUX DATA2A	Channel Data output from the Data Sequencer to the AUX2 A output driver. AUX2 A is the PROBE CAL signal on the UR14 and is output only.
AUX RH2A	Channel Response High input to the Data Sequencer from the AUX2 A (PROBE CAL) input receiver.
I/O CONTROL	Control Logic signals to control pin electronics, isolation, termination and configuration relays.
AUX EN4A	Channel Enable from the Data Sequencer to the AUX4 A LVTTL driver. AUX4 A is the PROBE COMP signal on the UR14 and is output only.
AUX DATA4 A	Channel Data from the Data Sequencer to the AUX4 A LVTTL driver. AUX4 A is the PROBE COMP signal on the UR14 and is output only.
AUX RH4A	Channel Response High input to the Data Sequencer from the AUX4 A (PROBE COMP) input receiver.
DUT_GND	When PROBE DETECT is true this input is inactive for the Pin Driver Logic. Any DUT_GND offsets are applied to the external probe module. When not used with the external probe this signal comes from the UUT and can be used to offset the reference levels up to ±3 V. Excursions of DUT_GND beyond ±390 mV with respect to signal ground yields a GND FAULT signal. DUT_GND can be used to apply this offset to the probe module input.
PROBE OUT	Signal path that can be used to adjust the compensation of the external probe. Note that this connection is not on the probe connector.
PROBE IN	Input signal from the external probe. When not used with a probe AUX1 A is a programmable level I/O signal.
GNDREF	This is the buffered DUT_GND and is currently not used for the external probe module
PROBE CAL	Calibration output signal for the external probe. Supplies compensation square wave and DC Calibration outputs. When not used with a probe AUX2 A is a programmable level I/O signal.
PROBE POWER	Supplies +12 V and -12 V to the external probe module.
PROBE MODE	This is a control signal from the Sequencer for support of external probe operations.
BCLK	This is a reserved output signal that can be used for further expansion of the external probe functions.
PBUT	This is a Probe Button input signal to the Sequencer for support of external probe operations.
PROBE DETECT	Detects the presence of an external probe module. When

detected the API functions for the UR14 probe are activated.

PROBE COMP — Signal used to enable the probe module compensation calibration logic. When not used with a probe AUX4 A is a LVTTL level I/O signal.

Programmable Driver and Receiver I/O

The Programmable Driver and Receiver I/O Block diagram (Figure H-7) illustrates Pin Electronics Driver & Receiver features for the Programmable AUX Channels.

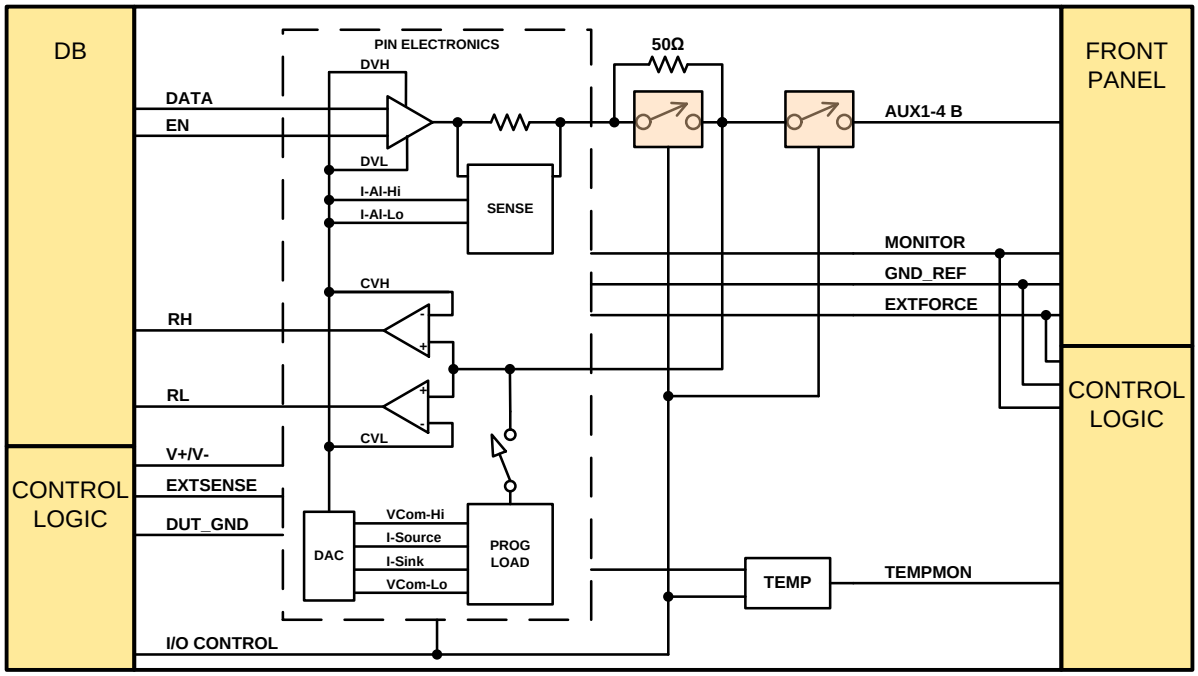


Figure I-7: Programmable Driver and Receiver I/O

Signal Descriptions (Figure I-7)

DATA — Auxiliary data output signals from the Data Sequencer to the programmable output drivers.

EN — Auxiliary enable output signals from the Data Sequencer to the programmable output drivers.

RH — Response High input signals to the Data Sequencer from the programmable input receivers. 1 = good 1, 0 = good 0.

RL — Response Low input signals to the Data Sequencer from the programmable input receivers. 0 = good 0, 1 = good 1.

V+/V- — Bias Power required for operation of the Pin Electronics devices.

EXTSENSE — Pin electronics signal used for calibration.

DUT_GND	This signal comes from the UUT and can be used to offset the reference levels up to ±3 V. Excursions of DUT_GND beyond ±390 mV with respect to signal ground yield a GND FAULT signal.
I/O CONTROL	Control Logic signals to control isolation relays, termination, pin electronics and temperature thresholds.
AUX1-4 B	Four programmable signals used to input or output test signals. See **Configuring the AUX Channels** in **Chapter 5**.
MONITOR	This is an analog output signal from the Pin Electronics devices which can be used to monitor DAC levels even the Channel I/O levels. This signal is used with the internal ADC but a buffered version also comes out the Front Panel.
GND_REF	This is the ground reference output signal from the Pin Electronics devices. It is used with MONITOR to make accurate ADC measurements. A buffered version also comes out the Front Panel.
EXTFORCE	External Force is an analog I/O signal which is connected to all of the Pin Electronics devices and can be used to force a level on the output of the driver. It may also be used to monitor a channel's state. EXTFORCE is also used for calibration.
TEMPMON	Real-time temperature monitors for the pin electronics.
DSB	Digital Board Sequencer B

Open Collector Channels I/O

The Open Collector Channel I/O block diagram (Figure H-8) illustrates the configuration and control of the Open Collector "utility channel" I/O on the UR14.

These channels can be used for slow LVTTL I/O. Four programmable input references INREF[1:4] allow testing input levels from 0 to +20V. Four Over Current references OCREF[1:4] can be used to limit the sink current from 0 to 1A when a channel is used as a high voltage inductive input.

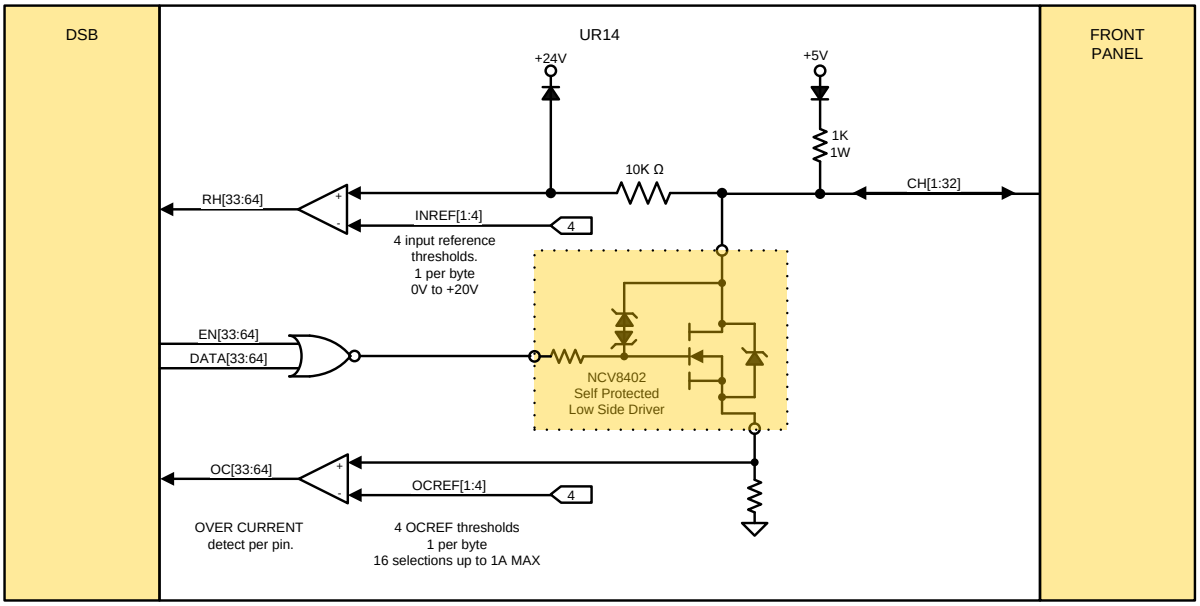


Figure I-8: Open Collector Channel I/O

Signal Descriptions (Figure I-8)

RH[33:64]	Sequencer B Response Data High
EN[33:64]	Sequencer B Channel Data Enable output from the Data Sequencer to the Open Collector Driver.
DATA[33:64]	Sequencer B Channel Data output from the Data Sequencer to the Open Collector Driver.
OC[33:64]	Sequencer B Channel Over Current detect signals to the Data Sequencer from Open Collector Driver over current detect comparator. Depending on Sequencer B settings a detected over current can shut off just the channel or all channels.
CH[1:32]	Data I/O Open Collector Channels. These channels can be used with high voltage inductive loads. The +5V pull-up on each channel allows the channel to be used for low speed TTL. A current sensor on each channel can programmatically limit the current on a per byte basis.
INREF[1:4]	Programmable input reference detect thresholds. There that can be programmed from 0V to 20V. There are four references, one per byte.
OCREF[1:4]	Programmable current detect thresholds. There are seventeen levels that can be programmed from 0 to 1A. There are four references, one per byte.

ADC Voltage and Temperature Monitoring

The ADC Voltage and Temperature Monitoring diagram (Figure I-9) illustrates the Power and Temperature & control features for the Programmable AUX Channels as well as the voltage reference generation used for the Open Collector I/O

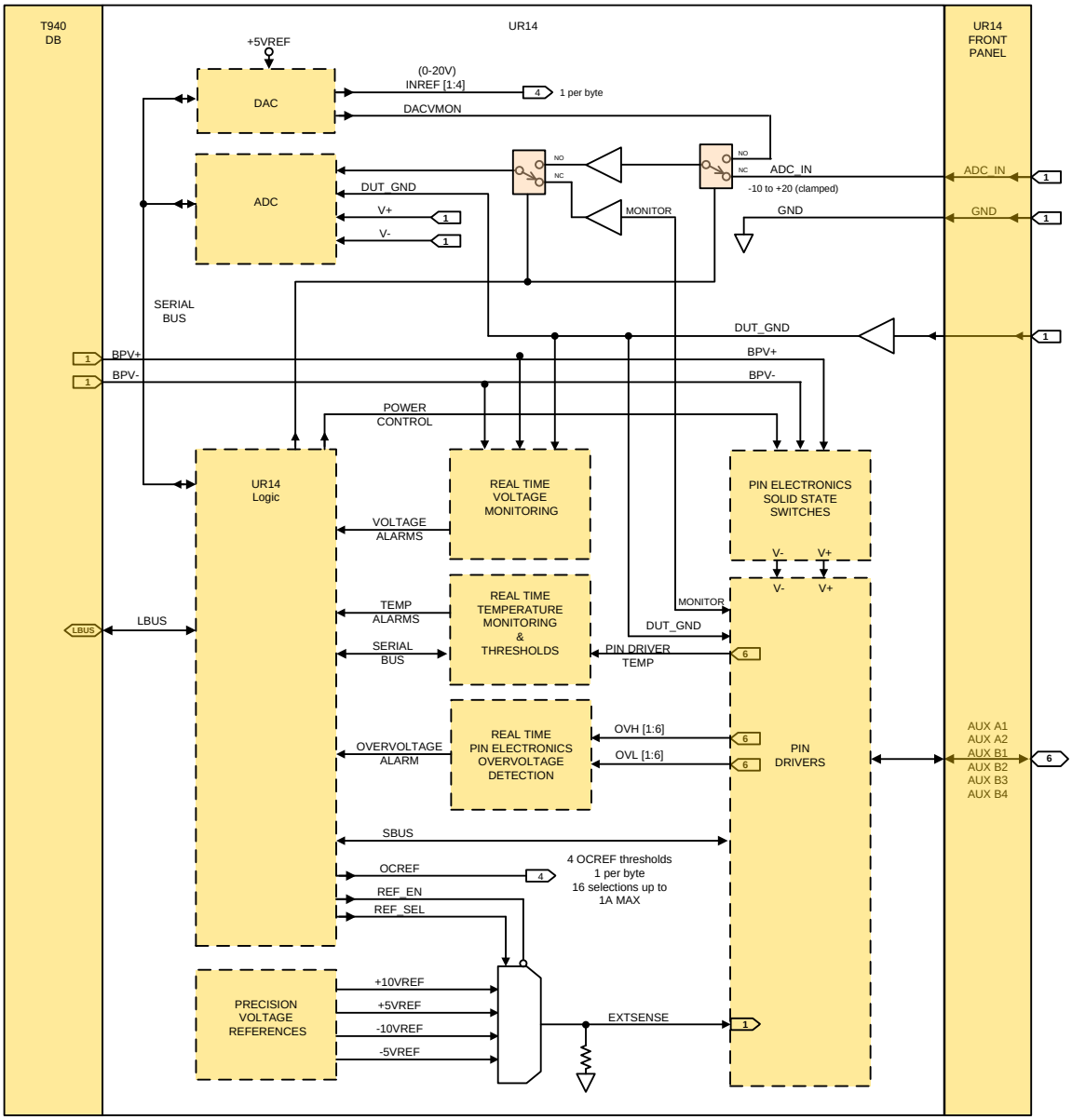


Figure I-9: ADC Voltage and Temperature Monitoring

Signal Descriptions (Figure I-9)

BPV-, BPV+	VXI Backplane derived power from the T940 Digital board.
V+, V-	Bias Power required for operation of the Pin Electronics devices.

POWER CONTROL The UR14 logic controls Pin Electronics solid state switches.

+10VREF, +5VREF, -5VREF, -10VREF Precision voltage references used for calibration of UR14 Pin Drivers. The UR14 Logic controls the enable and selection of these references. +5VREF is used for accurate generation of the DAC INREF[1:4] references.

EXTSENSE This analog signal connects to the Pin Driver for internal reference calibration. It is also used for calibrating the external probe.

AUX A 1, AUX A2, AUX B [1:4] Programmable level I/O to and from the PIN Electronics

OCREF[1:4] Programmable current detect thresholds for the Open Collector Channel I/O. There are seventeen levels that can be programmed from 0 to 1 A. There are four references, one per byte.

INREF[1:4] Programmable input reference detect thresholds for the Open Collector Channel I/O. There that can be programmed from 0 V to 20 V. There are four references, one per byte.

OVH[1:6], OVL[1:6] Connected to the Pin Driver electronics channel I/O and provide to the real-time Pin Electronics Overvoltage Detection circuitry with levels that indicate an Overvoltage condition.

OVERVOLTAGE ALARMS The output from the monitoring circuitry that goes to the UR14 LOGIC.

VOLTAGE ALARMS Real-time over-voltage which monitors the PIN ELECTRONICS Driver and Receivers to protect the UR14 board.

DUT_GND This signal comes from the UUT and can be used to offset the Pin Driver reference levels up to ±3V. Comparators on the UR14 monitor excursions of DUT_GND beyond ±390 mV with respect to signal ground yields to signal a GND FAULT to the UR14 LOGIC. The levels of DUT_GND can also be measured by the ADC.

MONITOR This is an analog output signal from the Pin Electronics devices which can be used to monitor DAC levels...even the Channel I/O levels.

DACVMON This signal comes from the DAC and allows monitoring of the INREF[1:4].

ADC_IN This input comes from the UR14 front panel and is used to measure DC levels from -10 to +20 V.

PIN DRIVER TEMP Real Time Pin Driver temperature monitoring diode connections. Programmable temperature thresholds allow the UR14 LOGIC to respond to OVERTEMP alarms to shut off the Pin Drivers to protect them from over-temperature damage.

TEMP ALARMS	Real-time temperature monitors for the Pin Electronics Driver and Receivers to protect the UR14 board.
CBUS	An internal Control Bus connecting the VXI Bridge to the Data Sequencers and the Driver/Receiver board's Control Logic.
SBUS	This bus allows the UR14 Control Logic to read and write programmable Driver and Receiver References and configuration.
SERIAL BUS	Communication and control by the UR14 Logic of the DAC and ADC are facilitated by this bus.

UR14 Control Logic

This control logic provides facilitates UR14 functions including; access to the Pin Electronics devices, Temperature Monitoring programming, Voltage, Over-voltage and Over Temperature detection.

Firmware and Calibration Storage

The UR14 Control Logic FPGA firmware is loaded via a serial PROM on power up or VXI Reset. The firmware is field upgradeable using our supplied loader utility. UR14 calibration data is stored in an on-board EEPROM and is loaded initialization of the T940 unit. UR14 power on time is stored for reference using an on-board timer.

External Probe Module Block Diagram

The External Probe Module (Figure I-10) is connected to the UR14 via a cable and mounted externally. It provides the interface for probe functions designed into the T940 Sequencer Logic to support probe functions.

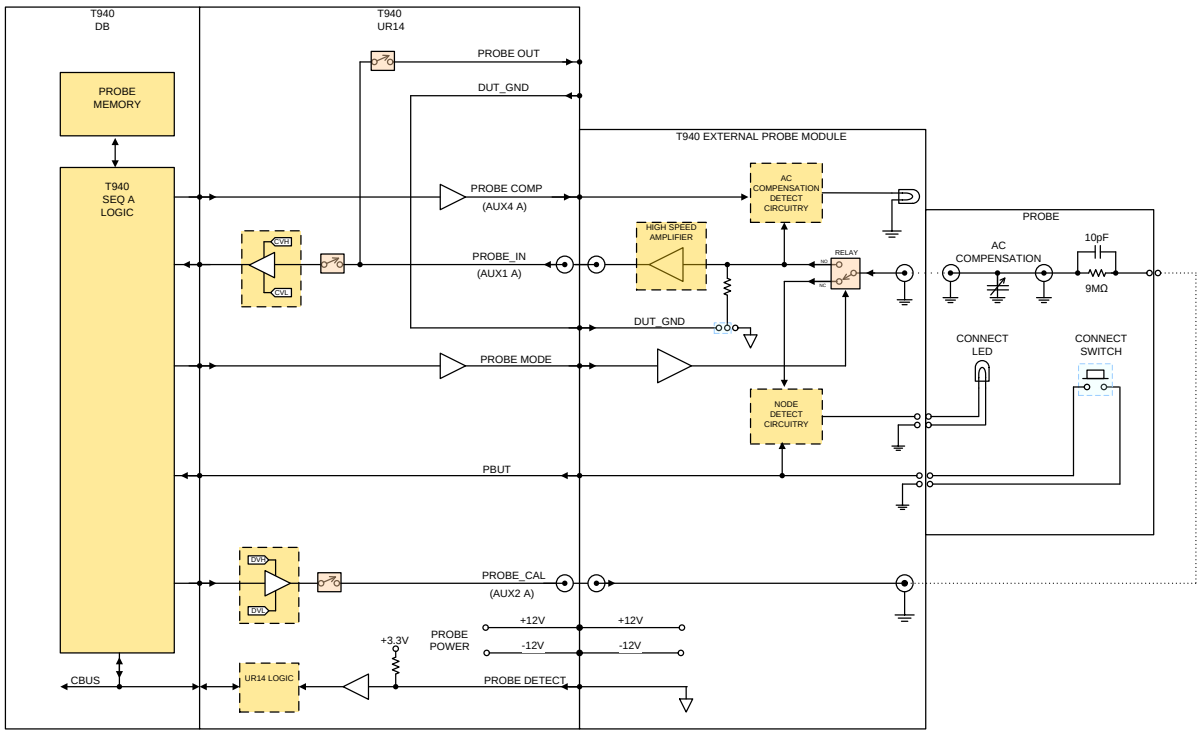


Figure I-10: External Probe Module

Signal Descriptions (Figure I-10)

EXTERNAL PROBE MODULE — is the external PCB assembly that is connected to the UR14 via a cable providing; a high speed buffer for probe data to the UR14, probe compensation circuitry, contact detection circuitry, and PROBE and CAL BNC connections.

PROBE COMP — AUX4 A Output to the external probe module to control the contact detect relay. When not used with the probe it can be used as an I/O signal.

PROBE OUT — Signal path that can be used to adjust the compensation of the external probe. Note that this connection is not on the probe connector.

PROBE IN — Input signal from the external probe. When not used with a probe AUX1 A is a programmable level I/O signal.

PROBE CAL — Calibration output signal for the external probe. Supplies compensation square wave and DC Calibration outputs. When not used with a probe AUX2 A is a programmable level I/O signal.

PROBE POWER — Supplies +12V and -12V to the external probe module.

PROBE MODE — This is a control signal from the Sequencer for support of external probe operations.

PBUT — This is a Probe Button input signal to the Sequencer for support of external probe operations.

DUT_GND — When PROBE DETECT is true this input is inactive. Any

DUT offsets are applied to the external probe module. When not used with the external probe this signal comes from the UUT and can be used to offset the reference levels up to ±3V. Excursions of DUT_GND beyond ±390 mV with respect to signal ground yields a GND FAULT signal.

PROBE — Probe Master 100 MHz probe assembly MODEL PM6139 that includes a push button and LED that connect to the External Probe Module via an included cable and connector.

CONNECT SWITCH — is a push button on the PROBE that is used to signal a sequence start to the T940 Sequencer via PBUT.

CONNECT LED — is an LED on the PROBE that, when lighted, indicates contact detection.

PROBE DETECT — this input detects the presence of an external probe module. When detected the API functions for the UR14 probe are activated.

CBUS — An internal Control Bus connecting the VXI Bridge to the Data Sequencers and the Driver/Receiver board's Control Logic.

External Probe Module

The T940 UR14 is specifically configured to support the external probe module. There are two module types: a Flush Mounted PCB Assembly (Figure I-11) and a Right Angle PCB Assembly (Figure I-12).

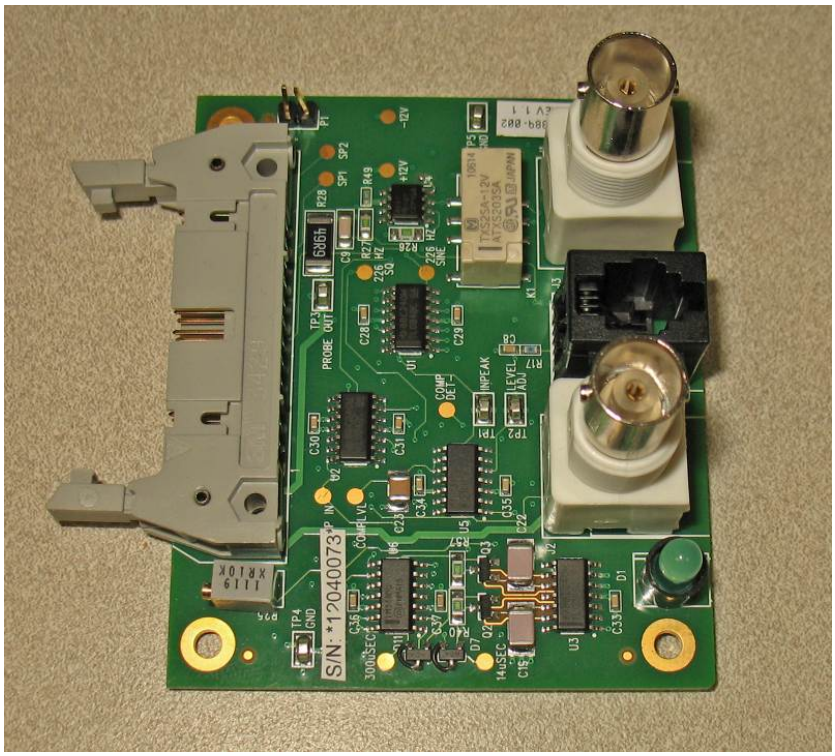


Figure I-11: External Probe Module Flush Mount

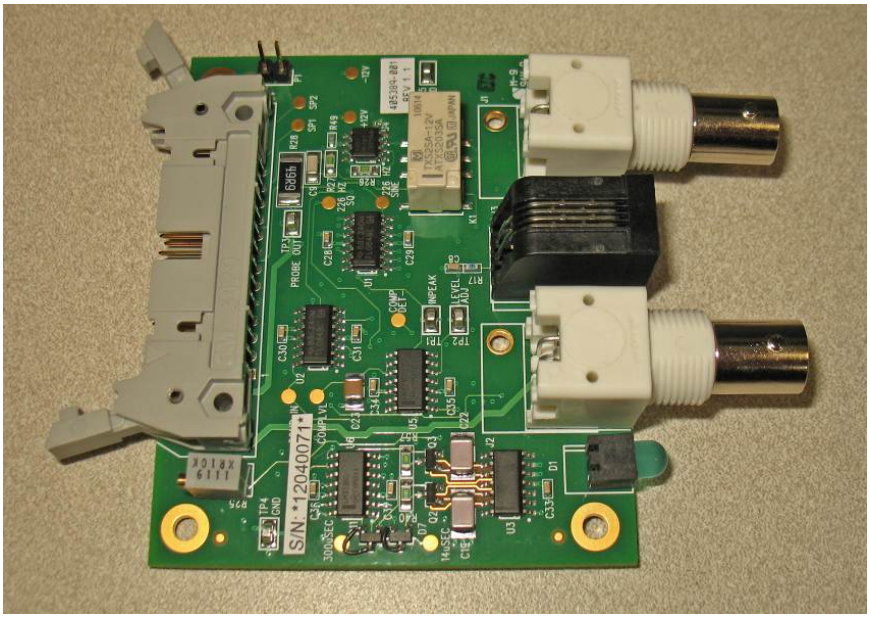


Figure I-12: External Probe Module Right Angle

Figure I-13 illustrates the External Probe Module Right Angle with the PM6139 Probe connected and the probe tip installed in the Probe Cal BNC.

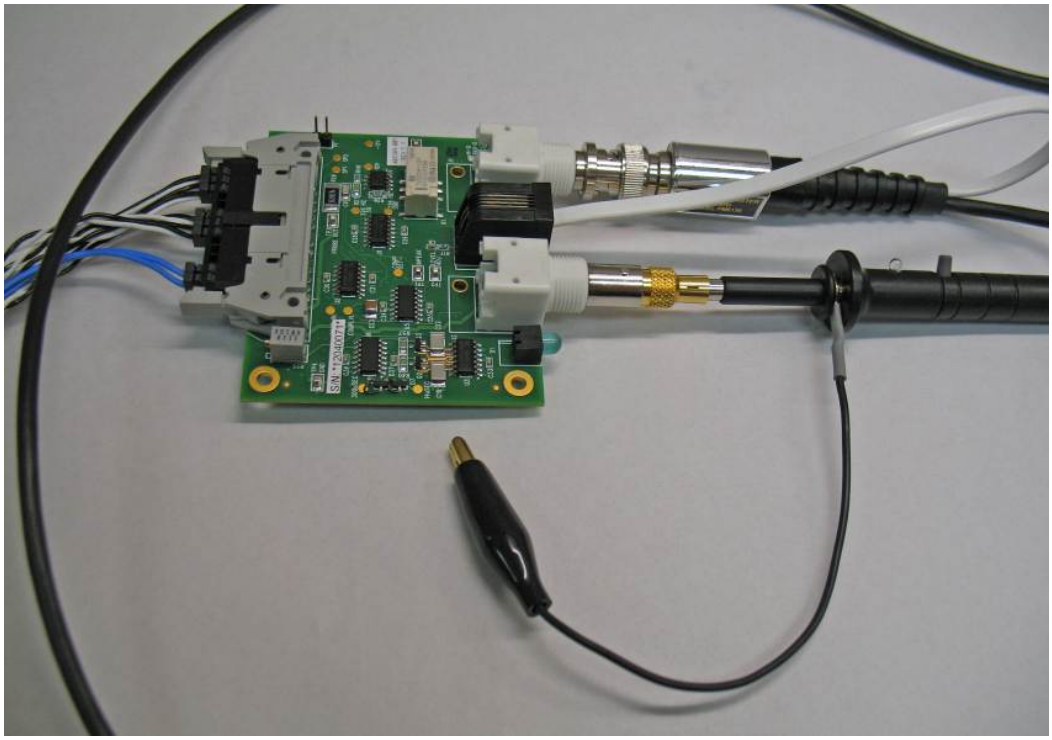


Figure I-13: External Probe Module with Probe

External Probe Module

Table I-1: External Probe Module Characteristics

Description	Notes
Interfaces to legacy panels.	
Two types of assemblies	Can mount vertically or horizontally
Provides a BNC connector for the Probe with and isolation provision when mounted to the customer panel	
Provides a BNC connector for calibrating the Probe at the Probe Tip	Compensation and DC Calibration
Utilizes a cable to connect the Probe Module to the D/R Board	Lengths from 36” to 120” in 12” increments. PN 408378-XXX PN 408378-036 36” PN 408378-120 120”

Description	Notes
AUX1 A and AUX2 A are 50 ohm coax.	When used with the external probe module these are dedicated I/O
Probe	ProbeMaster PN 853-068-00 100 MHz probe PM6139
Probe Module Interfaces to the UR14.	J1A 26 Pin connector
Secures power ±12V from the UR14	PolyFuse current limited
Provides contact detect through the probe tip	Details below
Supports Probe Handle pushbutton and Footswitch signaling through the D/R board to the Digital Board to initiate or resume a burst and deactivate the contact detect circuitry.	The Sequencer handles the sequencing once the pushbutton signal is received. Footswitch signaling simply requires tapping into the Probe Aux. connector
Supports dual threshold detection	Via the UR14 AUX1 A input
Utilizes Window 4 for Probe Data capturing	Implemented in the T940 DB Sequencer, see relevant manual section.
Detectable states: 34	Provided in the T940 DB Sequencer
Provides Capture/Learn and Expect/Compare of Probe input	Provided in the T940 DB Sequencer
Provides dual level CRC (CRC16 and pre-load of 1's)	Provided in the T940 DB Sequencer

UR14 Characteristics

UTILITY CHANNELS

Table I-2: Utility Channel Characteristics

Description	Characteristics
Digital I/O Type	Bi directional 32 Open Collector Output Channels with Single threshold Input Comparator
Output Voltage Compliance	0 to 30 V
Output Data Rate	Static to 5 kHz
Output Data Delay	82 µs from Phase to output.
Input Data Rate	Static to 500 kHz

Description	Characteristics
Input Data Delay	220 ns with at least 2 V overdrive with respect to the programmed input reference level. >700 ns when less than 1 V of overdrive
Driver Thermal Protection	If Channel FET exceeds 175°C
Driver Over-voltage protection	Driver clamps at 42 V, suitable for inductive loads
Programmable OC detect thresholds	0-1 A ±4% 4 thresholds, 1 per byte
OC detect levels	16 selections (in Amps) 0.06 0.12 0.19 0.25 0.31 0.37 0.44 0.5 0.56 0.63 0.69 0.75 0.81 0.87 0.94 1
Input Sink Current	Up to 1 A per channel, or 1 A max per byte
On-board pull-up	1 kΩ to +5 V default allows each channel to be used as low speed TTL
Output Impedance	< 520 mΩ per channel
Input References	4 input references INREF 1 Channels 1-8 INREF 2 Channels 9-16 INREF 3 Channels 17-24 INREF 4 Channels 25-32
Input Compare range	0 to +20 V
Input Reference resolution	5 mV steps
Input Compare Accuracy	±30 mV accuracy

PROGRAMMABLE CHANNELS

Table I-3: Programmable Channel Characteristics

Description	Characteristics
Digital I/O Type	Variable Voltage

Description	Characteristics
AUX Channels	6 SE Driver/Receivers per VXI slot Per channel relay isolation (2 are dedicated to the External Probe when used)
Output Voltage Ranges* (Selectable/Sequencer)	-15 V to +17 V (VM0) -7 V to +24 V (VM1)
Output Voltage Swing	500 mV[1] to 24 V
Output Resolution	< 5 mV
Output Accuracy	± (50mV + 1% of PV) Slow, Default, Medium slew settings ± (75mV + 1% of PV) Fast slew setting
Output Drive Current	± 65 mA typical (Source/Sink) ± 85 mA Max (Source/Sink)
Output Impedance (Selectable/Channel)	12 Ω or 50 Ω ± 4 Ω
Slew Rate (Selectable/Channel or custom)	0.25 V/ns 0.7 V/ns, 1.0 V/ns or 1.3 V/ns:typical
Input Threshold Ranges	-14.75 V to +14 V (VM0) -6.75 V to +21 V (VM1)
Input Threshold Resolution	< 5 mV
Input Threshold Accuracy	± (50mV + 1% of PV)
Current Source/Sink (Programmable/Channel)	Range: ±0.4 mA to ±20 mA (usable to 24 mA) Resolution: < 10 µA Accuracy: 3% of PV + 120uA
Commutating Voltage: V_{com} (CMH and CML)	Range: same as driver Resolution: < 5 mV Accuracy: ± (50mV + 1% of PV)
Over Current Alarm (IAH and IAL)	Range: ±800 mA Resolution: < 30 µA Accuracy: ± (50mA + 1% of PV)
Resistive Loads (Selectable/Channel)	140 Ω to ~1 KΩ (8 selections) to Vcom Accuracy: 30%
DUT_GND Reference Input	Offset range: ±3 V Interrupt Voltage: 390 mV ±50 mV Resistive load: 100 K ±2% Bypass Relay: On or Off
Pin Electronics Power Input	Supplied by the power converter board.
UR14: Channel Over-voltage Protection	Clamped to 0.4 V beyond V+ or V- • Max current 200mA for < 10ms Auto Shutdown: • DC level within 1 V of V+ or V- • A 5 µs spike exceeding V+ or V-
Pin Electronics Monitoring (per channel)	All programmed levels Output and Input levels Temperature

Description	Characteristics
Voltage Monitoring	V+, V- and Front Panel DUT_GND
Hybrid Connection	Connects F/P pin to any channel (need to disable drive to the channel) ~40 Ω series impedance, ~3 MHz bandwidth

* This range is limited by the power converter ranges.
[1] 700 mV at the fastest slew rate.

Programmable AUX I/O Min/Max Levels

The programmable AUX I/O level minimum and maximum values are determined by the V+ an V- bias voltage levels. The following table lists the min and max levels based on the V+ and V- level:

Table I-4: Programmable AUX I/O Min/Max Levels Front Panel

Level	Min	Max	Units
DVH	V- + 5	V+ - 3	V
DVL	V- + 4	V+ - 7	V
CVH	V- + 2	V+ - 7	V
CVL	V- + 2	V+ - 7	V
Vcom High (CMH)	V- + 2	V+ - 7	V
Vcom Low (CML)	V- + 2	V+ - 7	V

The following table lists the min and max levels based on the power converter type 1 or 3 setting:

Table I-5: Programmable AUX I/O Min/Max Levels Power Converter Type 1 or 3

Level	Power Converter Setting							Units
	-12 to +12	-15 to +5	-10 to +10	-5 to +7	-5 to +15	0 to +24	-2 to +22	
DVH max	12	5	10	7	15	24	22	V
DVH min	-10	-13.5	-8.5	-4	-4	1	-0.5	V
DVL max	8.5	2	8.5	4.5	11.6	21	18.8	V
DVL min	-11.6	-15	-10	-5	-5	0	-2	V
CVH max	9	2.6	9	5	12.2	21.8	19.4	V
CVH min	-12	-15	-10	-5	-5	0	-2	V
CVL max	9	2.6	9	5	12.2	21.8	19.4	V
CVL min	-12	-15	-10	-5	-5	0	-2	V
CMH max	9	2.6	9	5	12.2	21.8	19.4	V
CMH min	-12	-15	-10	-5	-5	0	-2	V
CML max	9	2.6	9	5	12.2	21.8	19.4	V
CML min	-12	-15	-10	-5	-5	0	-2	V

ADC_IN

Table I-6: ADC_IN Characteristics

Description	Characteristics
ADC_IN	-10 V to +20 V, ±10 mV ±0.6%
	Input impedance >1 MΩ

PROBE SUPPORT

Table I-7: Probe Support

Description	Characteristics
PROBE COMP (AUX4 A)	LVTTL output used to control compensation mode.
PROBE MODE PBUT BCLK	LVTTL dedicated external probe module support.
PROBE_IN (AUX1 A)	See Pin Electronic AUX Channels entry above or External Probe Module entry below
PROBE_CAL (AUX2 A)	See Pin Electronic AUX Channels entry above or External Probe Module entry below
PROBE_OUT	Connects to PROBE_IN for external probe compensation
PROBE_DETECT	LVTTL input used to detect the presence of the external probe module.
+12V -12V	Low current power for external probe support. Max current 200 mA

PROBE MODULE CHARACTERISTICS

Table I-8: Probe Module Characteristics

Description	Characteristics
Probe Tip Characteristics	Input capacitance <20 pF Input Impedance 10 MΩ ± 1%
CONTACT DETECT	<5 MΩ or >50 pF
	Illuminates the green LED on the Probe Handle when contact is made.
	Contact LED will extinguish while a pattern burst is in progress.
ANALOG PERFORMANCE	Input voltage detectable range: -19 V to +19 V Note: This input range will be attenuated by the Probe but amplified by the Probe Module to present to the D/R board a signal which is ±5 V max. with a 50 Ω source termination

Description	Characteristics
	Input voltage absolute maximum rating: -200 V to +200 V. Note: O V Protection to be provided on the Probe Module
	Detector voltage accuracy; ± (50 mV + 1%)
	Detector resolution: 10 mV
	DUT_GND correction done in the Probe Module (Aux. 1 input DUT_GND correction is automatically disabled).
TIMING PERFORMANCE	Absolute accuracy: ±5 ns With respect to Channel1
	Requires field calibration
PROBE CALIBRATION (FACTORY)	Trim-pot adjustment of the contact detect compare level.
	May also be done in the field if the user has a 50 pF cap. and a 5 MΩ resistor and can get access to the trim-pot.
PROBE CALIBRATION (FIELD)	Utilizes AUX A 2, provided by the D/R board, to provide a reference signal on the Probe Module's calibration connector which will be used for Probe Compensation Calibration and DC/Timing Calibration to the Probe tip.
MINIMUM DETECTABLE PULSE WIDTH	10 ns
BUFFERED PROBE OUTPUT	Provided on the UR14 as PROBE OUT
	Output range: Same as input from the Probe Module (± 5V)
	Output Impedance: Source terminated at 50ohms in the Probe Module
	Output accuracy from Probe tip to terminated output: ± (50 mV + 1%) From the Probe tip, thru the Probe Module to the UR14 and out the PRBOUT connector
	Bandwidth from Probe tip to terminated output: 50 MHz From the Probe tip, thru the Probe Module to the UR14 and out the PRBOUT connector
+12V	62 mA minimum 82 mA maximum (max: 16.5 Vp-p @ 70 Mhz)
-12V	49 mA minimum 69 mA maximum (max: 16.5 Vp-p @ 70 Mhz)

Auxiliary I/O Channels

Table I-9: Auxiliary I/O Channel Characteristics

Description	Characteristics
General	50 MHz data rate I/O Per channel relay isolation
AUX[1:2] A	AUX[1:2] dedicated to the Probe when used Programmable
AUX3 A	LVTTL 50 Ω series terminated
AUX4 A	LVTTL dedicated to the Probe when used
AUX[5|9] A AUX[6|10] A AUX[7|11] A AUX[8|12] A	LVTTL or ECL These channels share a pin on the connector. They are a programmable selection of one of three types; LVTTL, SE ECL or Differential ECL LVTTL selection is series 50 Ω terminated ECL is parallel terminated 50 Ω to -2 V
AUX[9:12]- A	Negative side of differential ECL AUX[9|12]A used when these channels are configured as differential ECL Parallel terminated 50 Ω to -2 V Bi directional General purpose I/O 50 MHz data rate I/O Per channel relay isolation
AUX[1:4] B	Programmable
AUX[5:8] B	LVTTL or ECL These channels are a programmable selection of either LVTTL or SE ECL LVTTL selection is series 50 Ω terminated ECL is parallel terminated 50 Ω to -2 V
AUX[9:11]+ B AUX[9:11]- B	SE ECL or Differential ECL Parallel terminated 50Ω to -2V

Power Requirements

Table I-10: Power Requirements (not including Power Converter power consumption)

Voltage	Peak Current	Dynamic Current
+5 V	3680 mA	330 mA
-5.2 V	800 mA	25 mA
-2 V	694 mA	10 mA
+12 V	710 mA	42 mA
-12 V	80 mA	20 mA
+24 V	3270 mA	300 mA
-24 V	2980 mA	290 mA

Note: *Use the UR14 Current Estimator calculation tool to estimate the power converter power consumption from the ±12V and ±24V power rails. This tool is available upon request from Astronics Test Systems at atssales@astronics.com.*

Environmental

Table I-11: Environmental

Temperature	Operating: 0° C – 45° C Storage: -40° C – 70° C
Humidity	5% to 95%
Altitude	10,000 ft
Cooling Required (10°C Rise; 2 UR14s)	Max: 14.4 lps @ 2.8 mmH^20 Typ.: 10.4 lps @ 1.6 mmH^20
MTBF (ground benign)	UR14: 179,889 hours T940: 180,855 hours Power Converter: 540,040 hours T940-UR14: 77,279 hours
Dimensions	20 x 114 x 305 mm
EMC (Council Directive 89/336/EEC)	Emission: EN61326-1: 2006, Class A Immunity: EN61326-1: 2006, Table 1 ***Designed to Meet – Testing in Progress***
Safety (Low Voltage Directive 73/23/EEC)	BS EN61010-1: 2007 ***Designed to Meet – Testing in Progress***

UR14 Signal Description

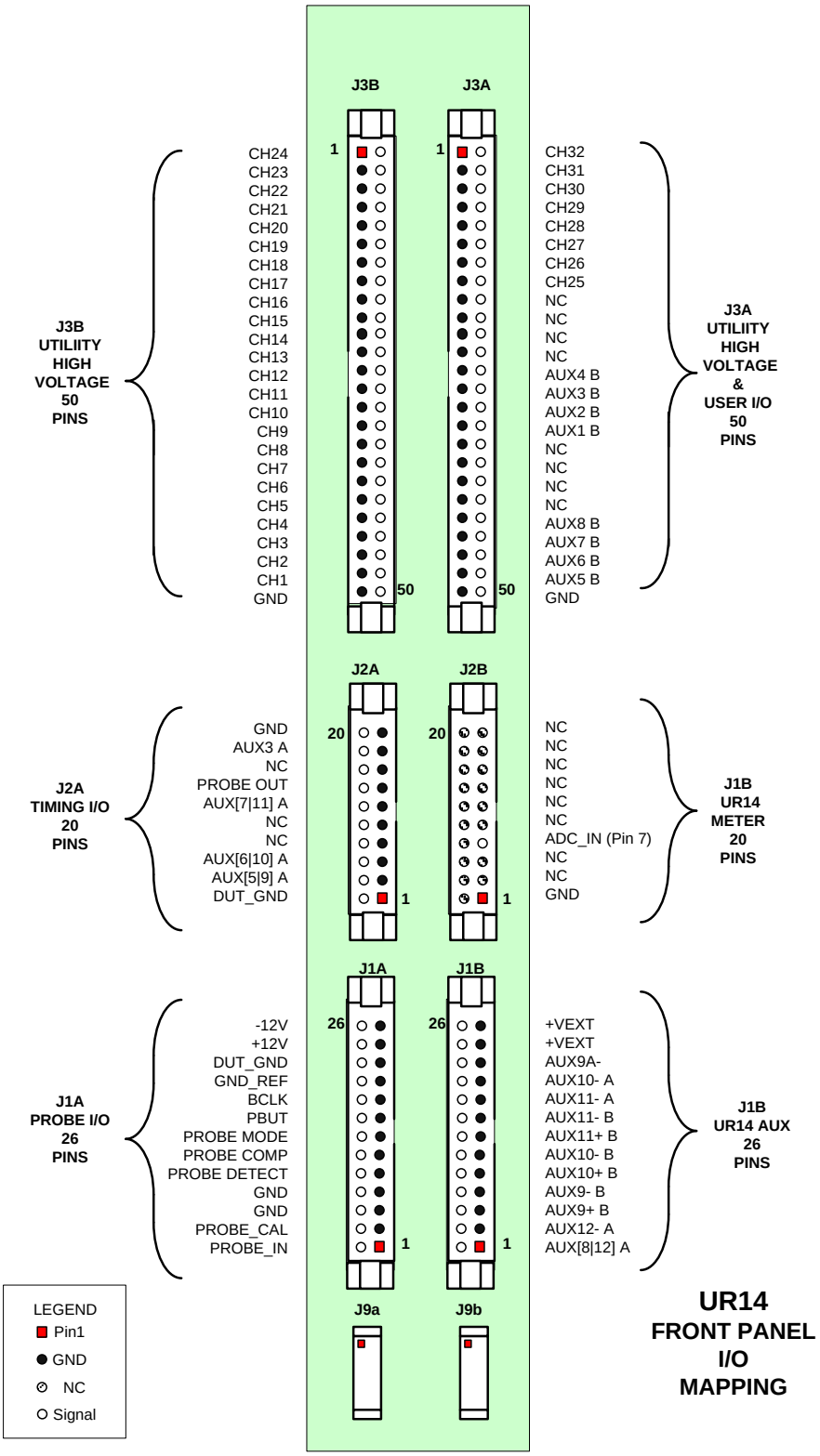


Figure I-14: Front Panel Connectors

UR14 I/O (J1A, J1B, J2A, J2B, J3A, J3B)

Table I-12: UR14 Resources

Name	Description
CH1– CH32	Bi-directional Open Collector Channels
PROBE_IN (AUX1 A)	Probe input channel or bi-directional)general purpose programmable level auxiliary I/O
PROBE_CAL (AUX2 A)	Probe calibration output channel or bi-directional general purpose programmable level auxiliary I/O
AUX[1:4] B	Programmable I/O
AUX3 A	Bi-directional general purpose LVTTL
AUX4 A	Probe support signal or bi-directional general purpose LVTTL
AUX[5|9] A AUX[6|10] A AUX[7|11] A AUX[8|12] A	LVTTL or ECL These channels share a pin on the connector. They are a programmable selection of one of three types; LVTTL, SE ECL or Differential ECL (see the next entry)
AUX[9:12]- A	Negative side of differential ECL AUX[9|12] A used when these channels are configured as differential ECL
AUX[5:8] B	LVTTL or ECL these channels are a programmable selection of either LVTTL or SE ECL
AUX[9:11]+ B AUX[9:11]- B	SE ECL or Differential ECL bi-directional general purpose I/O
PROBE OUT	Probe Support. External probe module probe compensation test point. This is a direct connection to PROBE_IN
PROBE MODE PBUT BCLK PROBE DETECT	Probe Support. These signals provide dedicated support for the external probe module.
+12V -12V	Probe Support. These power pins provide low current power for the external probe module. The maximum current is limited with an in-line poly fuse.
+VEXT	These power inputs provide a means to expand pull-up options for the Open Collector channels.
DUT_GND	DUT/UUT ground reference. All of the Pin Electronics devices have a UUT ground reference input that can be selected to be this signal or signal ground.
GND_REF	Buffered selected DUT_GND for the Pin Electronics.
GND	Signal Ground reference

Refer to Figure I-14 and Tables I-4 through I-9.

Table I-13: J3A Connector Pinout by Pin Number

Connector Pin	Signal	Connector Pin	Signal
1	GND	2	CH32
3	GND	4	CH31
5	GND	6	CH30
7	GND	8	CH29
9	GND	10	CH28
11	GND	12	CH27
13	GND	14	CH26
15	GND	16	CH25
17	GND	18	NC
19	GND	20	NC
21	GND	22	NC
23	GND	24	NC
25	GND	26	AUX4 B
27	GND	28	AUX3 B
29	GND	30	AUX2 B
31	GND	32	AUX1 B
33	GND	34	NC
35	GND	36	NC
37	GND	38	NC
39	GND	40	NC
41	GND	42	AUX8 B
43	GND	44	AUX7 B
45	GND	46	AUX6 B
47	GND	48	AUX5 B
49	GND	50	GND

Table I-14: J3B Connector Pinout by Pin Number

Connector Pin	Signal		Connector Pin	Signal
1	GND		2	CH24
3	GND		4	CH23
5	GND		6	CH22
7	GND		8	CH21
9	GND		10	CH20
11	GND		12	CH19
13	GND		14	CH18
15	GND		16	CH17
17	GND		18	CH16
19	GND		20	CH15
21	GND		22	CH14
23	GND		24	CH13
25	GND		26	CH12
27	GND		28	CH11
29	GND		30	CH10
31	GND		32	CH9
33	GND		34	CH8
35	GND		36	CH7
37	GND		38	CH6
39	GND		40	CH5
4	GND		42	CH4
13	GND		44	CH3
45	GND		46	CH2
47	GND		48	CH1
49	GND		50	GND

Table I-15: J2A Connector Pinout by Pin Number

Connector Pin	Signal	Connector Pin	Signal
1	GND	2	DUT_GND
3	GND	4	AUX[5|9] A
5	GND	6	AUX[6|10] A
7	GND	8	NC
9	GND	10	NC
11	GND	12	AUX[7|11] A
13	GND	14	PROBE OUT
15	GND	16	NC
17	GND	18	AUX3 A
19	GND	20	GND

Table I-16: J3B Connector Pinout by Pin Number

Connector Pin	Signal	Connector Pin	Signal
1	GND	2	NC
3	NC	4	NC
5	NC	6	NC
7	ADC_IN	8	NC
9	NC	10	NC
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	NC	20	NC

Table I-17: J1A Connector Pinout by Pin Number

Connector Pin	Signal	Connector Pin	Signal
1	GND	2	PROBE_IN
3	GND	4	PROBE_CAL
5	GND	6	GND
7	GND	8	GND
9	GND	10	PROBE_DETECT
11	GND	12	AUX4 A
13	GND	14	PMODE
15	GND	16	PBUT
17	GND	18	BCLK
19	GND	20	GND_REF
21	GND	22	DUT_GND
23	GND	24	+12V
25	GND	26	-12V

Table I-18: J1B Connector Pinout by Pin Number

Connector Pin	Signal	Connector Pin	Signal
1	GND	2	AUX[8|12] A
3	GND	4	AUX12- A
5	GND	6	AUX9+ B
7	GND	8	AUX9- B
9	GND	10	AUX10+ B
11	GND	12	AUX10- B
13	GND	14	AUX11+ B
15	GND	16	AUX11- B

Connector Pin	Signal
17	GND
19	GND
21	GND
23	GND
25	GND

Connector Pin	Signal
18	AUX11- A
20	AUX10- A
22	AUX9- A
24	+VEXT
26	+VEXT

J9 Connectors

The J9 connectors are currently used for calibration and for access to the auxiliary and probe signals.

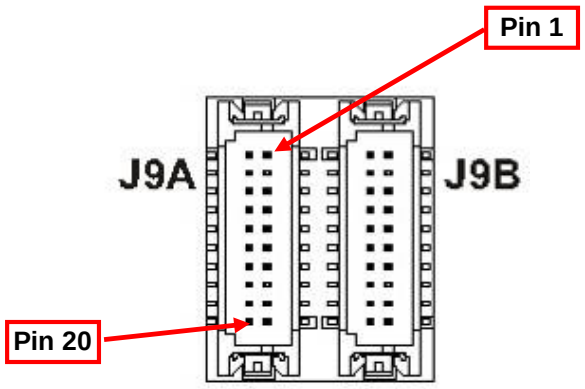


Figure I-15: UR14 J9 Calibration and Signal Connectors

Table I-19: J9A Pinout

Name	Pin No.	Description
AUX5 A	1	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
AUX6 A	3	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
AUX7 A	5	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
AUX8 A	7	(Bi-directional) General Purpose LVTTL I/O pin, 50 Ohm series
PROBE MODE A	9	(Output) Probe Support Output
BCLK A	11	(Output) Serial Clock
PBUT A	13	(Bi-directional) Probe Button Input
MPSIG A	15	(Output) Multi-purpose Signal
MONITOR	17	(Output) Monitor signal from the Pin Electronics devices ***Note**: Only one channel can be selected at a time.*
EXTFORCE A	19	(Input) External Force routed to all of the Pin Electronics devices
GND	2-20 (Even)	Ground

Table I-20: J9B Pinout

Name	Pin No.	Description
AUX5 B	1	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX6 B	3	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX7 B	5	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
AUX8 B	7	(Bi-directional) General Purpose LVTTL I/O pin, 51.1 Ohm series
PROBE MODE B	9	(Output) Probe Support Output
BCLK B	11	(Output) Serial Clock
PBUT B	13	(Bi-directional) Probe Button Input
MPSIG B	15	(Output) Multi-purpose Signal
MONITOR B	17	(Output) Monitor signal from the Pin Electronics devices ***Note**: Only one channel can be selected at a time.*
EXTFORCE B	19	(Input) External Force routed to all of the Pin Electronics devices
GND	2-20 (Even)	Ground

Calibration

Driver/Receiver boards are calibrated using the following settings prior to shipment:

- -15 V to +17 V Voltage Mode
  - Power Converter -12 to +12
- -7 V to +24 V Voltage Mode
  - Power Converter -5 to +15

DAC Basic	Factory stored in EEPROM
Driver channel deskew	Factory stored in EEPROM
ADC/Monitor	Field upgradable stored in EEPROM
DVH/DVL	Field upgradable stored in EEPROM
CVH/CVL	Field upgradable stored in EEPROM
Vcom High/Vcom Low	Field upgradable stored in EEPROM
Isource//Isink	Field upgradable stored in EEPROM
IAL/IAH	Field upgradable stored in EEPROM
Inter-module timing deskew	Static
End-of-cable deskew	Static

Appendix J
DRM Timing Characteristics

Introduction

The timing characteristics of the DRM are important when external input signals are used to alter normal “internal” operation of the Sequencer. Similarly, the Sequencer can also output signals for use by other instruments. The timing of these outputs may be important to the user.

Some of these timing characteristics are only applicable to the master sequencer. Others will vary depending on the number of DRMs in the DRS.

External inputs include the Auxiliary (AUX) and the VXI Trigger (TRG) inputs. There are five types of AUX inputs (Programmable, LVTTL, ECL, LVDS and 422/485). The LVTTL AUX input will be used as the timing reference with adjustment values provided for the other four. There are two types of VXI TRG inputs (TTL and ECL). The TTL input will be used as the timing reference with adjustment values provided for the ECL input.

Similarly, the External outputs include the AUX and TRG outputs. There are five types of AUX outputs (Programmable, LVTTL, ECL, LVDS and 422/485). The LVTTL AUX output will be used as the timing reference with adjustment values provided for the other three. There are two types of VXI TRG outputs (TTL and ECL). The TTL output will be used as the timing reference with adjustment values provided for the ECL output.

Notes:

- *The Programmable AUX I/O is only available on the DR3e.*
- *The LVDS AUX I/O is only available on the DR2.*
- *The 422/485 AUX I/O is only available on the DR7.*
- *The Programmable AUX I/O is based on LVTTL levels without any delay calibration.*
- *A DR3e Channel (with LVTTL levels) will have the same timing characteristics as a Programmable AUX I/O when calibrated.*

External AUX Input Timing Adjustments

LVTTL: timing reference

ECL: -1 ns (faster)

Programmable: +9 ns (slower)

422/485: TBD

External AUX Output Timing Adjustments

LVTTL: timing reference

ECL: 0 ns (same as LVTTL)

Programmable: +8 ns (slower)

422/485: TBD

TRG Input Timing Adjustments

TTLTRG Bus: timing reference (based on the leading edge*)

ECLTRG Bus: +5 ns (slower)

Note: *The TTLTRG Bus open-collector recovery time is 17 ns min. and increases ~4 ns for each DRM installed. Other VXI modules installed in the same chassis may further aggravate the recovery time.*

***** The leading edge for the TTLTRG Bus is a falling edge.

TRG Output Timing Adjustments

TTLTRG Bus: timing reference (to the leading edge)

ECLTRG Bus: -1 ns (faster)

AUX Input to TRG

AUX LVTTL to TTLTRG Bus: 16 ns

TRG Input to AUX Output

TTLTRG to AUX LVTTL: 15 ns (LE)

DRS Timing Adjustments

Independent: timing reference

Linked: +1 ns

VXI Local Bus: ~1.5 ns/DRM

TTLTRG Bus: ~1 ns/DRM

ECLTRG Bus: ~1 ns/DRM

External T0CLK to T0CLK In (at min. delay setting)

Independent:

AUX LVTTL to LVTTL: 86 ns (500 MHz master clock)

AUX LVTTL to LVTTL: 140 ns (250 MHz master clock)

x + 2n = 86 ns

x + 4n = 140 ns

Thus: n = 27 master clocks; x = 32 ns of fixed delay

Add to x: Linked or VXI Local Bus adjustments

Note: *The programmable delay can correct for this input offset.*

External Halt Setup Time to SEQ_CLK Out

AUX LVTTL to LVTTL: 22 ns min.

Note: *For all master clock frequencies, the master clock stops before a Phase at 0 ns will be asserted.*

External Pause to CLK Cease

There are no clocked elements in this path.

AUX LVTTL to CLK_Stop*: 22 ns.

In addition to this, there is an additional amount of time up to ½ the period of the master clock before the master clock appears to stop (FE).

***** An internal signal

External Pause/Phase Resume to CLK Resume

There are no clocked elements in this path.

AUX LVTTL to (NOT) CLK_Stop: 22 ns.

To addition to this, there is an additional amount of time up to one full period of the master clock before the master clock actually restarts (RE).

External Jump Setup Time to T0CLK In

AUX LVTTL to Jump Test (AUX LVTTL): 20 ns.

Jump Test setup time to Jump Strobe (AUX LVTTL): 2 ns

Jump Strobe to T0CLK_In (AUX LVTTL): 36 ns (500 MHz master clock)

Jump Strobe to T0CLK_In (AUX LVTTL): 140 ns (100 MHz master clock)

x + 2n = 36 ns

x + 10n = 140 ns

Thus: n = 13 master clocks; x = 10 ns

Add to x: Linked or VXI Local Bus adjustments

External Start Setup Time to T0CLK In

For a 10 master clock standby pattern:

AUX LVTTL to LVTTL: 60 ns max. (500 MHz master clock)

AUX LVTTL to LVTTL: 180 ns max. (100 MHz master clock)

x + 2n = 60 ns

x + 10n = 180 ns

Thus: n = 15 master clocks; x = 30 ns

“n” is composed of a 5 master clock intrinsic delay plus the period of the standby pattern (10 master clocks in this case). A longer Standby period will lengthen this maximum. If starting from Idle, the setup time is with respect to the last T0CLK of the Idle step.

Add to x: Linked or VXI Local Bus adjustments

External Stop Setup Time to T0CLK In

For a 10 master clock pattern period:

AUX LVTTL to T0CLK: 70 ns max. (500 MHz master clock)

AUX LVTTL to T0CLK: 222 ns max. (100 MHz master clock)

x + 2n = 70 ns

x + 10n = 222 ns

Thus: n = 19; x = 32 ns of fixed delay

“n” is composed of a 9 master clock intrinsic delay plus the period of the pattern one is currently trying to stop in. A longer pattern period will lengthen this maximum.

Add to x: Linked or VXI Local Bus adjustments

A Channel Input to TRG Bus (for a channel test)

DR1 Channel In to TTLTRG Bus: TBD

DR2 Channel In to TTLTRG Bus: TBD

DR3 Channel In to TTLTRG Bus: 29 ns

SEQ_ACT/IDLE_ACT/Sync Pulse/Seq. Flag to TRG Bus

AUX LVTTL to TTLTRG Bus: 1 ns

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