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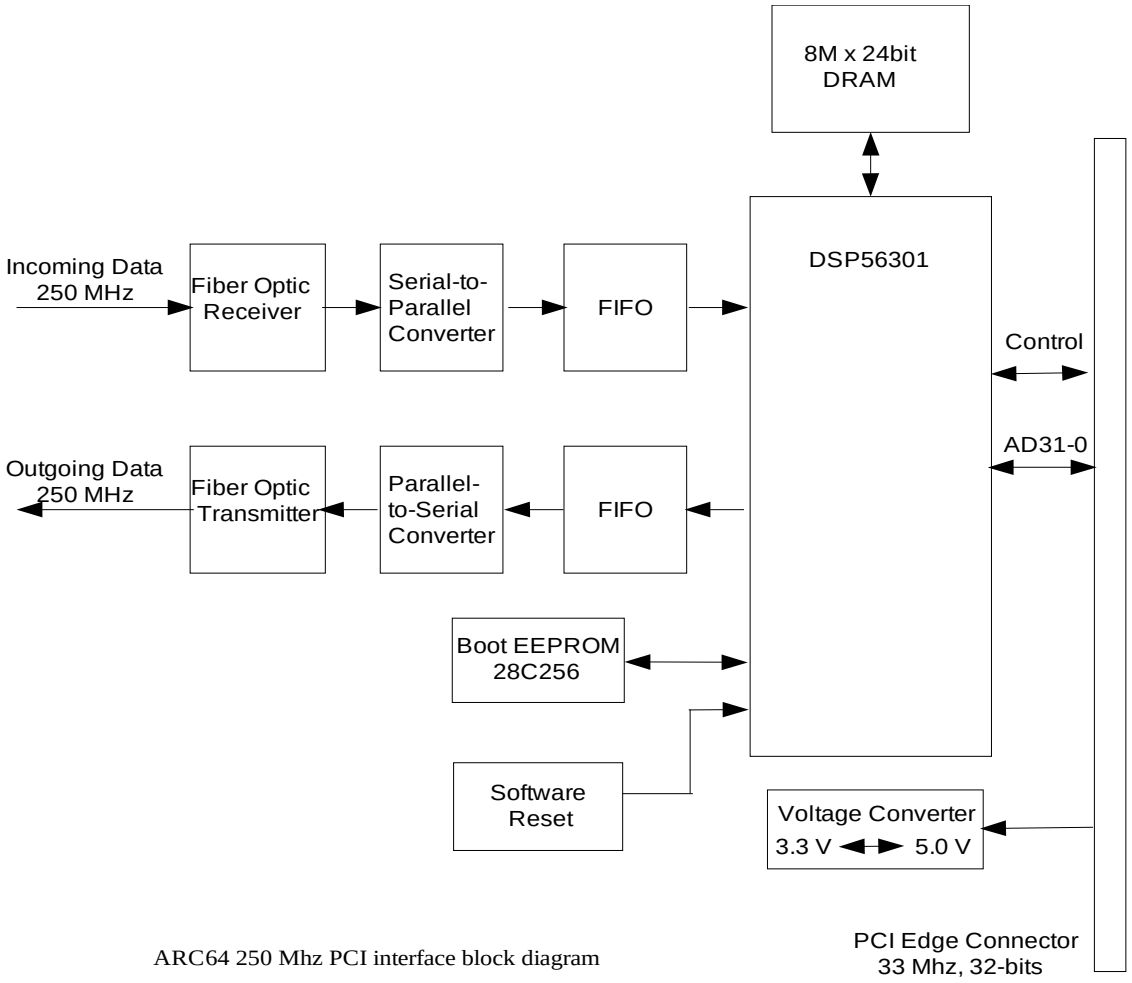
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ARC64: 250 MHz PCI INTERFACE BOARD, GEN III

This User's Manual describes the PCI interface board product number ARC-64. The board is designed to install in a Peripheral Component Interconnect (PCI) bus that supports 32-bit, 33 MHz operation with either 3.3 or 5.0 volt power source (or both) supplied by the host computer. The board is classified as a short card, measuring 174.6 mm in length and 106.7 mm in width (4.20 x 6.875 inches), including the edge connector, which has 124 pads. In the language of the PCI specification, the board receives commands and parameters from the host computer as a target and writes image and reply data to the host computer as an initiator, which is analogous to a DMA controller. A Freescale (formerly Motorola) DSP56301 manages the on-board resources and serves as the PCI bus controller. The interface board communicates to the controller over a fiber optics link operating at a bit rate of 250 MHz. This board is designed to operate with the ARC-22 timing board resident in the controller. The ARC-22 timing and ARC-64 PCI interface boards are designated as Gen-III controller boards.

Several documents and software packages are provided by Freescale that may be of interest. These are all available on the www.freescale.com web site. Several of the most useful documents are the DSP56300 Family Manual, the DSP56301 User's Manual, and the PCI application note AN1780.



ARC64 250 Mhz PCI interface block diagram

CIRCUIT DESCRIPTION

The DSP boots from a 32k x 8 bit 28-pin socketed DIP EEPROM (generic part number CAT28C256, any speed) when the RESET* signal input to the DSP makes a low to high transition. The RESET* line may be asserted low true by the host computer's assertion of the PCIRST* line if the jumper JP2 is installed or by a power-on reset circuit when power to the PCI backplane is applied. The EEPROM contains the complete program for operating the interface board, and further downloads of firmware from the host computer are needed only if the user requires a program different from the one contained in the EEPROM. In this respect the PCI board is quite different from the controller boards which require code downloads to fully operate. The boot code written to the EEPROM is generated with a short script named "rom" that assembles and links a DSP source code file named "pciboot.asm" written in assembly language to generate an S-record file named "pci.s" that is loadable into an EEPROM burning machine. Alternatively the stand-alone program “pciromburn” may be used to write a file named “pci.rom” (also generated by the “rom” script) to the EEPROM while the board is installed in the host computer if the write enable jumper WE in installed on the interface board. The script "host" generates a file named "pci.lod" that can be downloaded via the host over the PCI bus to the DSP, an option available in voodoo.

A software reset button is located on the front panel of the PCI interface board. It asserts the interrupt line IRQC* that causes the DSP program to jump to an interrupt service routine that sets the program counter to the beginning of the program INIT and sets the stack pointer to the top of the stack. It does not assert the hardware RESET* line to the DSP, which is asserted on power-up. This switch can be used to get out of locked up DSP code without having to reboot the host computer. The switch on the board is OR'd with two pins from the external 26-pin connector so a switch external to the host computer can be installed by the user.

Commands and parameters are transmitted to the controller timing board following the protocol discussed in the ARC-22 timing board User's Manual. The data words are all 33 bits long, containing a start bit, a preamble bit (either 0xAC or 0x53 for resetting the timing board), and 24 bits of data. They are buffered after the DSP by a byte-wide FIFO to ensure that there are no gaps in between the bytes of a word in the serial data stream. Commands, replies and image data are received by the fiber optics, converted to parallel form a byte at a time and stored in two byte-wide FIFOs before being read by the DSP. Commands and replies are read by the DSP one word at a time by having the DSP examine the FIFO empty flag, whereas image data is read in blocks of 512 pixels at a time unless the number of pixels remaining in the image is less than the 512 pixel block size.

The fiber optic circuits contain Agilent parts operating in the IR regime at a bit rate of 250 MHz, derived from Cypress Hot Link parallel-to-serial and serial-to-parallel converters that synthesize a 250 MHz clock from an input clock of 25 MHz. The parts required ten clocks to transmit or receive each byte, so the 250 MHz bit rate translates into a byte speed of 25 Mbytes/sec, or 12.5 Mpixels/sec. Image data can be transmitted from the timing board at this rate for a sustained time. The red LED mounted on the front panel being ON indicates that a valid fiber optic signal is NOT being received by the circuit.

A bank of dynamic random access memory (DRAM) parts is available to buffer images

should the host computer not be able to write images to user memory space fast enough to keep up with image data from the controller. It consists of three 8 Mbyte memories grouped into one 8M x 24 bit memory space. However, DSP code to actually use this DRAM is not part of the normal release and only available on special request.

There is a 26-pin, three row DB connector installed on the front panel of the board to support several input and output functions. The data bits D15-D0 from the DSP are available for connection to external hardware, as are the two LED driving signals and interrupt request lines. Also available are asynchronous communication lines from the DSP, appropriately buffered.

REVISION HISTORY

Rev. 5A: The initial revision of this board was Rev. 5A, dated 6/4/01. It was suitable for operating with PCI Revision 2.1 systems that provide 5.0 volt power to the PCI backplane. The newer PCI revision 2.2 does not require a 5.0 volt supply, but only a 3.3 volt supply.

Rev. 5B: This revision, dated 5/4/04, was designed to allow operation on PCI buses that do not provide a 5.0 volt power source. It will operate in a PCI Revision 2.2 bus, which supplies either 5.0 or 3.3 volt power, or both.

Rev. 5C: Dated 3/15/05, the PAL was changed on this revision from a Cypress to an Altera part because of increasing difficulty obtaining the Cypress part. The layout was improved with straighter and shorter lines as well as more copper on the power and ground planes. A driving circuit was added to the system clock distribution circuit to improve its integrity throughout the board. These changes enhanced the reliability.

Rev. 5D: This revision, dated June 13, 2006, incorporates a small change by special request from one user to have the empty flag of each of the two receiving FIFOs separately connected to the DSP so it can determine if wayward bytes have been received.

Rev. 5E: Dated May 17, 2006, this revision is not properly marked on the silk screen. Instead of being marked 5E it has a white rectangle in the silk screen, where the revision level is supposed to be written in. Anyway, this revision connects the PCI signal PVCL to the DSP to tell the DSP whether the PCI bus is signaling in 3.3 or 5 volt mode. Without this change earlier revision boards can fail if they are installed in busses with boards that signal at 5 volts. The symptom is pretty dramatic, as the PCI board will crash during image transfer, as it undergoes a power fail and reboot from EEPROM.

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