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# ATDH2200E Programming Kit

## User Guide



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# Section 1

# Atmel's ATDH2200E Configurator Programming Kit

## 1.1 Features

### 1.1.1 Hardware

- Supports Programming of all AT17LV Series Devices
- Conection to Allow In-System Programming (ISP)
- Runs off Portable 9V DC Power Supply
- 5.0V Supply

### 1.1.2 Software

- CPS – Configurator Programming System
- GUI-based Interface
- Supports Windows® 95/98/2000 and WindowsNT®
- Online Help
- Supports Programming Reset Polarity
- Verification Routines to Validate Programming
- Accepts HEX, MCS, POF, RBF and BST File Formats

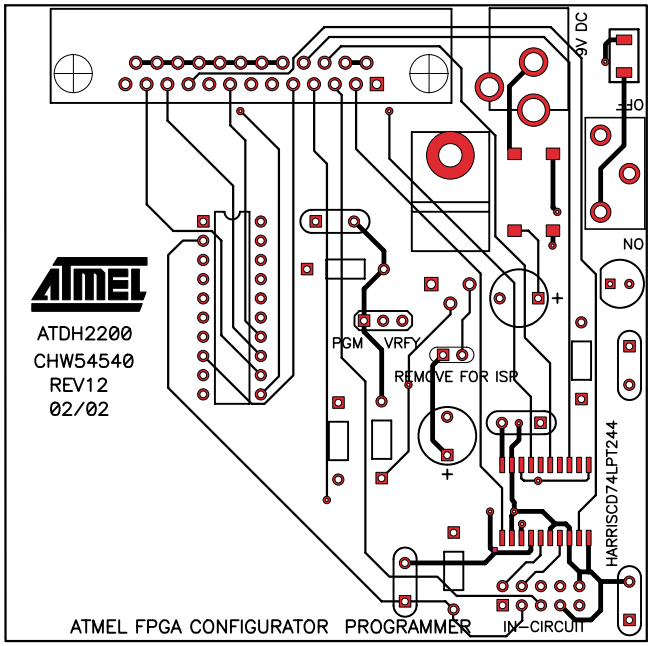
### 1.1.3 System Contents

- ATDH2200 Programming Board (Rev.12)
- ATDH2222 20-pin PLCC Adapter
- CPS Software
- ATDH2200E Programming Kit User Guide
- Standard (PC Printer Port) Parallel Cable
- 10-pin Ribbon Cable for ISP
- 9V DC, 500 mA, 2.1 mm Center Positive/Negative Power Supply
- Sample AT17LV Devices

## 1.2 Introduction

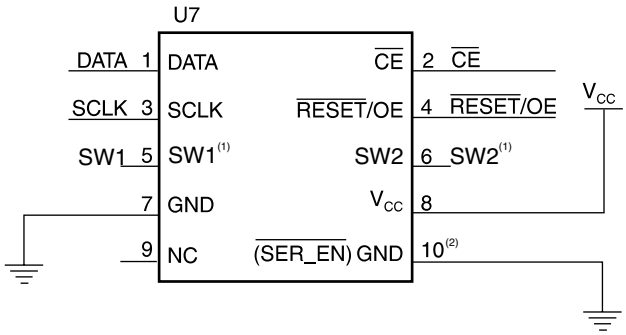
The ATDH2200E allows designers to quickly and economically program Atmel's family of AT17 Configuration Memories. The system also provides support for new devices in the AT17 family prior to third-party pogrammer support being available. A truly portable solution that allows engineers to work from their lab bench or office.

***Figure 1-1.*** ATDH2200E Configurator Programming Board




## 1.3 In-System Programming Connector

***Figure 1-2.*** In-System Programming Header




Notes:
1. SW1 and SW2 are designed to be used for special cascaded EEPROM circuitry in the future. SW1 and SW2 are connected to pin 3 and pin 4 of the parallel port on the ATDH2200E board (Rev.12).
2. Pin 10 activates $\overline{\text{SER_EN}}$ on target board.

The ATDH2200E programming board has a 10 pin header (0.1" spacing) to facilitate in-system programming (Figure 1-2) of the AT17 parts. The control signals generated by the software are fed to the header, as well as to socket U3 on the board. By placing a similar socket on the target system and connecting the programming board to that target system, the programming algorithms written by Atmel can be used to program an AT17 device in-system.

**Adapters Available for the ATDH2200E**

- ATDH2220 for 20-pin PLCC Devices (Excluding 2-Mbit Devices)
- ATDH2221 for 20-pin SOIC Devices
- ATDH2222 for all 20-pin PLCC Devices (Including 2-Mbit Devices)
- ATDH2223 for all 8-pin SOIC Devices
- ATDH2224 for 44-pin TQFP Devices
- ATDH2226 for 32-pin TQFP Devices
- ATDH2227 for 44-pin PLCC Devices
- ATDH2227A for 44-pin A Part PLCC Devices
- ATDH2228 for 8-pin LAP Devices

# Section 2

# Stand-alone Device Programming Using Atmel's ATDH2200E Configurator Programming System

## 2.1 Hardware Setup

This User Guide is intended for the ATDH2200 Programming Board Rev.12. In Rev.12, **JP1** is equivalent to **JP2** in Rev.11. In Rev.12, **J2** is equivalent to **JP3** in Rev.11.

### 2.1.1 Hardware Requirements

- ATDH2200 Programming Board Rev.12
- 25-pin Parallel Cable
- 9V DC Power Supply
- FPGA Configurators – AT17(A) Series Devices
- PC with Standard Configuration Parallel Port
- Socket Adapters
  - ATDH2220 for 20-pin PLCC Devices (Excluding 2-Mbit Devices)
  - ATDH2221 for 20-pin SOIC Devices
  - ATDH2222 for all 20-pin PLCC Devices (Including 2-Mbit Devices)
  - ATDH2223 for all 8-pin SOIC Devices
  - ATDH2224 for 44-pin TQFP Devices
  - ATDH2226 for 32-pin TQFP Devices
  - ATDH2227 for 44-pin PLCC Devices
  - ATDH2227A for 44-pin A Part PLCC Devices
  - ATDH2228 for 8-pin LAP Devices

### 2.1.2 Hardware Connections

1. Connect the **25-pin parallel cable** from the PC's parallel port to connector **U1** on the ATDH2200 programming board.
2. Connect the power supply from an AC wall outlet to the **9V DC** connector.
3. Set jumper **JP1** to **PGM** unless otherwise specified for a specific procedure.
4. Set jumper **J2** to use the power supply on the board.
5. Insert the AT17(A) Series device directly in the socket marked **U3** or via a socket adapter inserted into **U3**. Make sure the adapter is correctly placed into the socket.
6. Set **SW1** to the "**ON**" position to apply power to the board. **LED** (D1) **illuminates**.

## 2.2 Software Setup

### 2.2.1 Software Requirements

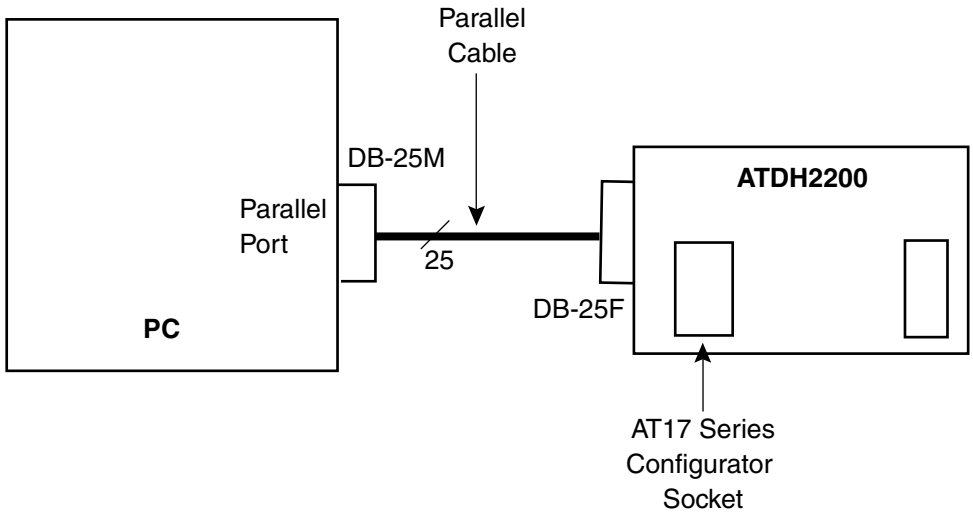
- CPS (Configurator Programming System)
- Windows® 98/2000 or WindowsNT®

### 2.2.2 Installing and/or Launching CPS

**If you are using Windows NT or Windows 2000, the installation must be performed by the System Administrator.**

1. Exit all open applications and insert the "AT17(A) Configurator Programming System" installation disk in the appropriate drive.
2. Click the **Start** button and select **Run**.
3. Type your disk drive letter followed by :**`\CPSInstall.exe`** (e.g., **`A:\CPSInstall.exe`**).
4. Follow the on-screen prompts to complete the installation.

***Figure 2-1.*** ATDH2200 Stand-alone Device Programming



## 2.3 Using a Configurator with Atmel FPGAs/FPSLICs

Perform the hardware and software setup as described in paragraphs 2.1 and 2.2.

### 2.3.1 Programming the Contents of a *.BST File to AT17 Devices

1. Procedure → Select "/P: Partition, program and verify from an Atmel file".
2. Input File → **<design>.bst**.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - Reset Polarity → Select the reset polarity.
   - FPGA Family → Select "AT40K/AT94K" or "AT6K/Other".
   - A2 Bit Level → Select "Low".
5. Press "Start Procedure" (1).

### 2.3.2 Reading the Contents of the Configurator to a *.BST File

1. Procedure → Select "/R: Read data from device and save to an Atmel file".
2. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT40K/AT94K" or "AT6K/Other".
   - A2 Bit Level → Select "Low".
4. Press "Start Procedure" (1).

### 2.3.3 Verifying the Device against a *.BST File

1. Procedure → Select "/V: Verify device against an Atmel file".
2. Input File → **<design>.bst**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT40K/AT94K" or "AT6K/Other".
   - A2 Bit Level → Select "Low".
4. Press "Start Procedure" (1).

### 2.3.4 Verifying the Device Reset Polarity

1. Procedure → Select "/X: Verify device reset polarity".
2. Options → Default or previous settings are given. You may need to modify the following:
   - Reset Polarity → Select the reset polarity.
3. Set **JP1** to the **VRFY** position on the ATDH2200 board.
4. Press "Start Procedure" (1).
5. Set **JP1** back to the **PGM** position on the ATDH2200 board.
6. Press the View Log files button to view reset polarity.

***Note:*** ***1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

## 2.4 Using a Configurator with Xilinx® FPGAs

Perform the hardware and software setup as described in paragraphs 2.1 and 2.2.

### 2.4.1 Program the Contents of a *.MCS File to AT17 Devices

1. Procedure → Select "/E: Convert, partition, program and verify from a Xilinx file".
2. Input File → **<design>.mcs** (Xilinx's straight hex file is also supported).
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - Reset Polarity → Select the reset polarity.
   - A2 Bit Level → Select "Low".
5. Press "Start Procedure" (1).

### 2.4.2 Converting a *.MCS File

1. Procedure → Select "/H: Convert a Xilinx file".
2. Input File → **<design>.mcs**.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Press "Start Procedure".

### 2.4.3 Reading the Contents of the Configurator to a *.BST File

1. Procedure → Select "/R: Read data from device and save to an Atmel file".
2. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT6K/Other".
   - A2 Bit Level → Select "Low".
4. Press "Start Procedure" (1).

### 2.4.4 Verifying the Device against a* .BST File

1. Procedure → Select "/V: Verify device against an Atmel file".
2. Input File → **<design>.bst**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT6K/Other".
   - A2 Bit Level → Select "Low".
4. Press "Start Procedure" (1).

***Note:*** ***1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

### 2.4.5 Verifying the Device Reset Polarity

1. Procedure → Select "/X: Verify device reset polarity".
2. Options → Default or previous settings are given. You may need to modify the following:
   – Reset Polarity → Select the reset polarity.
3. Set **JP1** to the **VRFY** position on the ATDH2200 board.
4. Press "Start Procedure" (1).
5. Set **JP1** back to the **PGM** position on the ATDH2200 board.

***Note:*** ***1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

## 2.5 Using a Configurator with Altera® FPGAs

Perform the hardware and software setup as described in paragraphs 2.1 and 2.2.

### 2.5.1 Programming the Contents of a *.POF/*.RBF File to AT17 Devices

1. Procedure → Select "/A: Convert, partition, program and verify from an Altera file".
2. Input File → **<design>.<pof | rbf>**.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   – EEPROM Density → Select the device density.
   – Reset Polarity → Select the reset polarity.
   – A2 Bit Level → Select "Low".
5. Press "Start Procedure" (1).

### 2.5.2 Converting and Partitioning a *.POF/*.RBF File

1. Procedure → Select "/B: Convert and partition an Altera file".
2. Input File → **<design>.<pof | rbf>**.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   – EEPROM Density → Select the device density.
5. Press "Start Procedure".

### 2.5.3 Reading the Contents of the Configurator to a *.BST File

1. Procedure → Select "/R: Read data from device and save to an Atmel file".
2. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
3. Options → Default or previous settings are given. You may need to modify the following:
   – EEPROM Density → Select the device density.
   – FPGA Family → Select "AT6K/Other".
   – A2 Bit Level → Select "Low".)
4. Press "Start Procedure" (1).

### 2.5.4 Verifying the Device against a *.BST File

1. Procedure → Select "/V: Verify device against an Atmel file".
2. Input File → **<design>.bst**.
3. Options → Default or previous settings are given. You may need to modify the following:
   – EEPROM Density → Select the device density.
   – FPGA Family → Select "AT6K/Other".
   – A2 Bit Level → Select "Low".
4. Press "Start Procedure" (1).

***Note:*** ***1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

### 2.5.5 Verifying the Device Reset Polarity

1. Procedure → Select "/X: Verify device reset polarity".
2. Options → Default or previous settings are given. You may need to modify the following:
   – Reset Polarity → Select the reset polarity.
3. Set **JP1** to the **VRFY** position on the ATDH2200 board.
4. Press "Start Procedure" (1).
5. Set **JP1** back to the **PGM** position on the ATDH2200 board.

### 2.5.6 Enabling the Clock Output on the AT17C/LV512A/010A/002A Configurator

1. Procedure → Select "/M: Enable AT17C512A/010A/020A/002A Internal Clock".
2. Options → Default or previous settings are given. You may need to modify the following:
   – EEPROM Density → Select the device density.
   – A2 Bit Level → Select "Low".
3. Press "Start Procedure" (1)(2).

### 2.5.7 Disabling the Clock Output on the AT17C/LV512A/010A/002A Configurator

1. Procedure → Select "/M: Disable AT17C512A/010A/020A/002A Internal Clock".
2. Options → Default or previous settings are given. You may need to modify the following:
   – EEPROM Density → Select the device density.
   – A2 Bit Level → Select "Low".
3. Press "Start Procedure" (1)(2).

***Notes:*** ***1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

***2.*** After the internal oscillator (DCLK) of the device is enabled/disabled, a power cycle (reset) of the programming board is required before any other programming procedure takes place.

## 2.6 Using a Configurator with Cypress® FPGAs

Perform the hardware and software setup as described in paragraphs 2.1 and 2.2.

### 2.6.1 Programming the Contents of a *.HEX File to AT17 Devices

1. Procedure → Select "/CP: Convert, partition, program and verify from a Cypress file".
2. Input File → **<design>.< hex>**.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - Reset Polarity → Select the reset polarity.
   - A2 Bit Level → Select "Low".
5. Press "Start Procedure" (1).

### 2.6.2 Converting and Partitioning a *.HEX File

1. Procedure → Select "/CB: Convert and partition a Cypress file".
2. Input File → **<design>.<hex>**.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
5. Press "Start Procedure".

### 2.6.3 Reading the Contents of the Configurator to a *.BST File

1. Procedure → Select "/R: Read data from device and save to an Atmel file".
2. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT6K/Other".
   - A2 Bit Level → Select "Low".
4. Press "Start Procedure" (1).

### 2.6.4 Verifying the Device against a *.BST File

1. Procedure → Select "/V: Verify device against an Atmel file".
2. Input File → **<design>.bst**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT6K/Other".
   - A2 Bit Level → Select "Low".
4. Press "Start Procedure" (1).

***Note:*** ***1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

### 2.6.5 Verifying the Device Polarity

1. Procedure → Select "/X: Verify device reset polarity".
2. Options → Default or previous settings are given. You may need to modify the following:
   – Reset Polarity → Select the reset polarity.
3. Set **JP1** to the **VRFY** position on the ATDH2200E board.
4. Press "Start Procedure".

# Section 3

# In-System Programming (ISP) Using Atmel's ATDH2200E Configurator Programming System

## 3.1 Hardware Setup

This User Guide is intended for the ATDH2200 Programming Board Rev.12. In Rev.12, **JP1** is equivalent to **JP2** in Rev.11. In Rev.12, **J2** is equivalent to **JP3** in Rev.11.

### 3.1.1 Hardware Requirements

- ATDH2200 Programming Board Rev.12
- 25-pin Parallel Cable
- 10-pin Ribbon Cable
- PC with Standard Configuration Parallel Port
- FPGA Configurators – AT17(A) Series Devices

### 3.1.2 Hardware Connections

1. Connect the **25-pin parallel cable** from the PC's parallel port to connector **P1** on the ATDH2200 programming board.
2. Connect the 10-pin ribbon cable from the **ATDH2200's** in-system programming **Header U1** to the **Target System's** matching ISP **Header**.
3. Set jumper **JP1** to **PGM**[1]**.**
4. Remove jumper **JP2**[1].
5. Insert the AT17(A) Configurator in the socket of the Target System.
6. Apply power to the Target System.

***Note:*** *1.* There is no jumper setting for the ATDH2225 ISP direct download cable. Only the connection described in Figure 3 is required.

## 3.2 Software Setup

### 3.2.1 Software Requirements

- CPS (Configurator Programming System)
- Windows 98/2000 or Windows NT

### 3.2.2 Installing and/or Launching CPS

**If you are using Windows NT or Windows 2000, the installation must be performed by the System Administrator.**

1. Exit all open applications and insert the "AT17(A) Configurator Programming System" installation disk in the appropriate drive.
2. Click the **Start** button and select **Run**.
3. Type your disk drive letter followed by :**`\CPSInstall.exe`** (e.g., **`A:\CPSInstall.exe`**).
4. Follow the on-screen prompts to complete the installation.

***Figure 3-1.*** ATDH2200 In-System Programming

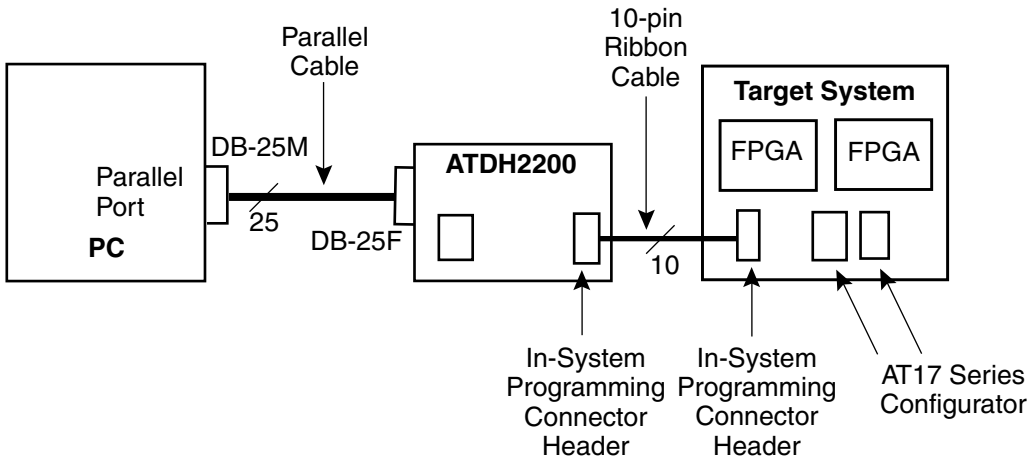
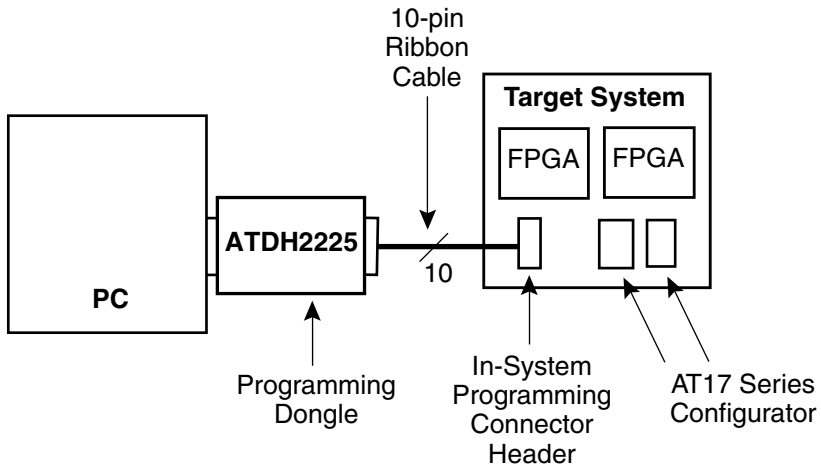



**Figure 3.** ATDH2225 In-System Programming



## 3.3 Using a Configurator with Atmel FPGAs/FPSLICs

Perform the hardware and software setup as described in paragraphs 3.1 and 3.2.

### 3.3.1 Programming the Contents of a *.BST File to AT17 Devices

1. Procedure → Select "/P: Partition, program and verify from an Atmel file".
2. Input File → **<design>.bst**.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - Reset Polarity → Select the reset polarity.
   - FPGA Family → Select "AT40K/AT94K" or "AT6K/Other".
   - A2 Bit Level → Select "Specify before each device" (2).
5. Press "Start Procedure" (1).

### 3.3.2 Reading the Contents of the Configurator to a *.BST File

1. Procedure → Select "/R: Read data from device and save to an Atmel file".
2. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT40K/AT94K" or "AT6K/Other".
   - A2 Bit Level → Select the level that matches the level seen on the A2 pin of the target device.
4. Press "Start Procedure" (1).

### 3.3.3 Verifying the Device against a *.BST File

1. Procedure → Select "/V: Verify device against an Atmel file".
2. Input File → **<design>.bst**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT40K/AT94K" or "AT6K/Other".
   - A2 Bit Level → Select the level that matches the level seen on the A2 pin of the target device.
4. Press "Start Procedure" (1).

***Notes:*** ***1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

***2.*** During programming, you will be asked to select the level that matches the level seen on the A2 input pin of each target device.

## 3.4 Using a Configurator with Xilinx FPGAs

Perform the hardware and software setup as described in paragraphs 3.1 and 3.2.

### 3.4.1 Programming the Contents of a *.MCS File to the AT17 Devices

1. Procedure → Select "/E: Convert, partition, program and verify from a Xilinx file".
2. Input File → **<design>.mcs.** Xilinx's straight hex file is also supported.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - Reset Polarity → Select the reset polarity.
   - A2 Bit Level → Select "Specify before each device" (2).
5. Press "Start Procedure" (1).

### 3.4.2 Converting a *.MCS File

1. Procedure → Select "/H: Convert a Xilinx file".
2. Input File → **<design>.mcs.** Xilinx's straight hex file is also supported.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Press "Start Procedure".

### 3.4.3 Reading the Contents of the Configurator to a *.BST File

1. Procedure → Select "/R: Read data from device and save to an Atmel file".
2. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT6K/Other".
   - A2 Bit Level → Select the level that matches the level seen on the A2 pin of the target device.
4. Press "Start Procedure" (1).

### 3.4.4 Verifying the Device against a *.BST File

1. Procedure → Select "/V: Verify device against an Atmel file".
2. Input File → **<design>.bst**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT6K/Other".
   - A2 Bit Level → Select the level that matches the level seen on the A2 pin of the target device.
4. Press "Start Procedure" (1).

***Notes: 1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

***2.*** During programming, you will be asked to select the level that matches the level seen on the A2 input pin of each target device.

## 3.5 Using a Configurator with Altera FPGAs

Perform the hardware and software setup as described in paragraphs 3.1 and 3.2.

### 3.5.1 Programming the Contents of a *.POF/*.RBF File to AT17 Devices

1. Procedure → Select "/A: Convert, partition, program and verify from an Altera file".
2. Input File → **<design>.<pof | rbf>**.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - Reset Polarity → Select the reset polarity.
   - A2 Bit Level → Select "Specify before each device" (2).
5. Press "Start Procedure" (1).

### 3.5.2 Converting and Partitioning a *.POF/*.RBF File

1. Procedure → Select "/B: Convert and partition an Altera file".
2. Input File → **<design>.<pof | rbf>**.
3. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
4. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
5. Press "Start Procedure".

### 3.5.3 Reading the Contents of the Configurator to a *.BST File

1. Procedure → Select "/R: Read data from device and save to an Atmel file".
2. Output File → Defaults to **<CPS_INSTALL_DIRECTORY>\out.bst** or the **most recently used output filename**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT6K/Other".
   - A2 Bit Level → Select the level that matches the level seen on the A2 pin of the target device.
4. Press "Start Procedure" (1).

***Notes:*** ***1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

***2.*** During programming, you will be asked to select the level that matches the level seen on the A2 input pin of each target device.

### 3.5.4 Verifying the Device against a *.BST File

1. Procedure → Select "/V: Verify device against an Atmel file".
2. Input File → **<design>.bst**.
3. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - FPGA Family → Select "AT6K/Other".
   - A2 Bit Level → Select the level that matches the level seen on the A2 pin of the target device.
4. Press "Start Procedure" (1).

### 3.5.5 Enabling the Clock Output on the AT17LV512A/ 010A/020A/002A Configurator

1. Procedure → Select "/M: Enable AT17C512A/010A/020A/002A Internal Clock".
2. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - A2 Bit Level → Select the level that matches the level seen on the A2 pin of the target device.
3. Press "Start Procedure" (1)(2).

### 3.5.6 Disabling the Clock Output on the AT17LV512A/ 010A/020A/002A Configurator

1. Procedure → Select "/M: Disable AT17C512A/010A/020A/002A Internal Clock".
2. Options → Default or previous settings are given. You may need to modify the following:
   - EEPROM Density → Select the device density.
   - A2 Bit Level → Select the level that matches the level seen on the A2 pin of the target device.
3. Press "Start Procedure" (1)(2).

***Notes:*** ***1.*** If CPS is being launched for the first time, the clock calibration dialog will appear. Press "Yes" to proceed and select "High" for accurate calibration.

***2.*** After the internal oscillator (DCLK) of the device is enabled/disabled, a power cycle (reset) of the programming board is required before any other programming procedure takes place.

***Figure 3-2.*** Programming Connections

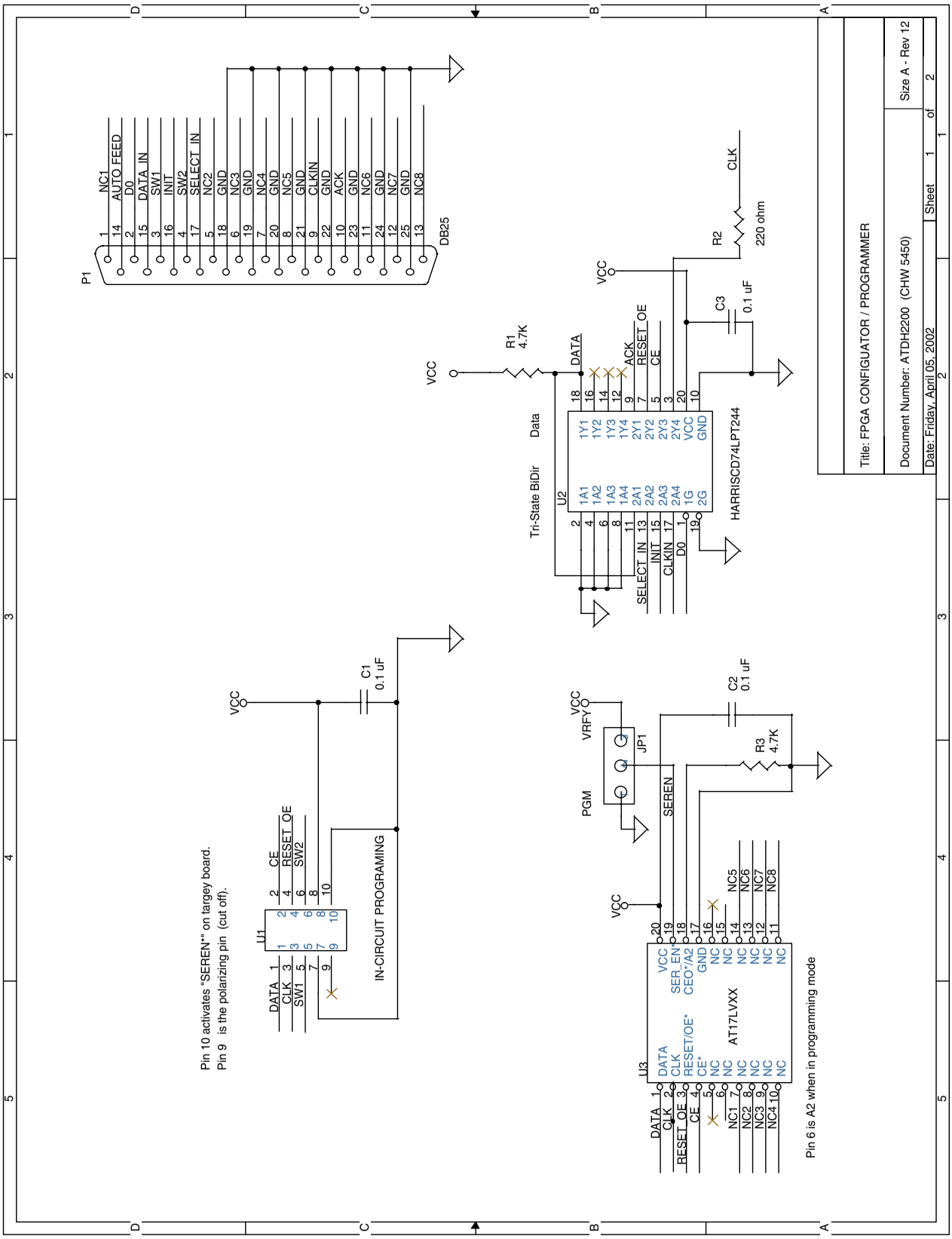
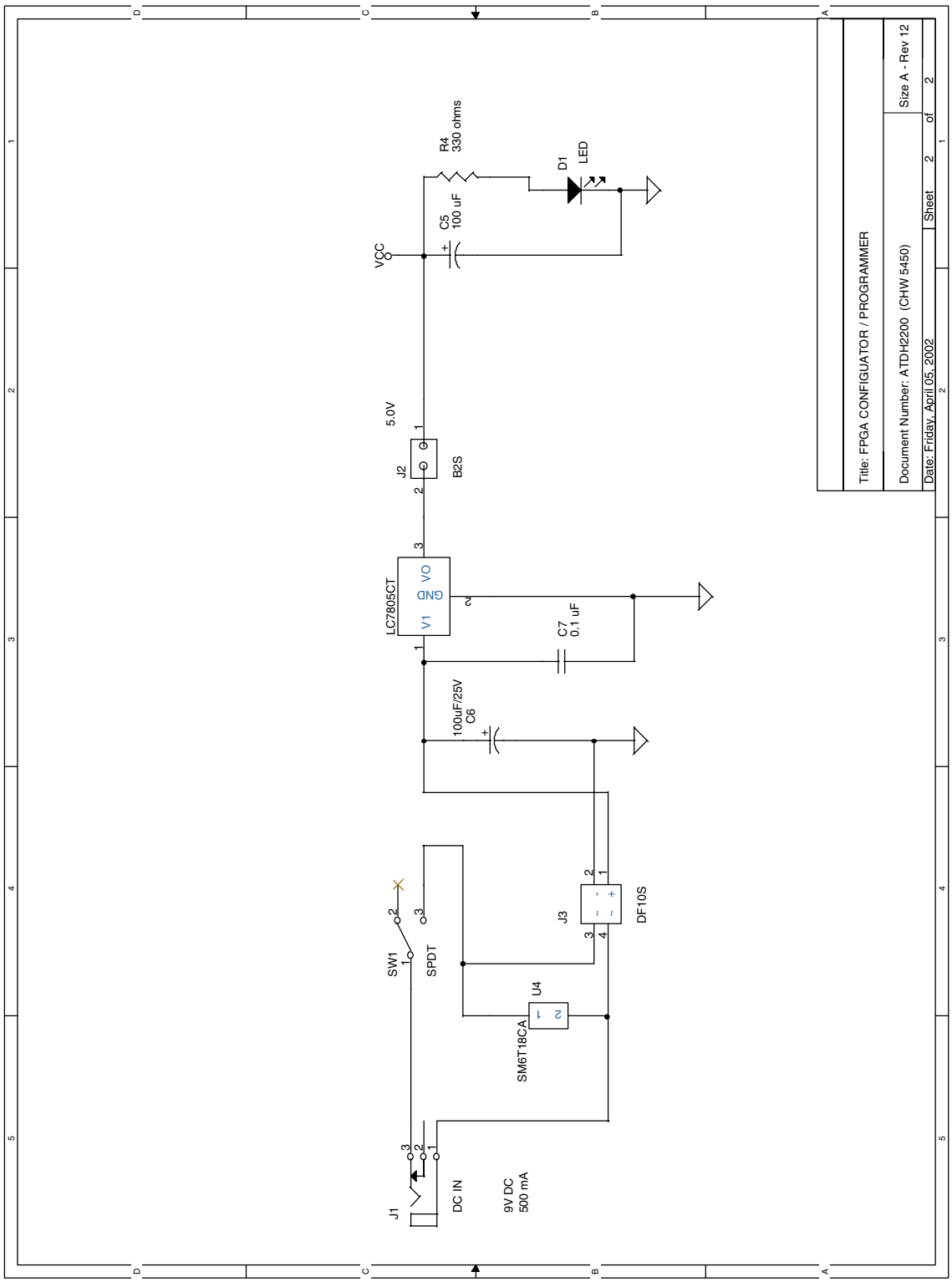


***Figure 3-3.*** Power Supply Generation



## Atmel Headquarters


*Corporate Headquarters*
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

*Europe*
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

*Asia*
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

*Japan*
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581


## Atmel Operations


*Memory*
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

*Microcontrollers*
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

*ASIC/ASSP/Smart Cards*
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

*RF/Automotive*
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

*Biometrics/Imaging/Hi-Rel MPU/*
*High Speed Converters/RF Datacom*
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80


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*Atmel Programmable SLI Hotline*
(408) 436-4119

*Atmel Programmable SLI e-mail*
configurator@atmel.com

*FAQ*
Available on web site

*e-mail*
literature@atmel.com

*Web Site*
http://www.atmel.com


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