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USERS MANUAL

SIA-322 SERIAL INTERFACE ADAPTER

Accessory for the

Audio Precision System One



Audio precision

January, 1994

Version 3.0

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Users Manual
SIA-322 Serial Interface Adapter

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1. The SIA-322 Serial Interface Adapter

The Serial Interface Adapter (SIA) provides a means of interfacing the System One Audio Measurement System to a variety of data acquisition, reconstruction and communication hardware that utilize a serial bus for the exchange of data. The SIA greatly increases System One's flexibility in interfacing to serial systems for a wide range of tests and measurements.

The SIA consists of a parallel-to-serial transmitter and a serial-to-parallel receiver, each completely independent of the other. Since few serial communication standards exist, flexibility and ease of use were of primary concern in the design of the SIA. Some of the primary features provided by the SIA are:

- ❒ Serial word length support of 8 to 32 bits, one or two channels (time multiplexed);
- ❒ System One data word length support of 8 to 24 bits, with optional 0 or 1 padding, LSB or MSB extension;
- ❒ Left- or right-justified data within the serial data frame;
- ❒ Data transmission and reception independently selectable as LSB- or MSB-first;
- ❒ Independently programmable word clock transition timing within the data frame, with bit-wide and word-wide clock widths;
- ❒ Independently programmable bit and word clock sources (internal or external);
- ❒ TTL and CMOS logic level support on all inputs and outputs;
- ❒ Logic polarity control of data, word clocks and bit clocks.

1.1. Connecting the SIA to System One

The SIA exchanges data and derives its power through the System One Dual Domain parallel ports. Two keyed 24-pin ground-plane ribbon cables are provided with the SIA, and should be used for the connection between System One and the SIA. Prior to connecting the SIA to System One, be sure that power to System One is turned off. The connectors are keyed to prevent incorrect installation of the cables. Note the location of the connector keys before attempting to install the cables. Install the two supplied cables between the System One parallel input/output ports and the corresponding ports on the rear panel of the SIA. If after installation the SIA does not appear to be operating, press the SIA reset switch located on the rear panel of the SIA.



2. Serial I/O Primer

2.1. Purpose of this Section

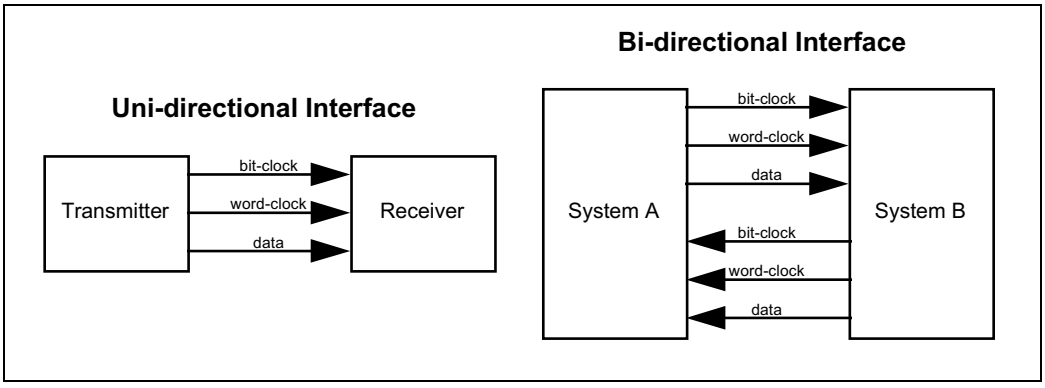
The following section presents a brief overview of serial I/O interfaces and the various parameters that are used, and is intended for those who are unfamiliar with serial communication techniques and their technical issues. In this section, the two principal data communication interfaces used in the digital audio world are identified, and their strengths and weaknesses are compared. An in-depth description of the serial data frame is provided, followed by a discussion of common serial clocking configurations.

2.2. Data Communication Interfaces

It is often desirable to exchange digital information between two or more systems -- for example, between System One and a digital to analog converter (DAC). To facilitate data transfer between systems, an electrical interface is required. There are two principal interfaces used for exchanging data between systems: the *serial* interface and the *parallel* interface.

A serial interface usually has three primary electrical connections between the communicating systems: 1) a bit-clock line, 2) a word-clock (or word-strobe) line, and 3) a data line (see figure 1). A *data word*, or group of bits, is transmitted from a *data source* to a *data sink* in a bit-by-bit sequence (that is, serially) over the three-wire interface. Some communicating systems that require the exchange of data in both directions utilize a serial interface that includes two such sets of electrical connections, one for each direction. Such an interface allows the simultaneous exchange of data in both directions. Yet another bi-directional serial data interface utilizes only one set of electrical connections between two or more systems. Known as I^2S, this interface allows the exchange of data between a number of interconnected systems using a common serial *bus*[1]. Only two systems at a time may communicate on an I^2S serial bus. The SIA-322 supports all of the above serial communication interfaces.

Figure 1. Typical serial interface configuration.



A parallel interface usually has two primary electrical connections between the communicating systems: 1) a word-clock line, and 2) two or more data lines (see figure 2). A data word is transmitted from the source to the destination one word at a time. The SIA-322 does

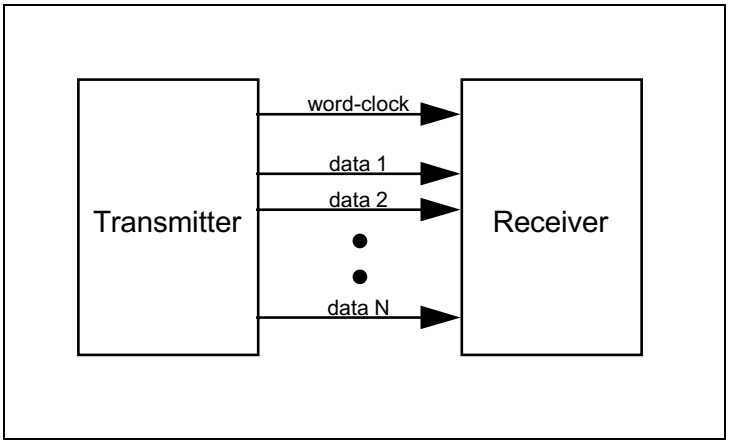
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1 The I^2S, or *Inter-IC Sound*, bus interface was developed by Signetics Company. A full specification for the interface can be found in *Insert Signetics Manual Name Here* (year of publication).

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not support parallel communication interfaces; however, the System One Digital I/O (DIO) option does support parallel communication interfaces with data word widths of up to 24 bits.

Figure 2. Typical parallel interface configuration.



2.2.1. Serial and Parallel I/O Compared

Serial and parallel interfaces each have unique advantages and disadvantages (see Table 1). The most obvious advantage of serial I/O over parallel I/O is the number of electrical connections that are required to facilitate communication between two systems. Data communication over a serial interface can be accomplished with as few as three connections -- regardless of data word size. A parallel interface requires at least N + 1 connections (where N is the word size in bits). Because of this, the cost of interconnect hardware is generally lower for serial I/O than for parallel I/O. Serial interfaces also tend to be more flexible than parallel interfaces because the data word size for a serial interface is user definable, while the data word size for a parallel interface is dictated by the number of interconnects between the communicating systems.

Table 1. Comparison of serial and parallel interfaces

Evaluation Criteria	Serial	Parallel
Reduced interconnect hardware and cost	✓	
Maximum flexibility of data word size	✓	
Highest data throughput		✓
Simplicity of interface logic		✓

Parallel interfaces have two significant advantages of their own. Since a serial interface must transmit one bit of data per bit-clock time, it takes N bit-clock periods to transmit a data word of size N bits (that is, there are N bit-clock periods per word-clock period). A parallel interface can transmit N bits in a single word-clock period -- therefore, a parallel interface can transmit N times more data than a serial interface in one clock period (it is assumed that the parallel word-clock period is equal to the serial bit-clock period). For example, if a 16-bit parallel interface has a word-clock period of 48 kHz, it can transfer 768 thousand bits of data per second (768 kbps). A comparable serial interface with a 48 kHz bit-clock can transfer only 48 thousand bits of data per second. To achieve the 768 kbps transfer rate, the serial interface would have to use a bit-clock period of 768 kHz. The lower clock rate for a given data throughput is a major advantage of

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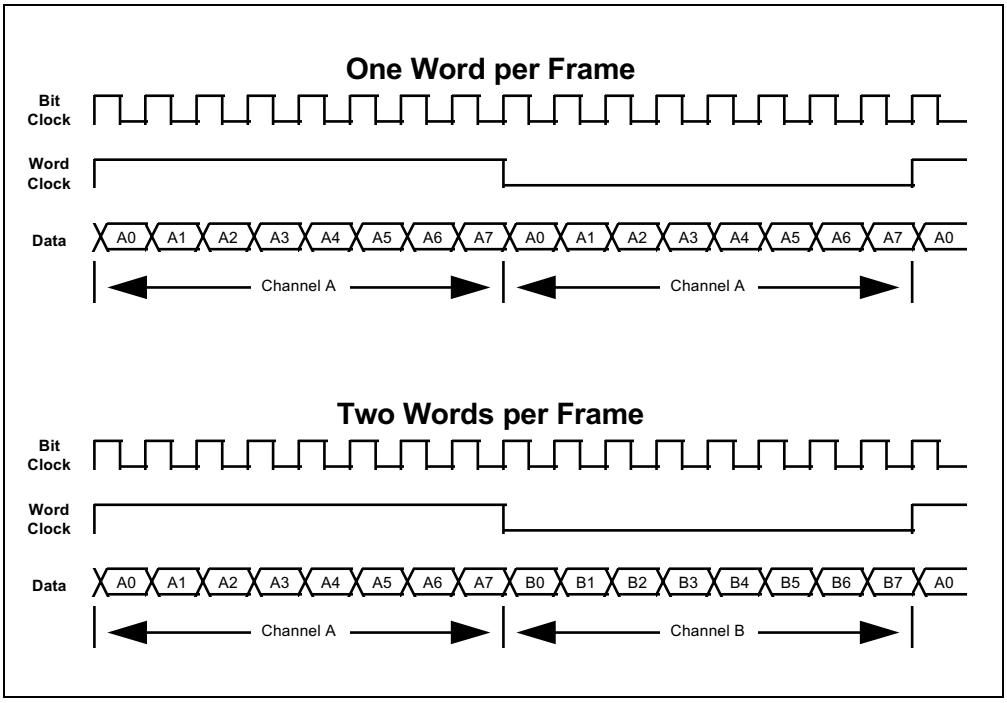
parallel interfaces over serial interfaces. Additionally, the design circuitry necessary to implement a parallel interface tends to be simpler than that required to implement a serial interface.

Traditionally, parallel interfaces were the preferred digital interface between communicating systems. Serial I/O, however, has rapidly grown to become the dominant interface for the exchange of information between two audio systems. This has been fueled by advances in semiconductor speed and cost reduction, and by the desire to minimize interconnect hardware between communicating systems.

2.3. The Serial Data Frame

Data that is transmitted over a serial interface is usually grouped in *frames*. A serial data frame is a grouping of one or more consecutive data words. The most common frame sizes are one (single channel or mono) and two (dual channel or stereo) data words per frame (see figure 3). There are four principal parameters that affect how data is transmitted within a data frame: the word-clock pulse width, the position of word-clock logic transitions relative to the data, data framing control, and word- and bit-clock polarity.

Figure 3. One- and two-channel serial data frame formats.

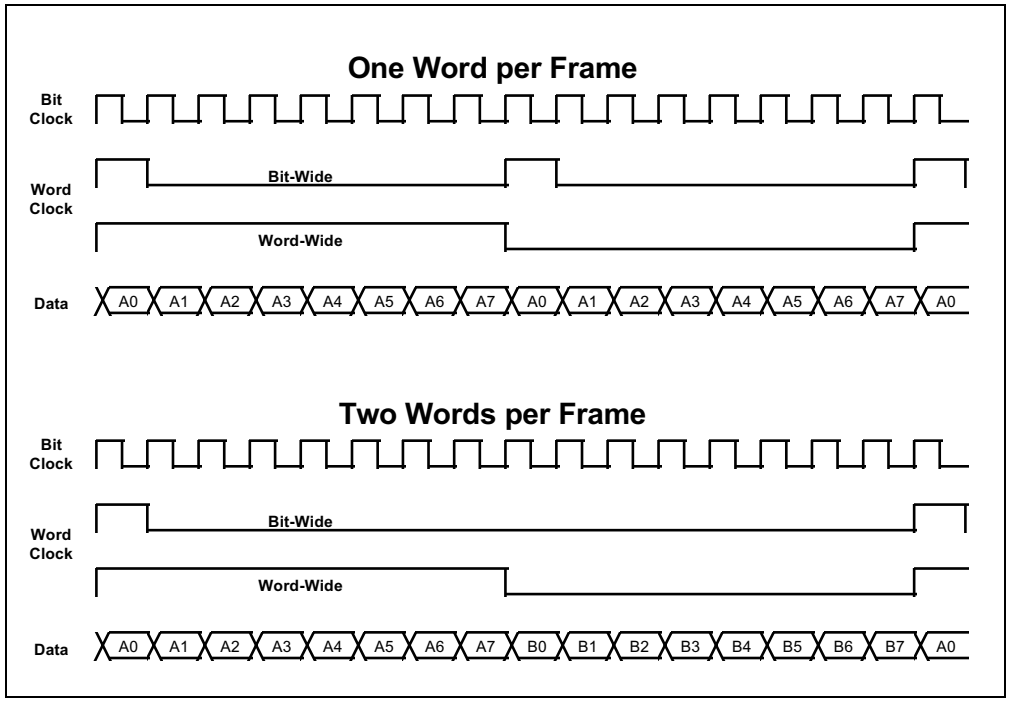


2.3.1. Word-Clock Pulse Width

The pulse width of the word-clock signal is usually either one bit-clock in duration (that is, the word-clock is *bit-wide*), or N bit-clocks in duration (the word-clock is *word-wide*), where N is the number of bits per word. As shown in figure **Error! Bookmark not defined.**, the *leading edge* of a bit-wide word-clock pulse usually delineates the start of the data frame. With a word-wide word-clock, the relevant edge depends upon the number of words per frame: with one word per frame, *either edge* delineates the start of the frame; with two words per frame, the *leading edge* delineates the start of the frame.

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Figure 4. Bit-wide and word-wide word-clocks.



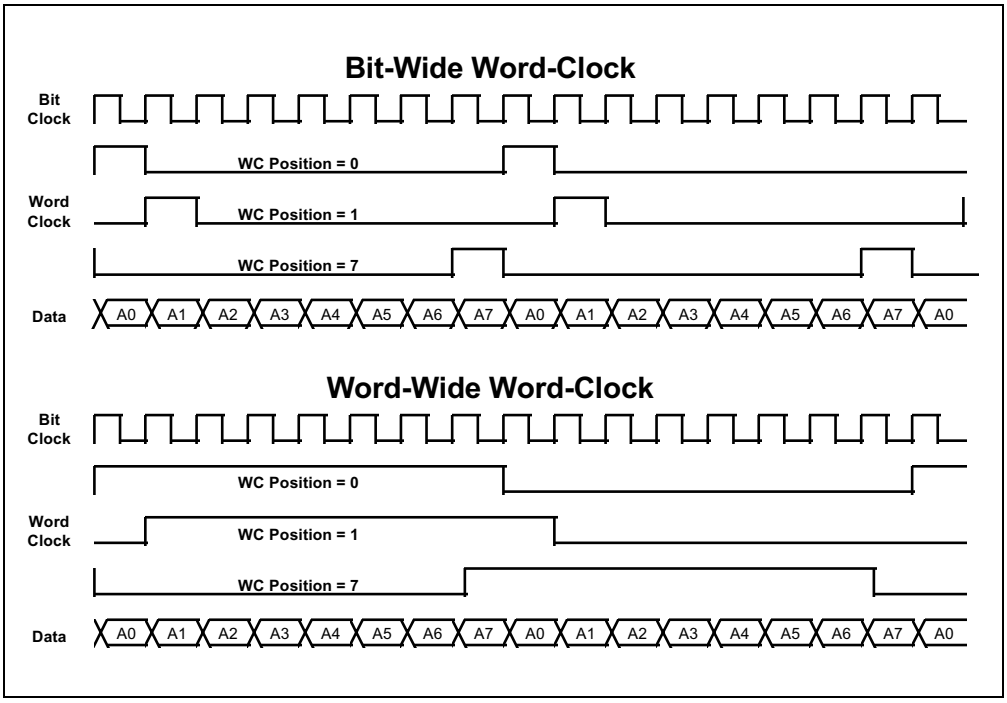
2.3.2. Word-Clock Position

While the edge of the word-clock pulse is used to delineate the start of the data frame, the location of the first data bit within the frame can vary (see figure **Error! Bookmark not defined.**). The location of the data relative to the start of the data frame is termed the *word-clock position*[2]. The word-clock position within a data frame can vary from zero to N-1, where position zero corresponds to the *first* bit position of the first word, and position N-1 corresponds to the *last* bit position of the first word in the frame. The word-clock position for a given interface depends upon the requirements of the communicating systems. For example, the I^2S bus standard dictates that the word-clock position be N-1. Most communicating systems utilize a word-clock position of zero or one.

2 Perhaps more appropriately, the word-clock position can be thought of as the location of word-clock relative to the start of the data frame. Either interpretation yields the same result -- the first data bit and the word-clock pulse can differ in position.

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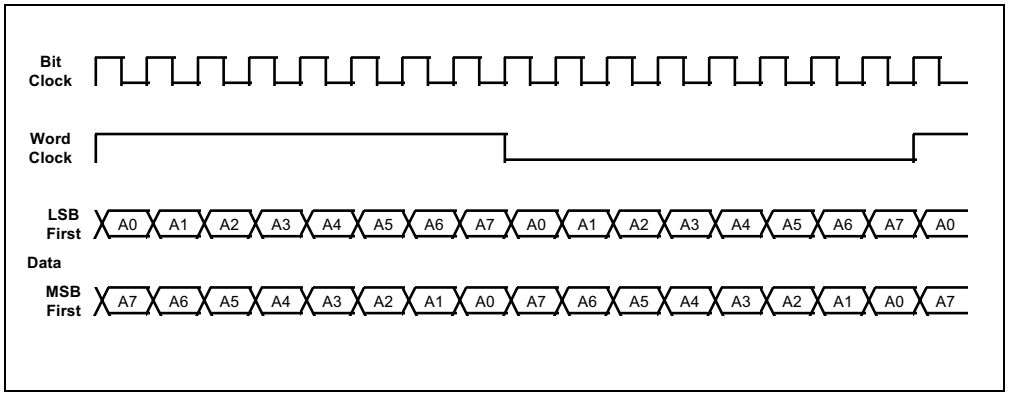
Figure 5. Word-clock positioning within the data frame.



2.3.3. Data Framing Control

In a serial I/O interface, data is transmitted one bit at a time. However, data can be transmitted either *least-significant bit first* (LSB first), or *most-significant bit first* (MSB first), as shown in figure 6. The bit ordering used is dependent upon the requirements of the communicating systems.

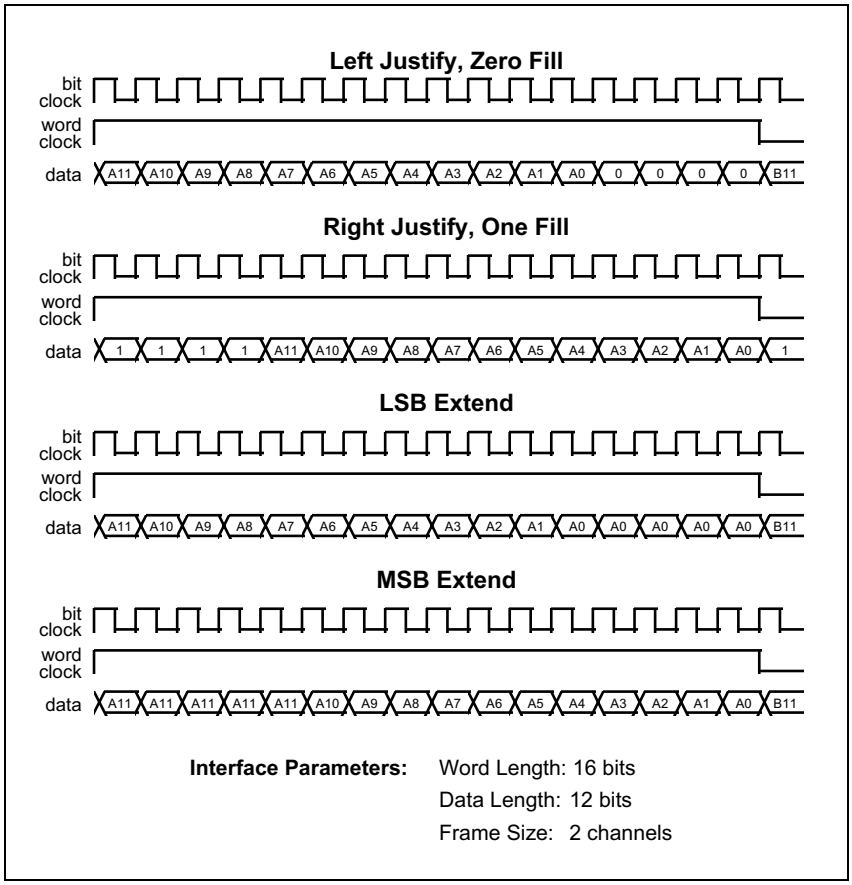
Figure 6. Bit ordering within the data frame.



Serial interfaces may also use a *transmission word length* that is longer than the data word length (see figure 7). This is usually the case when the length of the data word being transmitted is not a multiple of eight. For example, 12-bit data may be transmitted over a serial interface that utilizes a 16-bit word length. The word length is *always* greater than or equal to the data length.

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Figure 7. Data Framing Options.



When the word length differs from the data length, two issues arise: 1) how should the data be aligned in the word, and 2) what value should the unused bits take on? Serial interfaces always justify the data along the left or right side of the word. Unused bits within the frame can be filled with logic-zero or logic-one values, or they can be filled with the value of the nearest data bit (also known as *bit-extending*). Several examples are shown in figure 7. For a given interface, the data justification mode and unused bit values used depend upon the requirements of the communicating systems. The unused bits within a data frame are usually ignored by the communicating systems.

2.3.4. Data, Word-Clock, and Bit-Clock Polarity

The polarity of serial interface signals can vary, depending upon the needs of the communicating systems. The polarity of the serial data and word-clock signals is usually positive[3]. For a two-channel, word-wide word-clock signal, the positive pulse is usually associated with the first data word in the frame (that is, channel A), while the negative pulse is associated with the second word (channel B). Unlike the word-clock signal, the polarity of the bit-

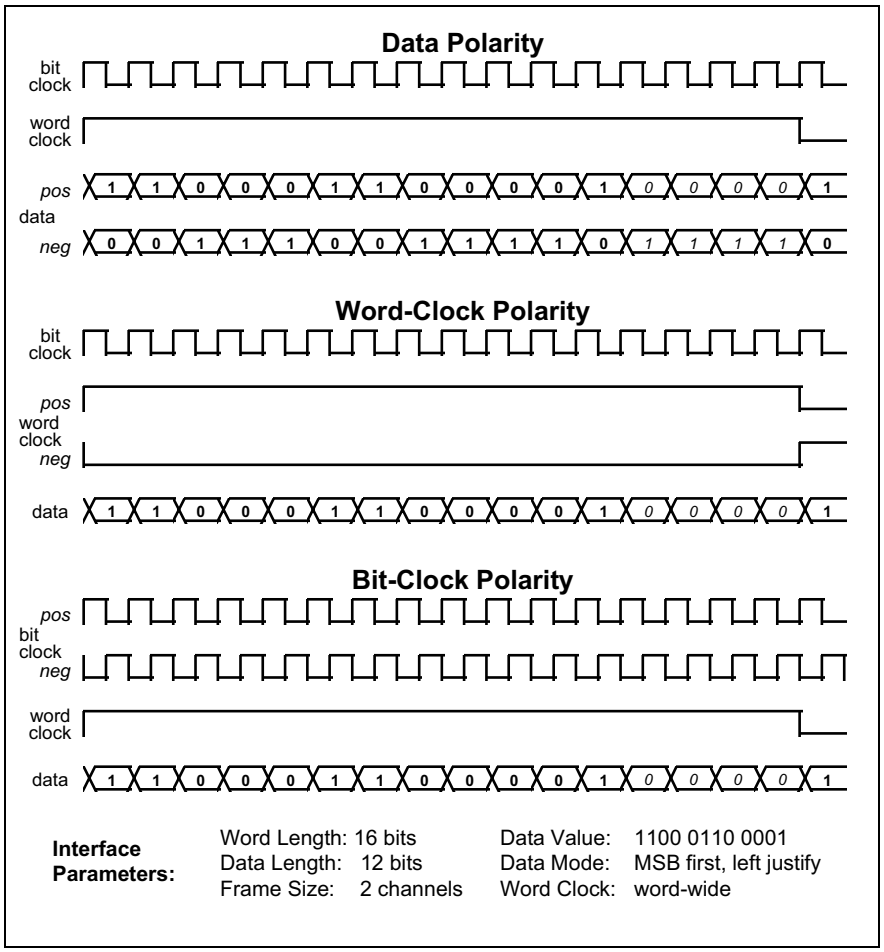
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3 A *positive* polarity signal is one that represents logic-one bit values with a 'high' level, and logic-zero bit values with a 'low' level. A *negative* polarity signal is one that represents logic-one bit values with a 'low' level, and logic-zero bit values with a 'high' level.

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clock signal often differs for the transmitter and the receiver (see figure 8). In order to meet stringent data timing requirements at the receiver, the transmitter typically uses positive bit-clock polarity while the receiver uses negative bit-clock polarity.

Figure 8. Data, word-clock and bit-clock polarity examples.



2.4. Serial Clocking Methods

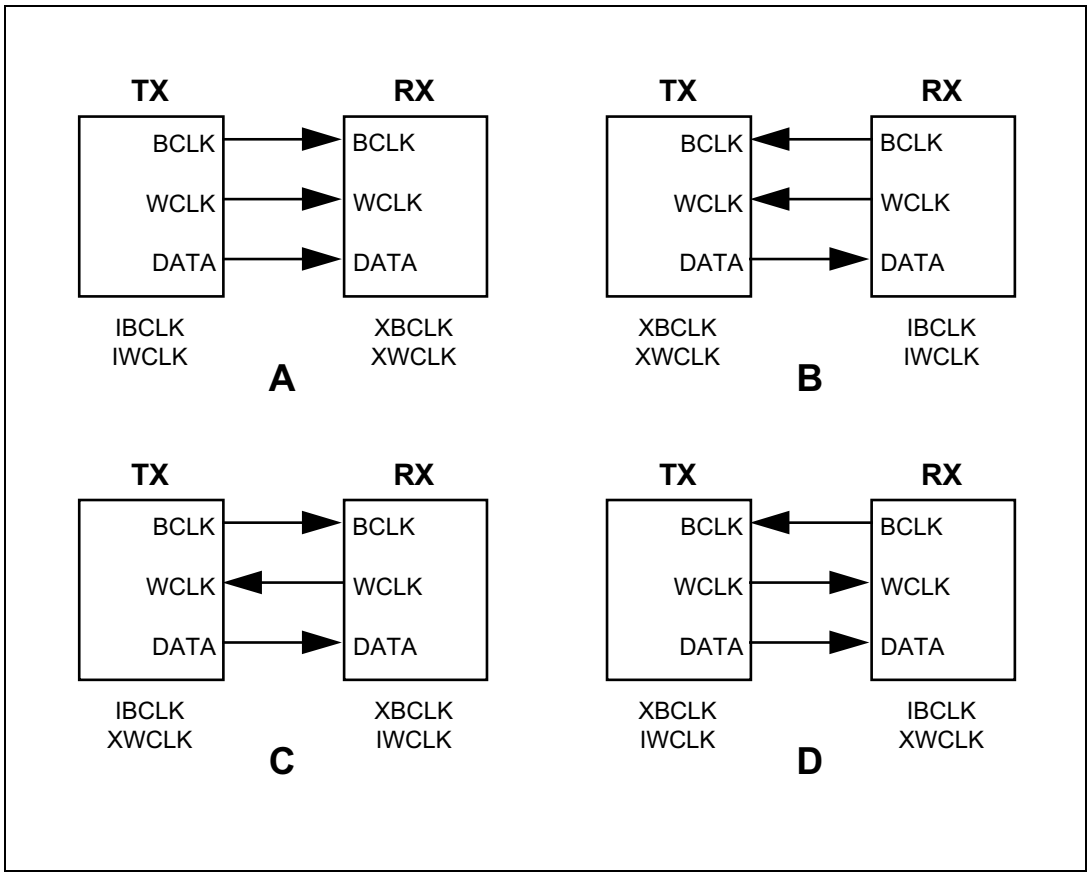
The four principal methods for interconnecting a transmitter and receiver in a communication system are shown in figures 9[A-D]. The most commonly used methods are shown in figures 9A and 9B. In 9A, the transmitter is the source of the bit-clock and word-clock signals. In this configuration, the transmitter acts as the bus *master* while the receiver acts as the bus *slave*[4]. In 9B, the receiver is the source of the bit-clock and word-clock signals -- here the receiver acts as the master while the transmitter acts as the slave. Figures 9C and 9D show two hybrid interconnect methods that are less commonly used. In 9C, the transmitter generates the bit-clock signal while the receiver generates the word-clock signal, and vice versa in figure 9D. Figure 9 also shows the origin of the transmitter and receiver clock sources for each of the four

4 A bus *master* is generally the device that generates the clocking signals. Non-master devices are termed *slaves* because they must synchronize their internal operation to the clock signals generated by the master.

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configurations; for example, in 9A the transmitter uses *internally* generated bit-clock (IBCLK) and word-clock (IWCLK) signals, while the receiver uses *externally* generated bit-clock (XBCLK) and word-clock (XWCLK) signals.

Figure 9. The four principal serial clocking methods.



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3. Interfacing the SIA-322 to the Target System

The SIA communicates with external serial devices (target systems or DUTs) through two 15-pin D-subminiature connectors located on the SIA front panel. The SIA user provides an interface cable with a DB-15 connector on one end, and the appropriate connections to the target system on the other end. Optionally, the user may use the SIA-DUT Interface Board that is supplied with the SIA to simplify the interfacing task (see section 5.).

3.1. Transmitter Interfacing to the Target System

The SIA transmitter interfaces to the target system through a 15-pin male D-subminiature connector. Five primary signals are available on the I/O port: serial data output, word (channel) clock I/O, bit clock I/O, N x FS clock output and reference clock input. Additionally, three tri-state control pins are provided, allowing the user to individually control the serial output, word and bit clock signals in shared-bus configurations. The pin-out for the transmitter DB-15 connector is shown in table 2 below. Note that a ground pin is associated with each primary signal. The ground pin should be used as the current return path for its corresponding signal. The use of shielded cable is recommended for all signals.

Table 2. SIA transmitter serial connector pin assignment.

Signal Pin	Ground Pin	Signal Name	Signal Description
1	2	SOD	Serial Output Data
3	4	SOWCLK	Word Clock I/O
5	6	SOBCLK	Bit Clock I/O
7	8, 10	SODE	SOD Enable (H)
9	8, 10	SOWCLKE	SOWCLK Enable (H)
11	8, 10	SOBCLKE	SOBCLK Enable (H)
13	12	TREFCLK	Master Reference Clock Input
15	14	TNFSCLK	N x FS Clock Output

Serial data is transmitted on the SOD pin. The serial output word clock (SOWCLK) and bit clock (SOBCLK) signals are bi-directional; The SIA transmitter can provide the word and bit clocks necessary for data transmission (as a clock master), or it can slave to an externally-generated word or bit clock. All output drivers are capable of driving TTL or CMOS loads. When configured for slave operation, the SOWCLK and SOBCLK signals can be driven by either TTL or CMOS logic. The logic family is user-selectable. Additionally, all I/O buffers are internally mounted in sockets for easy replacement.

The SIA transmitter can be used in a shared-bus configuration where the target system consists of more than one serial device. The SOD, SOWCLK and SOBCLK signals can be individually tri-stated by pulling their corresponding enable pins, SODE, SOWCLKE and SOBCLKE, low (logic zero, or ground). The SODE, SOWCLKE and SOBCLKE inputs are internally tied to +5V through 100 K-ohm resistors; these pins may be left unconnected if output tri-stating is not required. These inputs expect TTL logic levels for proper operation, however the logic loading is comparable to that of CMOS (the inputs are buffered using HCT logic family parts).

When the SIA is operated in master mode, the transmitter requires an external clock signal (applied to the TREFCLK input) which is used as the transmitter master reference clock. A

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separate clock related to SOBCLK is provided on the TNFSCLK pin. This symmetric signal is derived directly from the reference clock. The frequency of this clock is determined by the setting of the DIV1 configuration switch (see below). This signal is not tri-stateable.

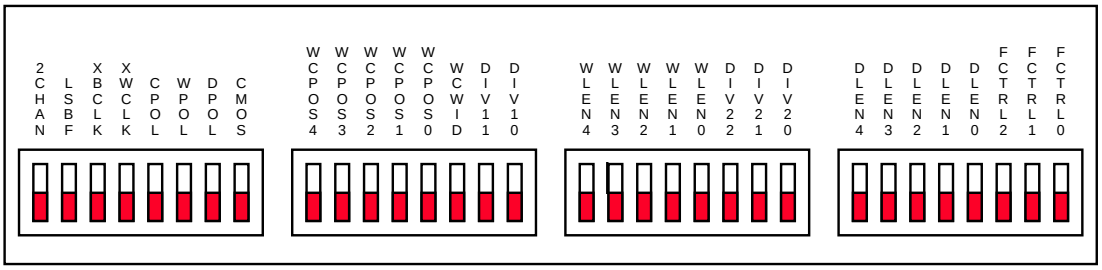
When interfacing the target system to the SIA, care must be taken in the selection of interface cabling if proper operation of the SIA and the target system is to be expected. Each of the primary signals has an associated ground pin (see table 2) which should be used as the logic reference for its corresponding signal. It is recommended that shielded cable be used for interfacing to the SIA, particularly on the SOD, SOWCLK, SOBCLK, TNFSCLK and TREFCLK lines.

All SIA inputs are internally buffered with CMOS family parts. CMOS inputs have a very high input impedance. If the interface cables are relatively long, it is recommended that all input signals be terminated at the DB-15 connector to minimize reflections and ringing. A passive termination (e.g. a 75 ohm resistor connected between the input pin and its corresponding ground pin) may be used as long as the signal source is capable of providing the necessary drive current while maintaining proper logic levels. Each SIA output is capable of driving a 50 ohm transmission line, and is able to continuously source or sink at least 24 mA of current.

3.2. Transmitter Configuration Switches

A set of DIP switches is used to configure the SIA transmitter for the various modes of operation. The switch settings for the transmitter are illustrated in figure 10 and described in table 3 below. The configuration switches can be logically grouped into four distinct groups: the serial word length select, data length select, word clock position and framing control.

Figure 10. Transmitter configuration switch locations.



3.2.1. Serial Word Length Selection

The serial word length is the number of actual bits transmitted in each serial word. The SIA is capable of transmitting a serial word of between 8 and 32 bits in length. The word length is specified by setting the WLEN DIP switch field to the desired word length minus 1. For example, for a serial word length of 18 bits, WLEN would be set to 17, or 10001 binary.

3.2.2. Serial Data Length Selection

The serial data length is the number of significant data bits to be transmitted in the serial word. System One is capable of transmitting up to 24 bits of data per sample; However, not all target devices require a full 24 bits of data. The SIA can be programmed to truncate each sample to any number of bits from 8 to 24 (where 24 is equivalent to no truncation). The serial data length is specified by setting the DLEN DIP switch field to the desired data length minus 1. For proper SIA operation, the data length must not exceed the word length.

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3.2.3. Serial Word Clock Position Selection

Since the SIA transmits serial data in a synchronous manner, the word clock signal (SOWCLK) is used to delineate the start of a new serial frame. In single channel applications, "frame" is synonymous with "word." In two channel applications, a frame is composed of two words, first channel A, then channel B. The timing of SOWCLK relative to the first bit of the serial frame is set by the word clock position (WCPOS) DIP switch field. The word clock signal transitions synchronously with the transmitted data (SOD), and may be configured to transition from zero to WLEN-1 bit clock times after the start of the word. For example, if the SIA transmitter is configured for a word length of 16 bits (i.e. WLEN=01111), and the transition of SOWCLK is to occur during the last bit time of the serial frame, WCPOS would be set to 15, or 01111 binary. For proper SIA operation, the word clock position must be less than the word length.

3.2.4. Serial Framing and Clocking Control

The SIA is capable of transmitting and receiving the word clock signal as either a bit-width or word-width signal, and is set by the WCWID configuration switch. If WCWID is OFF, SOWCLK will consist of a single pulse one bit-time in duration (i.e. one bit wide), transitioning at the appropriate bit time within the serial frame as defined by the setting of WCPOS. If WCWID is ON, SOWCLK will change state on each word boundary, yielding a square wave with a period equal to the serial frame time. The bit-width and word-width word clock are useful for both single- and dual-channel (time multiplexed) operation. See the section on T2CHAN below for more information.

When the data and word lengths are not the same, some control over the data within the serial word is necessary. The FCTRL0, FCTRL1 and FCTRL2 configuration switches are used to set the data-justification and sign-extension or padding of data within the word. FCTRL0 specifies whether the data within the serial word is left- or right-justified, with FCTRL0=OFF resulting in right-justified data. FCTRL1 specifies whether the data to be transmitted is sign-extended, zero padded or one padded to fit within the serial word, with FCTRL1=OFF resulting in zero or one padding. FCTRL2 specifies the bit pad value when FCTRL1=OFF; FCTRL2=OFF results in zero padding and FCTRL2=ON results in one padding.

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Table 3. Transmitter configuration switch description.

Switch Name	Description
2CHAN	**Transmitter Channel Select**. OFF = single channel operation, ON = two channel operation.
LSBF	**Transmitter First-Bit Select**. Selects LSB or MSB as first valid bit within the serial frame. OFF = MSB first, ON = LSB first.
XBCLK	**Transmitter Bit Clock Source Select.** Selects source of bit clock. OFF = internally generated bit clock, ON = external bit clock.
XWCLK	**Transmitter Word Clock Source Select.** Selects source of word clock. OFF = internally generated word clock, ON = external word clock.
CPOL	**Transmitter Bit Clock Polarity Select.** OFF = bit clock is asserted high, ON = bit clock is inverted (asserted low).
WPOL	**Transmitter Word Clock Polarity Select.** OFF = word clock is asserted high, ON = word clock is inverted (asserted low).
DPOL	**Transmitter Data Polarity Select.** OFF = transmitted serial data is asserted high, ON = serial data is inverted (asserted low).
CMOS	**Transmitter CMOS Input Select.** OFF = all inputs configured for TTL logic levels, ON = all inputs configured for CMOS.
WCPOS(4:0)	**Transmitter Word Clock Position**. Physical position of word clock transition within the serial word. Can be set from 0 to 31.
WCWID	**Transmitter Word Clock Width**. Width of transmitter word clock pulse. OFF = bit-wide clock pulse, ON = word wide (symmetric) clock.
DIV1(1:0)	**Transmitter N x FS Clock Control**. Sets TNFSCLK frequency by selecting master reference clock divide ratio (see section 3.2.4.).
WLEN(4:0)	**Transmitter Word Length**. Length of transmitted serial word, minus 1. Can be set from 7 to 31, corresponding to word lengths of 8 to 32 bits.
DIV2(2:0)	**Transmitter Bit Clock Frequency Control**. Sets bit clock frequency to 1/(DIV2+1) times TNFSCLK frequency (see section 3.2.4.).
DLEN(4:0)	**Transmitter Data Length**. Number of significant bits of System One data word to be transmitted, minus 1. Can be set from 7 to 23, corresponding to data lengths of 8 to 24 bits.
FCTRL0	**Transmitter Framing Control 0**. OFF = right-justified data within the serial frame, ON = left-justified.
FCTRL1	**Transmitter Framing Control 1**. OFF = zero/one pad out-of-bounds data, ON = sign extend out-of-bounds data.
FCTRL2	**Transmitter Framing Control 2**. If FCTRL1 = OFF, sets pad value for out-of-bounds data. OFF = zero, ON = one.

The SIA is capable of transmitting a single channel of data from System One, or two channels of data in a time-multiplexed fashion. The mode of operation is set by the 2CHAN configuration switch. When 2CHAN=OFF, a single channel of data from System One (the B channel) is transmitted. When 2CHAN=ON, two channels of data are transmitted (channels A and B). In two-channel mode with WCWID=ON (word-width word clock), the direction of

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transition of SOWCLK determines which channel is being transmitted at any given time. When WPOL=OFF (see below), a low-to-high transition within the data frame implies that channel A is being transmitted. In a similar manner, a high-to-low transition implies that channel B is being transmitted. In two-channel mode with WCWID=OFF (bit-width word clock) and WPOL=OFF, a low-to-high transition of SOWCLK signals the start of a new serial frame, with channel A transmitted first, followed by channel B.

The data sample may be transmitted either most significant bit (MSB) first, or least significant bit (LSB) first. The order is controlled by the LSBF configuration switch. When LSBF=OFF, the data is transmitted MSB first. When LSBF=ON, the data is transmitted LSB first.

The SIA transmitter is capable of generating a bit clock and word clock derived directly from the master reference clock (TREFCLK) input. Optionally, one or both of these clocks can be generated by the target system and supplied to the SIA , which will subsequently behave in a slave-transmitter fashion. The source of the word clock is defined by the state of the XWCLK configuration switch. If XWCLK=OFF, the transmitter will drive SOWCLK with a locally generated word clock. If XWCLK=ON, the transmitter will slave to the word clock signal received on SOWCLK from the target system. In a similar manner, if XBCLK=OFF the transmitter will drive SOBCLK with a locally generated bit clock. If XBCLK=ON, the transmitter will slave to the bit clock received on SOBCLK from the target system. The four possible operating modes are shown in table 4 below. Note that clocks supplied by the target system must be appropriate for a given transmitter configuration (i.e. the number of bit clocks per word clock interval must match the setting of WLEN, etc.).

Table 4. Transmitter clock source selection.

XBCLK	XWCLK	Transmitter Clock Source
OFF	OFF	Bit clock and word clock derived directly from master reference clock (TREFCLK).
OFF	ON	Not useful.
ON	OFF	Bit clock from target system used to generate word clock (TREFCLK generates TNFSCLK only).
ON	ON	Bit clock and word clock derived directly from target system (TREFCLK generates TNFSCLK only).

The polarity of the transmitted data, word and bit clocks are controlled by the DPOL, WPOL and CPOL configuration switches. When DPOL=OFF, serial data is transmitted using positive logic levels. When DPOL=ON, the transmitted data is inverted.

The WPOL configuration switch allows the user to change the logic sense of SOWCLK when WCWID=OFF (i.e. word clock is bit-wide), and to change the channel sense when WCWID=ON. As described above, when WPOL=OFF and WCWID=ON, a low-to-high transition within the data frame implies that channel A is being transmitted. In a similar manner, a high-to-low transition implies that channel B is being transmitted. When WPOL=ON, the channel sense is reversed.

CPOL is used to define which edge of SOBCLK the serial data (SOD) and serial output word (SOWCLK) transition on. When CPOL=OFF, both SOD and SOWCLK transition on the rising edge of SOBCLK. When CPOL=ON, both SOD and SOWCLK transition on the falling edge of

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SOBCLK. When SOWCLK is configured as an input, CPOL defines which edge of SOBCLK samples SOWCLK. With CPOL=OFF, SOWCLK is sampled on the rising edge. With CPOL=ON, SOWCLK is sampled on the falling edge.

When configured as inputs, SOBCLK and SOWCLK can be configured to accept TTL or CMOS logic levels. The logic family is selected by the CMOS configuration switch. When CMOS=OFF, both inputs expect TTL logic levels. When CMOS=ON, both inputs expect CMOS logic levels. In either configuration, input loading is very low (inputs are buffered using HC/HCT logic family parts).

The DIV1 configuration switch field is used to select the frequency of the N x FS clock (TNFSCLK) signal. The TNFSCLK signal is generated by a power-of-two divider driven by the master reference clock (TREFCLK). DIV1 selects one of four possible division ratios: 1, 2, 4, or 8. The power-of-two divider may optionally be configured to divide by 4, 8, 16, or 32; this mode is described in section 3.6. below. The DIV1 switch is typically used in conjunction with the DIV2 switch to generate a clock that is a multiple of the system sample rate.

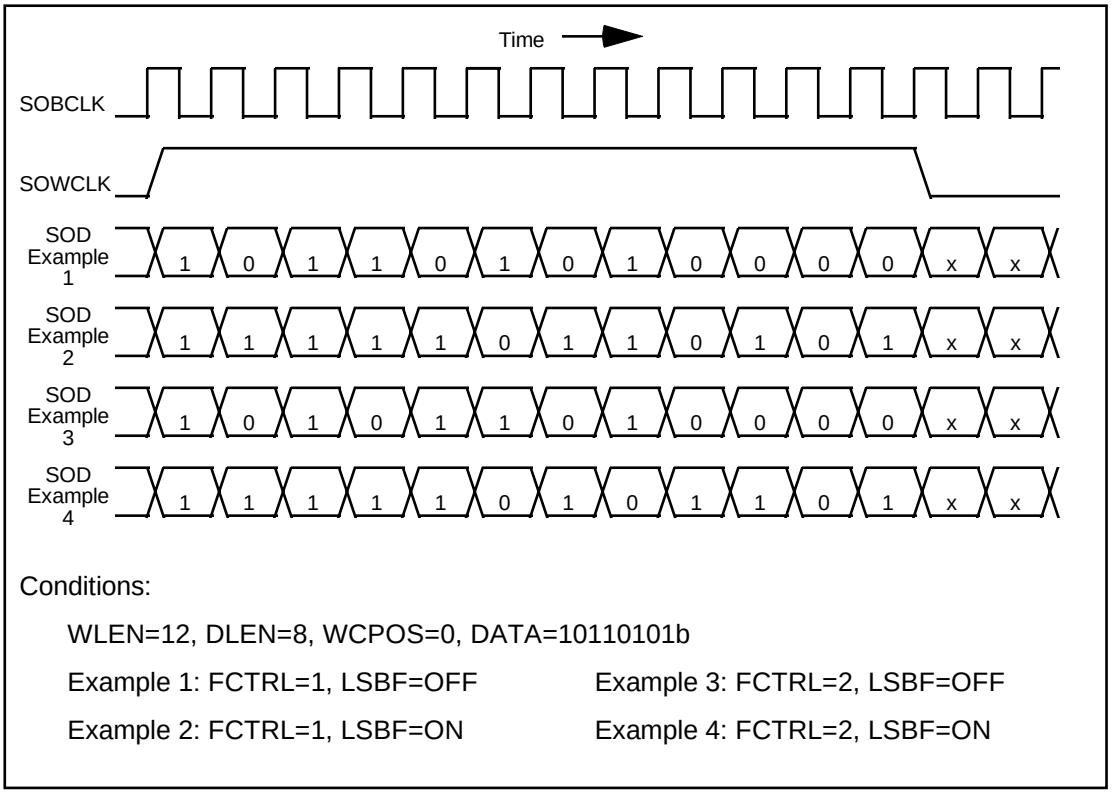
The DIV2 configuration switch field is used to set the bit clock (SOBCLK) frequency, and is derived from the N x FS clock signal. The transmitter bit clock is generated by a divider driven by TNFSCLK, where DIV2 is used to select the divide ratio. DIV2 selects one of eight possible division ratios: 1, 2, 3, 4, 5, 6, 7, or 8. DIV2 is typically used in conjunction with the DIV1 switch. For example, if TREFCLK is driven by a 12.288 MHz clock and the system is configured for two channels of 32-bit words at a sample rate of 48 kHz, the N x FS clock and bit clocks may be configured as follows: for a 256 x FS clock on TNFSCLK, DIV1 would be set to divide-by-one (DIV1 = 00 binary) and DIV2 would be set to divide-by-four (DIV2 = 011 binary); for a 128 x FS clock, DIV1 would be set to divide-by-two (DIV1 = 01 binary) and DIV2 would be set to divide-by-two (DIV2 = 001 binary). Note that in each of the above examples, the bit clock frequency remains constant (3.072 MHz) since the product of DIV1 and DIV2 is constant. Other N x FS clocks can be generated by the appropriate choice of reference clock frequency and DIV1 and DIV2 settings.

3.2.5. Serial Framing Examples

Figure 11 below shows some examples of serial data framing from four different transmitter configurations. The figure, illustrates four typical serial waveforms generated by the SIA on the SOD pin. All four configurations assume that WLEN=12, DLEN=8, WCPOS=0, and the data being transmitted is 10110101 binary. In examples 1 and 2, LSBF=OFF yields a waveform where the MSB is transmitted first. In examples 3 and 4, LSBF=ON yields a waveform where the LSB is transmitted first. In examples 1 and 3, the data in the frame is left-justified and zero-padded, while in examples 2 and 4, the data is right-justified and bit-extended (MSB-extended in example 2, LSB-extended in example 4).

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Figure 11. Serial output framing examples.



3.3. Receiver Interfacing to the Target System

The SIA receiver interfaces to the target system through a 15-pin female D-subminiature connector. Five primary signals are available on the I/O port: serial data input, word (channel) clock I/O, bit clock I/O, N x FS clock output and master reference clock input. Additionally, two tri-state control pins are provided, allowing the user to individually control the serial word and bit clock signals in shared-bus configurations. The pin-out for the receiver DB-15 connector is shown in table 5 below. Note that a ground pin is associated with each primary signal. The ground pin should be used as the current return path for its corresponding signal. The use of shielded cable is recommended for all signals.

Serial data is received on the SID pin. The serial input word clock (SIWCLK) and bit clock (SIBCLK) signals are bi-directional; The SIA receiver can provide the word and bit clocks necessary for data transmission when a master reference clock is supplied, or it can slave to an externally-generated word or bit clock. All output drivers are capable of driving TTL or CMOS loads. When configured for slave operation, the SIWCLK and SBCLK signals can be driven by either TTL or CMOS logic. The logic family is user-selectable. Additionally, all I/O buffers are internally mounted in sockets for easy replacement.

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Table 5. SIA receiver serial connector pin assignment.

Signal Pin	Ground Pin	Signal Name	Signal Description
1	2	SID	Serial Input Data
3	4	SIWCLK	Word Clock I/O
5	6	SIBCLK	Bit Clock I/O
7			No Connection
9	8, 10	SIWCLKE	SIWCLK Enable (H)
11	8, 10	SIBCLKE	SIBCLK Enable (H)
13	12	RREFCLK	Master Reference Clock Input
15	14	RNFSCLK	N x FS Clock Output

The SIA receiver can be used in a shared-bus configuration where the target system consists of more than one serial device. The SIWCLK and SIBCLK signals can be individually tri-stated by pulling their corresponding enable pins, SIWCLKE and SIBCLKE, low (logic zero, or ground). The SIWCLKE and SBCLKE inputs are internally tied to +5V through 100 K-ohm resistors; these pins may be left unconnected if output tri-stating is not required. These inputs expect TTL logic levels for proper operation, however the logic loading is comparable to that of CMOS (the inputs are buffered using HCT logic family parts).

When the SIA is used in master mode, the receiver requires an external clock (applied to the RREFCLK input) which is used as the receiver master reference clock. A separate clock related to SIBCLK is provided on the RNFSCLK pin. This symmetric signal is derived directly from the reference clock. The frequency of this clock is determined by the setting of the DIV1 configuration switch (see below). This signal is not tri-stateable.

When interfacing the target system to the SIA, care must be taken in the selection of interface cabling if proper operation of the SIA and the target system is to be expected. Each of the primary signals has an associated ground pin (see table 5) which should be used as the logic reference for its corresponding signal. It is recommended that shielded cable be used for interfacing to the SIA, particularly on the SID, SIWCLK, SIBCLK, RNFSCLK and RREFCLK lines.

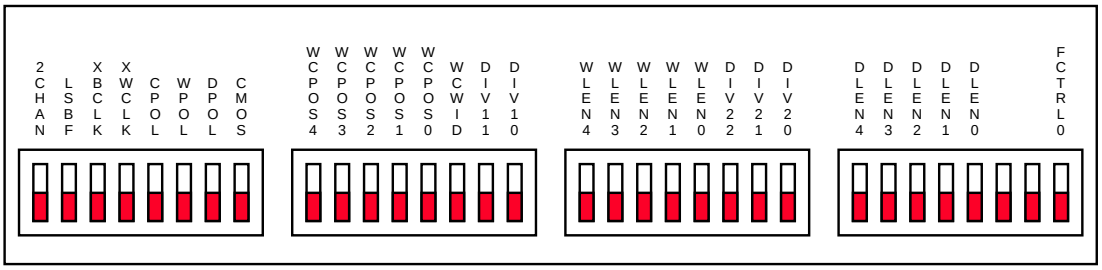
All SIA inputs are internally buffered with CMOS family parts. CMOS inputs have a very high input impedance. If the interface cables are relatively long, it is recommended that all input signals be terminated at the DB-15 connector to minimize reflections and ringing. A passive termination (e.g. a 75 ohm resistor connected between the input pin and its corresponding ground pin) may be used as long as the signal source is capable of providing the necessary drive current while maintaining proper logic levels. Each SIA output is capable of driving a 50 ohm transmission line, and is able to continuously source or sink at least 24 mA of current.

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3.4. Receiver Configuration Switches

A set of DIP switches is used to configure the SIA receiver for the various modes of operation. The switch settings for the receiver are illustrated in figure 12 and described in table 6 below. The configuration switches can be logically grouped into four distinct groups: the serial word length select, data length select, word clock position and framing control.

Figure 12. Receiver configuration switch locations.



3.4.1. Serial Word Length Selection

The serial word length is the number of actual bits received in each serial word. The SIA is capable of receiving a serial word of between 8 and 32 bits in length. The word length is specified by setting the WLEN DIP switch field to the desired word length minus 1. For example, for a serial word length of 18 bits, WLEN would be set to 17, or 10001 binary.

3.4.2. Serial Data Length Selection

The serial data length is the number of significant data bits to be received in the serial word. System One is capable of receiving up to 24 bits of data per sample; However, not all target devices are capable of supplying a full 24 bits of data. The SIA can be programmed to truncate each received data sample to any number of bits from 8 to 24. The serial data length is specified by setting the DLEN DIP switch field to the desired data length minus 1. For proper SIA operation, the data length must not exceed the word length.

3.4.3. Serial Word Clock Position Selection

Since the SIA receives serial data in a synchronous manner, the word clock signal (SIWCLK) is used to delineate the start of a new serial frame. In single channel applications, "frame" is synonymous with "word." In two channel applications, a frame is composed of two words, first channel A, then channel B. The timing of SIWCLK relative to the first bit of the serial frame can be configured by setting the word clock position (WCPOS) DIP switch field. The word clock signal transitions synchronously with the received data (SID), and the timing of word clock relative to the start of a received data frame may be set from zero to WLEN-1 bit clock times after the start of the word. For example, if the SIA receiver is configured for a word length of 16 bits (i.e. WLEN=01111), and the transition of SIWCLK is to occur during the last bit time of the serial frame, WCPOS would be set to 15, or 01111 binary. For proper SIA operation, the word clock position must be less than the word length.

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Table 6. Receiver configuration switch description.

Switch Name	Description
2CHAN	**Receiver Channel Select**. OFF = single channel operation, ON = two channel operation.
LSBF	**Receiver First-Bit Select**. Selects LSB or MSB as first valid bit within the serial frame. OFF = MSB first, ON = LSB first.
XBCLK	**Receiver Bit Clock Source Select.** Selects source of bit clock. OFF = internally generated bit clock, ON = external bit clock.
XWCLK	**Receiver Word Clock Source Select.** Selects source of word clock. OFF = internally generated word clock, ON = external word clock.
CPOL	**Receiver Bit Clock Polarity Select.** OFF = bit clock is asserted high, ON = bit clock is inverted (asserted low).
WPOL	**Receiver Word Clock Polarity Select.** OFF = word clock is asserted high, ON = word clock is inverted (asserted low).
DPOL	**Receiver Data Polarity Select.** OFF = received serial data is asserted high, ON = serial data is inverted (asserted low).
CMOS	**Receiver CMOS Input Select.** OFF = all inputs configured for TTL logic levels, ON = all inputs configured for CMOS.
WCPOS(4:0)	**Receiver Word Clock Position**. Physical position of word clock transition within the serial word. Can be set from 0 to 31.
WCWID	**Receiver Word Clock Width**. Width of receiver word clock pulse. OFF = bit-wide clock pulse, ON = word wide (symmetric) clock.
DIV1(1:0)	**Receiver N x FS Clock Control**. Sets RNFSCLK frequency by selecting master reference clock divide ratio (see section 3.4.4.).
WLEN(4:0)	**Receiver Word Length**. Length of received serial word, minus 1. Can be set from 7 to 31, corresponding to word lengths of 8 to 32 bits.
DIV2(2:0)	**Receiver Bit Clock Frequency Control**. Sets bit clock frequency to 1/(DIV2+1) times RNFSCLK frequency (see section 3.4.4.).
DLEN(4:0)	**Receiver Data Length**. Number of significant bits from received serial word to be transmitted to the System One, minus 1. Can be set from 7 to 23, corresponding to data lengths of 8 to 24 bits.
FCTRL0	**Receiver Framing Control 0**. OFF = right-justified data within the serial frame, ON = left-justified.

3.4.4. Serial Framing and Clocking Control

The SIA is capable of transmitting and receiving the word clock signal as either a bit-width or word-width signal, and is set by the WCWID configuration switch. If WCWID=OFF, SIWCLK will consist of a single pulse one bit-time in duration (i.e. one bit wide), transitioning at the appropriate bit time within the serial frame as defined by the setting of WCPOS. If WCWID=ON, SIWCLK will change state on each word boundary, effectively yielding a square wave with a period equal to the serial frame time. The bit-width and word-width word clock are useful for both single- and dual-channel (time multiplexed) operation. See the section on 2CHAN below for more information.

When the data and word lengths are not the same, it is necessary to specifying whether the data is left- or right-justified within the data word. FCTRL0 is used to specify this configuration.

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When FCTRL0=OFF, the received data is expected to be right-justified within the data word. When FCTRL0=ON, the received data is expected to be left-justified within the word.

The SIA is capable of receiving a single channel of data from the target system, or two channels of data in a time-multiplexed fashion. The mode of operation is set by the 2CHAN configuration switch. When 2CHAN=OFF, a single channel of data from the target system is received and transferred to System One (the B channel). When 2CHAN=ON, two channels of data are received (channels A and B). In two-channel mode with WCWID=ON (word-width word clock), the direction of transition of SIWCLK determines which channel is being received at any given time. When WPOL=OFF (see below), a low-to-high transition within the data frame implies that channel A is being received. In a similar manner, a high-to-low transition implies that channel B is being received. In two-channel mode with WCWID=OFF (bit-width word clock) and WPOL=OFF, a low-to-high transition of SIWCLK signals the start of a new serial frame, with channel A received first, followed by channel B.

The data sample within the frame may be sent by the target system either most significant bit (MSB) first, or least significant bit (LSB) first. The receiver can be configured for data in either format by setting LSBF to match the desired configuration. When LSBF=OFF, the received data is expected to be sent MSB first. When LSBF=ON, the received data is expected to be sent LSB first.

The SIA receiver is capable of generating a bit clock and word clock derived directly from the master reference clock (RREFCLK) input. Optionally, one or both of these clocks can be generated by the target system and supplied to the SIA, which will subsequently behave in a slave-receiver fashion. The source of the word clock is defined by the state of the XWCLK configuration switch. If XWCLK=OFF, the receiver will drive SIWCLK with a locally generated word clock. If XWCLK=ON, the receiver will slave to the word clock signal received on SIWCLK from the target system. In a similar manner, if XBCLK=OFF the receiver will drive SIBCLK with a locally generated bit clock. If XBCLK=ON, the receiver will slave to the bit clock received on SIBCLK from the target system. The four possible operating modes are shown in table 7 below. Note that clocks supplied by the target system must be appropriate for a given receiver configuration (i.e. the number of bit clocks per word clock interval must match the setting of WLEN, etc.).

The polarity of the received data, word and bit clocks are controlled by the DPOL, WPOL and CPOL configuration switches. When DPOL=OFF, serial data received is transferred to System One without modification (subject to the setting of DLEN, etc.). When DPOL=ON, the received data is inverted prior to transmission to System One.

The WPOL configuration switch allows the user to change the logic sense of SIWCLK when WCWID=OFF (i.e. word clock is bit-wide), and to change the channel sense when WCWID=ON. As described above, when WPOL=OFF and WCWID=ON, a low-to-high transition within the data frame implies that channel A is being received. In a similar manner, a high-to-low transition implies that channel B is being received. When WPOL=ON, the channel sense is reverse.

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Table 7. Receiver clock source selection.

XBCLK	XWCLK	Receiver Clock Source
OFF	OFF	Bit clock and word clock derived directly from master reference clock (RREFCLK).
OFF	ON	Not useful.
ON	OFF	Bit clock from target system used to generate word clock (RREFCLK generates RNFSCLK only).
ON	ON	Bit clock and word clock derived directly from target system (RREFCLK generates RNFSCLK only).

CPOL is used to define which edge of SIBCLK the received data (SID) and/or word clock (SIWCLK) are sampled on. When CPOL=OFF, both SID and SIWCLK are sampled on the rising edge of SIBCLK. When CPOL=ON, SID and SIWCLK are sampled on the falling edge of SIBCLK. When SIWCLK is configured as an output, CPOL defines which edge of SIBCLK that SIWCLK transitions on. When CPOL=OFF, SIWCLK transitions on the rising edge of SIBCLK. When CPOL=ON, SIWCLK transitions on the falling edge.

When configured as inputs, SIBCLK and SIWCLK can be configured to accept TTL or CMOS logic levels. The logic family is selected by the CMOS configuration switch. When CMOS=OFF, both inputs expect TTL logic levels. When CMOS=ON, both inputs expect CMOS logic levels. In either configuration, input loading is very low (inputs are buffered using HC/HCT logic family parts).

The DIV1 configuration switch field is used to select the frequency of the N x FS clock (RNFSCLK) signal. The RNFSCLK signal is generated by a power-of-two divider driven by the master reference clock (RREFCLK). DIV1 selects one of four possible division ratios: 1, 2, 4, or 8. The power-of-two divider may optionally be configured to divide by 4, 8, 16, or 32; this mode is described in section 3.6. below. The DIV1 switch is typically used in conjunction with the DIV2 switch to generate a clock that is some multiple of the system sample rate.

The DIV2 configuration switch field is used to set the bit clock (SIBCLK) frequency, and is derived from the N x FS clock signal. The transmitter bit clock is generated by a divider driven by RNFSCLK, where DIV2 is used to select the divide ratio. DIV2 selects one of eight possible division ratios: 1, 2, 3, 4, 5, 6, 7, or 8. DIV2 is typically used in conjunction with the DIV1 switch. For example, if RREFCLK is driven by a 12.288 MHz clock and the system is configured for two channels of 32-bit words at a sample rate of 48 kHz, the N x FS clock and bit clocks may be configured as follows: for a 256 x FS clock on RNFSCLK, DIV1 would be set to divide-by-one (DIV1 = 00 binary) and DIV2 would be set to divide-by-four (DIV2 = 011 binary); for a 128 x FS clock, DIV1 would be set to divide-by-two (DIV1 = 01 binary) and DIV2 would be set to divide-by-two (DIV2 = 001 binary). Note that in each of the above examples, the bit clock frequency remains constant (3.072 MHz) since the product of DIV1 and DIV2 is constant. Other N x FS clocks can be generated by the appropriate choice of reference clock frequency and DIV1 and DIV2 settings.

3.5. System Performance Issues

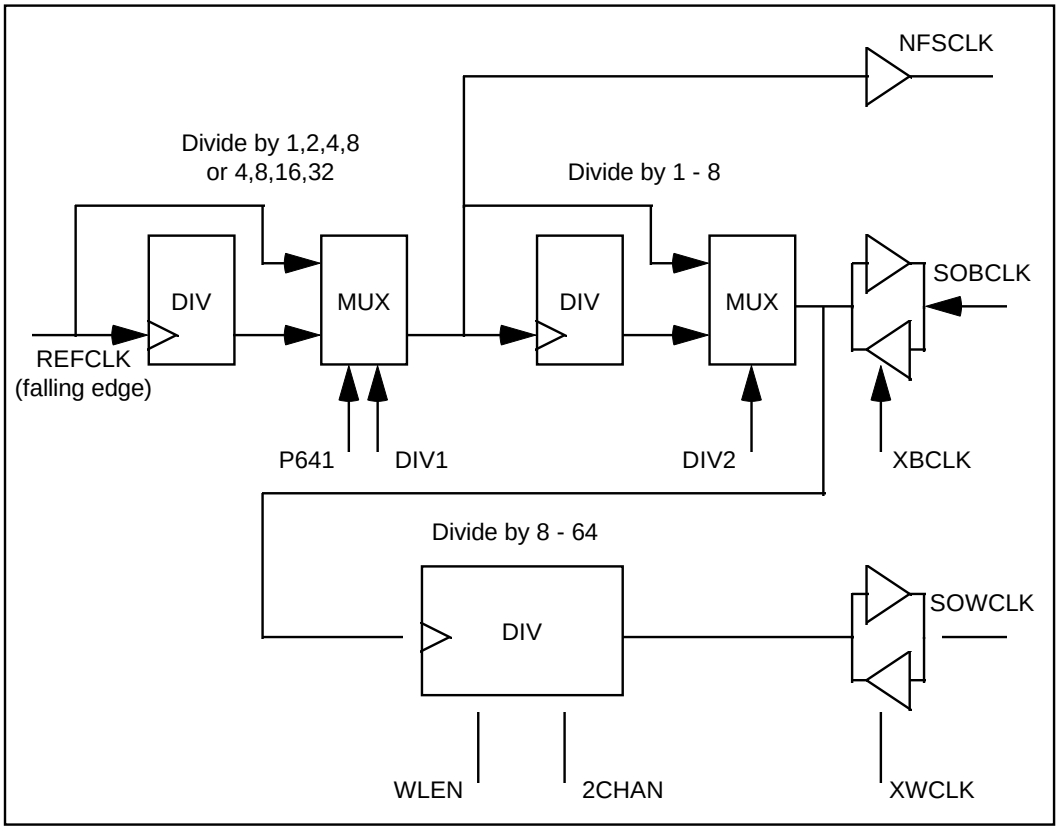
One of the most critical parameters affecting high-performance A/D and D/A converter systems is clock jitter. Many high-precision converter systems require bit, word, or reference

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clocks with residual jitter of less than 200 pS RMS. While the SIA is capable of generating clocks with residual jitter in the 100 to 200 pS range, optimum performance is achieved when reference clocks derived from a crystal oscillator are used to drive both the converter system and the SIA in slave mode (many A/D and D/A evaluation boards provide crystal-derived low-jitter bit and word clocks that are ideal for driving the SIA). When using a crystal oscillator for the system reference, great care must be taken in the interface between the SIA and the converter system. Attention must be paid to the quality and length of the interface cables, as well as signal terminations at the SIA and the system I/O connectors.

When using the SIA to generate bit and word clocks, the SIA uses the falling edge of the reference clock to drive the system dividers. In such instances, the reference clock used to drive the SIA should be optimized to have minimum jitter on its falling edge. Figure 13 below shows the internal clock divider chain for the transmitter section of the SIA that is used to generate bit and word clocks from an external reference. The internal clock divider chain for the receiver section of the SIA is identical to that shown in the figure.

Figure 13. Transmitter Internal clock divider chain.



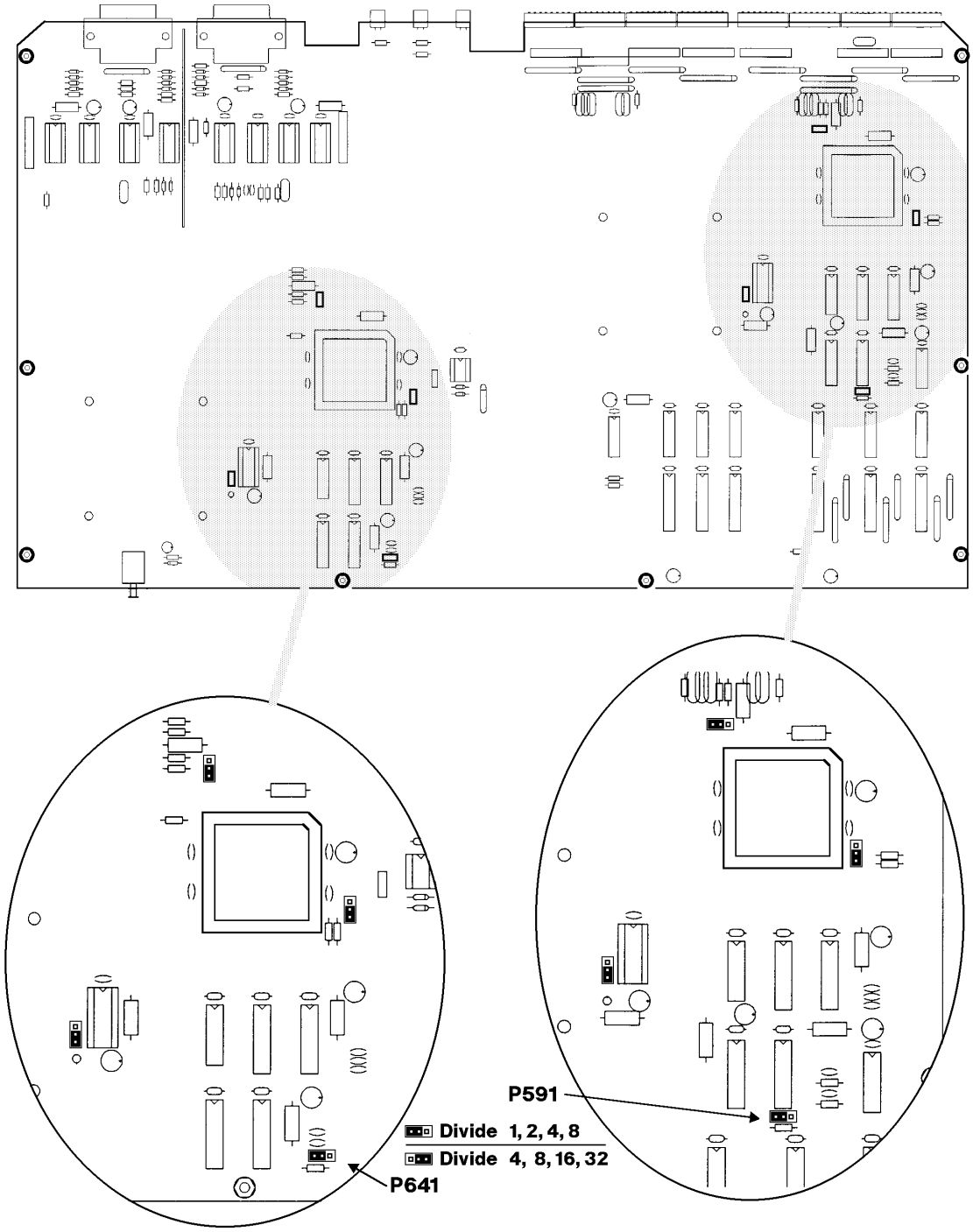
3.6. Transmitter and Receiver N x FS Clock Control

The N x FS clocks of the transmitter and receiver (TNFSCLK and RNFSCLK, respectively) are generated by programmable dividers on the SIA circuit board. As shipped from the factory, the transmitter and receiver dividers can be independently programmed to divide by 1, 2, 4, or 8 by way of the front panel configuration switches DIV1. Each divider can alternatively be configured to divide by 4, 8, 16, or 32 for those applications that require higher divide ratios. This mode is configured via two jumpers located on the SIA circuit board. The jumpers are accessible

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by removing the top cover of the SIA. Referring to figure 14, jumper P641 is used to select the divide range for the transmitter, and jumper P591 is used to select the divide range for the receiver. The appropriate configuration of the jumpers for each mode is shown in the figure.

Figure 14. Location of P641 and P591 jumpers on SIA circuit board.



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4. Serial Interface Timing

4.1. Transmitter I/O Timing

Table 8 below defines the various AC timing characteristics of the SIA transmitter. All timing information is measured at the DB-15 connector and assumes an output loading capacitance of 50 pF and an operating temperature of 25 degrees C.

Table 8. Transmitter AC Timing Characteristics

Parameter	XBCLK	XWCLK	Min	Typical	Max	Units
TREFCLK period	-	-	65	-	-	nS
SOBCLK to SOD delay	OFF	-	0	2	20	nS
SOBCLK to SOD delay	ON	-	-	42	58	nS
SOBCLK to SOWCLK delay	OFF	OFF	0	12	41	nS
SOBCLK to SOWCLK delay	ON	OFF	-	53	69	nS
SOWCLK to SOBCLK setup	OFF	ON	53	-	-	nS
SOWCLK to SOBCLK hold	OFF	ON	0	-	-	nS
SOWCLK to SOBCLK setup	ON	ON	10	-	-	nS
SOWCLK to SOBCLK hold	ON	ON	0	-	-	nS
SOD, SOWCLK, SOBCLK output enable time	-	-	-	16	24	nS
SOD, SOWCLK, SOBCLK output disable time	-	-	-	17	24	nS

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4.2. Receiver I/O Timing

Table 9 below defines the various AC timing characteristics of the SIA receiver. All timing information is measured at the DB-15 connector and assumes an output loading capacitance of 50 pF and an operating temperature of 25 degrees C.

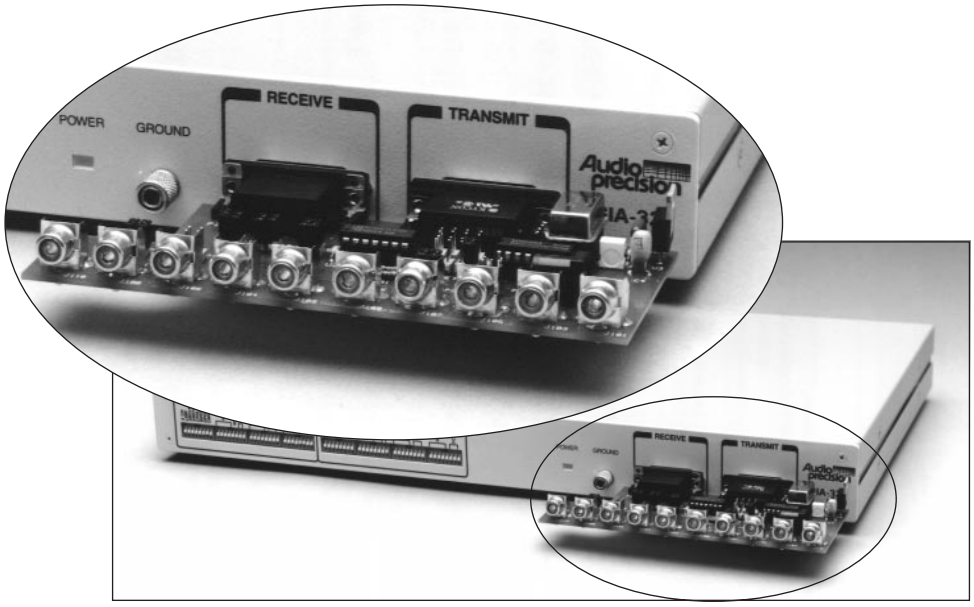
Table 9. Receiver AC Timing Characteristics

Parameter	XBCLK	XWCLK	Min	Typical	Max	Units
RREFCLK period	-	-	65	-	-	nS
SIBCLK to SIWCLK delay	OFF	OFF	0	12	42	nS
SIBCLK to SIWCLK delay	ON	OFF	-	53	70	nS
SIWCLK to SID setup	OFF	-	53	-	-	nS
SIWCLK to SID hold	OFF	-	0	-	-	nS
SIWCLK to SID setup	ON	-	10	-	-	nS
SIWCLK to SID hold	ON	-	0	-	-	nS
SIWCLK to SIBCLK setup	OFF	ON	53	-	-	nS
SIWCLK to SIBCLK hold	OFF	ON	0	-	-	nS
SIWCLK to SIBCLK setup	ON	ON	10	-	-	nS
SIWCLK to SIBCLK hold	ON	ON	0	-	-	nS
SIWCLK, SIBCLK output enable time	-	-	-	16	24	nS
SIWCLK, SIBCLK output disable time	-	-	-	17	24	nS

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5. The SIA-DUT Interface Board

The SIA-322 comes equipped with a device-under-test (DUT) interface board that can be used to easily connect the SIA to a target system. The interface board plugs into the two DB-15 connectors on the front of the SIA and provides direct access to all of the main SIA I/O pins via standard female phono connectors. The interface also has an on-board crystal oscillator with two programmable divider taps that can be used to drive the TREFCLK/RREFCLK and SOBCLK/SIBCLK signals on the SIA and their corresponding inputs on the DUT. A set of ten (10) interface cables with male phono connectors at each end are supplied to simplify interconnection between the SIA and the DUT. The DUT interface board operates from a single low-voltage DC supply.



5.1. I/O Connections to the SIA

The SIA-DUT interface board has two DB-15 connectors on the rear of the board that plug directly into the I/O connectors on the front panel of the SIA. No other connections to the SIA are necessary.

5.2. I/O Connections to the DUT

The SIA-DUT interface board has a set of ten female phono connectors that are used to interface to the DUT. The signal name associated with each connector is clearly marked on the interface board directly behind the connectors (see figure **Error! Bookmark not defined.**). Table 10 identifies all ten connectors and their function.

Table 10. SIA-DUT interface board I/O connections.

SIA-DUT Phono Jack Number	SIA Signal Name	Signal Description
J101	SOD	Serial output data

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J103	SOWCLK	Serial output word clock
J105	SOBCLK	Serial output bit clock
J107	TREFCLK	Serial output master reference clock
J108	TNFSCLK	Serial output NxFS clock
J102	SID	Serial input data
J104	SIWCLK	Serial input word clock
J106	SIBCLK	Serial input bit clock
J108	RREFCLK	Serial input master reference clock
J110	RNFSCLK	Serial input NxFS clock

5.3. Configuring the SIA-DUT Interface Board

The SIA-DUT interface board has 23 push-on jumpers that are used to configure the board for various modes of operation. Eight of the jumpers are used to selectively drive the bit-clock (SOBCLK/SIBCLK) and master reference clock (TREFCLK/RREFCLK) lines, eight of the jumpers are used to select the divide ratio for the programmable divider, one of the jumpers is used to configure the clock oscillator, and the remaining six jumpers are used to configure the board for loopback operation (see table 11 and figure **Error! Bookmark not defined.**).

Table 11. SIA-DUT interface board configuration jumpers.

Signal Jumper	Ground Jumper	Function of Jumper
P23	P22	Connects divider-tap-A output to SOBCLK
P19	P18	Connects divider-tap-A output to SIBCLK
P21	P20	Connects divider-tap-B output to TREFCLK
P17	P16	Connects divider-tap-B output to RREFCLK
P1	—	Sets divider-tap-A to divide by 1
P2	—	Sets divider-tap-A to divide by 2
P3	—	Sets divider-tap-A to divide by 4
P4	—	Sets divider-tap-A to divide by 8
P5	—	Sets divider-tap-B to divide by 1
P6	—	Sets divider-tap-B to divide by 2
P7	—	Sets divider-tap-B to divide by 4
P8	—	Sets divider-tap-B to divide by 8
P26-NC[5]	—	X1 pin 1 unconnected (floating)
P26-(1,2)	—	Connects X1 pin 1 to +5V
P26-(2,3)	—	Connects X1 pin 1 to ground

5 NC = "No Connection."

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P15	P14	Connects SOD to SID
P13	P12	Connects SOWCLK to SIWCLK
P11	P10	Connects SOBCLK to SIBCLK

5.3.1. Crystal Oscillator and Divider-Tap Configuration

The SIA-DUT interface board has an on-board 24.576 MHz crystal oscillator and divider that can be used to drive the clock inputs on the SIA and the DUT. There are two independent divider outputs -- divider-tap-A and divider-tap-B. Divider-tap-A is used to drive the bit-clock signals SOBCLK and SIBCLK. Divider-tap-B is used to drive the master reference clock signals TREFCLK and RREFCLK. As shown in table 11, the divider taps are connected to the four signals by installing their associated jumpers (P16 - P23). Note that each signal requires the installation of two jumpers -- one for the clock signal and one for the ground signal.

The frequencies of the clock signals at divider-tap-A and divider-tap-B are determined by jumpers P1 - P8. The divide ratio can be set to 1, 2, 4 or 8 independently for each divider tap. The divide ratio for divider-tap-A is set by installing **only one** jumper on P1, P2, P3 **or** P4. The divide ratio for divider-tap-B is set by installing **only one** jumper on P5, P6, P7 **or** P8.

The crystal oscillator is installed in a standard 14-pin DIP socket (marked on the board as X1), allowing the user to select an oscillator frequency that is appropriate for his or her application. Many off-the-shelf crystal oscillators have special requirements for the voltage level at pin one on the oscillator package. P26 on the SIA-DUT board allows the user to configure pin one of the oscillator to be unconnected (the default), connected to +5V, or connected to ground by selecting the appropriate jumper locations as shown in table 11.

5.3.2. SIA Loopback Mode Configuration

The SIA may be placed in loopback mode by installing three jumper pairs (P10 - P15) on the SIA-DUT interface board. Loopback mode can be used to test the operation of the SIA, or to experiment with different SIA configurations. A loopback configuration example can be found in section 6.2..

5.4. SIA-DUT Interface Board Power Requirements

The DUT interface operates off of a DC voltage supply of between 6 and 18 volts. The power source supplying the voltage must be capable of sourcing up to 1 ampere of current. The DC voltage is applied at J14, with the connector ring connected to the positive terminal and the connector tip connected to the negative terminal of the power source.

5.5. SIA-DUT Interface Board Schematic

The SIA-DUT interface board is designed for maximum flexibility and ease of use.

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6. SIA-DUT Interfacing Examples

This section presents a number of...

6.1. General Interconnection Example

THIS SECTION NEEDS TO BE COMPLETED.

There are a number of.... Most designs will reduce to the following steps.

_ Remove SIA-DUT jumpers P10 - P15
_ Remove SIA-DUT jumpers P16 - P19 if the DUT is to be connected to the SIA receiver, or P20 - P23 if the DUT is to be connected to the SIA transmitter.
_ Turn off all SIA transmitter or receiver configuration switches.
_ Configure the SIA-DUT board and the SIA configuration switches.

Question: Does the DUT generate the bit clock signal (SOBCLK/SIBCLK)?

Yes:

_ Set XBCLK switch to ON.

No:

Question: Does the DUT generate a clock reference that is N times the frequency of bit-clock?

Yes:

_ If N is 2, 4 or 8, set DIV1 switches to 01, 10 or 11, respectively.
_ If N is 3, 5, 6 or 7, set DIV2 switches to 010, 100, 101, 110 or 111, respectively.
_ Connect the DUT clock reference to the SIA reference input (TREFCLK/RREFCLK).

No:

_ Install a crystal oscillator in the SIA-DUT interface board at X1 of the appropriate frequency (the required bit-clock frequency, or some power-of-two multiple of it).
_ Install jumper P1, P2, P3 or P4 as appropriate.
_ Install jumpers P19/P18 for the transmitter, or P23/P22 for the receiver.
_ Set XBCLK switch to ON.

Question: Does the DUT generate the word clock signal (SOWCLK/SIWCLK)?

Yes:

_ Set XWCLK switch to ON.

_ Set LSBF ON if data is transmitted least-significant bit first in the data frame.
_ Set XXXX ON if...
_ Set WCPOS to the appropriate number
_ Set WLEN to the word length from 8 to 32 bits (WLEN = 00111 to 11111).
_ Set DLEN to the data length from 8 to 24 bits (DLEN = 00111 to 10111).

_ Connect the data line to SOD/SID
_ Connect the word clock line to SOWCLK/SIWCLK
_ Connect the bit clock line to SOBCLK/SIBCLK

6.2. Configuring the SIA for Local Loopback

The SIA can be easily configured for *loopback* operation with the use of the SIA-DUT interface board. The term *loopback* refers to the physical connection of the SIA transmitter's serial I/O lines to the receiver's lines. Data sent by the SIA transmitter is simultaneously received by the receiver. Loopback operation is helpful for verifying proper SIA hardware operation and experimenting with various serial configurations.

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To configure the SIA for loopback operation, install the SIA-DUT interface board on the SIA I/O connectors. The SIA-DUT jumper configurations for loopback are shown in table 12 below.

Table 12. SIA-DUT jumper configuration for SIA loopback operation.

SIA-DUT Jumper	Connection	Function
P11, P10	SOD → SID	Serial Data, Ground
P13, P12	SOWCLK → SIWCLK	Word Clock, Ground
P15, P14	SOBCLK → SIBCLK	Bit Clock, Ground
P21, P20	Oscillator → TREFCLK	Reference Clock, Ground
P8	Oscillator Divider	Selects Divide-by-8
All Others	Not Installed	#

In this loopback configuration, the transmitter is configured as the system master and the receiver as the slave. The data rate is 48 kHz with two 24-bit words transmitted per 64-bit frame. The correct configuration switch settings for the transmitter and receiver are shown in figures 15 and 16 below. The transmitter receives its clock signal from the oscillator on the SIA-DUT interface board (for this example, it is assumed that the crystal oscillator frequency is 24.576 MHz). Since divider-tap-B is set to divide-by-8 (with P8 installed), the frequency of the clock that is applied to TREFCLK is 3.072 MHz.

Figure 15. Transmitter configuration for loopback operation.

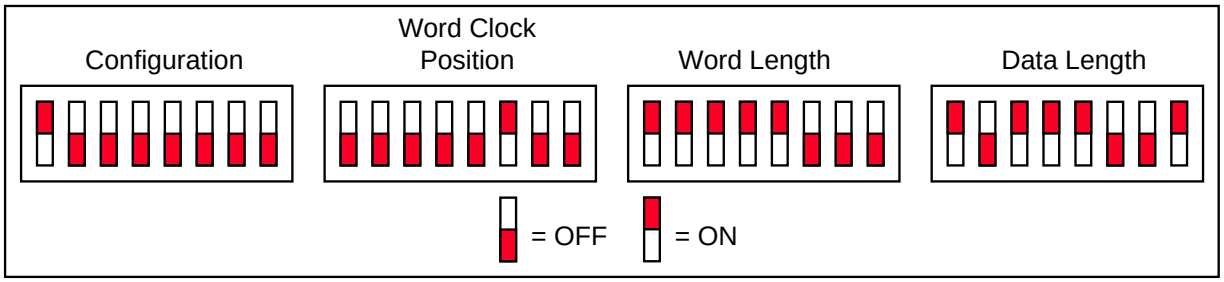
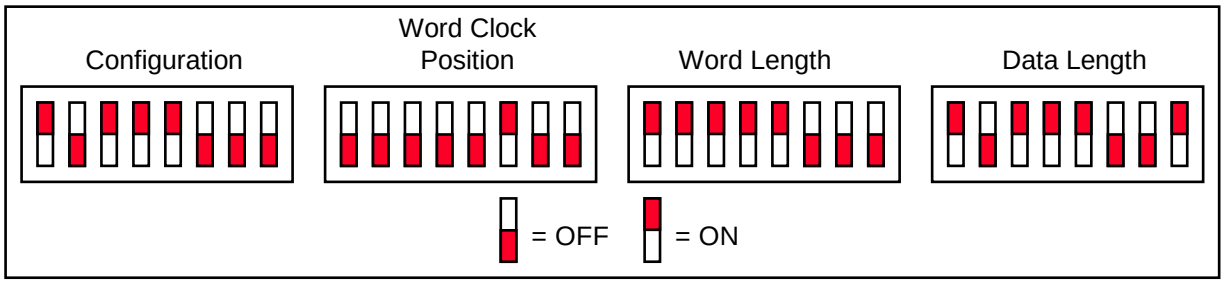


Figure 16. Receiver configuration for loopback operation.



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6.3. Connecting the SIA Receiver to the Crystal CDB5336 Evaluation Board

The Crystal CDB5336 Evaluation Board is used to evaluate the Crystal CS5336 dual-channel analog-to-digital converter. The CS5336 is a particularly interesting converter as it can be configured for either master or slave operation, each having different interface requirements. The SIA receiver can interface properly to the CS5336 in either mode.

6.3.1. The Crystal CDB5336 in Slave Mode

When the CS5336 is configured as a slave device, the SIA receiver operates as the master, thereby generating the bit, word, and high-frequency clocks for the CS5336. In order to correctly drive the CS5336 in this mode, you must make the following changes to the CDB5336 evaluation board:

- ❒ Remove R6, the clock termination resistor
- ❒ Set P4 to '5336/38'
- ❒ Set P5 to 'B'
- ❒ Set P6 to 'zero'
- ❒ Set P7 to 'external'
- ❒ Set P8, P9 to 'in'
- ❒ Connect SMODE (pin ***PIN_NUMBER*** on the CS5336) to ground (LOW).
- ❒ Connect FSYNC (pin ***PIN_NUMBER*** on the CS5336) to VCC (HIGH).

Interfacing the SIA to the CDB5336 board is simple when the SIA-DUT interface board is used. After installing the SIA-DUT interface board on the SIA I/O connectors, install the SIA-DUT jumpers as described in table 13. The connections necessary between the SIA-DUT interface board and the CDB5336 board are described in table 14 and shown in figure 17. The proper configuration switch settings for the SIA receiver are shown in figure 18.

Table 13. SIA-DUT jumper configuration for CDB5336 as slave.

SIA-DUT Jumper	Connection	Function
P17, P16	Oscillator → RREFCLK	Reference Clock, Ground
P6	Oscillator Divider	Selects Divide-by-2
All Others	Not Installed	#

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Table 14. SIA-DUT / CDB5336 interconnection (CDB5336 as slave).

SIA-DUT Interface Board Connection		CDB5336 Board Connection	Signal Description
J102	SID	SDATA	Serial Data from CDB5336 to SIA
J104	SIWCLK	L/R	Word Clock from SIA to CDB5336
J106	SIBCLK	SCLK	Bit Clock from SIA to CDB5336
J108	RREFCLK	EXTCLKIN	Reference Clock from SIA-DUT to CDB5336

Figure 17. Receiver / CDB5336 physical interconnection (CDB5336 as slave).

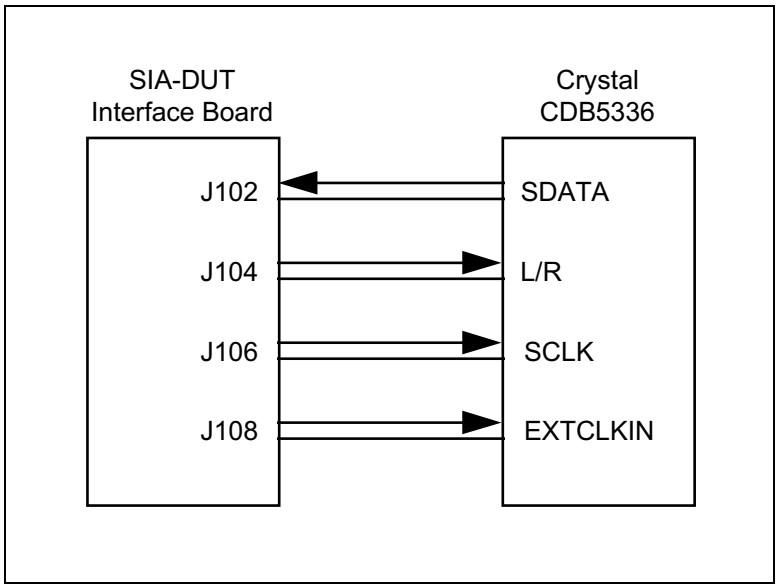
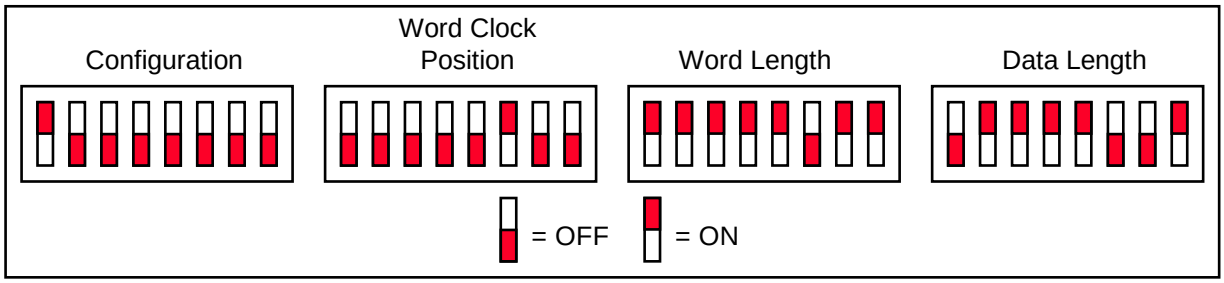


Figure 18. SIA receiver configuration for CDB5336 as slave.



6.3.2. The Crystal CDB5336 in Master Mode

When the CS5336 is configured as a master device (with the SIA operating as the slave), the CS5336 generates the bit and word clocks for the SIA. To correctly configure the CDB5336 evaluation board for master mode operation, you must make the following changes to the board:

- ❒ Remove R6, the clock termination resistor

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- ❒ Set P4 to '5336/38'
- ❒ Set P5 to 'B'
- ❒ Set P6 to 'zero'
- ❒ Set P7 to 'internal'
- ❒ Set P8, P9 to 'in'

Interfacing the SIA to the CDB5336 board is simple when the SIA-DUT interface board is used. After installing the SIA-DUT interface board on the SIA I/O connectors, remove all jumpers from the SIA-DUT interface board (no jumpers are required when the CS5336 is in master mode) . The connections necessary between the SIA-DUT interface board and the CDB5336 board are described in table 15 and shown in figure 19. The proper configuration switch settings for the SIA receiver are shown in figure 20. Note that the CS5336 in Master mode transmits data in a manner compatible with the Signetics I^2S Bus Standard.

Table 15. SIA-DUT / CDB5336 interconnection (CDB5336 as master).

SIA-DUT Interface Board Connection		CDB5336 Board Connection	Signal Description
J102	SID	SDATA	Serial Data from CDB5336 to SIA
J104	SIWCLK	L/R	Word Clock from CDB5336 to SIA
J106	SIBCLK	SCLK	Bit Clock from CDB5336 to SIA

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Figure 19. Receiver / CDB5336 physical interconnection (CDB5336 as master).

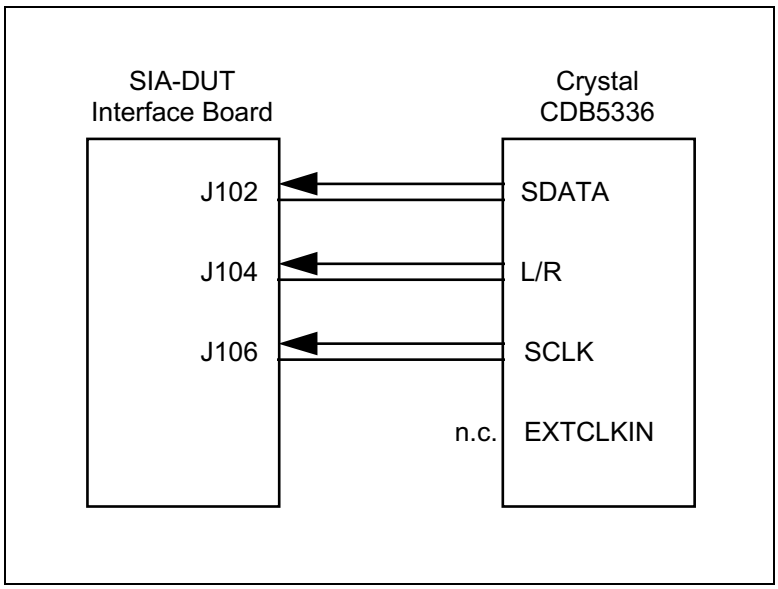
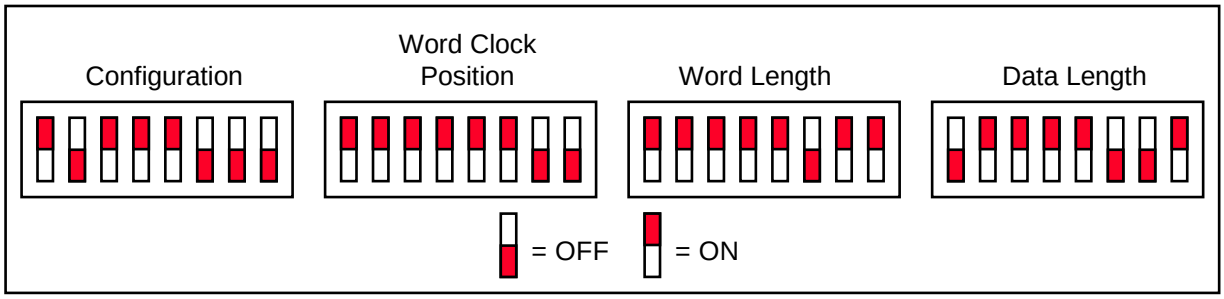


Figure 20. SIA receiver configuration for CDB5336 in master mode.



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6.4. Connecting the SIA Receiver to the Analog Devices AD1879 Evaluation Board

The Analog Devices AD1879 is a dual-channel, 18-bit analog-to-digital converter capable of both master and slave mode operation. The SIA can interface properly to the AD1879 in either mode. This example shows how to connect the SIA to the AD1879 evaluation board when the AD1879 is configured for master operation.

In master mode, the AD1879 generates the bit and word clocks for the SIA. To correctly configure the AD1879 board for master mode operation, make the following changes to the board:

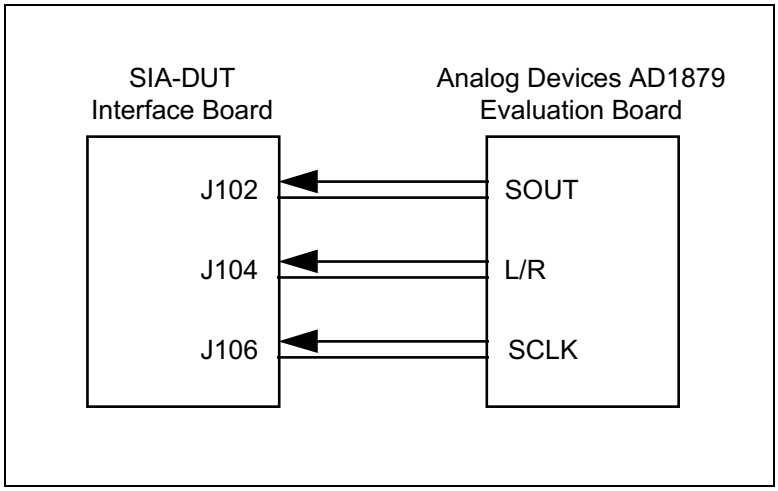
- ❒ Remove jumper JP1
- ❒ Install jumpers JP2-7
- ❒ Set switch SW1 for internal reference clock

Interfacing the SIA to the AD1879 evaluation board is simple when the SIA-DUT interface board is used. After installing the SIA-DUT interface board on the SIA I/O connectors, remove all jumpers from the SIA-DUT interface board (no jumpers are required when the AD1879 is in master mode) . The connections necessary between the SIA-DUT interface board and the AD1879 evaluation board are described in table 16 and shown in figure 21. The proper configuration switch settings for the SIA receiver are shown in figure 22.

Table 16. SIA-DUT / AD1879 evaluation board interconnection (AD1879 as master).

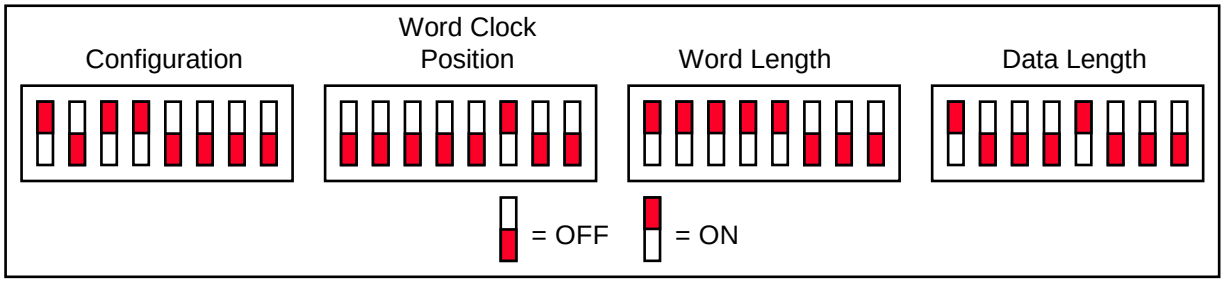
SIA-DUT Interface Board Connection		AD1879 Board Connection	Signal Description
J102	SID	SOUT	Serial Data from AD1879 to SIA
J104	SIWCLK	L/R	Word Clock from AD1879 to SIA
J106	SIBCLK	SCLK	Bit Clock from AD1879 to SIA

Figure 21. Receiver / AD1879 physical interconnection (AD1879 as master).



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Figure 22. SIA receiver configuration for AD1879 in master mode.



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6.5. Connecting the SIA Transmitter to the Signetics TDA1541

The Signetics TDA1541 is a dual-channel, 16-bit digital-to-analog converter that can be configured for the I^2S Bus Standard. Interfacing the SIA to the TDA1541 board is simple when the SIA-DUT interface board is used. After installing the SIA-DUT interface board on the SIA I/O connectors, install the SIA-DUT jumpers as described in table 17. The connections necessary between the SIA-DUT interface board and the TDA1541 are described in table 18 and shown in figure 23. The proper configuration switch settings for the SIA transmitter are shown in figure 24.

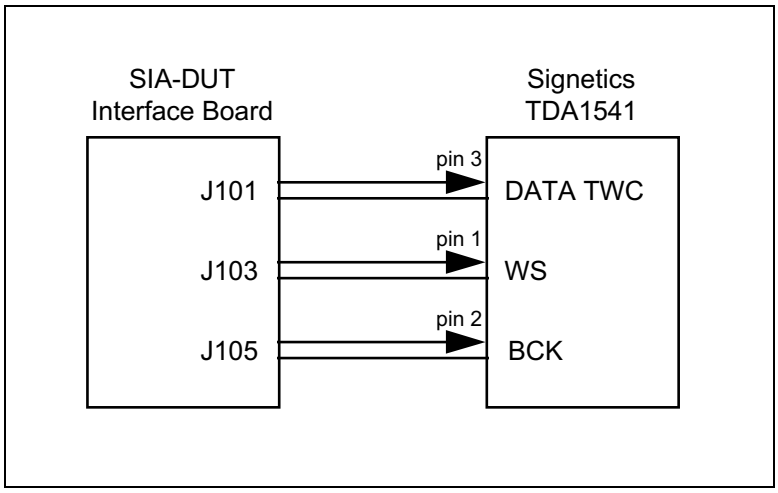
Table 17. SIA-DUT jumper configuration for TDA1541.

SIA-DUT Jumper	Connection	Function
P21, P20	Oscillator → TREFCLK	Reference Clock, Ground
P6	Oscillator Divider	Selects Divide-by-2
All Others	Not Installed	#

Table 18. SIA-DUT / TDA1541 interconnection.

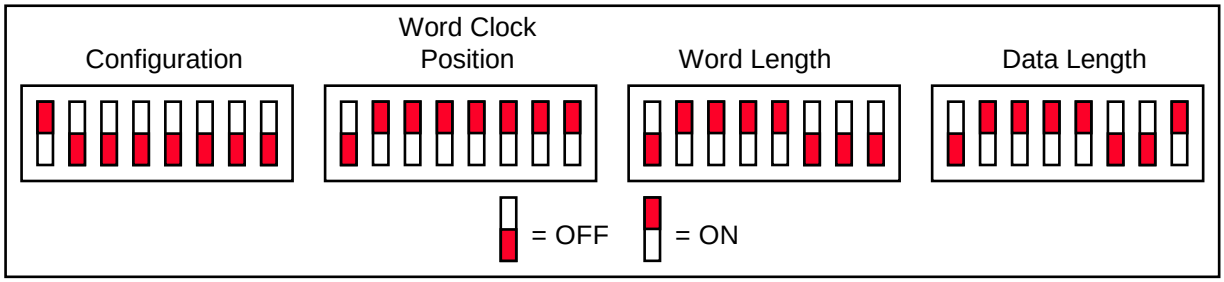
SIA-DUT Interface Board Connection		TDA1541 Connection	Signal Description
J101	SOD	DATA TWC (3)	Serial Data from SIA to TDA1541
J103	SOWCLK	WS (1)	Word Clock from SIA to TDA1541
J105	SOBCLK	BCK (2)	Bit Clock from SIA to TDA1541

Figure 23. SIA transmitter / TDA1541 physical interconnection.



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Figure 24. SIA transmitter configuration for TDA1541 in slave mode.



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