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Xilinx® Virtex™ -4 FX12 Evaluation Kit

User Guide

AVNET electronics marketing

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1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the Virtex-4 FX12 Evaluation Kit from Avnet Electronics Marketing. This document includes instructions for operating the board, descriptions of the hardware features and explanations of the example projects.

1.1 Description

The Virtex-4 FX12 Evaluation Kit provides a platform for engineers designing with the Xilinx Virtex-4 FX12 FPGA. The board provides the necessary hardware to not only evaluate the advanced features of the Virtex-4 FX12 but also to implement complete user applications. Example projects are provided to help the user understand the design tool flow of the Xilinx Embedded Development Kit (EDK) software environment.

1.2 Features

FPGA
- — Xilinx XC4VFX12-FF668 Virtex-4 FX12 FPGA

Board I/O Connectors
- — Two 140-pin general-purpose I/O expansion connectors (AvBus)
- — 30 LVDS pairs

Memory
- — Micron DDR SDRAM – 32 MB
- — 4 MB FLASH

Communication
- — 10/100 base T Ethernet
- — RS-232 serial port

Power
- — 10+ Watt AC/DC +5.0V power supply
- — National Linear regulators

Configuration
- — Xilinx XCFX12xP Platform Flash PROM
- — Support for Xilinx Parallel Cable IV
- — Fly-wire support for any Xilinx or compatible cable

1.3 Demo Applications

The Virtex-4 FX12 Evaluation Kit from Avnet Electronics Marketing comes with both source code and example projects designed in Xilinx Platform Studio (XPS). XPS is a software tool in the Xilinx Embedded Development Kit (EDK) that provides the user with a single tool flow for creating both hardware and software for processor-based systems. The source code and example projects that will be discussed in detail later in this document are listed below.

Source Code
- — OLED Display Example

XPS Example Projects
- — Base System Builder
- — Custom Peripheral Project

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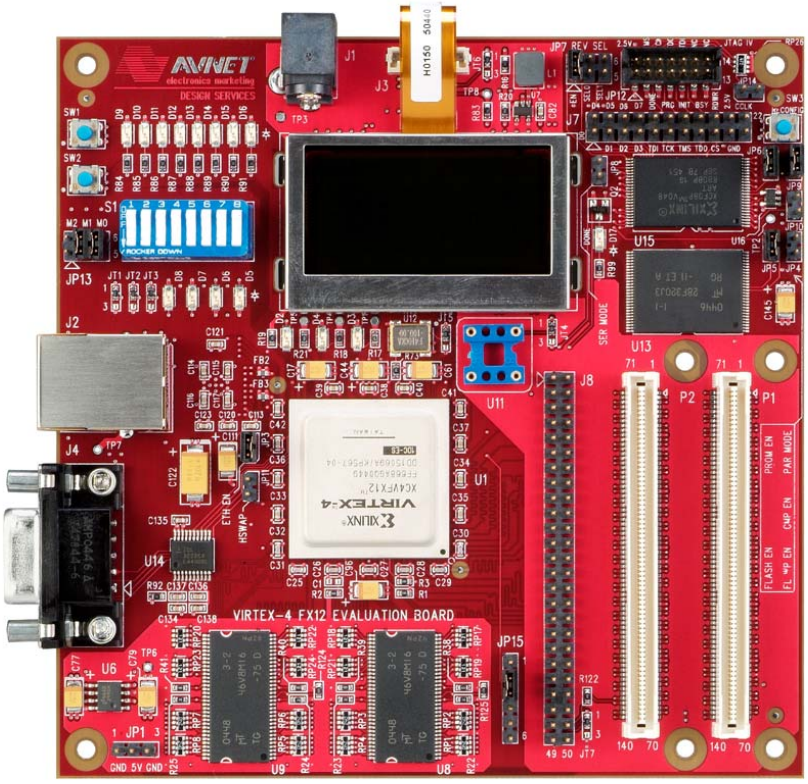


Figure 1 - Virtex-4 FX12 Evaluation Board Picture

1.4 Ordering Information

The following table lists the evaluation kit part numbers and available software options.
Internet link at http://www.em.avnet.com/ads

Part Number	Hardware
ADS-XLX-V4FX-EVL12	Xilinx Virtex-4 FX12 Evaluation Kit populated with an XC4VFX12 device
ADS-FOUNDATION-BUNDLE	ISE *Foundation* (only available with purchase of the above part number)

Table 1 - Ordering Information

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2.0 User Information

This section provides the user with information on how to get started using the Virtex-4 FX12 Evaluation Board. It discusses how to power the board, configure the FPGA device and set-up the jumpers.

2.1 Power

The Virtex-4 FX12 Evaluation Kit includes a 5V AC/DC Adapter that plugs into the board at “J1”.

2.2 Configuration

The Virtex-4 FX12 Evaluation Board supports several methods of configuration including boundary-scan, master serial and master/slave parallel (SelectMAP). Configuration data can come from the following sources: the on-board configuration PROM or an external download cable. The boundary-scan, serial and parallel configuration ports are brought out to a 0.1” header for user access (labeled “J7” on the Virtex-4 FX12 Evaluation Board). The following sections discuss the different configuration options. For more detailed information, see the “Configuration Reference Manual” in the documents folder on the kit CD.

2.2.1 Boundary Scan

Programming the Virtex-4 FX12 FPGA via Boundary Scan requires a JTAG download cable be attached to one of two interfaces that are wired in parallel on the board (see Figure 2). A download cable can be attached to either the 14-pin 2mm spaced header “JP12” with a ribbon cable or to the 0.1” header “J7” with flying leads as appropriate for your cable. For more information about JTAG download cables see the Xilinx web page http://www.xilinx.com. Click on the “Products & Services” tab and then click on the “Configuration Solutions” link. Scroll down to “Configuration Hardware” and select the download cable of interest.

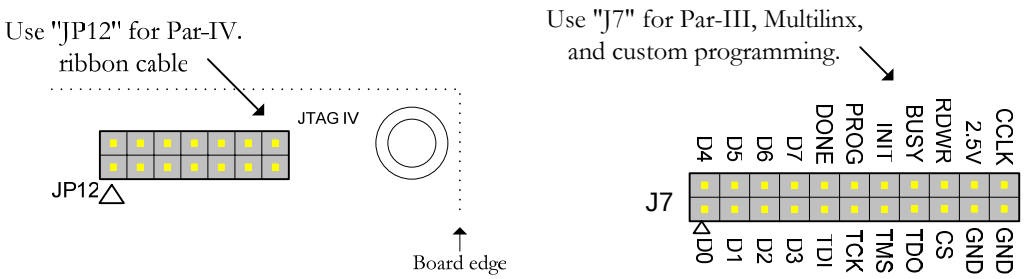


Figure 2 - Configuration Connectors

If the Parallel Cable IV is used, the ribbon cable connector mates with the JP12 connector. This connector is keyed to ensure the connections are made correctly.

The Virtex-4 FX12 Evaluation Board provides the user with the ability to add/remove devices from the JTAG chain. By the default settings, the chain of the Virtex-4 FX12 Evaluation Board includes the configuration PROM and the Virtex-4 FX12 FPGA. The header labeled “JP15” allows the user to select additional devices for inclusion in the chain. This will be discussed in greater detail in the hardware section of this manual. Most users will only need the PROM and FPGA to be in the JTAG chain, which is referred to as “Standalone” mode. Standalone mode is selected by a jumper installed across pins 2-3 on JP15 as shown in Figure 3. The Virtex-4 FX12 Board is already set for Standalone mode by the default jumper selection.

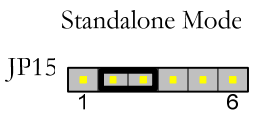


Figure 3 - JTAG Chain Standalone Mode

The configuration modes of the FPGA must be selected before applying power to the board. Jumper settings allow the Virtex-4 device to be set to any of the available configuration modes. The Virtex-4 FX12 FPGA is set to Master Serial mode when no jumpers are installed on JP13. To set the FPGA to boundary-scan mode, install shunts on JP13 at locations 1-2 & 5-6 as shown in Figure 4. For a complete list of available modes, please see the “Configuration Overview” chapter in the “Virtex-4 FPGA Handbook.”

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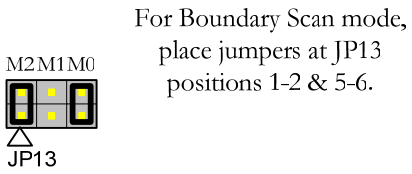


Figure 4 - Boundary Scan Mode Selection via JP13

After the download cable, chain and modes have been set; apply power to the board and open/run the iMPACT software to configure the boundary-scan devices. The Virtex-4 FX12 FPGA is supported by the version of iMPACT in the Xilinx Integrated Software Environment (ISE) 7.1i or later tools. Earlier versions of the tools may not fully support the Virtex-4 FX12 FPGA.

2.2.2 Configuration PROM

The Xilinx Platform Flash PROM provides non-volatile storage for the configuration file. This device is in-system programmable via the boundary-scan chain and can configure the FPGA on power-up. The parallel version of the Platform Flash PROM, the XCFX12xP, supports both serial and parallel configuration modes. The default jumper settings on the board set the XCFX12xP PROM to configure the FPGA on power-up using parallel configuration, or Master SelectMAP mode. The PROM has been pre-programmed with a demo design that displays an image of the Virtex-4 FX12 Evaluation Board on the OLED Display. The LED labeled "DONE" on the board illuminates to indicate when the FPGA has been successfully configured.

The PROM can be re-programmed with new configuration data using a JTAG download cable and the iMPACT software that comes with the Xilinx ISE tools. See the "Configuration Reference Manual" in the documents folder on the Kit CD for more detailed information. The iMPACT software puts the PROM in either serial or parallel mode during programming based on a user-selectable programming option (the default in iMPACT is serial). After the PROM has been re-programmed, remove power and set the FPGA configuration mode that corresponds with the programming option that was selected in iMPACT. The jumper settings for Master Serial and Master SelectMAP (Parallel) modes are shown in Figure 5. A jumper must be installed on JP6 (labeled "PROM EN") to enable configuration from the PROM. When power is re-applied, the FPGA will clock the configuration data from the PROM.

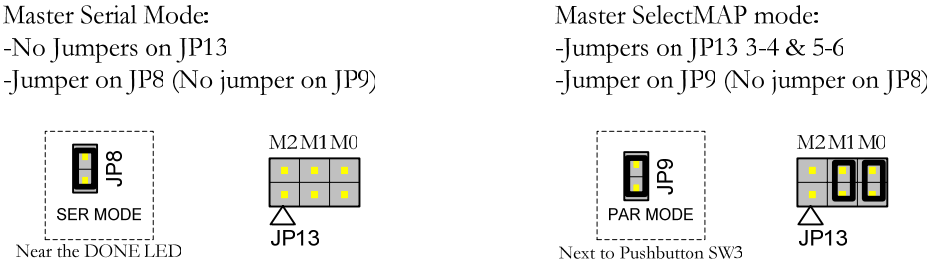


Figure 5 - Jumper Settings for Master Serial/SelectMAP modes

As shown in Figure 5, to configure the Virtex-4 FX12 FPGA in serial mode, remove the jumper on JP9 (labeled "PAR MODE") and install it on JP8 (labeled "SER MODE"). Then remove the jumpers on JP13 to select Master Serial mode. After applying power to the board, the DONE LED indicates when the configuration has successfully completed. For serial mode, this usually takes about 3 seconds. For faster configuration on power-up, select the "Parallel" programming option in iMPACT when programming the PROM. Then set the jumper settings for Master SelectMAP mode as shown in Figure 5.

The Virtex-4 FX12 Evaluation Board is designed to support the advanced features of the parallel Platform Flash PROM including support for multiple design revisions and compressed configuration files. These features are disabled by the default jumper settings. See the "Configuration Reference Manual" in the documents folder on the Kit CD for detailed information on how to use these features.

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2.3 Jumper Settings

This section provides a description of the jumper settings for the Evaluation board. The jumpers are listed in order of JP number. The board is ready to use out of the box with the default jumper settings.

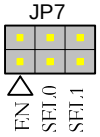
JP3 "ETH_EN" – Ethernet Enable, connects an I/O pin on the FPGA to the reset pin of the Ethernet PHY. See the "PHY_RST#" net on the schematic. The PHY is held in reset by a pull-down resistor when a jumper is not installed. Default: Installed, FPGA drives the PHY reset.

JP4 "FL_WP_EN" – Flash Write-protect Enable, install a shunt to protect programmed data in the Flash memory. Default: Open, read/write enabled (unprotected).

JP5 "FLSH_EN" – Flash Enable, connects an I/O pin on the FPGA to the reset pin of the Flash device. See the "FLASH_RST#" net on the schematic. The Flash is held in reset by a pull-down resistor when a jumper is not installed. Default: Installed, FPGA drives the Flash reset.

JP6 "PROM EN" – PROM Enable, connects the DONE pin on the FPGA to the chip enable pin of the PROM(s). The PROM is disabled by a pull-up resistor when a jumper is not installed. Default: Installed, the PROM is enabled when the FPGA is not configured.

JP7 "REV SEL" – Design Revision Select, selects the configuration design when the PROM is programmed with multiple revisions. When no jumpers are installed, the PROM is set for external selection mode with revision 0 selected. Installing jumpers on JP7 will pull the corresponding select pin high, as indicated in Figure 7. Default: Installed across pins 1-2, disables external selection.



JP7 Revision Select	1-2	3-4	5-6
External disabled	1	x	x
Enabled – Rev. 0	0	0	0
Enabled – Rev. 1	0	1	0
Enabled – Rev. 2	0	0	1
Enabled – Rev. 3	0	1	1

Figure 6 - Design Revision Select

JP8 "SER MODE" – Serial Mode Enable, connects the D0 pin of the parallel PROM to the DIN pin of the FPGA. The Virtex-4 FX12 FPGA has a separate pin, DIN, for serial configuration data. When using the parallel PROM in a serial configuration mode, install a shunt on JP8. Default: Open, serial mode is not used.

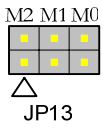
JP9 "PAR MODE" – Parallel Mode Enable, connects the BUSY pin of the parallel PROM to the BUSY pin of the FPGA. The parallel configuration mode uses the BUSY signal of the FPGA for flow-control purposes. When using the ES version of the parallel PROM in a serial configuration mode, do not install a shunt on JP9. Default: Installed, a parallel configuration mode is used to load the demo design on power-up.

JP10 "CMP EN" – Compression Enable, when installed enables the parallel PROM to drive the configuration clock of the FPGA. The PROM must supply CCLK when a compressed configuration file is used. If using the PROM device as the clock source, make sure the jumper settings on JP13 put the FPGA in a Slave configuration mode. Default: Open, the FPGA provides the configuration clock.

JP11 "HSWAP EN" – Enables pull-ups on the Virtex-4 I/O pins during configuration. A pull-down resistor "R111" is used to enable the I/O pull-ups during configuration. Install a jumper to disable the configuration pull-ups. Default: Open; pull-ups enabled.

JP13 – Configuration mode selection. Use to select the configuration mode for the FPGA. With no jumpers installed, these pins are pulled low enabling Master Serial mode. Installing jumpers on JP13 will pull the corresponding mode pin high, as indicated in Figure 7. See the Configuration section of this document or Chapter 3 of the Virtex-4 Platform FPGA Handbook for further information. Default: Installed across pins 3-4 and 5-6; Master SelectMAP mode.

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JP13 Config Mode	1-2 M2	3-4 M1	5-6 M0
Master Serial	0	0	0
Slave Serial	1	1	1
Master SelectMAP	0	1	1
Slave SelectMAP	1	1	0
Boundary Scan	1	0	1

Figure 7 - FPGA Configuration Mode Select

JP14 – JTAG TRST#, forces TRST low. Default: Open, pulled-high.

JP15 – JTAG chain configuration. Selects the JTAG chain configuration. Install a jumper across pins 2-3 for standalone mode. Install jumpers across pins 1-2 and pins 4-5 to add the AvBus connector labeled “P1” (or “J5”) to the standalone chain. These settings are described in detail in the Hardware section of this manual (see section 3.9).
Default: Installed across pins 2-3; standalone chain mode.

Additional flexibility has been designed into the circuit in the form of resistor jumpers “JTx” and series resistors that can be moved or removed to alter the functionality of the board. The purpose of some of these components may be discussed in other sections of this manual others may not be discussed at all. The position of these components should not be altered without careful review of the schematics and associated component data sheets to prevent damage to the board.

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3.0 Hardware

This section of the manual describes the hardware of the Virtex-4 FX12 Evaluation board. The hardware was designed with the Virtex-4 FX12 FPGA as the focal point. The block diagram is shown in Figure 8.

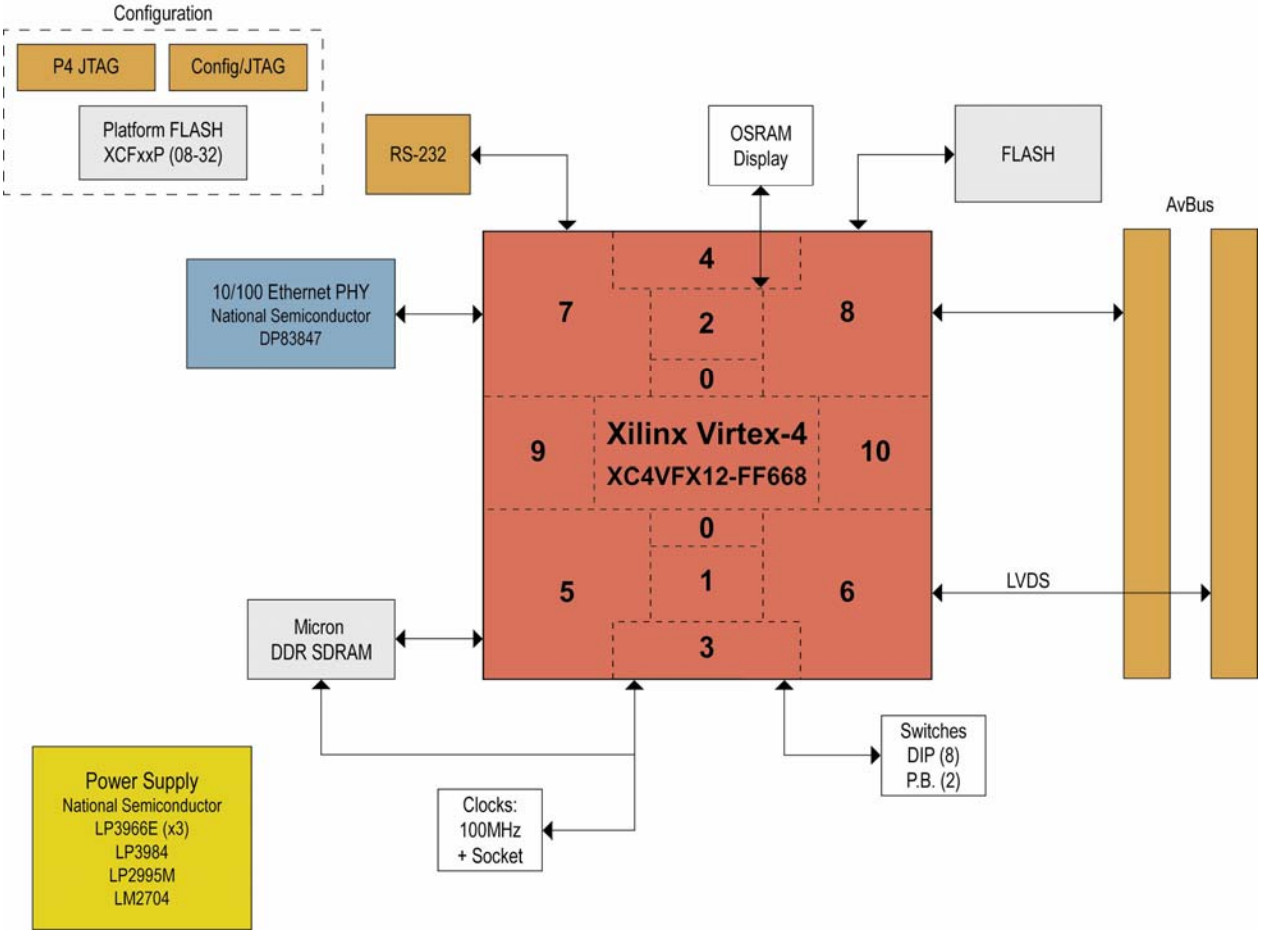


Figure 8 - Virtex-4 FX12 Evaluation Board Block Diagram

3.1 Virtex-4 FX12 FPGA

The Virtex-4 FX12 Evaluation board was designed to support the Virtex-4 FX12 FPGA in the 668-pin, flip-chip BGA package (FF668). The 4VFX1212 device in the FF668 package has a total of 320 I/Os broken into 8 I/O banks (two of the 64-pin I/O banks are not connected to the 4VFX12 die). The Block Diagram in Figure 8 illustrates the location of the I/O banks on the FF668 package. Bank 0 contains all of the dedicated configuration pins. The eight I/O banks consist of four banks of 16 I/O and four banks of 64 I/O. The 4VFX12 device is the only FX12 part that fits in this package.

The smaller 16-pin banks run down the center of the device. Two of these banks, banks 3 and 4, contain the global clock inputs. All four of these center banks, banks 1 through 4, contain the special low input capacitance pins, designated by a trailing "_LC" on the schematic pin name. These pins do not have differential output drivers resulting in the lower capacitance and higher performance. The larger 64-pin banks make up the left and right sides of the device.

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3.2 Clocks

The available clock sources on the Virtex-4 FX12 Evaluation board are shown below.

- Single-ended, 100 MHz Oscillator – FPGA pin "AD11"
- 8-pin DIP Clock Socket – FPGA pin "AD12"

The on-board 100 MHz oscillator is used as the clock source for all of the example designs. The 8-pin DIP clock socket allows the user to supply their oscillator of choice. The socket interface supports 3.3V, single-ended oscillators with the following pin-out.

Signal Name	Socket pin#
Enable	1
GND	4
Output	5
VDD (3.3V)	8

Table 2 - Clock Socket "U11" Pin-out

3.3 Memory

The Virtex-4 FX12 Evaluation board is populated with both high-speed RAM and non-volatile ROM to support various types of applications. The board has 32 Megabytes (MB) of DDR SDRAM and 4 MB of FLASH. If additional memory is necessary for development, the Virtex-4 FX12 Evaluation board supports the Avnet Communications/Memory Module (sold separately). The Memory Module is a daughter board that plugs into the board-to-board connectors on the Virtex-4 FX12 Evaluation Board.

3.3.1 DDR SDRAM

Two Micron DDR SDRAM devices, part number MT46V8M16TG-75, make up the 32-bit data bus. Each device provides 16 MB of memory on a single IC and is organized as 2 Megabits x 16 x 4 banks (128 Megabit). The Virtex-4 FX12 Evaluation Board can support larger devices with addressing support for up to 256 MB (two 1-Gigabit devices). The device has an operating voltage of 2.5V and the interface is JEDEC Standard SSTL_2 (Class I for unidirectional signals, Class II for bidirectional signals). The -75 speed grade supports 7.5 ns cycle times with a 2 ½ clock read latency (DDR266B). The following table provides timing and other information about the Micron device necessary to implement a DDR memory controller.

MT46V8M16TG-75: Timing Parameters	Time (ps) or Number
Load Mode Register time (TMRD)	15000
Write Recovery time (TWR)	15000
Write-to-Read Command Delay (TWTR)	1
Delay between ACT and PRE Commands (TRAS)	40000
Delay after ACT before another ACT (TRC)	65000
Delay after AUTOREFRESH Command (TRFC)	75000
Delay after ACT before READ/WRITE (TRCD)	20000
Delay after ACT before another row ACT (TRRD)	15000
Delay after PRECHARGE Command (TRP)	20000
Refresh Command Interval (TREFC)	140600000
Avg. Refresh Period (TREFI)	15600000
Memory Data Width (DWIDTH) (x2 devices)	32
Row Address Width (AWIDTH)	12
Column Address Width (COL_AWIDTH)	9
Bank Address Width (BANK_AWIDTH)	2
Memory Range (32 MB total)	0x1FFFFFF

Table 3 - DDR SDRAM Timing Parameters

The following guidelines were used in the design of the DDR interface to the Virtex-4 FX12 FPGA. These guidelines were determined based on Micron recommendations and board level simulation.

- Dedicated bus with matched trace lengths (+/- 100 mils)
- Memory clocks routed differentially
- 50 ohm* controlled trace impedance
- Series termination on bidirectional signals at the memory device
- Parallel termination following the memory device connection on all signals

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    - 50 ohm* pull-up resistor to the termination supply (1.25V) on dedicated signals (data, strobe, mask)
    - 100 ohm* pull-up resistor to the termination supply on each branch of shared signals (control, address)
- Termination supply that can both source and sink current
- Feedback clock routed with twice the length to simulate the total flight time

* Ideal impedance values. Actual may vary.

Some of the design considerations were specific to the Virtex-4 architecture. For example, the data strobe signals (DQS) were placed on Clock Capable I/O pins so that the user has the option of using the BUFIO resources to clock read data into the IOB. The appropriate DDR memory signals were placed in the clock regions that correspond to these particular Clock Capable I/O pins.

The DDR signals are connected to I/O Banks 3 and 5 of the Virtex-4 FX12 FPGA. The output supply pins (VCCO) for Banks 3 and 5 are connected to 2.5 Volts. This supply rail can be measured at test point TP4, which can be found in the area between the OLED display and the FPGA. The reference voltage pins (VREF) for Banks 3 and 5 are connected to the reference output of the National LP2995 DDR Termination Linear Regulator. This rail provides the voltage reference necessary for the SSTL_2 I/O standard. The LP2995 regulator also provides the termination supply rail. The termination voltage is 1.25 Volts and can be measured at test point TP6, which can be found next to the DB9 connector labeled "J4".

The following table contains the FPGA pin numbers for the DDR SDRAM interface.

Signal Name	FPGA pin#		Signal Name	FPGA pin#
DDR_A0	C13		DDR_D0	A18
DDR_A1	C12		DDR_D1	B20
DDR_A2	A10		DDR_D2	B18
DDR_A3	B10		DDR_D3	C20
DDR_A4	E26		DDR_D4	C17
DDR_A5	H26		DDR_D5	D20
DDR_A6	G25		DDR_D6	D17
DDR_A7	C24		DDR_D7	E17
DDR_A8	D24		DDR_D8	B24
DDR_A9	A22		DDR_D9	B23
DDR_A10	C14		DDR_D10	B21
DDR_A11	A21		DDR_D11	C21
DDR_A12	A20		DDR_D12	C19
DDR_A13	B17		DDR_D13	E18
			DDR_D14	D18
DDR_BA0	B15		DDR_D15	F18
DDR_BA1	A19			
			DDR_D16	F19
DDR_CS0#	B13		DDR_D17	F20
DDR_CS1#	H25		DDR_D18	E20
			DDR_D19	E22
DDR_WE#	B14		DDR_D20	E23
DDR_RAS#	A15		DDR_D21	C26
DDR_CAS#	A16		DDR_D22	D23
DDR_CLKEN	G17		DDR_D23	C23
DDR_DM0	F17		DDR_D24	H24
DDR_DM1	E21		DDR_D25	H23
DDR_DM2	G19		DDR_D26	H20
DDR_DM3	F26		DDR_D27	G26
			DDR_D28	G24
DDR_DQS0	G18		DDR_D29	G20
DDR_DQS1	A24		DDR_D30	E25
DDR_DQS2	F24		DDR_D31	E24
DDR_DQS3	D26			
			DDR_CLK_FB_O	C15
			DDR_CLK_FB_I	A17

Table 4 - DDR SDRAM FPGA Pin-out

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3.3.2 Flash Memory

Non-volatile data storage is provided in the form of Flash memory. A single Intel StrataFlash® device, part number TE28F320J3C120 or a compatible part from another manufacturer, makes up the 16-bit data bus. This device provides 4 MB of memory on a single IC and is organized as 2Megabits x 16 (32 Megabit). The device has an operating voltage of 3.0V and is compatible with the LVCMOS25 and LVCMOS33 I/O standards of the FPGA. The Flash device is held in a reset state by a pull-down resistor on the active-low RP pin. To use the Flash device, install a jumper on JP5, labeled "FLSH EN" on the board, and drive a logic high level on the "FLASH_RST#" net. The Virtex-4 FX12 Evaluation Board supports the write protection feature of the StrataFlash device. To protect the Flash contents from being overwritten, install a jumper on JP4, labeled "FL WP EN" on the board. The Flash interface is shared with the AvBus connector "P1". This means the FPGA I/O pins that are connected to the Flash device are also connected to AvBus connector "P1". The user should keep this in mind when attempting to use either interface to avoid contention on the bus. The following table provides the FPGA pin numbers for the Flash interface.

Flash Name	Flash Pin#	Signal Name	FPGA pin#		Flash Name	Flash Pin#	Signal Name	FPGA pin#
A0	32	GND	-		D0	33	AV_D0	AB9
A1	28	AV_A0	AB6		D1	35	AV_D1	AC9
A2	27	AV_A1	Y10		D2	38	AV_D2	AE9
A3	26	AV_A2	AA10		D3	40	AV_D3	AD8
A4	25	AV_A3	AB5		D4	44	AV_D4	AC8
A5	24	AV_A4	AC4		D5	46	AV_D5	AC7
A6	23	AV_A5	Y9		D6	49	AV_D6	AB7
A7	22	AV_A6	AA9		D7	51	AV_D7	AC6
A8	20	AV_A7	AB4		D8	34	AV_D8	AE6
A9	19	AV_A8	AC3		D9	36	AV_D9	AF6
A10	18	AV_A9	AF9		D10	39	AV_D10	AC5
A11	17	AV_A10	Y8		D11	41	AV_D11	AD5
A12	13	AV_A11	AB2		D12	45	AV_D12	AF5
A13	12	AV_A12	AC2		D13	47	AV_D13	AD4
A14	11	AV_A13	AA8		D14	50	AV_D14	AE4
A15	10	AV_A14	AF8		D15	52	AV_D15	AF4
A16	8	AV_A15	AD1					
A17	7	AV_A16	AC1		CE0	14	FLASH_CS#	C16
A18	6	AV_A17	AD7		RP#	16	FLASH_RST#	AE14
A19	5	AV_A18	AE7		WE#	55	MEM_WE#	AA14
A20	4	AV_A19	AA7		OE#	54	MEM_OE#	C11
A21	3	AV_A20	AA4					
A22	1	AV_A21	AF7		BYTE#	31	3.xV	-
NC/A23	30	AV_A22	AD6		STS	53	3.xV	-

Table 5 - Flash FPGA Pin-out

3.4 RS-232 Transceiver

The RS-232 transceiver is a 3222 available from Harris/Intersil (ICL3222CA) and Analog Devices (ADM3222). This transceiver is operating at 3.3V for VCC with an internal charge pump to create the RS-232 compatible output levels. This level converter supports two channels. Both channels are connected to the FPGA.

The RS-232 console interface is brought out on the DB9 connector labeled "J4". A straight through serial cable should be used to plug "J4" into a standard PC serial port (male DB9). The following table shows the pin-out for the FPGA and connector interface.

Signal Name	FPGA pin#	Xcvr pin#	DB9 (J4)
Primary channel Transmit (RS232_TX1)	AA26	13	2
Primary channel Receive (RS232_RX1)	AB26	15	3
Secondary channel Transmit (RS232_CTS)	Y26	12	8
Secondary channel Receive (RS232_RTS)	W26	10	7

Table 6 - RS232 FPGA Pin-out

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3.5 10/100 Ethernet

The on-board Ethernet PHY is a National Semiconductor DP83847ALQA56A DsPHYTER® II. The DP83847 is a small, low power physical layer transceiver that only requires a single 3.3V supply. The PHY supports 3.3V signaling levels to the MAC interface, in this case the Virtex-4 FX12 FPGA. The PHY is connected to a Pulse RJ-45 jack with integrated magnetics (part number: J0026D01B). The jack also integrates two LEDs to show Link and Receive Activity. Four more LEDs are provided on the board for status indication. These LEDs indicate Link Speed (D8), Transmit Activity (D7), Collision Detect (D6) and Full Duplex operation (D5). The PHY clock is generated from its own 25 MHz crystal. The PHY address is set to binary "00011". Three-pad resistor jumpers were used to set the operating mode (JT1, JT2 and JT3). An illustration of the resistor jumper footprint is shown below.

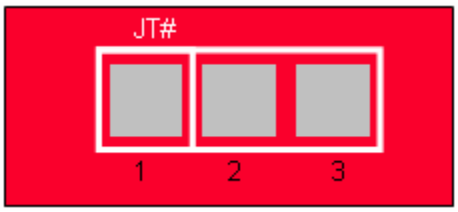


Figure 9 - Resistor Jumper Pin-out

These jumper pads provide the user with the ability to change the operating mode by moving the resistors. By default the PHY is set to auto negotiate a link with a peer. The available modes of operation are shown in the table below.

Operating Modes	JT3	JT2	JT1
10BaseT Half Duplex, Forced Mode	2-3	2-3	2-3
10BaseT Full Duplex, Forced Mode	2-3	2-3	1-2
100Base-TX Half Duplex, Forced Mode	2-3	1-2	2-3
100Base-TX Full Duplex, Forced Mode	2-3	1-2	1-2
10BaseT Half/Full Duplex Advertised, Auto-negotiate	1-2	2-3	2-3
100Base-TX Half/Full Duplex Advertised, Auto-negotiate	1-2	2-3	1-2
10BaseT/100Base-TX Half Duplex Advertised, Auto-negotiate	1-2	1-2	2-3
10BaseT/100Base-TX Half/Full Duplex, Auto-negotiate (Default)	1-2	1-2	1-2

Table 7 - Ethernet PHY Modes

The use of this port requires an Ethernet MAC core to be instantiated in the FPGA project. The Virtex-4 FX12 FPGA has two embedded MAC cores that can be used to implement the Ethernet link. See the "Virtex-4 Embedded Tri-mode Ethernet MAC User Guide" on the Xilinx website for more information: http://direct.xilinx.com/bvdocs/userguides/ug074.pdf. The following table provides the FPGA pin numbers for the Ethernet PHY interface.

Signal Name	FPGA pin#		Signal Name	FPGA pin#
MII_MDC	AA23		MII_CRS	W20
MII_MDIO	AB25		MII_COL	V20
MII_TXD0	V22		MII_RXD0	W25
MII_TXD1	W21		MII_RXD1	W24
MII_TXD2	V21		MII_RXD2	Y24
MII_TXD3	Y21		MII_RXD3	Y25
MII_TXEN	Y22		MII_RXDV	Y23
MII_TXERR	W22		MII_RXERR	W23
MII_TX_CLK	AA24		MII_RXCLK	AC26

Table 8 - Ethernet FPGA Pin-out

3.6 User I/O

Basic user I/O is provided for on the Virtex-4 FX12 Evaluation Board in the form of switches and LED indicators. These peripherals have been added to give the user the ability to monitor and control the execution of a project early in development.

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3.6.1 Push Buttons

Two momentary closure push buttons have been installed on the board and attached to the FPGA. These buttons can be programmed by the user and are ideal for logic reset and similar functions. Pull down resistors hold the signals low (0) until the switch closure pulls it high (1).

Part #	Signal Name	FPGA pin#
SW1	SWITCH_PB1	Y19
SW2	SWITCH_PB2	Y20

Table 9 - Pushbutton FPGA Pin-out

3.6.2 DIP-switch

An eight-position DIP-switch (SPST) has been installed on the board and attached to the FPGA. These switches provide digital inputs to user logic as needed. The signals are pulled low (0) by 10K ohm resistors when the switch is open and tied to 3.3V (1) when the switch is closed (except S1-8, net name SWITCH7, is tied to 2.5V when closed).

Switch #	Signal Name	FPGA pin#
S1-1	SWITCH0	AB24
S1-2	SWITCH1	AB23
S1-3	SWITCH2	AC25
S1-4	SWITCH3	AC24
S1-5	SWITCH4	AD26
S1-6	SWITCH5	AD25
S1-7	SWITCH6	AC23
S1-8	SWITCH7	G10

Table 10 - Dipswitch FPGA Pin-out

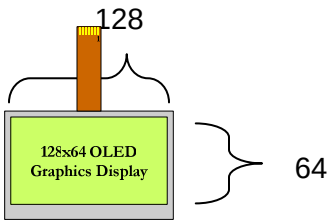
3.6.3 Discrete LEDs

Eight discrete LEDs are installed on the board and can be used to display the status of the internal logic. These LEDs are attached as shown below and are lit by forcing the associated FPGA I/O pin to a logic (1) and are off when the pin is either Low (0) or not driven.

LED #	Signal Name	FPGA pin#
D9	LED0	AE24
D10	LED1	AF24
D11	LED2	AF23
D12	LED3	AF22
D13	LED4	AE21
D14	LED5	AF21
D15	LED6	AE20
D16	LED7	AF20

Table 11 - LED FPGA Pin-out

3.6.4 OLED Graphics Display



4-Bits/Pixel Single Color Graphics Display

The Virtex-4 FX12 Evaluation Board includes a 128x64 OSRAM Pictiva™ OLED (Organic Light Emitting Diode) graphics display. This is a 4-bit per pixel (grayscale) single-color passive matrix display. The display has a contrast ratio of 100:1 and a 160° viewing angle. The Pictiva displays are available in a serial or parallel interface, although applications in this kit use the 8-bit parallel interface.

The parallel bus interface is compatible with 68-series and 80-series microcontrollers and is selectable at pin 4 of the ribbon cable (see pinout below). This will affect the function of several other pins as noted in the table below. The Virtex-4 FX12 Evaluation Board uses a resistor jumper (JT6) to select the desired level of pin 4. By default the

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jumper is placed at pads 1-2 enabling a 68-series interface. This placement is subject to change based on future demo applications.

Display Pin#	Pin Name	I/O	Description
1	CS#	I	Chip Select – Active Low
2	RES#	I	Reset – Active Low
3	BS1	I	Interface Protocol Select. LOW = 68-series HIGH = 80-series
4	D/C#	I	Data / Command HIGH = Bus contains data for DDRAM LOW = Bus contains command
5	R/W# (WR#)	I	Read/Write in 68 series mode Write strobe in 80-series mode
6	E (RD#)	I	E clock in 68-series mode Read strobe in 80-series mode
7	D0	I/O	Data 0
8	D1	I/O	Data 1
9	D2	I/O	Data 2
10	D3	I/O	Data 3
11	D4	I/O	Data 4
12	D5	I/O	Data 5
13	D6	I/O	Data 6
14	D7	I/O	Data 7
15	VSSB	I	n/c
16	VDD	I	Positive supply (2.4V – 3.5V)
17	VCC(VLL)	I	OLED Drive power (12V – 16V)
18	VSS	I	Ground

Table 12 - OLED Display Pin-out

The OLED drive voltage (VLL) must be between 12V and 16V. However, it requires very little operating current. Typical ILL is 20-24mA. So an on-board 12V supply could be used with little affect on the power budget. If there is no 12V supply on board, one may design in a low-cost, low-power 12V source. The Virtex-4 FX12 Board uses a National Semiconductor LM2704 Micropower Step-up DC/DC Converter. This small (SOT23) converter has an input range of 2.2V-7V and an adjustable output up to 20V.

For more display information visit: www.osram-os.com or www.pictiva.com.
For power supply information please see www.national.com.

The following table shows the FPGA pin-out of the OLED interface.

OLED Signal	FPGA pin#
DISP_CSB	AA13
DISP_RSTB	AB13
DISP_RS	AA15
DISP_RD_WRB	-
DISP_ECLK	AA16
DISP_D0	AD13
DISP_D1	AC13
DISP_D2	AC15
DISP_D3	AC16
DISP_D4	AA11
DISP_D5	AA12
DISP_D6	AD14
DISP_D7	AC14

Table 13 - OLED Display FPGA Pin-out

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3.7 I/O Connectors

The Virtex-4 FX12 Evaluation Board is an Avalon compliant motherboard that incorporates board-to-board connectors to support Avalon expansion boards. The connection between the Virtex-4 FX12 Evaluation Board and the Avalon compliant daughter boards is via the Avnet standard AvBus connectors (P1 and P2). The connectors on the topside of the evaluation board (P1 and P2) are the host connectors, AMP part number 179031-6. The host connectors, mate with AMP part number 5-179010-6 on the bottom of AvBus daughter cards. The connectors on the bottom side (J5 and J6) are not installed but could be used to operate as a daughter card as well as a host. When interfacing to other boards care must be taken to tri-state any signals that could interfere with those of the other board. The Virtex-4 FX12 Evaluation Board also has a 50-pin 0.1" header for user access to the FPGA I/O.

3.7.1 AvBus Connectors

The Virtex-4 FX12 FPGA is connected to two mirrored 140-pin board-to-board AvBus standard connectors. This means that each signal connected to P1 is mirrored on the opposite side of the board by the same pin number on J5. Similarly, P2 is mirrored by J6. This allows the evaluation board to serve as either motherboard or expansion board in an Avalon system. While many of the FPGA I/O are directly connected to the AvBus connectors, some of the I/O on the AvBus are also shared with other interfaces. For example, many of the signals on "P1" are shared with the Flash memory. The user must evaluate the potential conflicts when using this interface. This will be addressed in greater detail in the following sections.

AvBus "P1"

The AvBus connector labeled "P1" has some direct connections to the FPGA and some I/O that are shared with the Flash device. The net names of the I/O on "P1" are labeled AV_D(0:31), AV_A(0:31) and AV_CTL(0:23). These signals are connected to I/O banks 1, 2, 4, 7 and 8 of the FPGA. The majority of the signals are connected to banks 7 and 8. Access to the global clock inputs is provided on signals AV_CTL4 and AV_CTL6. This connector also provides access to 21 low-input capacitance pins. The following signals are shared with the Flash interface: AV_A(0:22), AV_D(0:15) and AV_CTL(0,2 & 3). When using these I/O for the AvBus interface only, consider removing the jumper on JP5, "FLASH EN", to prevent the Flash memory from driving AV_D(0:15).

AvBus "P2"

The AvBus connector labeled "P2" is connected to 93 I/O of the Virtex-4 FX12 FPGA. These signals, labeled GEN_IO(0:32), LVDS_N(0:29) and LVDS_P(0:29) are connected to I/O banks 1, 2, 4, 6 and 7 of the FPGA. Note that the signals labeled LVDS are routed as differential pairs. This means that, for example, LVDS_N(0) is tightly coupled with LVDS_P(0). Consequently, any LVDS signal left floating will experience cross-talk from its counterpart signal. This should be taken into account by the user when developing custom expansion cards. All of the LVDS signals are connected to Bank 6, which has a VCCO of 2.5V. Note that the Virtex-4 FPGA only supports the 2.5 Volt version of the LVDS I/O standard. The Virtex-4 FX12 Board does not have resistor pads for differential termination (for LVDS receiver termination). To implement LVDS receivers, enable the on-chip differential termination feature of the Virtex-4 FPGA (UCF syntax: INST "LVDS_RX_net" DIFF_TERM = "TRUE").

Some of the signals labeled "GEN_IO" are also connected to the 50-pin header labeled "J8".

AvBus "J5"

The AvBus connector labeled "J5" is a mirror of "P1". All signals are connected, pin-to-pin with P1. The user is responsible for the purchase and installation of this connector since it is not installed.

AvBus "J6"

The AvBus connector labeled "J6" is a mirror of "P2". All signals are connected, pin-to-pin with P2. The user is responsible for the purchase and installation of this connector since it is not installed.

The tables below show the FPGA connections to these connectors.

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Name	FPGA PIN #	Connector	PIN #	FPGA PIN #	Name
AV_A0	AB6	71	1	-	+5VDC
GND	-	72	2	Y10	AV_A1
AV_A3	AB5	73	3	AA10	AV_A2
AV_A4	AC4	74	4	-	GND
GND	-	75	5	Y9	AV_A5
AV_A7	AB4	76	6	AA9	AV_A6
AV_A8	AC3	77	7	-	GND
+3.3VDC	-	78	8	AF9	AV_A9
AV_A11	AB2	79	9	Y8	AV_A10
AV_A12	AC2	80	10	-	GND
GND	-	81	11	AA8	AV_A13
AV_A15	AD1	82	12	AF8	AV_A14
AV_A16	AC1	83	13	-	+5VDC
GND	-	84	14	AD7	AV_A17
AV_A19	AA7	85	15	AE7	AV_A18
AV_A20	AA4	86	16	-	GND
GND	-	87	17	AF7	AV_A21
AV_A23	Y7	88	18	AD6	AV_A22
AV_A24	Y6	89	19	-	GND
+3.3VDC	-	90	20	Y1	AV_A25
AV_A27	Y3	91	21	Y2	AV_A26
AV_A28	W1	92	22	-	GND
GND	-	93	23	W2	AV_A29
AV_A31	V5	94	24	W3	AV_A30
AV_D0	AB9	95	25	-	+5VDC
GND	-	96	26	AC9	AV_D1
AV_D3	AD8	97	27	AE9	AV_D2
AV_D4	AC8	98	28	-	GND
GND	-	99	29	AC7	AV_D5
AV_D7	AC6	100	30	AB7	AV_D6
AV_D8	AE6	101	31	-	GND
+3.3VDC	-	102	32	AF6	AV_D9
AV_D11	AD5	103	33	AC5	AV_D10
AV_D12	AF5	104	34	-	GND
GND	-	105	35	AD4	AV_D13
AV_D15	AF4	106	36	AE4	AV_D14
AV_D16	AD3	107	37	-	+5VDC
GND	-	108	38	AE3	AV_D17
AV_D19	AD2	109	39	AF3	AV_D18
AV_D20	AB3	110	40	-	GND
GND	-	111	41	AB1	AV_D21
AV_D23	AA1	112	42	AA3	AV_D22
AV_D24	Y5	113	43	-	GND
+3.3VDC	-	114	44	Y4	AV_D25
AV_D27	W4	115	45	W5	AV_D26
AV_D28	W6	116	46	-	GND
GND	-	117	47	W7	AV_D29
AV_D31	V7	118	48	V6	AV_D30
AV_CTL0	C16	119	49	-	+5VDC
GND	-	120	50	AC12	AV_CTL1
AV_CTL3	AA14	121	51	C11	AV_CTL2
AV_CTL4	AC17	122	52	-	GND
GND	-	123	53	AC18	AV_CTL5
AV_CTL7	AB18	124	54	AB17	AV_CTL6
AV_CTL8	D16	125	55	-	GND
+3.3VDC	-	126	56	AA17	AV_CTL9
AV_CTL11	AA18	127	57	Y17	AV_CTL10
AV_CTL12	Y18	128	58	-	GND
GND	-	129	59	D11	AV_CTL13
AV_CTL15	AA19	130	60	D12	AV_CTL14
AV_CTL16	W19	131	61	-	+5VDC
GND	-	132	62	AA20	AV_CTL17
AV_CTL19	AB21	133	63	D13	AV_CTL18
AV_CTL20	AC22	134	64	-	GND
GND	-	135	65	AD22	AV_CTL21
AV_CTL23	F14	136	66	F16	AV_CTL22
AVBUS_TMS	-	137	67	-	GND
+3.3VDC	-	138	68	-	AVBUS_TDO
AVBUS_TDI	-	139	69	-	AVBUS_TCK
JTAG_TRST#	-	140	70	-	GND

Table 14 - AvBus P1/J5 FPGA Pin-out

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Name	FPGA PIN #	Connector		PIN #	FPGA PIN #	Name
GEN_IO0	AD21	71		1	-	+5VDC
GND	-	72		2	F9	LVDS_N0
LVDS_N1	G1	73		3	E9	LVDS_P0
LVDS_P1	G2	74		4	-	GND
GND	-	75		5	AD20	GEN_IO1
LVDS_N2	F3	76		6	AC20	GEN_IO2
LVDS_P2	F4	77		7	-	GND
+3.3VDC	-	78		8	G8	LVDS_N3
LVDS_N4	E2	79		9	F8	LVDS_P3
LVDS_P4	E3	80		10	-	GND
GND	-	81		11	AF19	GEN_IO3
LVDS_N5	D1	82		12	AD19	GEN_IO4
LVDS_P5	D2	83		13	-	+5VDC
GND	-	84		14	G7	LVDS_N6
LVDS_N7	E4	85		15	F7	LVDS_P6
LVDS_P7	D3	86		16	-	GND
GND	-	87		17	H5	LVDS_N8
GEN_IO5	AC19	88		18	H6	LVDS_P8
GEN_IO6	AF18	89		19	-	GND
+3.3VDC	-	90		20	H3	LVDS_N9
LVDS_N10	B4	91		21	H4	LVDS_P9
LVDS_P10	A4	92		22	-	GND
GND	-	93		23	H1	LVDS_N11
LVDS_N12	G3	94		24	H2	LVDS_P11
LVDS_P12	G4	95		25	-	+5VDC
GND	-	96		26	F1	LVDS_N13
GEN_IO7	AE18	97		27	E1	LVDS_P13
GEN_IO8	AD17	98		28	-	GND
GND	-	99		29	AD16	GEN_IO9
GEN_IO11	AF12	100		30	AE13	GEN_IO10
GEN_IO12	AE12	101		31	-	GND
+3.3VDC	-	102		32	E5	LVDS_N14
LVDS_N15	G5	103		33	E6	LVDS_P14
LVDS_P15	G6	104		34	-	GND
GND	-	105		35	AF10	GEN_IO13
GEN_IO15	AE10	106		36	AF11	GEN_IO14
GEN_IO16	AD10	107		37	-	+5VDC
GND	-	108		38	AC10	GEN_IO17
LVDS_N16	C7	109		39	AB10	GEN_IO18
LVDS_P16	B7	110		40	-	GND
GND	-	111		41	C1	LVDS_N17
LVDS_N18	A7	112		42	C2	LVDS_P17
LVDS_P18	A8	113		43	-	GND
+3.3VDC	-	114		44	B3	LVDS_N19
LVDS_N20	H7	115		45	A3	LVDS_P19
LVDS_P20	H8	116		46	-	GND
GND	-	117		47	D4	LVDS_N21
GEN_IO19	AC11	118		48	C4	LVDS_P21
GEN_IO20	AB14	119		49	-	+5VDC
GND	-	120		50	D5	LVDS_N22
LVDS_N23	C8	121		51	C5	LVDS_P22
LVDS_P23	D9	122		52	-	GND
GND	-	123		53	A5	LVDS_N24
LVDS_N25	C10	124		54	A6	LVDS_P24
LVDS_P25	D10	125		55	-	GND
+3.3VDC	-	126		56	D6	LVDS_N26
LVDS_N27	E10	127		57	E7	LVDS_P26
LVDS_P27	F10	128		58	-	GND
GND	-	129		59	D7	LVDS_N28
GEN_IO21	AB20	130		60	D8	LVDS_P28
GEN_IO22	AC21	131		61	-	+5VDC
GND	-	132		62	B9	LVDS_N29
GEN_IO23	AB22	133		63	A9	LVDS_P29
GEN_IO24	AD23	134		64	-	GND
GND	-	135		65	D15	GEN_IO25
GEN_IO27	D14	136		66	F15	GEN_IO26
GEN_IO28	F13	137		67	-	GND
+3.3VDC	-	138		68	E14	GEN_IO29
GEN_IO31	F12	139		69	E13	GEN_IO30
GEN_IO32	F11	140		70	-	GND

Table 15 - AvBus P2/J6 FPGA Pin-out

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3.7.2 0.1" I/O Header

Some of the FPGA I/O on the AvBus connectors are also connected to the 50-pin, 0.1" header labeled "J8". This header provides the user with access to 47 I/O and includes one pin for VCC and two GND pins. The voltage present on pin 47 is selectable to either 3.3V or 5.0V with the jumper resistor labeled "JT7" (default = 3.3V). The following tables show the pin-out for the header.

Signal Name	FPGA pin#	Header Pin#			FPGA pin#	Signal Name
GEN_IO0	AD21	1		2	AD20	GEN_IO1
GEN_IO2	AC20	3		4	AF19	GEN_IO3
GEN_IO4	AD19	5		6	AC19	GEN_IO5
GEN_IO6	AF18	7		8	AE18	GEN_IO7
GEN_IO8	AD17	9		10	AD16	GEN_IO9
GEN_IO10	AE13	11		12	AF12	GEN_IO11
GEN_IO12	AE12	13		14	AF10	GEN_IO13
GEN_IO14	AF11	15		16	AE10	GEN_IO15
GEN_IO16	AD10	17		18	AC10	GEN_IO17
GEN_IO18	AB10	19		20	AC11	GEN_IO19
AV_CTL1	AC12	21		22	AB14	GEN_IO20
AV_CTL3	AA14	23		24	AC17	AV_CTL4
AV_CTL5	AC18	25		26	AB17	AV_CTL6
AV_CTL7	AB18	27		28	AA17	AV_CTL9
AV_CTL10	Y17	29		30	AA18	AV_CTL11
AV_CTL12	Y18	31		32	AA19	AV_CTL15
AV_CTL16	W19	33		34	AB20	GEN_IO21
AV_CTL17	AA20	35		36	AC21	GEN_IO22
AV_CTL19	AB21	37		38	AC22	AV_CTL20
GEN_IO23	AB22	39		40	AD22	AV_CTL21
GEN_IO24	AD23	41		42	F16	AV_CTL22
GEN_IO25	D15	43		44	F15	GEN_IO26
GEN_IO27	D14	45		46	F14	AV_CTL23
VCC	-	47		48	F13	GEN_IO28
GND	-	49		50	-	GND

Table 16 - I/O Header "J8" Pin-out

3.8 Power

The Virtex-4 FX12 Evaluation Board uses a 5V AC/DC adapter (supplied with the kit) with center positive barrel connector. The barrel connector "J1" is shown below in Figure 10. The 5VDC rail is used as the input to two National Semiconductor LP3966-ADJ parts (3 Amp, Low drop-out Regulators), which provide the 2.5V and 3.3V power rails. A third LP3966-ADJ part is used to create the 1.2V FPGA core supply from the 2.5V rail. A National Semiconductor LP3984 provides 1.8V at 150 mA for the Xilinx Platform Flash PROM core supply. Finally, a LM2704 Step-up DC/DC Converter also from National Semiconductor provides the 12V supply for the OLED Display.

IMPORTANT:
Note that there is **no protection for reverse power supply polarity** so take necessary precautions to ensure that the center pin is 4.5V – 5.5V, and the ring is ground!

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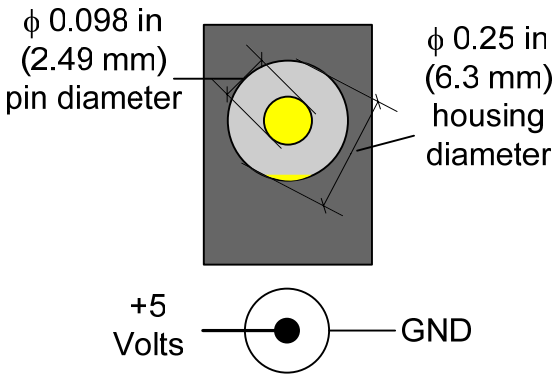


Figure 10 - Barrel Power Connector "J1"

3.9 Configuration

The Virtex-4 FX12 Evaluation Board provides access to the configuration mode pins (JP13), and the boundary-scan and SelectMAP configuration ports (J7). This allows the user to evaluate all of the available configuration modes. See the "Configuration Reference Manual" in the documents folder on the Kit CD for detailed information on how to the use the different configuration modes.

The boundary-scan chain of this board includes the FPGA and the PROM. Additional components attached through the AvBus connector can be included in this chain by setting the appropriate jumpers on the board. The header "JP15" is used to include components from AvBus connector P1 (or J5 if installed). This allows the user to include the boundary-scan devices from an attached daughter-board in the JTAG chain of the Virtex-4 FX12 Evaluation Board. This is convenient for programming all of the boundary-scan devices in a multi-board system from one download cable connection. Review the schematics and the table below for more information.

If the Virtex-4 FX12 Evaluation Board is not the host board and the JTAG chain is driven by an alternate source, place a shunt on pins 8-10 of the header "JP12" to close the chain (or place a jumper wire from J7 pin 9 (TDI) to J7 pin 15 (TDO)).

"JP15" JTAG Chain Selection – Jumper Settings	
Pins 2-3	**Standalone Mode** – Virtex-4 FX12 FPGA and PROM(s)
Pins 1-2 and 4-5	Add AvBus P1/J5 Connector to standalone

Table 17 - JTAG Chain Selection "JP15"

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4.0 Source Code/EDK Projects

This section of the manual describes the source code and example projects included in the kit. The hardware interfaces discussed in the previous section can be implemented very quickly as peripherals in a processor system. Putting the Xilinx MicroBlaze™ soft processor core into the Virtex-4 FX12 FPGA and connecting the hardware interfaces to the peripheral bus of the MicroBlaze processor creates a complete test system. There are several benefits to using MicroBlaze for test purposes. Using a MicroBlaze system provides the user with a debug terminal to easily access control and data registers of multiple hardware interfaces by running very simple C code and using the UART peripheral. Hardware modules that are created with the peripheral bus interface (On-chip Peripheral Bus or OPB) are portable and can easily be re-used in later designs. Xilinx provides a standard set of peripherals for commonly used interfaces so the designer can focus his/her time and energy on the IP that differentiates the design from the competition. This kit includes complete example projects that implement MicroBlaze processor systems, but also includes VHDL source code for the more traditional FPGA designer.

4.1 What is included

Some of the example source code used to validate the hardware interfaces is included. All of the source code was written in VHDL. The MicroBlaze example projects included in the Virtex-4 FX12 Evaluation Kit were created in the Xilinx Embedded Development Kit (EDK) version 6.3. The examples include the Xilinx Platform Studio (XPS) project files and supporting directory structures, all of the required files to run the XPS projects. The user must have both the Xilinx Integrated Software Environment (ISE) version 6.3 and the EDK version 6.3 software installed to utilize the example projects. The following list provides an outline of the Source Code/EDK Projects section. All of the example code/projects are included on the Virtex-4 FX12 Evaluation Kit CD.

— Source Code
  > OLED Display Example
— XPS Example Projects
  > Base System Builder
  > Custom Peripheral Project

4.2 Source Code: OLED Display Example

The OLED Display code implements a parallel interface to the OLED segment driver/controller device on the OSRAM Pictiva display. The OLED Display code consists of two source files: “pictiva_128x64_module.vhd” and “opb_pictiva_128x64.vhd”. The “pictiva_128x64_module.vhd” source provides the low-level interface to the display controller and contains the state machine to write commands and transfer data to the display interface. This module provides a register interface for user access. The registers are accessible by a generic memory bus interface with the following memory map.

Register	Address	Type	Description
Revision	0x0000	RO	Source code revision register
Status	0x0004	RO	Display status
General Purpose	0x0008	R/W	General purpose register
Data	0x000C	R/W	Display data

Table 18 - OLED Memory Map

The following tables provide descriptions of the user registers. The General Purpose register is not tied to any logic. It is just a placeholder in the memory map for expansion purposes.

Bits	Name	Description	Reset Value
31:0	Revision	Source code revision	0x00000004

Table 19 - OLED Revision Register - 0x0

Bits	Name	Description	Reset Value
31	Write_disp_busy	Indicates a write in progress	0
30:0	Unused	Not used	0x00000000

Table 20 - OLED Status Register – 0x4

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Bits	Name	Description	Reset Value
31:9	Unused	Not Used	0x000000
8	Unused	Not Used	0
7:0	Display_data	Command/display data	0x03

Table 21 - OLED Data Register – 0xC

This example code simply provides the hardware interface to the display controller by implementing the necessary timing and protocol to transfer data to the display driver/controller. The burden is on the user to send this module the proper commands to initialize the display controller and write data to the graphical data memory.

The remaining source file "opb_pictiva_128x64.vhd" is an optional wrapper file that provides the address translation and handshaking signals to make the OLED design into an On-chip Peripheral Bus (OPB) peripheral for use with the MicroBlaze soft processor. This file is not necessary if the MicroBlaze processor is not being used. To see an example of the OLED Display code running on the Virtex-4 FX12 Evaluation Board, download the "display_test.bit" file to the FPGA. This bit file is from the Custom Peripheral Project discussed below. To write commands to the display over the RS232 interface, connect a straight-through serial cable from a PC to the DB9 connector J4 and open a terminal session for 19200-8-N-1-N. At the prompt, use the "Dump mem region" (mrd) and "Write mem location" (mwr) commands (type 'help' for instructions) to address 0x81040000 to read/write the user registers of the OLED code. Please note that if a static image is displayed on the OSRAM Pictiva for several days it is possible to permanently burn an image onto the display.

4.3 XPS Project: Base System Builder

Base System Builder (BSB) is a graphical wizard in Platform Studio that allows the user to quickly develop a complete MicroBlaze system for supported evaluation boards. The wizard lets the user define the system from an overview perspective and then automatically generates the necessary low-level, tool-specific files that make up the system. BSB even generates a simple application to test some of the peripherals on the evaluation board.

Specifically, BSB creates the microprocessor hardware specification (MHS), software specification (MSS), board-specific pin location constraints (UCF) and boundary-scan information (download.cmd). The C code generated for the test application is dependent on the peripherals selected by the user in the wizard.

The default installation of the Embedded Development Kit (EDK) only includes Xilinx evaluation boards. However, a CD containing the Xilinx Board Definition (XBD) files for Avnet evaluation boards is provided with the EDK software package. The Virtex-4 FX12 Evaluation Board XBD file should be included on the CD in the EDK 7.1 package, but it is also on the CD provided with the Avnet Virtex-4 FX12 Evaluation Kit. To install the Virtex-4 FX12 Evaluation Board XBD file, create the following folder structure under the install path of the EDK software and copy the "Avnet_V4FX12_Evl" folders from the kit CD into the "\EDK\board\Avnet\boards" folder as shown below.

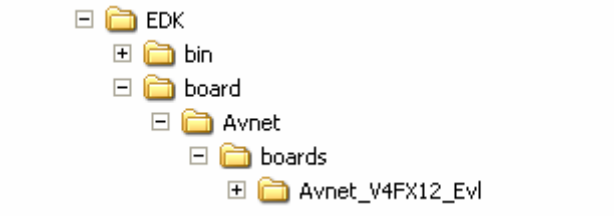


Figure 11 - XBD Install Path

The folder names and structure shown in Figure 14 must be used in order for Platform Studio to detect the XBD file for the Virtex-4 FX12 Evaluation Board.

To use the Base System Builder wizard, re-open Platform Studio and select the "Base System Builder Wizard" option from the start-up window or open it from the File menu by selecting "New Project -> Base System Builder." After browsing to a location to save the project, choose the "I would like to create a new design" option. Next select the target evaluation board by setting the Board Vendor to "Avnet" and choosing "Virtex-4 FX12 Evaluation Board" from the Board Name menu. If Avnet or the board name does not appear in the drop-down menus, the XBD file wasn't detected. Check to make sure your folder names match Figure 14 and close/re-open Platform Studio. After selecting the Virtex-4 FX12 Board, BSB will guide the user to select the available peripherals and generate an embedded-processor system. See the "Platform Studio User's Guide" (ps_ug.pdf) in the \EDK\doc folder for more information.

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4.4 XPS Project: Custom Peripheral Project

This project makes use of a custom OPB peripheral designed by Avnet Electronics Marketing to enable the MicroBlaze processor to access the OSRAM Pictiva Display interface on the Virtex-4 FX12 Evaluation board. The optional OPB wrapper code was applied to the source code discussed in the previous sections to add an OPB interface to the user registers of the design. When combined with the required peripheral definition files (MPD, PAO, BBD), the design becomes an OPB peripheral. See the "Embedded System Tools Reference Manual" (est_rm.pdf) in the \EDK\doc folder for more information about creating peripherals. The custom peripheral that is being used can be found in the "pcores" folder of this project. The memory-map for all of the peripherals in this project, both custom and standard, is shown below.

Processor Bus	Peripheral	Address Location
PLB	BRAM Controller	0xFFFF8000 – 0xFFFFFFFF
	DDR (SDRAM)	0x00000000 – 0x01FFFFFF
OPB	EMC (Flash)	0x21000000 – 0x217FFFFF
	GPIO (LEDs)	0x40000000 – 0x4000FFFF
	GPIO (DIP_Switches)	0x40020000 – 0x4002FFFF
	UART (lite)	0x40600000 – 0x4060FFFF
	Pictiva_128x64*	0x60000000 – 0x60003FFF

Table 22 - Custom Peripheral Project Memory-Map

To use the Custom Peripheral design, download the "custom_periphal.bit" file to the FPGA and connect the board to a PC via a serial cable. Open a terminal session (19200-8-N-1-N) and type 'help' <enter> at the prompt to see a list of commands. The "Custom Peripheral Project" document in the Custom Peripheral Project directory discusses the memory map and use of the custom peripherals in greater detail.

5.0 List of partners

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