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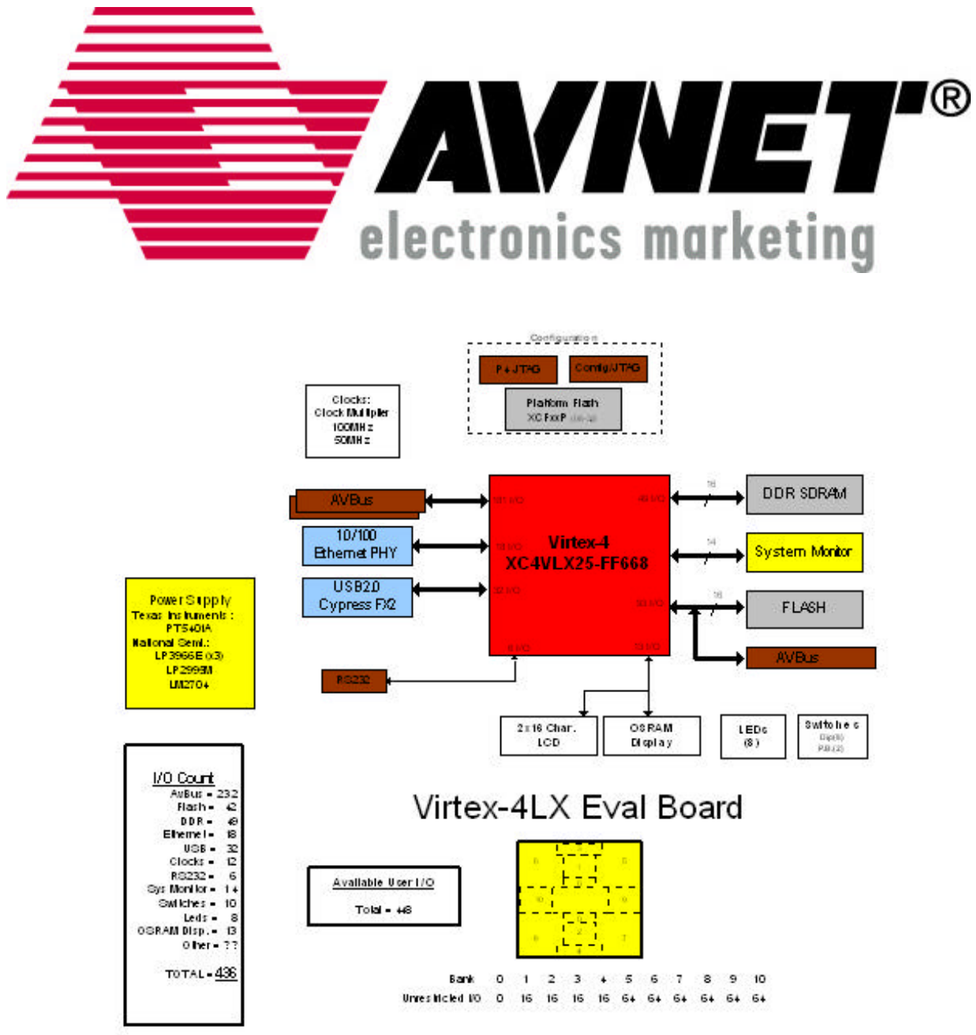
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Title: Xilinx Virtex-4 LX Evaluation Board — Cover Sheet

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3,15,16 AV_CTL[0:23]

3,15,16 AV_D[0:31]

AV_D29
AV_D30
AV_D31

AV_CTL0
AV_CTL2
AV_CTL4
AV_CTL6
AV_CTL8
AV_CTL9
AV_CTL10
AV_CTL11
AV_CTL12
AV_CTL13
AV_CTL14
AV_CTL15
AV_CTL16
AV_CTL17
AV_CTL18
AV_CTL19

3,4,5,17 AV_SEC_IO[0:50]

11,18 D[0:7]

D0
D1
D2
D3
D4
D5
D6
D7

AV_SEC_IO31
AV_SEC_IO32
AV_SEC_IO35
AV_SEC_IO36
AV_SEC_IO37
AV_SEC_IO38
AV_SEC_IO39
AV_SEC_IO40
AV_SEC_IO41
AV_SEC_IO42
AV_SEC_IO43
AV_SEC_IO44
AV_SEC_IO45
AV_SEC_IO46
AV_SEC_IO47
AV_SEC_IO48
AV_SEC_IO49
AV_SEC_IO50

SelectMAP Configuration Data[7:0]:
- After configuration, used for USB interface
- Configuration sources:
  - PROM when enabled with a jumper
  - Download over USB using Configuration Utility

U1B

AV_CTL13	F14	IO_L1P_D31_LC_1	Bank1	AA14	IO_L1P_D15_CC_LC_2	AV_SEC_IO49	
AV_CTL8	F13	IO_L1N_D30_LC_1	Bank1	AB14	IO_L1N_D14_CC_LC_2	AV_SEC_IO50	
AV_CTL2	F12	IO_L2P_D29_LC_1	Bank1	AC12	IO_L2P_D13_LC_2	AV_SEC_IO39	
AV_CTL0	F11	IO_L2N_D28_LC_1	Bank1	AC11	IO_L2N_D12_LC_2	AV_SEC_IO44	
AV_CTL18	F16	IO_L3P_D27_LC_1	Bank1	AA16	IO_L3P_D11_LC_2	AV_SEC_IO42	
AV_CTL14	F15	IO_L3N_D26_LC_1	Bank1	AA15	IO_L3N_D10_LC_2	AV_SEC_IO46	
AV_CTL10	D14	IO_L4P_D25_LC_1	Bank1	AB13	IO_L4P_D9_LC_2	AV_SEC_IO35	
AV_CTL6	D13	IO_L4N_D24_VREF_LC_1	Bank1	AA13	IO_L4N_D8_VREF_LC_2	AV_SEC_IO32	
AV_CTL16	D15	IO_L5P_D23_LC_1	Bank1	AC14	IO_L5P_D7_LC_2	D7	USB_FD7 11,18
AV_CTL12	E14	IO_L5N_D22_LC_1	Bank1	AD14	IO_L5N_D6_LC_2	D6	USB_FD6 11,18
AV_D31	C11	IO_L6P_D21_LC_1	Bank1	AA12	IO_L6P_D5_LC_2	D5	USB_FD5 11,18
AV_D30	D11	IO_L6N_D20_LC_1	Bank1	AA11	IO_L6N_D4_LC_2	D4	USB_FD4 11,18
AV_CTL19	D16	IO_L7P_D19_LC_1	Bank1	AC16	IO_L7P_D3_LC_2	D3	USB_FD3 11,18
AV_CTL17	C16	IO_L7N_D18_LC_1	Bank1	AC15	IO_L7N_D2_LC_2	D2	USB_FD2 11,18
AV_CTL9	E13	IO_L8P_D17_CC_LC_1	Bank1	AC13	IO_L8P_D1_LC_2	D1	USB_FD1 11,18
AV_CTL4	D12	IO_L8N_D16_CC_LC_1	Bank1	AD13	IO_L8N_D0_LC_2	D0	USB_FD0 11,18
AV_CTL15	B15	IO_L1P_GC_CC_LC_3	Bank2	AE12	IO_L1P_GC_LC_4		RST# 11
AV_CTL11	B14	IO_L1N_GC_CC_LC_3	Bank2	AE12	IO_L1N_GC_LC_4	AV_SEC_IO40	
AV_CTL3	A12	IO_L2P_GC_VRN_LC_3	Bank2	AC10	IO_L2P_GC_LC_4		USB_INT1# 11
AV_D29	A11	IO_L2N_GC_VRP_LC_3	Bank2	AB10	IO_L2N_GC_LC_4		DDR_CLK_FB 5
13 CLK_PLL	C15	IO_L3P_GC_LC_3	Bank2	AB17	IO_L3P_GC_LC_4	AV_SEC_IO37	
13 CLK_PLL#	C14	IO_L3N_GC_LC_3	Bank2	AC17	IO_L3N_GC_LC_4	AV_SEC_IO38	
13 PLL_P2	B13	IO_L4P_GC_LC_3	Bank2	AE11	IO_L4P_GC_LC_4	AV_SEC_IO43	
13 PLL_P1	B12	IO_L4N_GC_VREF_LC_3	Bank2	AE10	IO_L4N_GC_VREF_LC_4	AV_SEC_IO47	
13 PLL_P0	A16	IO_L5P_GC_LC_3	Bank2	AE14	IO_L5P_GC_LC_4	AV_SEC_IO31	
13 PLL_MULT1	A15	IO_L5N_GC_LC_3	Bank2	AE13	IO_L5N_GC_LC_4	AV_SEC_IO36	
13 PLL_MULT0	A10	IO_L6P_GC_LC_3	Bank2	AE10	IO_L6P_GC_LC_4	AV_SEC_IO48	
13 PLL_STOP#	B10	IO_L6N_GC_LC_3	Bank2	AD10	IO_L6N_GC_LC_4		USB_INT0# 11
13 CLK_PLL_REF	B17	IO_L7P_GC_LC_3	Bank2	AD17	IO_L7P_GC_VRN_LC_4	AV_SEC_IO41	
13 PLL_DLYCTRL	A17	IO_L7N_GC_LC_3	Bank2	AD16	IO_L7N_GC_VRP_LC_4	AV_SEC_IO45	
13 CLK_100MHz	C13	IO_L8P_GC_LC_3	Bank3	AD12	IO_L8P_GC_CC_LC_4		USB_CLKOUT 11
13 PLL_LEADLAG	C12	IO_L8N_GC_LC_3	Bank3	AD11	IO_L8N_GC_CC_LC_4		USB_IFCLK 11

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Title	Xilinx Virtex4 LX Evaluation Board	FPGA Banks 1-4	
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15,16 GEN_IO[0:32]

2,15,16 AV_CTL[0:23]

AV_CTL1
AV_CTL5
AV_CTL7
AV_CTL20
AV_CTL21
AV_CTL22
AV_CTL23

GEN_IO0
GEN_IO1
GEN_IO2
GEN_IO3
GEN_IO4
GEN_IO5
GEN_IO6
GEN_IO7
GEN_IO8
GEN_IO9
GEN_IO10
GEN_IO11
GEN_IO12
GEN_IO13
GEN_IO14
GEN_IO15
GEN_IO16
GEN_IO17
GEN_IO18
GEN_IO19
GEN_IO20
GEN_IO21
GEN_IO22
GEN_IO23
GEN_IO24
GEN_IO25
GEN_IO26
GEN_IO27
GEN_IO28
GEN_IO29
GEN_IO30
GEN_IO31
GEN_IO32

2,4,5,17 AV_SEC_IO[0:50]

AV_SEC_IO0

5,14 SWITCH[0:7]

SWITCH7

5,15,16 LVDS_P[0:29]

5,15,16 LVDS_N[0:29]

LVDS_N0
LVDS_N1
LVDS_N2
LVDS_N3
LVDS_N4
LVDS_N5
LVDS_N6
LVDS_N8
LVDS_N9
LVDS_N11
LVDS_N13

LVDS_P0
LVDS_P1
LVDS_P2
LVDS_P3
LVDS_P4
LVDS_P5
LVDS_P6
LVDS_P8
LVDS_P9
LVDS_P11
LVDS_P13

For LVDS receive pairs,
install 100 ohm.

LVDS_N0	DNI	R3	LVDS_P0
LVDS_N1	DNI	R4	LVDS_P1
LVDS_N2	DNI	R5	LVDS_P2
LVDS_N3	DNI	R6	LVDS_P3
LVDS_N4	DNI	R7	LVDS_P4
LVDS_N5	DNI	R8	LVDS_P5
LVDS_N6	DNI	R9	LVDS_P6
LVDS_N8	DNI	R11	LVDS_P8
LVDS_N9	DNI	R12	LVDS_P9
LVDS_N11	DNI	R14	LVDS_P11
LVDS_N13	DNI	R16	LVDS_P13

U1C

AV_CTL20	C17	IO_L1P_5	Bank5
AV_CTL21	D17	IO_L1N_5	
GEN_IO18	C20	IO_L2P_5	
GEN_IO17	B20	IO_L2N_5	
AV_CTL22	B18	IO_L3P_5	
AV_CTL23	A18	IO_L3N_5	
GEN_IO14	D20	IO_L4P_5	
GEN_IO29	D19	IO_L4N_VREF_5	
GEN_IO31	E17	IO_L5P_5	
GEN_IO32	F17	IO_L5N_5	
GEN_IO9	C21	IO_L6P_5	
GEN_IO10	B21	IO_L6N_5	
GEN_IO26	C19	IO_L7P_5	
GEN_IO30	D18	IO_L7N_5	
GEN_IO0	A24	IO_L8P_CC_LC_5	
GEN_IO6	A23	IO_L8N_CC_LC_5	
GEN_IO23	G18	IO_L9P_CC_LC_5	
GEN_IO28	G17	IO_L9N_CC_LC_5	
GEN_IO1	B24	IO_L10P_5	
GEN_IO2	B23	IO_L10N_5	
GEN_IO24	E18	IO_L11P_5	
GEN_IO27	E18	IO_L11N_5	
GEN_IO11	F21	IO_L12P_5	
GEN_IO12	D21	IO_L12N_VREF_5	
GEN_IO20	A20	IO_L13P_5	
GEN_IO25	A19	IO_L13N_5	
GEN_IO3	D22	IO_L14P_5	
GEN_IO4	C22	IO_L14N_5	
GEN_IO8	A22	IO_L15P_5	
GEN_IO15	A21	IO_L15N_5	
LVDS_P6	D24	IO_L16P_5	
LVDS_N6	C24	IO_L16N_5	
GEN_IO21	G19	IO_L17P_5	
GEN_IO22	F19	IO_L17N_5	
LVDS_P1	E23	IO_L18P_5	
LVDS_N1	E22	IO_L18N_5	
GEN_IO19	F20	IO_L19P_5	
GEN_IO13	E20	IO_L19N_5	
LVDS_P3	C26	IO_L20P_5	
LVDS_N3	C25	IO_L20N_VREF_5	
LVDS_P0	D23	IO_L21P_5	
LVDS_N0	C23	IO_L21N_5	
SWITCH7	H20	IO_L22P_5	
GEN_IO16	G20	IO_L22N_5	
LVDS_P2	G22	IO_L23P_VRN_5	
LVDS_N2	G21	IO_L23N_VRP_5	
AV_SEC_IO3	E24	IO_L24P_CC_LC_5	
AV_SEC_IO0	F23	IO_L24N_CC_LC_5	
GEN_IO5	D26	IO_L25P_CC_LC_5	
GEN_IO7	D25	IO_L25N_CC_LC_5	
AV_SEC_IO4	H22	IO_L26P_5	
AV_SEC_IO29	H21	IO_L26N_5	
LVDS_P8	E25	IO_L27P_5	
LVDS_N8	E24	IO_L27N_5	
LVDS_P4	G24	IO_L28P_5	
LVDS_N4	G23	IO_L28N_VREF_5	
LVDS_P9	F26	IO_L29P_5	
LVDS_N9	E26	IO_L29N_5	
LVDS_P5	H24	IO_L30P_5	
LVDS_N5	H23	IO_L30N_5	
LVDS_P11	G26	IO_L31P_5	
LVDS_N11	G25	IO_L31N_5	
LVDS_P13	H26	IO_L32P_5	
LVDS_N13	H25	IO_L32N_5	Bank5

Bank6

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IO_L1P_6	D10	AV_D27	
IO_L1N_6	C10	AV_D25	
IO_L2P_6	D9	AV_D24	
IO_L2N_6	C8	AV_D16	
IO_L3P_6	A8	AV_D14	
IO_L3N_6	A7	AV_D9	
IO_L4P_6	D8	AV_D19	
IO_L4N_VREF_6	D7	AV_D12	
IO_L5P_6	E10	AV_D28	
IO_L5N_6	E10	AV_D26	
IO_L6P_6	A6	AV_D7	
IO_L6N_6	A5	AV_D3	
IO_L7P_6	E9	AV_D21	
IO_L7N_6	F9	AV_D22	
IO_L8P_CC_LC_6	B6	AV_D8	
IO_L8N_CC_LC_6	C6	AV_D11	
IO_L9P_CC_LC_6	G10	AV_CTL7	
IO_L9N_CC_LC_6	G9	AV_CTL5	
IO_L10P_6	F8	AV_D18	
IO_L10N_6	G8	AV_CTL1	
IO_L11P_6	B7	AV_D10	
IO_L11N_6	C7	AV_D13	
IO_L12P_6	C5	AV_D4	
IO_L12N_VREF_6	D5	AV_D1	
IO_L13P_6	A9	AV_D20	
IO_L13N_6	B9	AV_D23	
IO_L14P_6	A3	AV_A26	
IO_L14N_6	B3	AV_A27	
IO_L15P_6	A4	AV_A31	
IO_L15N_6	B4	AV_D0	
IO_L16P_6	C4	AV_A29	
IO_L16N_6	D4	AV_A30	
IO_L17P_6	E7	AV_D15	
IO_L17N_6	D6	AV_D5	
IO_L18P_6	E6	AV_D6	
IO_L18N_6	E5	AV_D2	
IO_L19P_6	E7	AV_D17	
IO_L19N_6	G7	AV_A16	
IO_L20P_6	C2	AV_A22	
IO_L20N_VREF_6	C1	AV_A20	
IO_L21P_6	H8	AV_A0	
IO_L21N_6	H7	AV_A3	
IO_L22P_6	D3	AV_A25	
IO_L22N_6	E4	AV_A28	
IO_L23P_VRN_6	G6	AV_A15	
IO_L23N_VRP_6	G5	AV_A10	
IO_L24P_CC_LC_6	E3	AV_A19	
IO_L24N_CC_LC_6	E2	AV_A21	
IO_L25P_CC_LC_6	D2	AV_A24	
IO_L25N_CC_LC_6	D1	AV_A23	
IO_L26P_6	E1	AV_A18	
IO_L26N_6	F1	AV_A13	
IO_L27P_6	F4	AV_A17	
IO_L27N_6	F3	AV_A14	
IO_L28P_6	G4	AV_A9	
IO_L28N_VREF_6	G3	AV_A12	
IO_L29P_6	H6	AV_A1	
IO_L29N_6	H5	AV_A2	
IO_L30P_6	G2	AV_A11	
IO_L30N_6	G1	AV_A8	
IO_L31P_6	H4	AV_A6	
IO_L31N_6	H3	AV_A5	
IO_L32P_6	H2	AV_A7	
IO_L32N_6	H1	AV_A4	

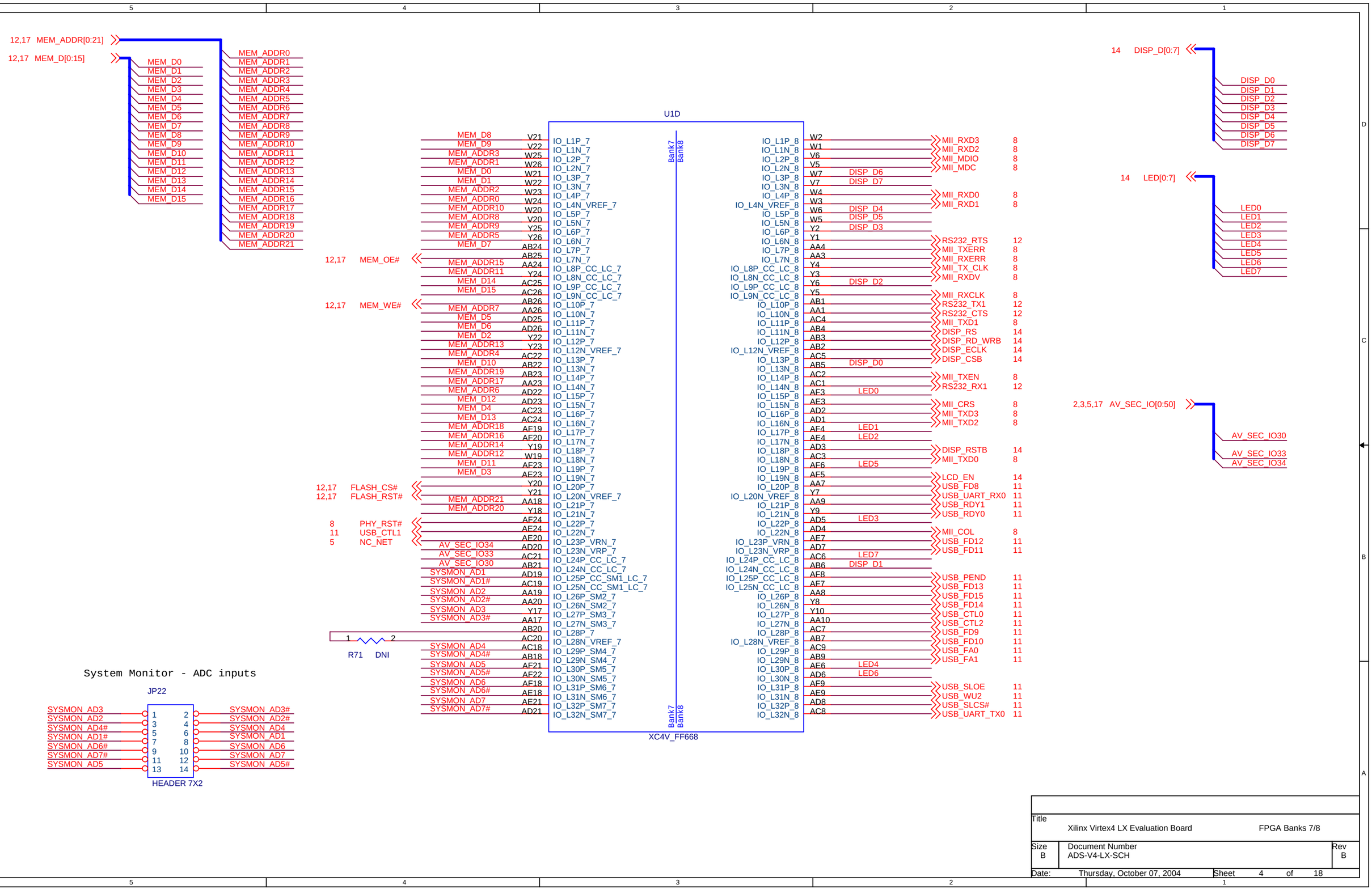
2,15,16 AV_D[0:31]

15,16 AV_A[0:31]

AV_A0
AV_A1
AV_A2
AV_A3
AV_A4
AV_A5
AV_A6
AV_A7
AV_A8
AV_A9
AV_A10
AV_A11
AV_A12
AV_A13
AV_A14
AV_A15
AV_A16
AV_A17
AV_A18
AV_A19
AV_A20
AV_A21
AV_A22
AV_A23
AV_A24
AV_A25
AV_A26
AV_A27
AV_A28
AV_A29
AV_A30
AV_A31

AV_D0
AV_D1
AV_D2
AV_D3
AV_D4
AV_D5
AV_D6
AV_D7
AV_D8
AV_D9
AV_D10
AV_D11
AV_D12
AV_D13
AV_D14
AV_D15
AV_D16
AV_D17
AV_D18
AV_D19
AV_D20
AV_D21
AV_D22
AV_D23
AV_D24
AV_D25
AV_D26
AV_D27
AV_D28

Title	Xilinx Virtex4 LX Evaluation Board	FPGA Banks 5/6	
Size B	Document Number ADS-V4-LX-SCH		Rev B
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12,17 MEM_ADDR[0:21]
12,17 MEM_D[0:15]
MEM_D0
MEM_D1
MEM_D2
MEM_D3
MEM_D4
MEM_D5
MEM_D6
MEM_D7
MEM_D8
MEM_D9
MEM_D10
MEM_D11
MEM_D12
MEM_D13
MEM_D14
MEM_D15
MEM_ADDR0
MEM_ADDR1
MEM_ADDR2
MEM_ADDR3
MEM_ADDR4
MEM_ADDR5
MEM_ADDR6
MEM_ADDR7
MEM_ADDR8
MEM_ADDR9
MEM_ADDR10
MEM_ADDR11
MEM_ADDR12
MEM_ADDR13
MEM_ADDR14
MEM_ADDR15
MEM_ADDR16
MEM_ADDR17
MEM_ADDR18
MEM_ADDR19
MEM_ADDR20
MEM_ADDR21
U1D
Bank7
Bank8
XC4V_FF668
12,17 MEM_OE#
12,17 MEM_WE#
12,17 FLASH_CS#
12,17 FLASH_RST#
8 PHY_RST#
11 USB_CTL1
5 NC_NET
R71 DNI
14 DISP_D[0:7]
DISP_D0
DISP_D1
DISP_D2
DISP_D3
DISP_D4
DISP_D5
DISP_D6
DISP_D7
14 LED[0:7]
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
2,3,5,17 AV_SEC_IO[0:50]
AV_SEC_IO30
AV_SEC_IO33
AV_SEC_IO34
MII_RXD3 8
MII_RXD2 8
MII_MDIO 8
MII_MDC 8
MII_RXD0 8
MII_RXD1 8
RS232_RTS 12
MII_TXERR 8
MII_RXERR 8
MII_TX_CLK 8
MII_RXDV 8
MII_RXCLK 8
RS232_TX1 12
RS232_CTS 12
MII_TXD1 8
DISP_RS 14
DISP_RD_WRB 14
DISP_ECLK 14
DISP_CSB 14
MII_TXEN 8
RS232_RX1 12
MII_CRS 8
MII_TXD3 8
MII_TXD2 8
DISP_RSTB 14
MII_TXD0 8
LCD_EN 14
USB_FD8 11
USB_UART_RX0 11
USB_RDY1 11
USB_RDY0 11
MII_COL 8
USB_FD12 11
USB_FD11 11
USB_PEND 11
USB_FD13 11
USB_FD15 11
USB_FD14 11
USB_CTL0 11
USB_CTL2 11
USB_FD9 11
USB_FD10 11
USB_FA0 11
USB_FA1 11
USB_SLOE 11
USB_WU2 11
USB_SLCS# 11
USB_UART_TX0 11
System Monitor - ADC inputs
JP22
SYSMON_AD3
SYSMON_AD2
SYSMON_AD4#
SYSMON_AD1#
SYSMON_AD6#
SYSMON_AD7#
SYSMON_AD5
SYSMON_AD3#
SYSMON_AD2#
SYSMON_AD4
SYSMON_AD1
SYSMON_AD6
SYSMON_AD7
SYSMON_AD5#
HEADER 7X2
Title
Xilinx Virtex4 LX Evaluation Board
FPGA Banks 7/8
Size B
Document Number ADS-V4-LX-SCH
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3,15,16 GEN_IO[0:32]

2,3,4,17 AV_SEC_IO[0:50]

AV_SEC_IO1
AV_SEC_IO2
AV_SEC_IO5
AV_SEC_IO6
AV_SEC_IO7
AV_SEC_IO8
AV_SEC_IO9
AV_SEC_IO10
AV_SEC_IO11
AV_SEC_IO12
AV_SEC_IO13
AV_SEC_IO14
AV_SEC_IO15
AV_SEC_IO16
AV_SEC_IO17
AV_SEC_IO18
AV_SEC_IO19
AV_SEC_IO20
AV_SEC_IO21
AV_SEC_IO22
AV_SEC_IO23
AV_SEC_IO24
AV_SEC_IO25
AV_SEC_IO26
AV_SEC_IO27
AV_SEC_IO28

GEN_IO30
GEN_IO31
GEN_IO32

3,15,16 LVDS_P[0:29]

3,15,16 LVDS_N[0:29]

LVDS_N7
LVDS_N10
LVDS_N12
LVDS_N15
LVDS_N16
LVDS_N17
LVDS_N18
LVDS_N19
LVDS_N20
LVDS_N21
LVDS_N22
LVDS_N23
LVDS_N24
LVDS_N25
LVDS_N26
LVDS_N27
LVDS_N28
LVDS_N29

LVDS_P7
LVDS_P10
LVDS_P12
LVDS_P15
LVDS_P16
LVDS_P17
LVDS_P18
LVDS_P19
LVDS_P20
LVDS_P21
LVDS_P22
LVDS_P23
LVDS_P24
LVDS_P25
LVDS_P26
LVDS_P27
LVDS_P28
LVDS_P29

For LVDS receive pairs,
install 100 ohm.

LVDS_N7	DNI	R10	LVDS_P7
LVDS_N10	DNI	R13	LVDS_P10
LVDS_N12	DNI	R15	LVDS_P12
LVDS_N14			LVDS_P14
LVDS_N15	DNI	R17	LVDS_P15
LVDS_N16	DNI	R18	LVDS_P16
LVDS_N17	DNI	R19	LVDS_P17
LVDS_N18	DNI	R20	LVDS_P18
LVDS_N19	DNI	R21	LVDS_P19
LVDS_N20	DNI	R22	LVDS_P20
LVDS_N21	DNI	R23	LVDS_P21
LVDS_N22	DNI	R24	LVDS_P22
LVDS_N23	DNI	R25	LVDS_P23
LVDS_N24	DNI	R26	LVDS_P24
LVDS_N25	DNI	R27	LVDS_P25
LVDS_N26	DNI	R28	LVDS_P26
LVDS_N27	DNI	R29	LVDS_P27
LVDS_N28	DNI	R30	LVDS_P28
LVDS_N29	DNI	R31	LVDS_P29
	DNI	R32	

Place close to FPGA

U1E

AV_SEC_IO7	J21	IO_L1P_9	Bank9	IO_L1P_10	J7
AV_SEC_IO25	J20	IO_L1N_9		IO_L1N_10	J6
LVDS_P7	J23	IO_L2P_9		IO_L2P_10	J5
LVDS_N7	J22	IO_L2N_9		IO_L2N_10	J4
LVDS_P17	K22	IO_L3P_9		IO_L3P_10	K7
LVDS_N17	K21	IO_L3N_9		IO_L3N_10	K6
LVDS_P14	J26	IO_L4P_9		IO_L4P_10	J2
LVDS_N14	J25	IO_L4N_VREF_9		IO_L4N_VREF_10	J1
AV_SEC_IO18	L19	IO_L5P_9		IO_L5P_10	L7
AV_SEC_IO22	K20	IO_L5N_9		IO_L5N_10	L6
AV_SEC_IO11	L21	IO_L6P_9		IO_L6P_10	K5
AV_SEC_IO17	L20	IO_L6N_9		IO_L6N_10	K4
LVDS_P10	K24	IO_L7P_9		IO_L7P_10	K3
LVDS_N10	K23	IO_L7N_9		IO_L7N_10	K2
AV_SEC_IO8	K26	IO_L8P_CC_LC_9		IO_L8P_CC_LC_10	L4
AV_SEC_IO21	K25	IO_L8N_CC_LC_9		IO_L8N_CC_LC_10	L3
AV_SEC_IO14	M19	IO_L9P_CC_LC_9		IO_L9P_CC_LC_10	M8
AV_SEC_IO10	N19	IO_L9N_CC_LC_9		IO_L9N_CC_LC_10	L8
LVDS_P12	L24	IO_L10P_9		IO_L10P_10	L1
LVDS_N12	L23	IO_L10N_9		IO_L10N_10	K1
LVDS_P15	M25	IO_L11P_9		IO_L11P_10	M2
LVDS_N15	M24	IO_L11N_9		IO_L11N_10	M1
LVDS_P19	L26	IO_L12P_9		IO_L12P_10	M4
LVDS_N19	M26	IO_L12N_VREF_9		IO_L12N_VREF_10	M3
AV_SEC_IO12	M21	IO_L13P_9		IO_L13P_10	M6
AV_SEC_IO13	M20	IO_L13N_9		IO_L13N_10	M5
AV_SEC_IO16	M23	IO_L14P_9		IO_L14P_10	N3
AV_SEC_IO15	M22	IO_L14N_9		IO_L14N_10	N2
LVDS_P21	N25	IO_L15P_9		IO_L15P_10	N5
LVDS_N21	N24	IO_L15N_9		IO_L15N_10	N4
LVDS_P16	N23	IO_L16P_9		IO_L16P_10	P3
LVDS_N16	N22	IO_L16N_9		IO_L16N_10	P2
AV_SEC_IO20	N21	IO_L17P_9		IO_L17P_10	N7
AV_SEC_IO19	N20	IO_L17N_9		IO_L17N_10	M7
LVDS_P22	P25	IO_L18P_9		IO_L18P_10	P5
LVDS_N22	P24	IO_L18N_9		IO_L18N_10	P4
LVDS_P18	P23	IO_L19P_9		IO_L19P_10	P8
LVDS_N18	P22	IO_L19N_9		IO_L19N_10	N8
LVDS_P20	R26	IO_L20P_9		IO_L20P_10	R4
LVDS_N20	R25	IO_L20N_VREF_9		IO_L20N_VREF_10	R3
AV_SEC_IO23	P20	IO_L21P_9		IO_L21P_10	P7
AV_SEC_IO9	P19	IO_L21N_9		IO_L21N_10	P6
LVDS_P24	R24	IO_L22P_9		IO_L22P_10	R2
LVDS_N24	R23	IO_L22N_9		IO_L22N_10	R1
AV_SEC_IO24	R22	IO_L23P_VRN_9		IO_L23P_VRN_10	R6
AV_SEC_IO26	R21	IO_L23N_VRP_9		IO_L23N_VRP_10	R5
AV_SEC_IO27	T24	IO_L24P_CC_LC_9		IO_L24P_CC_LC_10	U1
AV_SEC_IO28	T23	IO_L24N_CC_LC_9		IO_L24N_CC_LC_10	T1
AV_SEC_IO6	R20	IO_L25P_CC_LC_9		IO_L25P_CC_LC_10	R8
AV_SEC_IO5	R19	IO_L25N_CC_LC_9		IO_L25N_CC_LC_10	R7
LVDS_P26	T26	IO_L26P_9		IO_L26P_10	T4
LVDS_N26	U26	IO_L26N_9		IO_L26N_10	T3
LVDS_P29	U23	IO_L27P_9		IO_L27P_10	T7
LVDS_N29	V23	IO_L27N_9		IO_L27N_10	T6
LVDS_P28	U25	IO_L28P_9		IO_L28P_10	U3
LVDS_N28	U24	IO_L28N_VREF_9		IO_L28N_VREF_10	U2
LVDS_P27	U22	IO_L29P_9		IO_L29P_10	V4
LVDS_N27	U21	IO_L29N_9		IO_L29N_10	U4
LVDS_P23	T21	IO_L30P_9		IO_L30P_10	V2
LVDS_N23	T20	IO_L30N_9		IO_L30N_10	V1
AV_SEC_IO1	U20	IO_L31P_9		IO_L31P_10	T8
AV_SEC_IO2	T19	IO_L31N_9		IO_L31N_10	U7
LVDS_P25	V26	IO_L32P_9		IO_L32P_10	U6
LVDS_N25	V25	IO_L32N_9		IO_L32N_10	U5

Bank10

XC4V_FF668

1.25V_REF

DDR_A6
DDR_A5
DDR_A4
DDR_A2
DDR_DM1 9,10
DDR_D8
DDR_A3
DDR_D11
DDR_D10
DDR_D9
DDR_D7
DDR_D6
DDR_D5
DDR_DQS0 9
SWITCH_PB1 14
SWITCH5
SWITCH6
DDR_A0
DDR_A1
DDR_BA1 9,10
DDR_A10
DDR_BA0 9,10
DDR_A8
DDR_A9
DDR_CS0# 9,10
DDR_RAS# 9,10
DDR_CLKEN 9,10
DDR_WE# 9,10
DDR_A13
DDR_CAS# 9,10
DDR_A11
DDR_A7
DDR_D3
DDR_DM0 9,10
DDR_D15
DDR_D12
DDR_A12
DDR_D14
DDR_D13
DDR_D2
DDR_D4
DDR_DQS1 9
SWITCH_PB2 14
NC_NET 4
SWITCH0
CLK_DDR_0 9,10
CLK_DDR_0# 9,10
CLK_DDR_FB 2
DDR_CLK_FB
SWITCH1
SWITCH2
SWITCH4
SWITCH3
DDR_D1
DDR_D0

JP21
HEADER 2X2

2.5V
R1 50
R2 50

DDR_D[0:15] 9
DDR_D0
DDR_D1
DDR_D2
DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D7
DDR_D8
DDR_D9
DDR_D10
DDR_D11
DDR_D12
DDR_D13
DDR_D14
DDR_D15

DDR_A[0:13] 9,10
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13

SWITCH[0:7] 3,14
SWITCH0
SWITCH1
SWITCH2
SWITCH3
SWITCH4
SWITCH5
SWITCH6

1.25V_TT
R167 50
DDR_CLK_FB
C261
DNI

Match lengths of DDR
traces, except DDR_CLK_FB
make 2X the length

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U1F

XC4V_FF668

No Connects for LX15/SX25

No Connects for LX15/SX25

1.2V

2.5V

3.xV

VIO_SEL

VREF_2.5V

TMP_VP 14

R33 6R49

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15
680pF 680pF 680pF 680pF 680pF 680pF 680pF 680pF 680pF 0.01uF 0.01uF 0.01uF 0.01uF 0.1uF 0.1uF

C18 TANB_47uF

C34 0.01uF C35 0.1uF

C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49
680pF 680pF 680pF 680pF 680pF 680pF 680pF 680pF 680pF 680pF 680pF 680pF 680pF 680pF

C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C50 TANB_47uF
0.01uF 0.01uF 0.01uF 0.01uF 0.01uF 0.01uF 0.01uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF

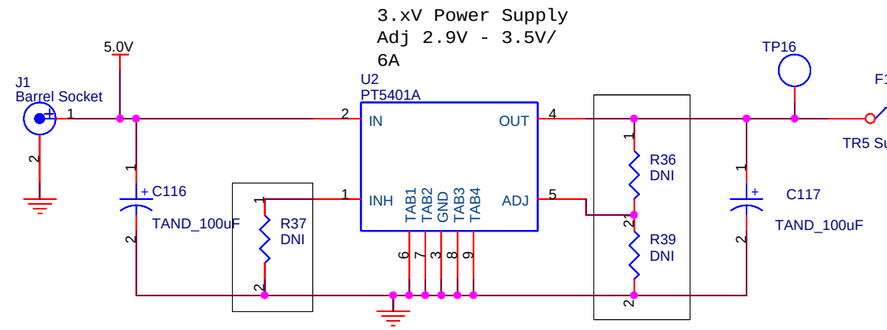
C63 C64 C65 C66 C67 C68 C69
680pF 680pF 680pF 680pF 680pF 680pF 680pF

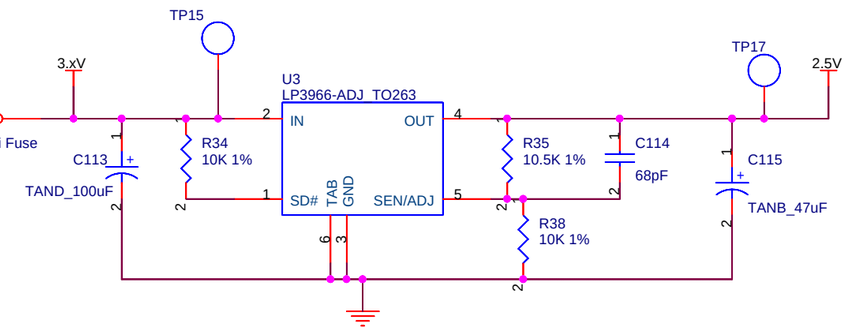
C81 C82 C83 C84 C85 C86 C87 C88 C89 C80 TANB_47uF
680pF 680pF 0.01uF 0.01uF 0.01uF 0.01uF 0.01uF 0.1uF 0.1uF

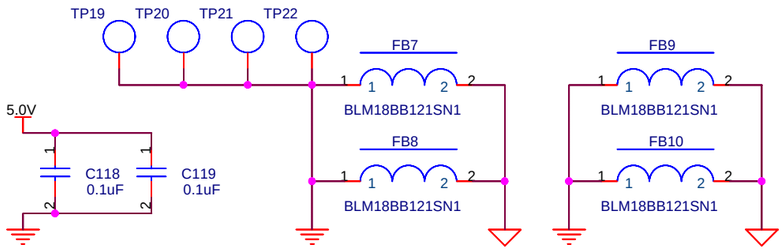
C96 TANB_47uF

C100 C101 C102 C103 C104 C105 C106 C107 C108 C109 C110 C111 C112
680pF 680pF 680pF 680pF 680pF 680pF 680pF 0.01uF 0.01uF 0.01uF 0.01uF 0.1uF 0.1uF

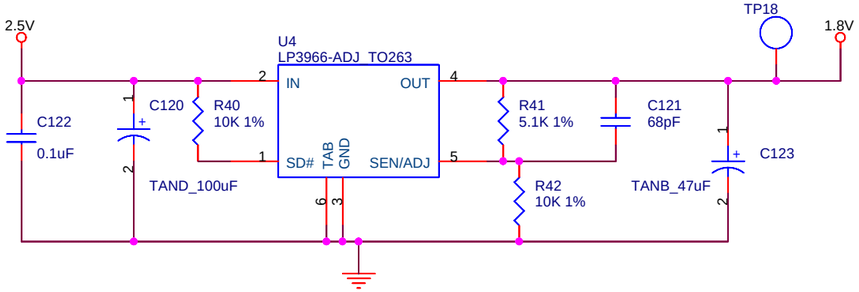
Title: Xilinx Virtex4 LX Evaluation Board		
Size: B	Document Number: ADS-V4-LX-SCH	Rev: B
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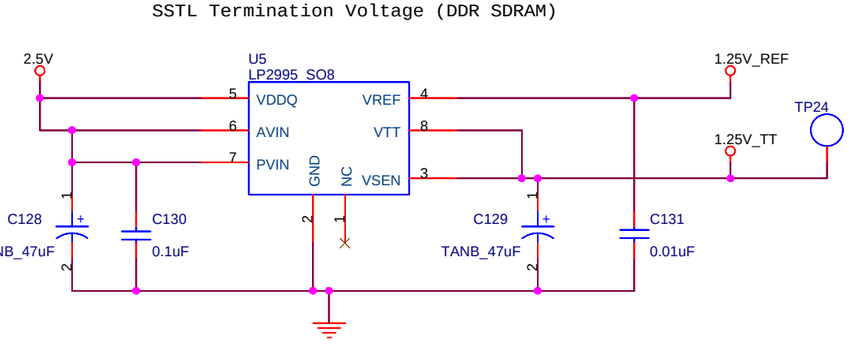


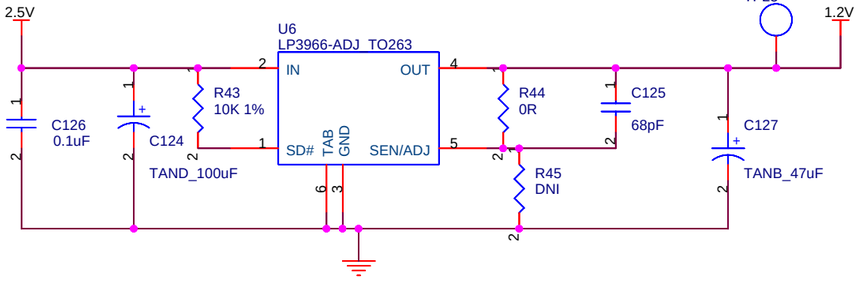


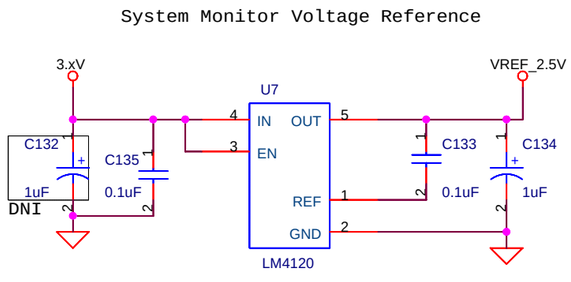


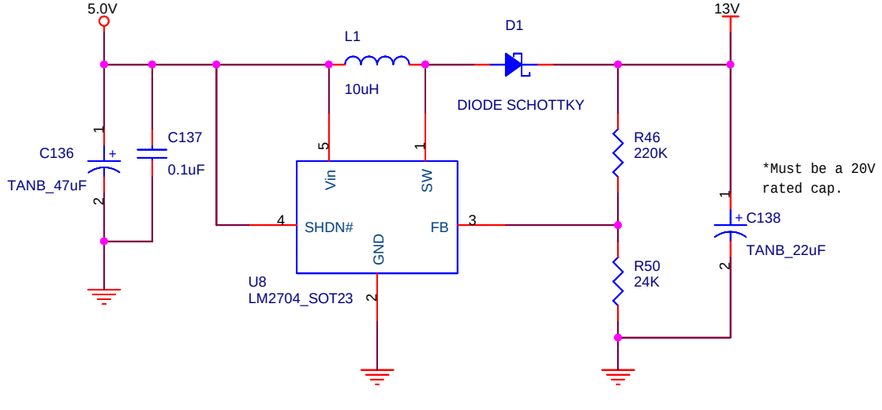
SSTL Termination Voltage (DDR SDRAM)

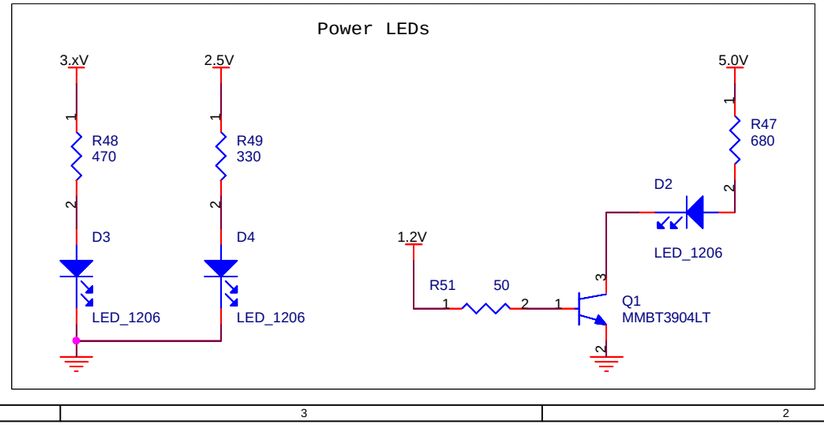










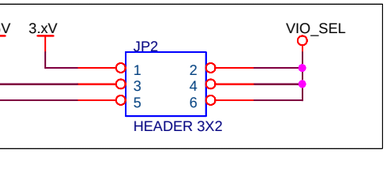


LP3966 Output Voltage

$$R2 = R1\left(\frac{Vo}{1.216} - 1\right)$$

$$Vo = 1.216\left(\frac{R2}{R1} + 1\right)$$

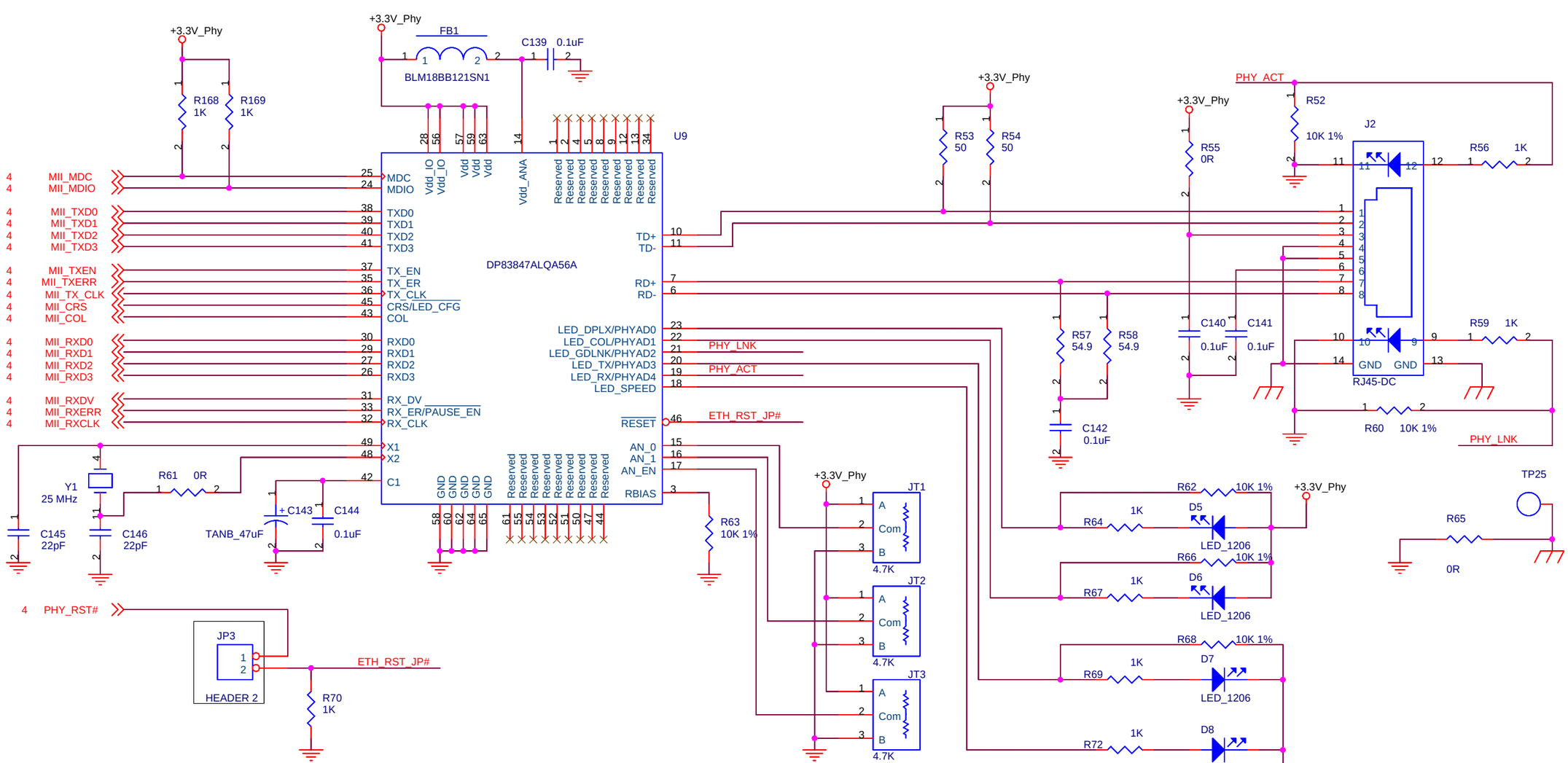




FPGA Bank I/O Voltage Selection

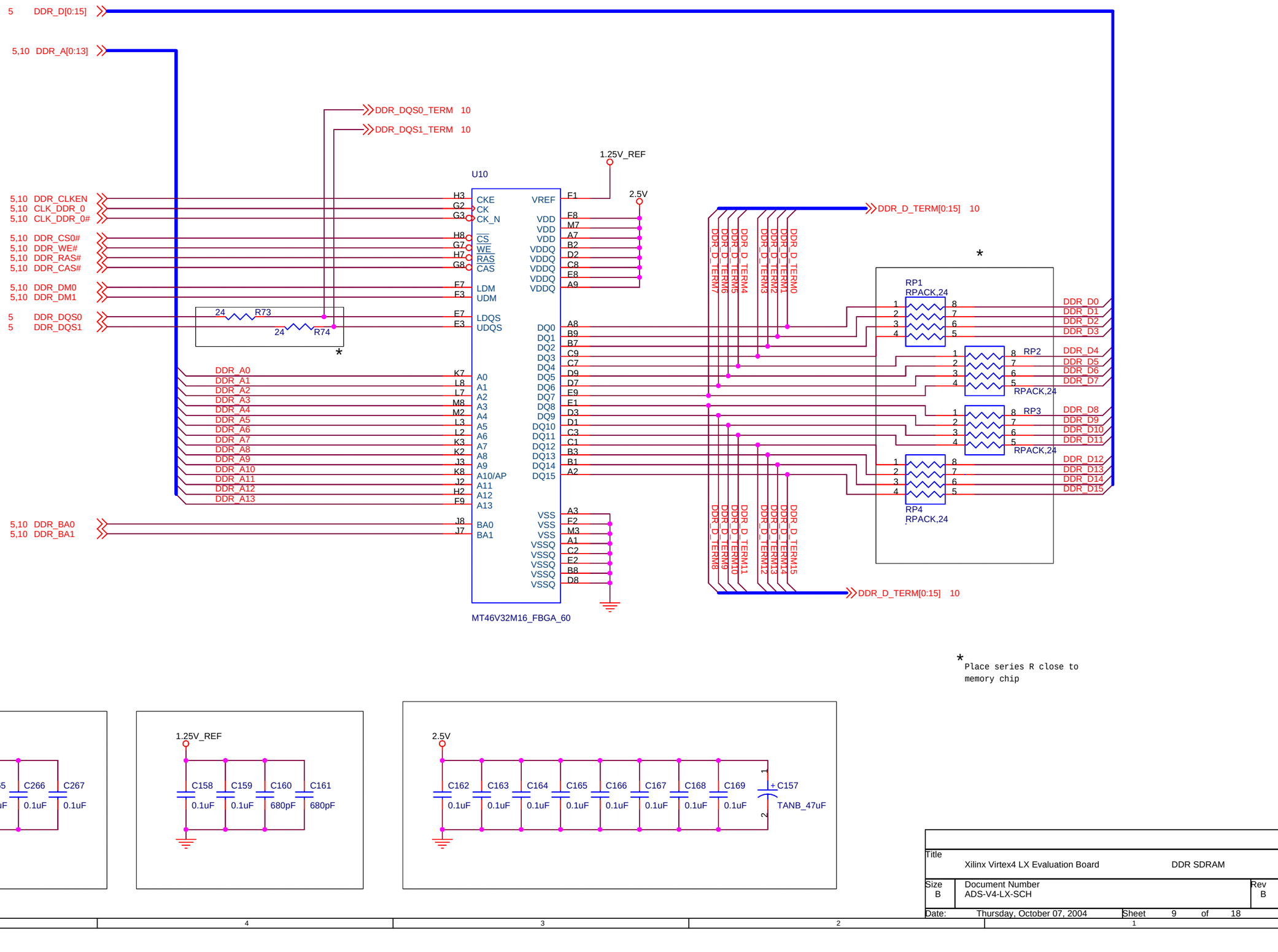
(Shunt required. One voltage must be selected at all times. Do not switch VCCO voltages while power is applied to the board.)

Title: Xilinx Virtex4 LX Evaluation Board		Board Power
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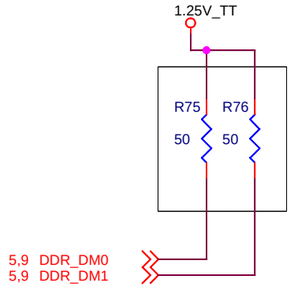
JT3	JT2	JT1	
2-3	2-3	2-3	10BaseT, Half Duplex, Forced Mode
2-3	2-3	1-2	10BaseT, Full Duplex, Forced Mode
2-3	1-2	2-3	100Base-TX, Half Duplex, Forced Mode
2-3	1-2	1-2	100Base-TX, Full Duplex, Forced Mode
1-2	2-3	2-3	10BaseT, Half/Full Duplex, Advertised Auto-negotiation Enabled
1-2	2-3	1-2	100Base-TX, Half/Full Duplex, Advertised Auto-negotiation Enabled
1-2	1-2	2-3	10BaseT, Half Duplex/100Base-TX Half Duplex, Advertised Auto-negotiation Enabled
1-2	1-2	1-2	10BaseT, Half/Full Duplex/100Base-TX Half/Full Duplex, Advertised Auto-negotiation Enabled

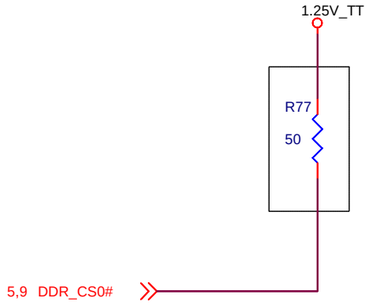
Title	Xilinx Virtex4 LX Evaluation Board	Ethernet PHY
Size B	Document Number ADS-V4-LX-SCH	Rev B
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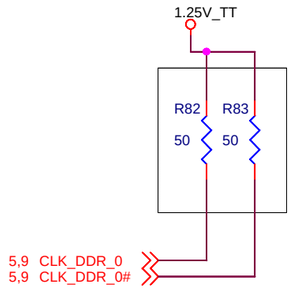


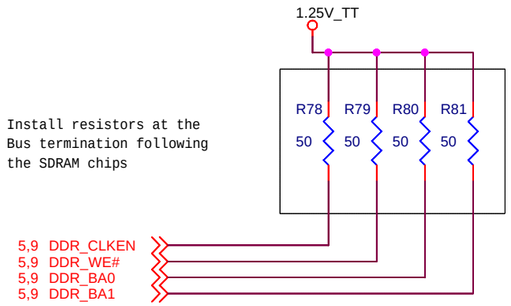
* Place series R close to memory chip

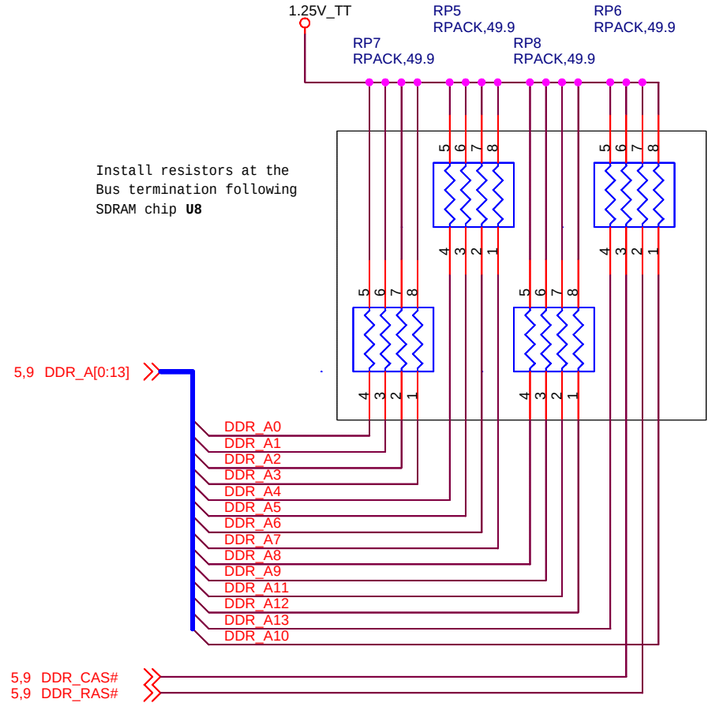
Title	Xilinx Virtex4 LX Evaluation Board	DDR SDRAM
Size B	Document Number ADS-V4-LX-SCH	Rev B
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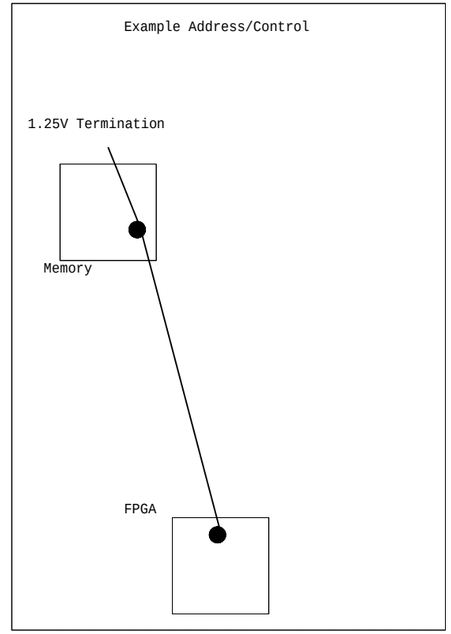


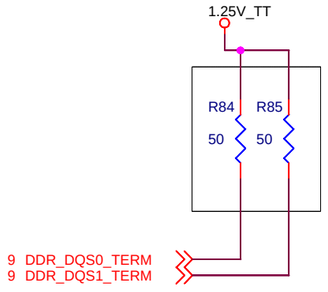


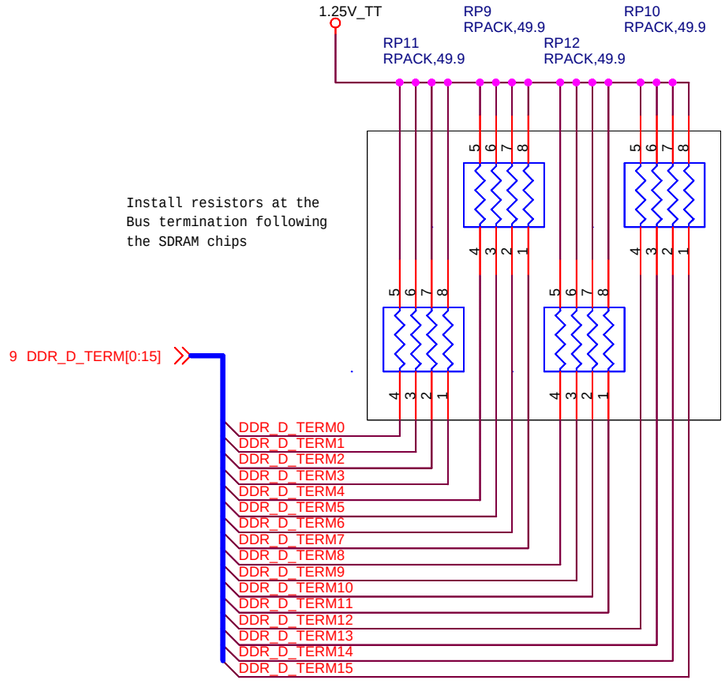


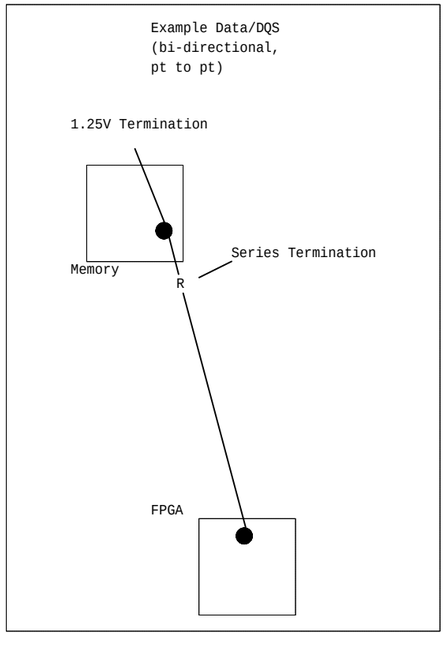




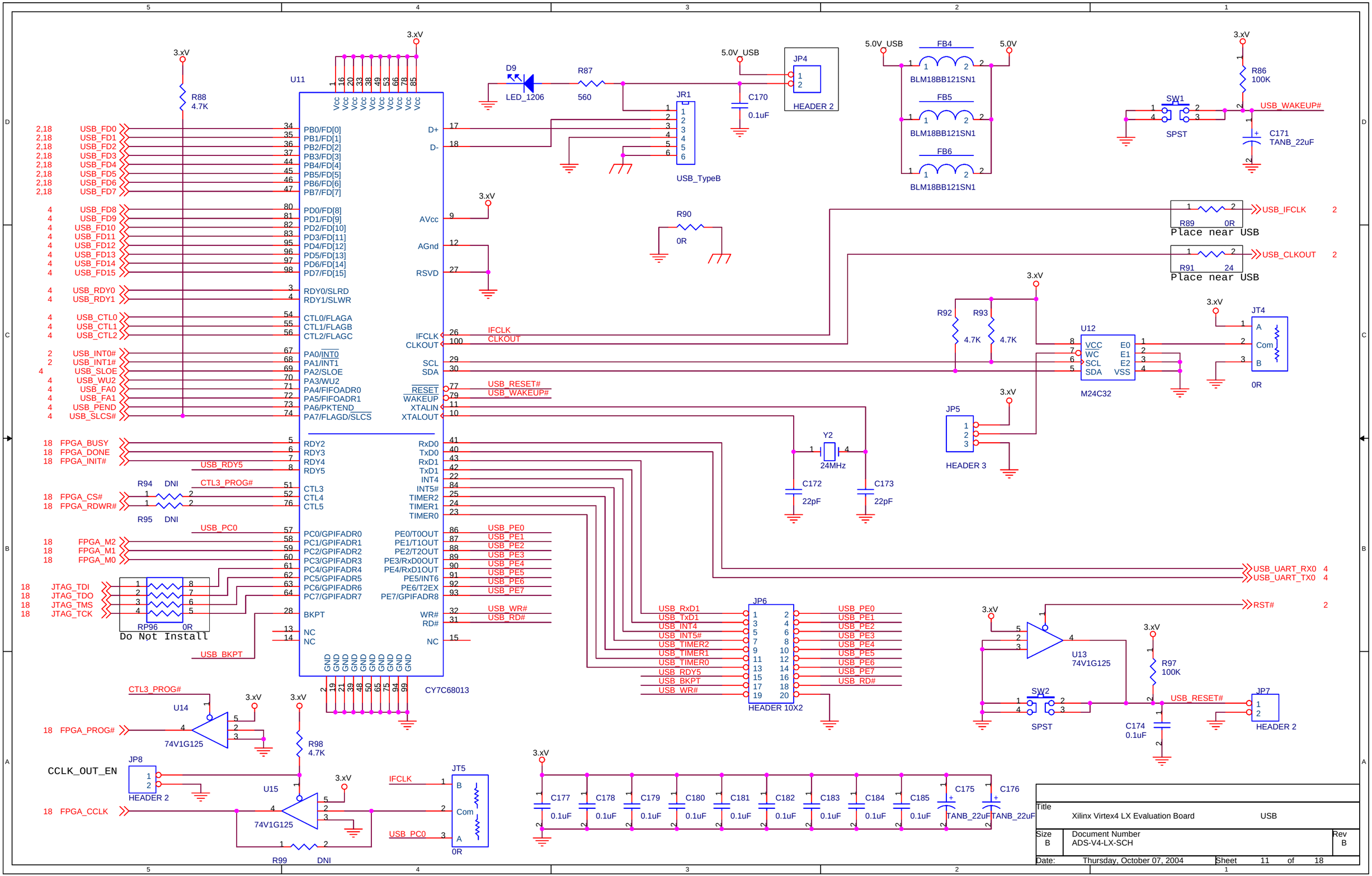


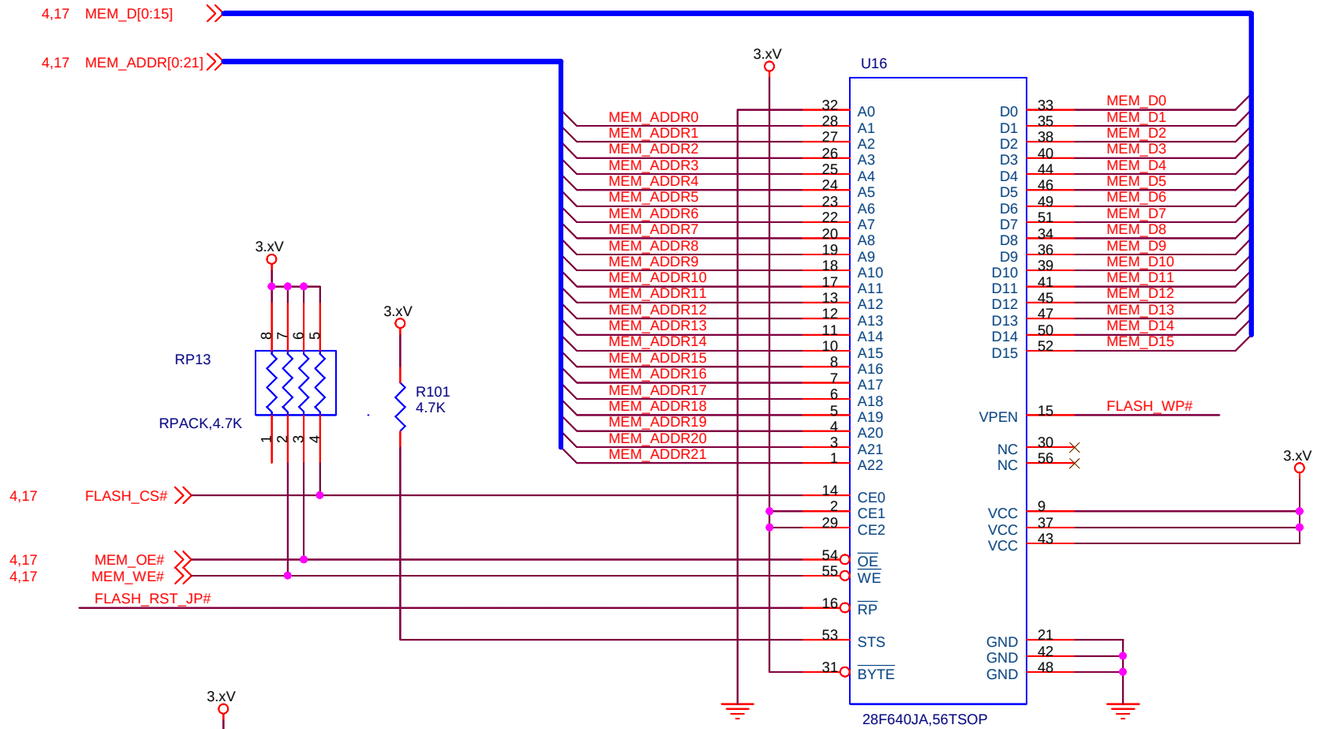


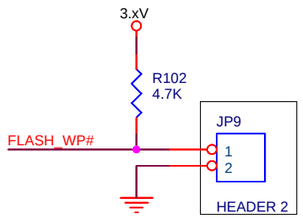


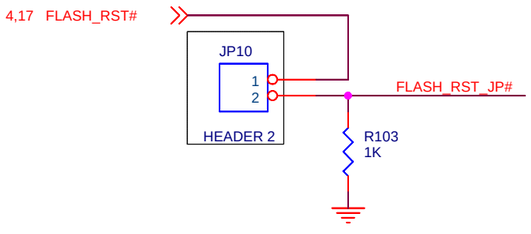


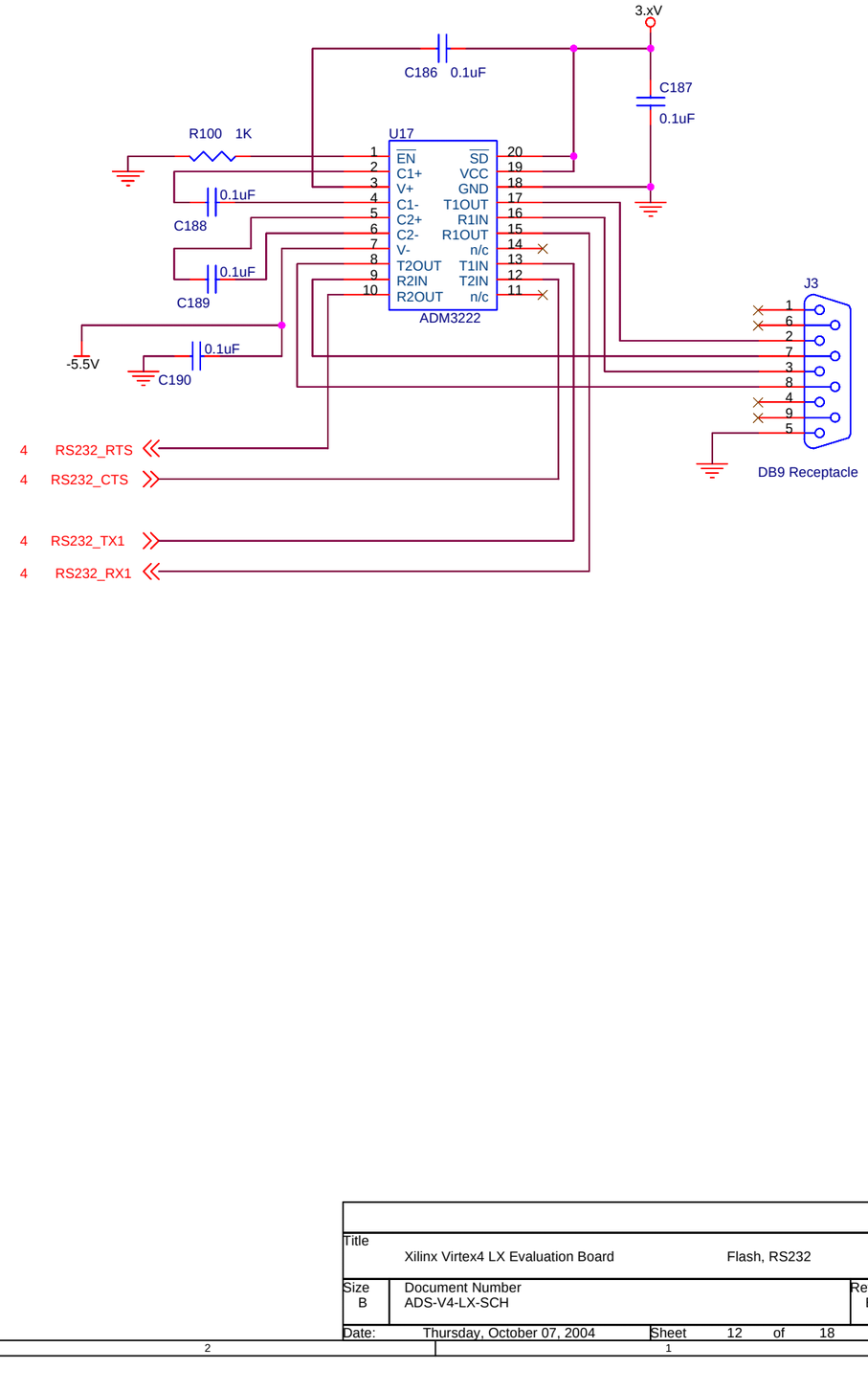
Title: Xilinx Virtex4 LX Evaluation Board		DDR Termination
Size: B	Document Number: ADS-V4-LX-SCH	Rev: B
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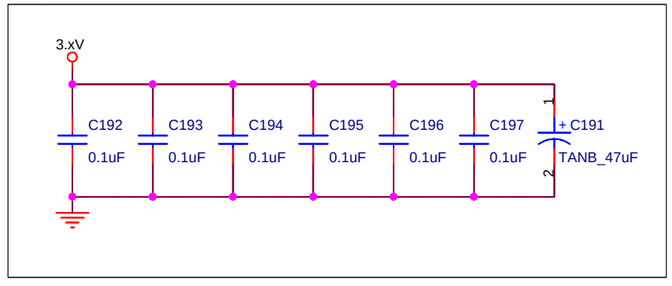

U11
CY7C68013
R88 4.7K
3.xV
D9
LED_1206
R87
560
JR1
USB_TypeB
5.0V_USB
JP4
HEADER 2
C170
0.1uF
FB4
FB5
FB6
BLM18BB121SN1
5.0V
SW1
SPST
R86
100K
USB_WAKEUP#
C171
TANB_22uF
R90
0R
R89
0R
Place near USB
USB_IFCLK
R91
24
USB_CLKOUT
R92
R93
4.7K
U12
M24C32
JT4
JP5
HEADER 3
Y2
24MHz
C172
22pF
C173
22pF
JP6
HEADER 10X2
RP96
0R
Do Not Install
U13
74V1G125
R97
100K
SW2
C174
0.1uF
JP7
RST#
U14
R98
4.7K
JP8
CCLK_OUT_EN
U15
R99
DNI
JT5
0R
C177
C178
C179
C180
C181
C182
C183
C184
C185
C175
TANB_22uF
C176
TANB_22uF
USB_FD0
USB_FD1
USB_FD2
USB_FD3
USB_FD4
USB_FD5
USB_FD6
USB_FD7
USB_FD8
USB_FD9
USB_FD10
USB_FD11
USB_FD12
USB_FD13
USB_FD14
USB_FD15
USB_RDY0
USB_RDY1
USB_CTL0
USB_CTL1
USB_CTL2
USB_INT0#
USB_INT1#
USB_SLOE
USB_WU2
USB_FA0
USB_FA1
USB_PEND
USB_SLCS#
FPGA_BUSY
FPGA_DONE
FPGA_INIT#
USB_RDY5
CTL3_PROG#
FPGA_CS#
FPGA_RDWR#
USB_PC0
FPGA_M2
FPGA_M1
FPGA_M0
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
USB_BKPT
FPGA_PROG#
FPGA_CCLK
USB_RESET#
USB_WAKEUP#
IFCLK
CLKOUT
USB_PE0
USB_PE1
USB_PE2
USB_PE3
USB_PE4
USB_PE5
USB_PE6
USB_PE7
USB_WR#
USB_RD#
USB_RxD1
USB_TxD1
USB_INT4
USB_INT5#
USB_TIMER2
USB_TIMER1
USB_TIMER0
USB_RDY5
USB_BKPT
USB_WR#
USB_UART_RX0
USB_UART_TX0
Title
Xilinx Virtex4 LX Evaluation Board
USB
Size
B
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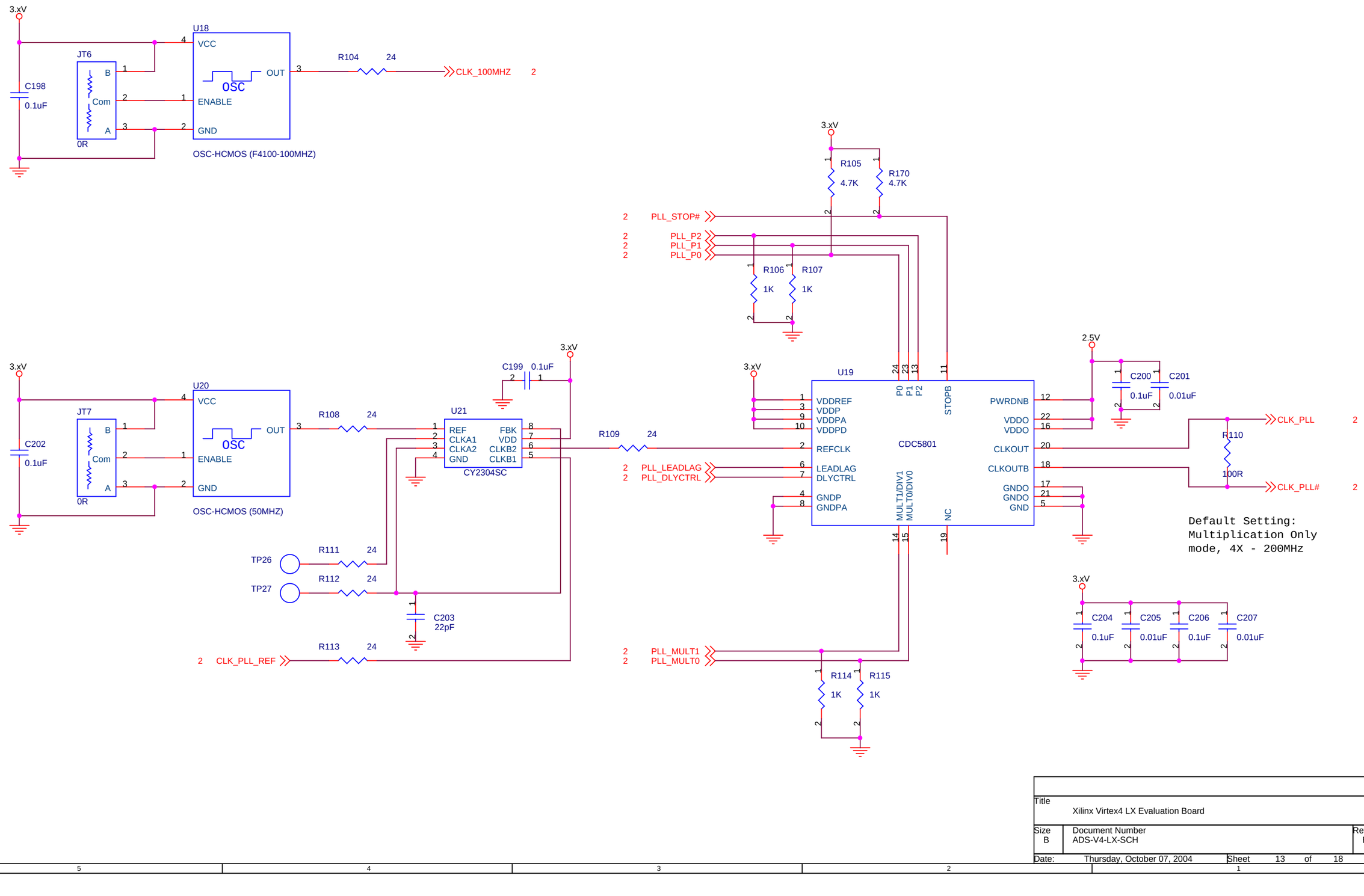




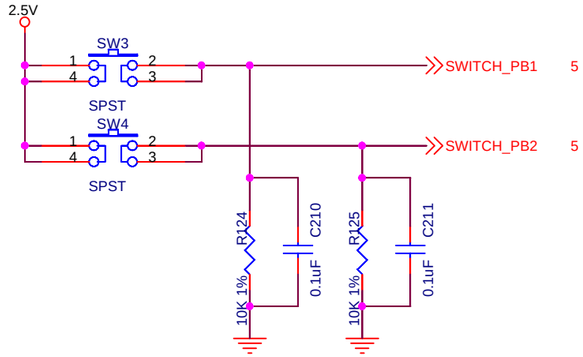


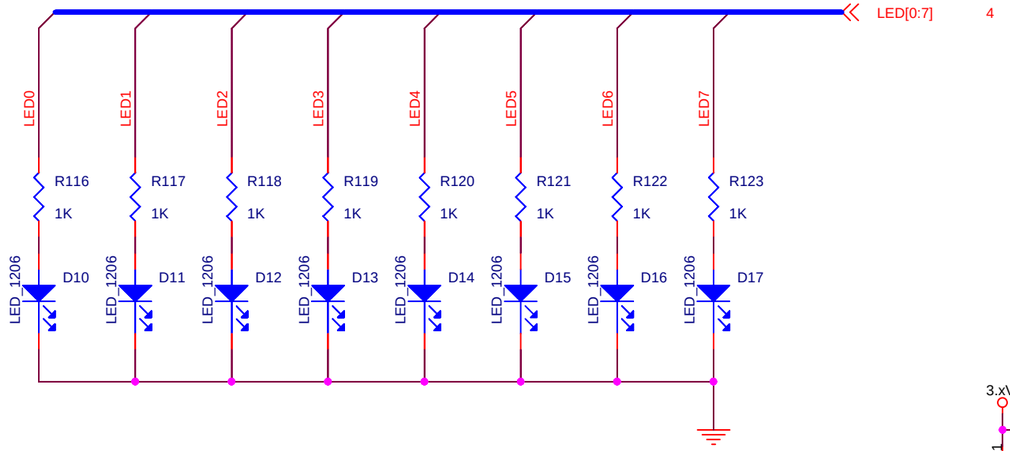


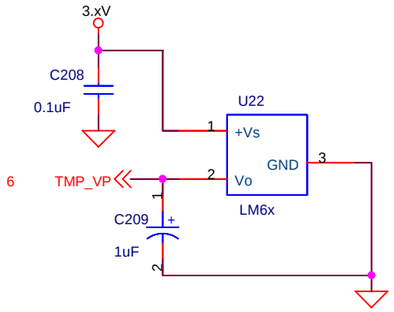
Title	Xilinx Virtex4 LX Evaluation Board	Flash, RS232
Size B	Document Number ADS-V4-LX-SCH	Rev B
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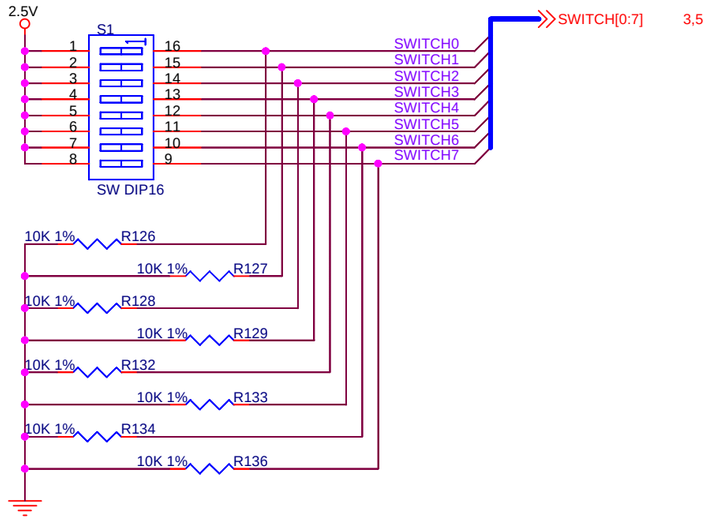


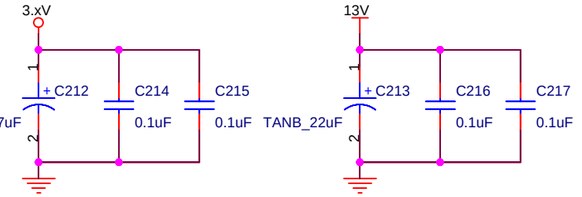
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Size B	Document Number ADS-V4-LX-SCH	Rev B
Date: Thursday, October 07, 2004	Sheet 13 of 18	

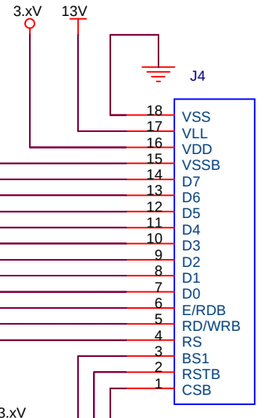


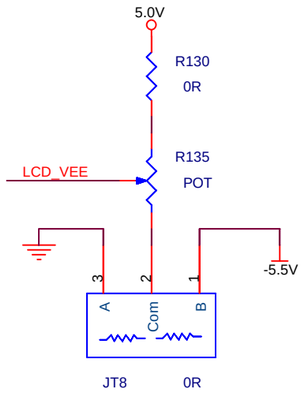


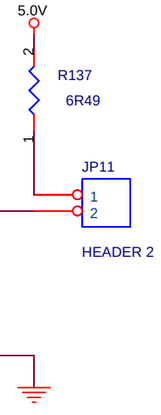


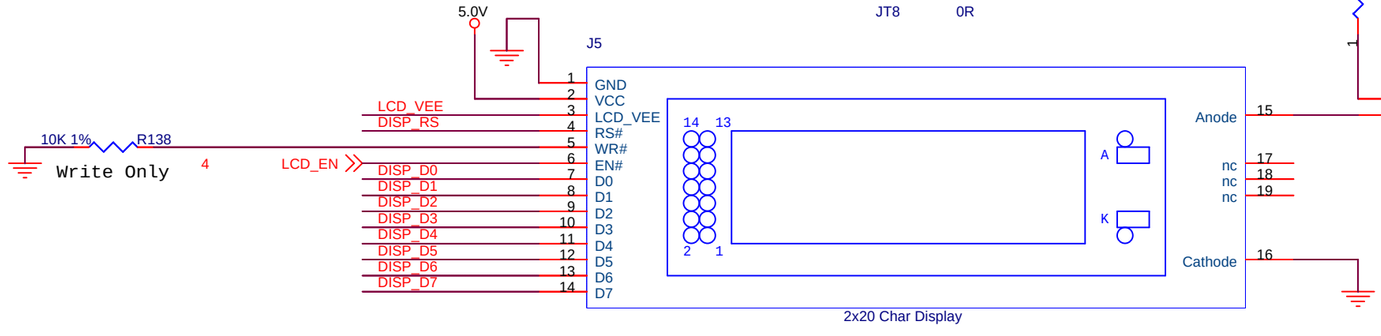


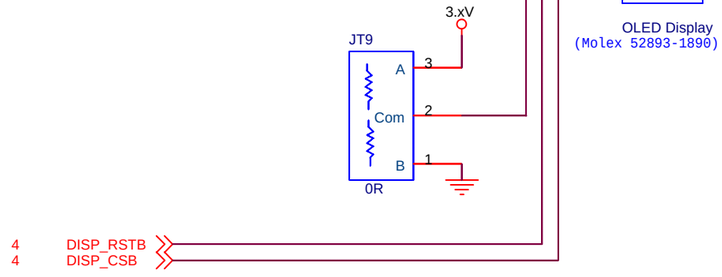






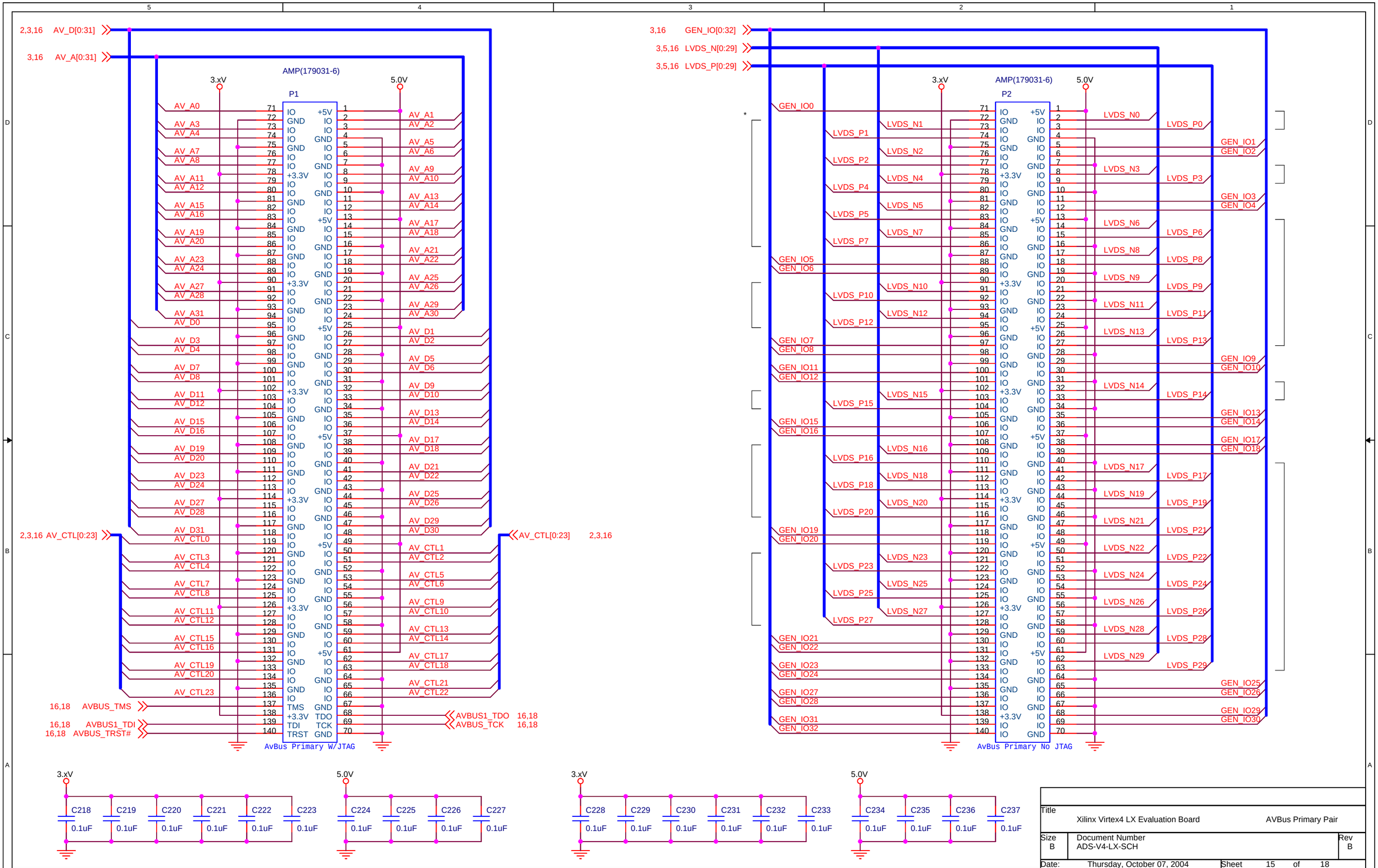




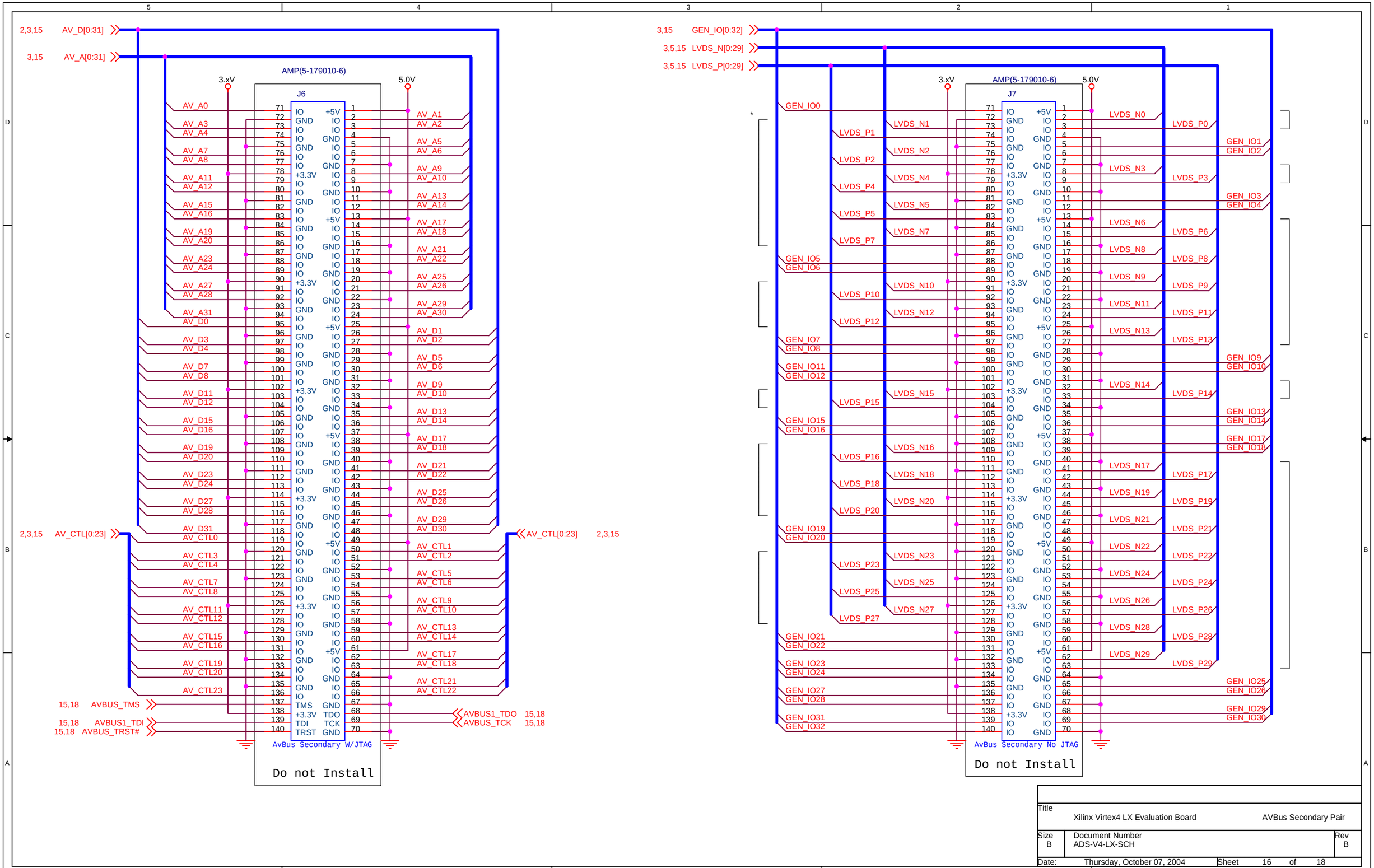


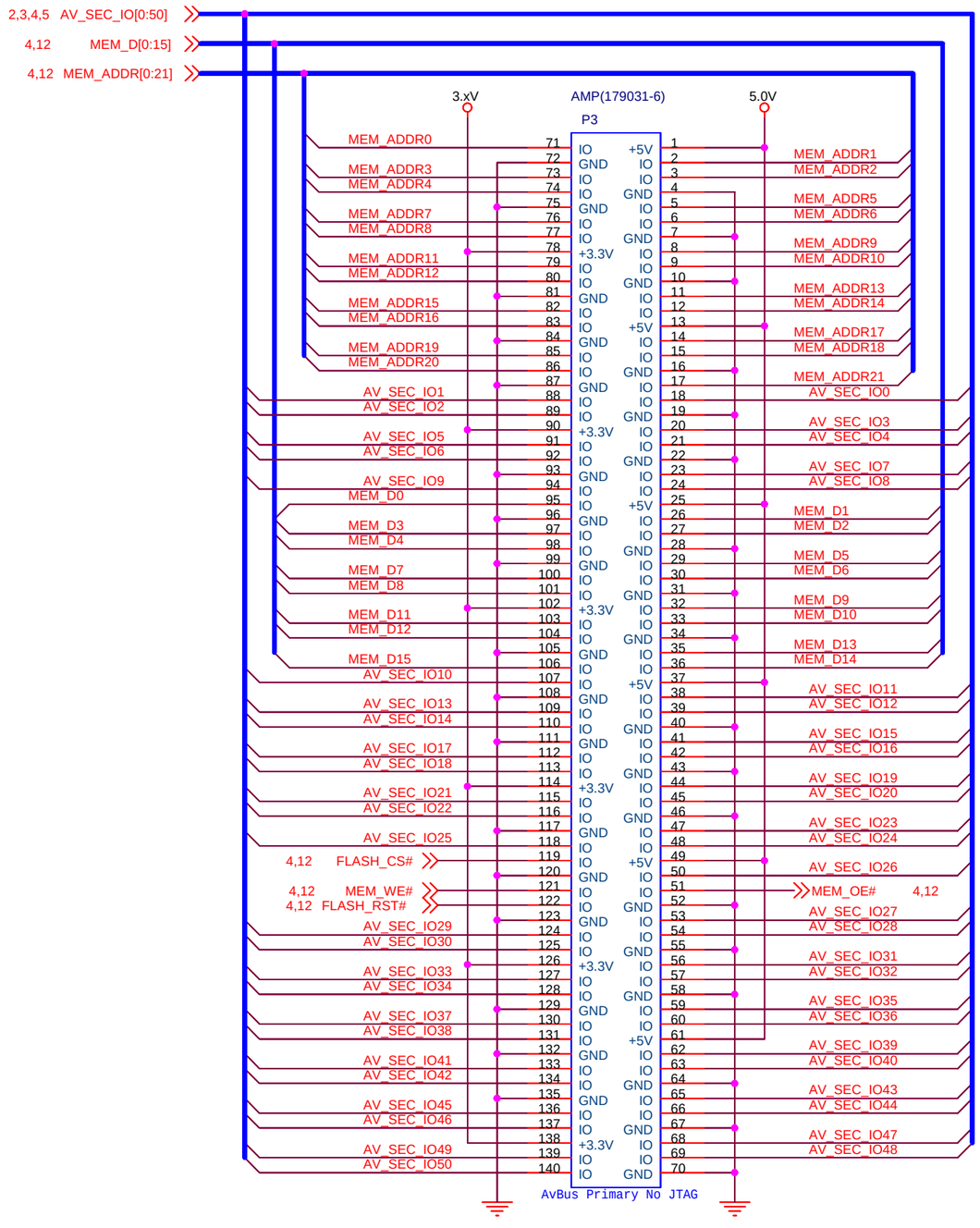
Note: For 15-19, use 1x5 and Cut pins 2-4

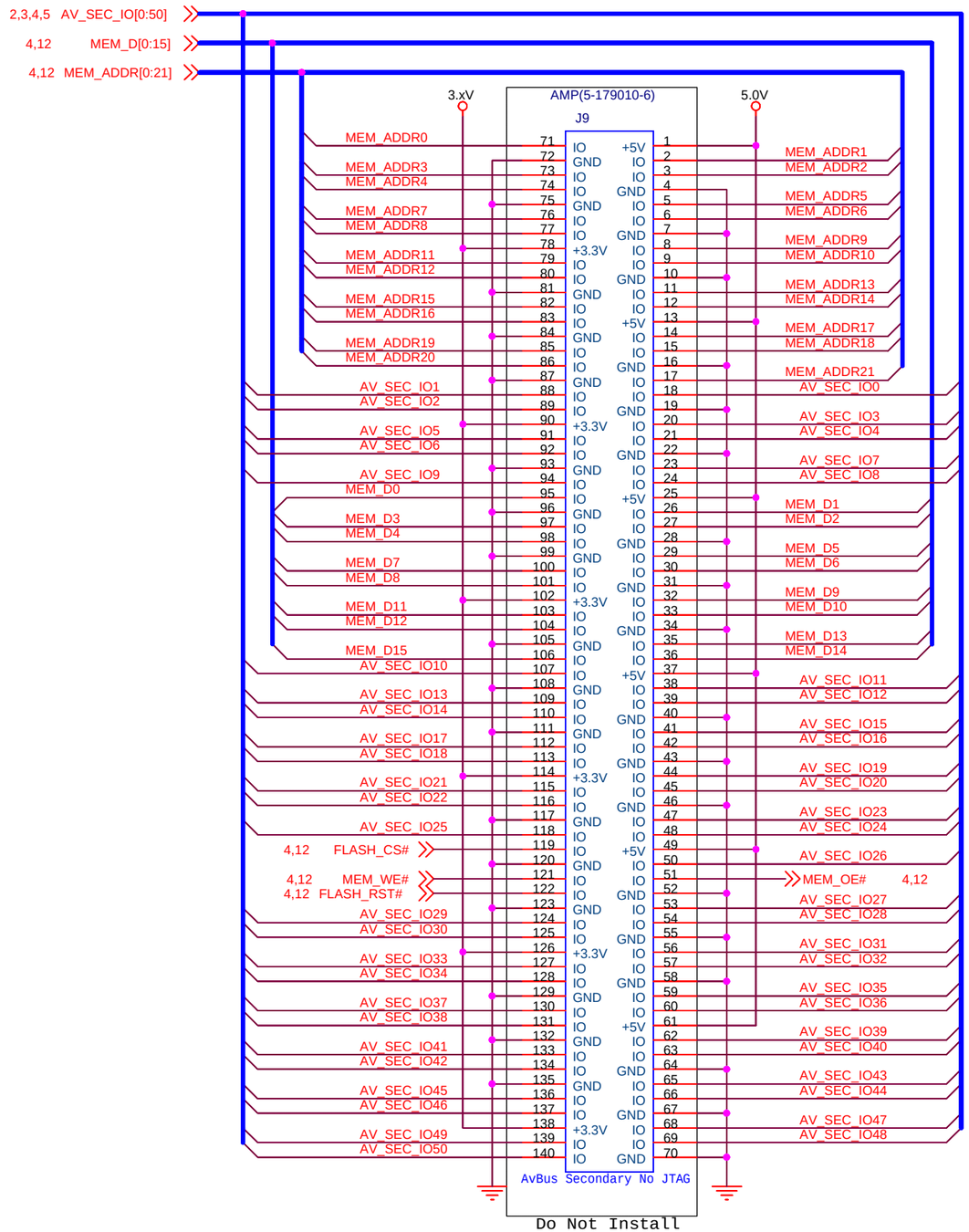
Title	Xilinx Virtex4 LX Evaluation Board	LED, Switches, Display, Temp
Size B	Document Number ADS-V4-LX-SCH	Rev B
Date: Thursday, October 07, 2004	Sheet 14 of 18	

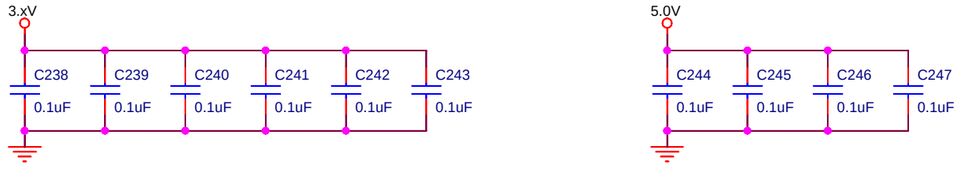


Title	Xilinx Virtex4 LX Evaluation Board	AVBus Primary Pair
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2,3,15 AV_D[0:31]
3,15 AV_A[0:31]
AMP(5-179010-6)
3.xV
5.0V
J6
AV_A0 AV_A1 AV_A2 AV_A3 AV_A4 AV_A5 AV_A6 AV_A7 AV_A8 AV_A9 AV_A10 AV_A11 AV_A12 AV_A13 AV_A14 AV_A15 AV_A16 AV_A17 AV_A18 AV_A19 AV_A20 AV_A21 AV_A22 AV_A23 AV_A24 AV_A25 AV_A26 AV_A27 AV_A28 AV_A29 AV_A30 AV_A31
AV_D0 AV_D1 AV_D2 AV_D3 AV_D4 AV_D5 AV_D6 AV_D7 AV_D8 AV_D9 AV_D10 AV_D11 AV_D12 AV_D13 AV_D14 AV_D15 AV_D16 AV_D17 AV_D18 AV_D19 AV_D20 AV_D21 AV_D22 AV_D23 AV_D24 AV_D25 AV_D26 AV_D27 AV_D28 AV_D29 AV_D30 AV_D31
2,3,15 AV_CTL[0:23]
AV_CTL0 AV_CTL1 AV_CTL2 AV_CTL3 AV_CTL4 AV_CTL5 AV_CTL6 AV_CTL7 AV_CTL8 AV_CTL9 AV_CTL10 AV_CTL11 AV_CTL12 AV_CTL13 AV_CTL14 AV_CTL15 AV_CTL16 AV_CTL17 AV_CTL18 AV_CTL19 AV_CTL20 AV_CTL21 AV_CTL22 AV_CTL23
AV_CTL[0:23] 2,3,15
15,18 AVBUS_TMS
15,18 AVBUS1_TDI
15,18 AVBUS_TRST#
AVBUS1_TDO 15,18
AVBUS_TCK 15,18
AvBus Secondary W/JTAG
Do not Install
3,15 GEN_IO[0:32]
3,5,15 LVDS_N[0:29]
3,5,15 LVDS_P[0:29]
AMP(5-179010-6)
3.xV
5.0V
J7
GEN_IO0 LVDS_N0 LVDS_P0 LVDS_N1 LVDS_P1 GEN_IO1 GEN_IO2 LVDS_N2 LVDS_P2 LVDS_N3 LVDS_P3 LVDS_N4 LVDS_P4 GEN_IO3 GEN_IO4 LVDS_N5 LVDS_P5 LVDS_N6 LVDS_P6 LVDS_N7 LVDS_P7 LVDS_N8 LVDS_P8 GEN_IO5 GEN_IO6 LVDS_N9 LVDS_P9 LVDS_N10 LVDS_P10 LVDS_N11 LVDS_P11 LVDS_N12 LVDS_P12 LVDS_N13 LVDS_P13 GEN_IO7 GEN_IO8 GEN_IO9 GEN_IO10 GEN_IO11 GEN_IO12 LVDS_N14 LVDS_P14 LVDS_N15 LVDS_P15 GEN_IO13 GEN_IO14 GEN_IO15 GEN_IO16 GEN_IO17 GEN_IO18 LVDS_N16 LVDS_P16 LVDS_N17 LVDS_P17 LVDS_N18 LVDS_P18 LVDS_N19 LVDS_P19 LVDS_N20 LVDS_P20 LVDS_N21 LVDS_P21 GEN_IO19 GEN_IO20 LVDS_N22 LVDS_P22 LVDS_N23 LVDS_P23 LVDS_N24 LVDS_P24 LVDS_N25 LVDS_P25 LVDS_N26 LVDS_P26 LVDS_N27 LVDS_P27 LVDS_N28 LVDS_P28 GEN_IO21 GEN_IO22 LVDS_N29 LVDS_P29 GEN_IO23 GEN_IO24 GEN_IO25 GEN_IO26 GEN_IO27 GEN_IO28 GEN_IO29 GEN_IO30 GEN_IO31 GEN_IO32
AvBus Secondary No JTAG
Do not Install
Title
Xilinx Virtex4 LX Evaluation Board
AVBus Secondary Pair
Size B
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Title	Xilinx Virtex4 LX Evaluation Board	AVBus Auxilliary
Size B	Document Number ADS-V4-LX-SCH	Rev B
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PROM	Capacity
XCF08P	8,388,608
XCF16P	16,777,216
XCF32P	33,554,432

JTAG Parallel IV Connector

JTAG Parallel III Connector

Default 2-3

Title	Xilinx Virtex4 LX Evaluation Board		Configuration/JTAG
Size B	Document Number ADS-V4-LX-SCH		Rev B
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