FSIO2

Frame Synchronizer / Telemetry Output Board

AVTEC SYSTEMS

VM-1120 / VM-1130 / VM-1140 / VM-1250
VM-1350 / VM-1420 / VM-1440

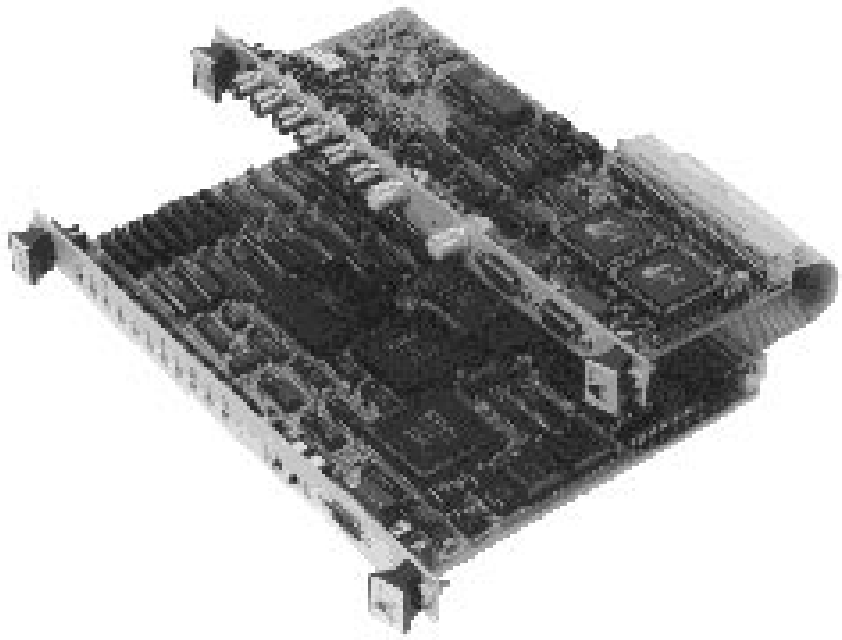
Applications

- Frame Synchronizer
- PCM Simulator
- NASCOM Blocker/Deblocker

Features

- 10 Mbps bidirectional serial I/O port under full DMA control
- Supports TDM telemetry, NASCOM block formats, and CCSDS transfer frame format
- Frame synchronization using an adaptive strategy up to 10 Mbps
- Programmable 64 bit sync pattern and mask, word size an frame length
- Simulation of PCM data streams at bit rates up to 10 Mbps
- Motorola MC68340 integrated microcontroller with DMA running at 16.6 MHz
- 4 MBytes of dual access DRAM for data buffering
- High performance VIC/VAC 32-bit master/slave VME interface with block mode transfer capability
- Transition module options provide TTL and RS-422 clock and data I/O, direct digital synthesizer and CRC encoder/decoder
- Supports NRZ-L, S, M, and BIΦ-L, S, M data codes

RELATED PRODUCTS
Hardware: FSIO2-TM-9U

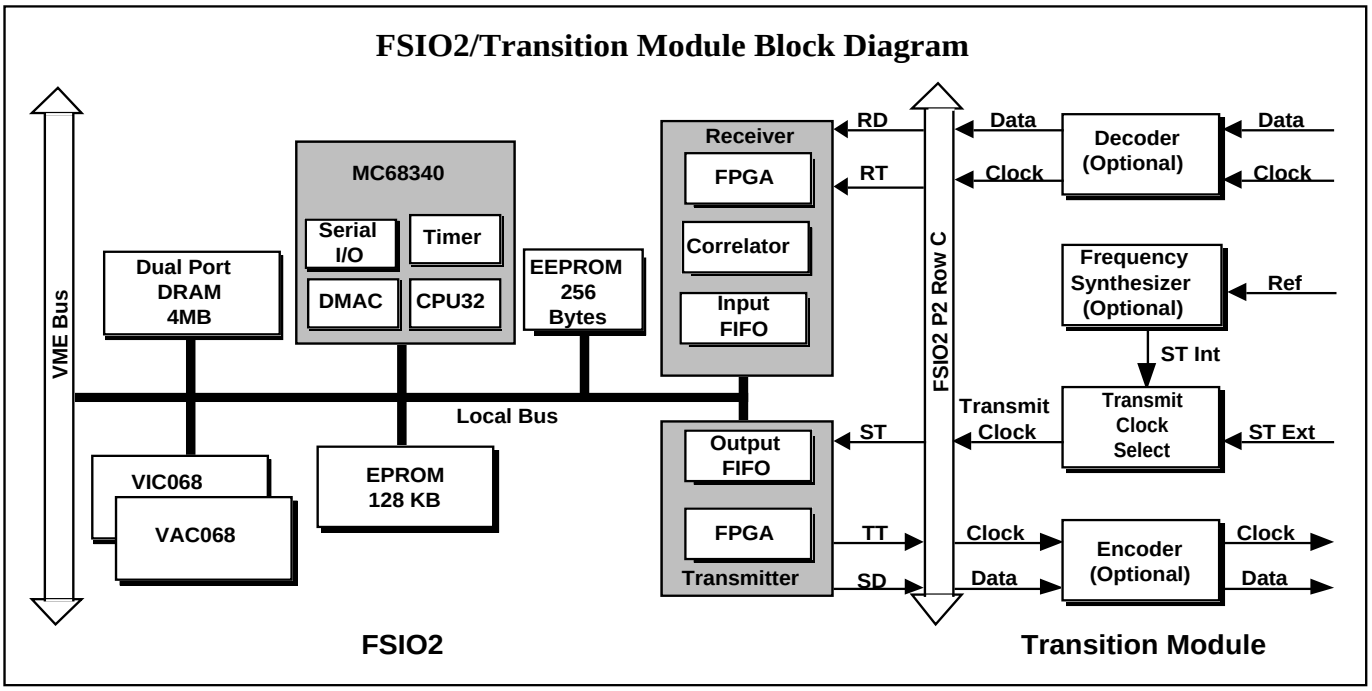


The FSIO2 provides powerful, intelligent, I/O handling between a VMEbus system and a serial communications link.

Overview

The FSIO2 is a high speed telemetry interface that provides complete front end processing capability for a variety of data formats, including those used by NASA and the aerospace industry. In addition to the high speed serial I/O module, it contains an MC68340 32-bit microcontroller, 4 Mbytes of dual-access DRAM, and a 32-bit master/slave VMEbus interface with block transfer capability.

The board's bidirectional, multifunction operation and real-time data processing capability makes it the intelligent choice for VME-based telemetry ground systems. The FSIO2 supports a wide variety of telemetry applications including TDM telemetry and NASCOM interface for satellite ground stations, a telemetry link to local or wide area network gateway systems, a front end processor for operations control centers, and satellite simulation and test systems.



AVD 95-066-01

Hardware

High Speed Serial I/O Controller

The high speed serial I/O controller performs high speed serial-to-parallel and parallel-to-serial conversion and is implemented in field programmable gate arrays. The receiver consists of the code converter, the input correlator, the bit counter and octet counter, the input control logic, the FIFO buffers, and the DMA control and interrupt control. All of the receiver logic except the FIFO buffers and the digital correlator are implemented in a single field programmable gate array. The receiver provides automatic polarity correction and can sync to true or inverted data.

The transmitter consists of the code converter, bit and octet counters, synchronous transmitter, FIFO buffers, and DMA and interrupt request logic. All of the transmitter logic except the transmit clock synthesizer and the FIFO buffers are implemented in a single field programmable gate array.

CPU and Memory

The local CPU is a Motorola 68340 32-bit microcontroller with an integrated 2 channel DMA controller. Local memory consists of 4 MB of fast page mode DRAM which is dual ported to the VMEbus.

The local CPU on the FSIO2 is a Motorola 68340 32-bit integrated microcontroller with DMA running at 16.6 MHz. The DMA controller is used to transfer data from the FIFO buffers to local memory at rates up to 11 Mbps. The FSIO2 has 4 MB of dual access DRAM with 32-bit wide data path for data buffering and storing downloaded code. In addition, it has 128 KB of EPROM and 256 Bytes of EEPROM.

VME Interface

The VME interface is based on Cypress Semiconductor's VIC068 and VAC068 integrated controllers which implement all of the required features in the IEEE 1014 VMEbus Specification Rev C.1. They also provide local DMA control for high speed block transfers over the VMEbus and interprocessor communications facilities for multiprocessor systems.

Transition Modules

Four transition modules are available that provide signal level translation, CRC encoding/decoding, and/or a transmit clock direct digital synthesizer. Descriptions of these modules are found on page 3-5.

Functional Description

The FSIO2 can perform frame synchronization, PCM simulation and NASCOM blocking/deblocking. With its bidirectional, multifunction capability it can perform frame synchronization and PCM simulation simultaneously on the same board. Various capabilities are achieved by configuring the system with different firmware modules and transition modules. Four transition modules are offered that provide signal level translation, CRC encoding/decoding and/or a transmit clock direct digital synthesizer.

The firmware is dynamically loaded in the FSIO2 by the host, allowing the same device to be used with different firmware modules for different applications. All firmware modules perform self diagnostic testing and accept setup parameters from the host system via onboard shared memory. They provide event-driven and periodic status messages to the host system. The configuration data can be read by the host at any time.

Frame Synchronizer

The frame synchronizer receives synchronous serial data in transparent or blocked format at rates up to 10 Mbps and provides the following capabilities:

- Inputs pulse code modulation (PCM) data streams
- Decommutation
- Monitors data quality

The serial input logic performs frame synchronization using an adaptive strategy. User-programmable frame sync parameters include sync pattern and mask, frame length, word size, search and lock error tolerances, number of check frames, number of flywheel frames, bit slip window width, auto polarity correction, and data orientation.

The frame synchronizer performs subframe synchronization using the ID counter method. User-programmable sub frame sync parameters include ID counter size, location, orientation, start value, stop value, search and lock error tolerances, check frames, and flywheel frames. It also compiles data quality statistics for each frame received. Status information available to the host includes frame sync state, subframe state, data polarity, frames received, sync pattern bit errors, clock status, dropout count, and bit slip count.

The frame synchronizer is available with the TM1 transition module.

PCM Simulator

- generates and outputs PCM data streams
- uses a variety of frame characteristics and data patterns

The simulator outputs serial data streams from a VME platform using one of two modes. One mode uses the telemetry simulator to output data provided by a host system. The other uses the telemetry simulator to generate a telemetry stream with a variety of frame characteristics and data patterns.

The simulator is used for simple, fixed pattern, telemetry stream generation. User-programmable parameters for the telemetry simulator include frame sync pattern and location, word size, frame length, fill pattern, ID counter range and location, data polarity, and data orientation. The simulator also provides the following fault conditions: sync pattern error, frame counter error, data error, and bit slip insertion.

When a more complex or specific telemetry stream is needed, the PCM simulator will output a data stream that was generated by a simulation running on the host computer in real-time or was stored to a data file. Output data provided by the host is stored in the FSIO2 dual access memory before being transmitted by the serial output module. Alternatively, interrupts to the host are generated when data transfers are completed or error conditions occur.

The simulator also controls the on-board direct digital synthesizer. User-specified parameters include transmit clock source, DDS reference source, and transmit clock frequency.

PCM Simulator is available with the TM1 and TM-SYNTH transition modules.

NASCOM Blocker/Deblocker

The NASCOM blocker/deblocker and the FSIO2 form a fully programmable NASCOM interface device. It can be used for line monitoring, blocking and deblocking of telemetry and commands, and block MUX/DEMUX applications.

The NASCOM blocker/deblocker receives 4800 or 1200 bit NASCOM blocks either back-to-back or with gaps. It performs CRC decoding, block sequence checking, and block filtering based on as many as 4 header fields. Two sets of block filters are available to distinguish between telemetry and non-telemetry blocks. Accepted blocks are stored in the dual-access memory. The data field of accepted telemetry blocks is retransmitted by the serial output for input to a frame synchronizer or data storage device. Non-telemetry blocks are read from the dual-access memory by the host.

The block processor provides status counts to the host including blocks received, blocks accepted, blocks accepted with CRC errors, and blocks accepted with sequence number errors.

The output formatter outputs both host application generated blocks and blocks it creates from the serial input data based on user-specified header information. Host generated blocks are written into the FSIO2 dual access memory. Insertion of the 22-bit CRC remainder

Transition Modules

into transmitted blocks can be enabled or disabled by the host.

The output formatter provides status information to the host including data quality counts for the telemetry stream and a count of blocks transmitted. The output formatter also controls the optional direct digital synthesizer. User-specified parameters include transmit clock source, DDS reference source, and transmit clock frequency.

NASCOM Blocker/Deblocker is available with the TM-CRC and TM-CRC2 transition modules.

System Integration

Avtec provides a range of technical assistance for system integration from software support to turn-key installation. The FSIO2 is compliant with the industry standard VME architecture and will operate with a wide variety of host platforms including embedded CISC or RISC boards and workstations or mainframes with a VME expansion bus. Example device driver code is available for a number of host platforms and operating systems.

The FSIO2 firmware modules provide the flexibility to support a large number of telemetry formats. Special requirements can be met using custom firmware modules. A debug monitor is available to support the development of custom firmware.

The FSIO2 requires a firmware module and a transition module to support each of the functional options. The following table shows the functional options and the transition module requirements.

	Frame Sync	PCM Simulator	NASCOM Blocker/Deblocker
signal level translation	TM-1	TM-1	
signal level translation & local transmit clock synthesizer		TM-SYNTH	
signal level translation & CRC encoding/decoding			TM-CRC
signal level translation & CRC encoding/decoding & local transmit clock synthesizer			TM-CRC2

The FSIO2 supports both RS-422 and TTL data and clock input/output via a transition module that resides in either the rear of the VME chassis or in an adjacent slot. The transition module architecture provides flexibility in adapting a system to specific user requirements. All transition modules provide signal level translation with options that provide CRC encoding/decoding and/or a transmit clock direct digital synthesizer. The transition module options currently available are the TM1, TM-SYNTH, TM-CRC and TM-CRC2. The PCM serial input/output specifications are the same for all of the transition modules.

TM1

The TM1 is a transition module for the FSIO2 that provides signal level translation.

TM-SYNTH

The TM-SYNTH is a transition module for the FSIO2 that provides signal level translation and a local transmit clock synthesizer.

- Direct digital synthesizer with a 32-bit phase accumulator for frequency synthesis
- Output frequency range from 10 Hz to 12 MHz with 5 digit resolution and ± 25 ppm stability

TM-CRC

The TM-CRC is a transition module for the FSIO2 that provides signal level translation and CRC encoding and decoding for connection to the NASCOM network.

- Data rates from 10 bps to 10 Mbps
- NASCOM 24-bit sync 627627 hex MSB transmitted first
- 1200 or 4800 bits per block
- NASCOM 22-bit CRC polynomial
- Selectable error status indication

TM-CRC2

The TM-CRC2 is a transition module for the FSIO2 that provides a direct digital synthesizer (DDS) in addition to all the functionality of the TM-CRC. The TM-CRC2's direct digital synthesizer provides a programmable send timing signal for data output.

Ordering Guide

Part No.	Description
VM-1120-FE	FSIO2 Frame Sync / Simulator with front TM-1
VM-1120-RE	FSIO2 Frame Sync / Simulator with rear TM-1
VM-1130-FE	FSIO2 Frame Sync with front TM-1
VM-1130-RE	FSIO2 Frame Sync with rear TM-1
VM-1140-FE	FSIO2 PCM Simulator with front TM-1
VM-1140-RE	FSIO2 PCM Simulator with rear TM-1
VM-1250-FE	FSIO2 NASCOM Blocker/Deblocker with front TM-CRC
VM-1250-RE	FSIO2 NASCOM Blocker/Deblocker with rear TM-CRC
VM-1350-FE	FSIO2 NASCOM Blocker/Deblocker with front TM-CRC2
VM-1350-RE	FSIO2 NASCOM Blocker/Deblocker with rear TM-CRC2
VM-1420-FE	FSIO2 Frame Sync / Simulator with front TM-SYNTH
VM-1420-RE	FSIO2 Frame Sync / Simulator with rear TM-SYNTH
VM-1440-FE	FSIO2 PCM Simulator with front TM-SYNTH
VM-1440-RE	FSIO2 PCM Simulator with rear TM-SYNTH

Specifications

High Speed Serial Input/Output

Format

- NRZ-L, S, M and BIΦ–L, S, M bit serial data
- Coherent 0 or 180 degree clock, continuous or gated
- Bidirectional, synchronous serial I/O up to 10 Mbps
- 0-64 bit sync pattern with programmable mask & threshold
- Sync pattern first or last in frame
- Auto-polarity correction based on detected sync pattern polarity
- Frame sync acquisition states: Search, Check, Lock and Flywheel
- 0-15 check frames and 0-15 flywheel frames
- Word size from 4 to 16 bits/word
- Minor frame length from 2 to 64K words/frame
- 0 to ± 3 bit slip window
- MSB or LSB first data orientation

Levels

- TTL single ended, 50 Ω termination
- RS-422 differential, 62 Ω termination

Mechanical

- BNC and 9 pin DSUB connectors for TTL level signals
- TRIAX connectors for RS-422 signals

CPU and Memory

- Motorola MC68340 microcontroller with 16.6 MHz clock rate and 2 channel DMA controller
- 4 MB dual-access DRAM with 32-bit wide data path for data buffering and storing downloaded code
- 128 KB of EPROM including self test and boot facilities
- 256 Bytes of EEPROM for configuration data
- Two RS-232 serial ports for debugging and control

VME Interface

- Standard 6U VME card format with P1 and P2 connectors (Also available in 9U format, as seen on opposite page)
- VME interface based on the Cypress VIC068 and VAC068 integrated controller chip
- VMEbus arbiter supports prioritized (PRI), round robin select (RRS), and single level (SGL) arbitration schemes
- VME interrupt handler supports Release on Register Access (RORA) and Release on Acknowledge (ROAK) interrupters
- VMEbus system controller functions:
  - 16 MHz system clock driver
  - System reset generation
  - Arbiter
  - Interrupt Handler
  - VMEbus Timer
- Four level VMEbus requester with Fair Requester mode. Supports Release on Request (ROR), Release when Done (RWD), or Release on Clear (ROC) release modes
- Full Master and Slave VME Interface supporting the following data transfer types:
  - Master: A32, A24, A16: D32, D16, D8(EO)
  - Slave: A32, A24, A16: D32, D16, D8(EO)

  Address only (AO), Unaligned Transfers (UAT), and Read-modify-write (RMW) cycles
- VME block transfers with local DMA up to 30 Mbps with programmable burst length and 256 byte boundary crossing