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SBC82621 Series

Socket370 Half-size
All-in-One CPU Card

User's Manual

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- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before handling a board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. This helps to discharge any static electricity on your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

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Chapter 1
Introduction

1.1 General Description



The **SBC82621** is an industrial grade CPU card. It provides reliable high performance and function-rich capability.

The CPU incorporates the VIA VT8606 chipset and the VT82C686B with built-in AGP-4x VGA controller. This combination ensures its compatibility with ISA bus passive backplanes.

Designed for the professional embedded developers, the Socket370 all-in-one **SBC82621** CPU card is virtually the ultimate one-step solution to various applications.

1.2 Specifications

- **CPU: Intel Celeron, Pentium III, Tualatin and VIA Cyrix III**
- **System Chipset: VIA TwisterT (PN133T) VT8606, VT82C686B with integrated real-time clock**
- **BIOS: Award PnP BIOS**
- **Standard I/O:**
  - Two serial ports; 1x RS-232, 1x RS-232/422/485
  - 1 x parallel port, SPP/EPP/ECP
  - 1 x IDE Interface
  - 1 x FDD Interface
  - 1 x PS/2 Keyboard Interface
  - 1 x PS/2 Mouse Interface
  - 1 x IrDA interface for wireless communication
- **System Memory:**
  - 1 x 168-pin DIMM socket
  - Maximum of 512MB SDRAM
  - ECC/parity checking
- **L2 Cache: integrated in CPU**
- **Watchdog Timer:**
  - Generates a system reset or NMI by jumper selectable
  - Software programmable time interval
  - 64 levels, 0.5~8/5~80/50~800/100~1600 seconds
- **Ethernet:**
  - Dual Realtek 8100C PCI Bus 10/100M Base-T or One Realtek 8100C PCI Bus 10/100M Base-T 、Realtek 8110s PCI Bus 10/100/1000M Base-T
  - Wake On LAN (via ATX power supply)
  - Onboard RJ-45 connector

- **VGA/Flat Panel Controller:**
  - AGP interface controller with integrated system main-memory supporting CRT/LCD displays
  - Supports up to 1280 x 1024 256-color resolution on non-interlaced CRT monitors, and 1024 x 768 16 bit-color on LCD panel monitors
- **USB Interface: use a VIA VT6212 4-Port Host Controller support two ports; USB Spec. Rev. 2.0 compliant**
- **DiskOnChip®: ports DisksupOnChip®**
- **Expansion Slots: one 16-bit PC/104 connector**
- **Dimensions: 121.92 x 185 mm**

NOTE: *Specifications are subject to change without notice.*

1.3 Utilities Supported

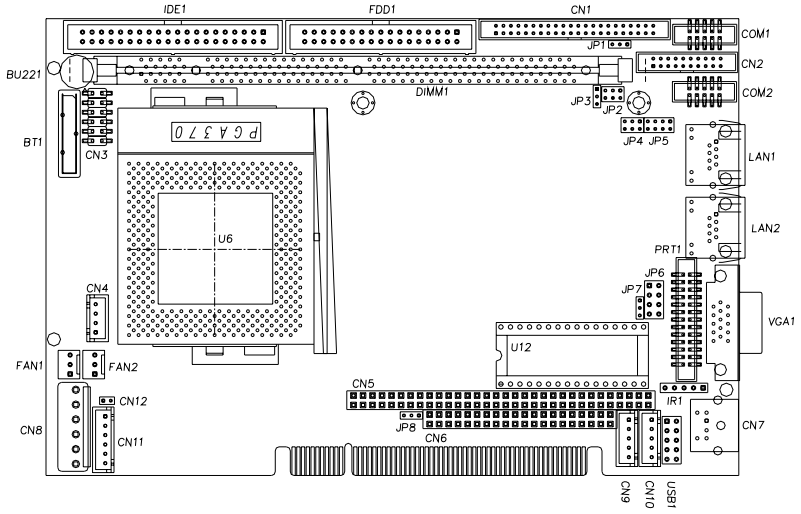
- **VIA Chipset Drivers**
- **Ethernet Utility**
- **Flat panel/CRT Drivers**
- **System Doctor**

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Chapter 2
Jumpers and Connectors

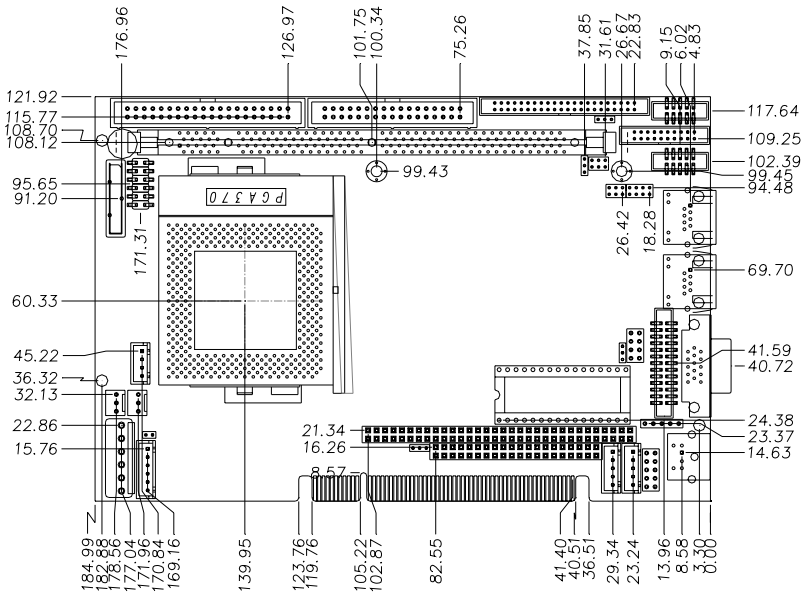
2.1 Jumpers and Connectors Layout

The following figure shows the layout of all jumpers and connectors on the **SBC82621** CPU card.



2.2 Jumpers and Connectors Dimensions

The following figure shows the location of all jumpers and connectors on the **SBC82621** CPU card.



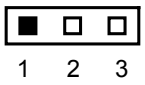
2.3 Jumper Settings

Making the proper jumper settings configures the **SBC82621** to match the needs of your application. The following tables show the correct jumper settings for the onboard devices.

Jumper	Default Setting	Jumper Setting
JP1	Connector LCD Power Selection: VDDM at 5V	Short 2-3
JP2	COM2 Port Setting: RS-232	Short 3-5, 4-6
JP3	Watchdog Trigger Mode: Disabled	Open
JP4	COM2 Port Setting: RS-232	Short 3-5, 4-6
JP5	COM2 Port Setting: RS-232	Short 1-2
JP6	DiskOnChip Memory Segment : D0000-D1FFF	Short 1-2
JP7	USB Wake-Up Selection: Disabled	Short 2-3
JP8	Clear CMOS Setting: Normal	Short 1-2

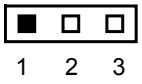
2.3.1 Watchdog Trigger Mode Setting: JP3

The watchdog timer is an indispensable feature of the **SBC82621**. It has a sensitive error detection function and a report function. When the CPU processing comes to a halt, the watchdog either generates a NMI or resets the CPU.



Options	Setting
NMI	Short 1-2
RESET	Short 2-3
Disabled (default)	Open

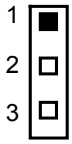
2.3.2 CMOS Clear Jumper: JP8



Options	Settings
Clear CMOS	Short 2-3
Normal (default)	Short 1-2

2.3.3 Power Selection of Flat Panel Connector (VDDM of CN1): JP1

SBC82621 supports +3.3V or +5V flat panel displays. When using such type of flat panels, configure jumper **JP1** to the appropriate voltage of the flat panel.

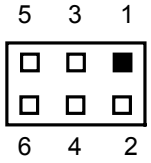


VDDM	Settings
5V (default)	Short 2-3
3.3V	Short 1-2

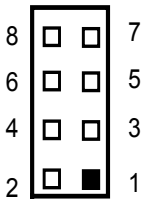
2.3.4 COM RS232/422/485 Settings: JP2, JP4, JP5

COM4	JP2	JP4	JP5
RS-232 (default)	Short 3-5, 4-6	Short 3-5, 4-6	Short 1-2
RS-422	Short 1-3, 2-4	Short 1-3, 2-4	Short 3-4
RS-485	Short 1-3, 2-4	Short 1-3, 2-4	Short 5-6, 7-8

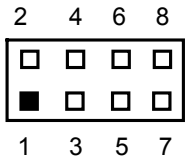
JP2 and JP4



JP5

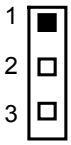


2.3.5 DiskOnChip® Memory Segment: JP6



Options	Settings
D0000 – D1FFF (default)	Short 1-2
D2000-D3FFF	Short 3-4
D4000-D5FFF	Short 5-6
D6000-D7FFF	Short 7-8

2.3.6 USB Wake-Up Settings: JP7



Options	Settings
Enabled (default)	Short 1-2
Disabled	Short 2-3

2.4 Connectors

The connectors allow the CPU card to connect with other parts of the system. Some problems encountered by your system may be a result from loose or improper connections. Ensure that all connectors are in place and firmly attached. The following table lists the function of each connector on the **SBC82621**.

Connectors	Label
IDE Connector	IDE1
FDD Connector	FDD1
44-pin LCD Connector	CN1
20-pin LCD Connector	CN2
Flat Panel Bezel Connector	CN3
Power Input Connectors	CN4 & CN8
PC104 Connector	CN5 & CN6
PS/2 Keyboard and Mouse Connector	CN7
Keyboard Connector	CN9
Mouse Connector	CN10
ACPI Connector	CN11
ATX PS_ON Switch	CN12
Printer Port Connector	PRT1
VGA Connector	VGA1
IrDA Connector	IR1
COM1	COM1
COM2	COM2
USB Connector	USB1
Ethernet1 Connector	LAN1
Ethernet2 Connector	LAN2
CPU Fan Connector	FAN1 & FAN2

2.4.1 VGA Interface

2.4.1.1 Flat Panel/CRT Interface Controller

The VT8606 built-in a high-performance flat panel/super VGA display controller (S3 Savage4) on chipset. TheVGA RAM use system main-memory. It is capable of driving a wide array of flat panel and CRT displays. It can also support CRT at a maximum resolution of up to 1920x1440 with 24-bits colors, and panel resolutions of up to 1280x1024. It displays up to 226,981 different colors on passive DSTN/TFT flat panels and up to 16M colors on 36-bit active matrix flat panels.

2.4.1.2 Features

- Fully compatible with IBM™ VGA
- Flat panel and CRT monitor can be displayed simultaneously
- The VGA RAM support system main-memory up to 64MB
- Supports panel resolution up to 1280x1024
- Supports non-interlaced CRT monitors with resolutions up to 1920x1440 24-bits colors
- Direct interface to Color and Monochrome Dual Drive and Single Drive panels
- SMARTMAP™ intelligent color to gray scale conversion enhances text legibility
- Integrated programmable linear address feature accelerates GUI performance
- Hardware Windows acceleration
- Built-in 44 pins general purpose connector for flat panel display, and an extended 20-pin for 36 bit XVGA flat panel

2.4.1.3 VGA/Flat Panel Connector: VGA1, CN1, CN2

The **SBC82621** has three connectors that support CRT VGA and flat panel displays, individually or simultaneously. **VGA1** is a standard 15-pin pin header connector commonly used for the CRT VGA display, and **CN1** (44-pin) **CN2** (20-pin) are dual-in-line headers for flat panel connection. Configuration of the VGA interface is done via the software utility and no jumper setting is required. The following two tables are the pin assignments for the CRT/VGA connector and the flat panel connector.

VGA1: CRT/VGA Connector Pin Assignment

Pin	Description	Pin	Description	Pin	Description
1	Red	2	Green	3	Blue
4	N/A	5	GND	6	AGND
7	AGND	8	AGND	9	N/A
10	GND	11	N/A	12	DDC DAT
13	Horizontal Sync	14	Vertical Sync	15	DDC CLK

CN1: Flat Panel Connector Pin Assignment

Pin	Description	Pin	Description	Pin	Description
1	-12V	2	+12VM	3	GND
4	GND	5	VDDM	6	VDDM
7	ENAVEE	8	GND	9	P0
10	P1	11	P2	12	P3
13	P4	14	P5	15	P6
16	P7	17	P8	18	P9
19	P10	20	P11	21	P12
22	P13	23	P14	24	P15
25	P16	26	P17	27	P18
28	P19	29	P20	30	P21
31	P22	32	P23	33	GND
34	GND	35	SHFCLK	36	FLM
37	M	38	LP	39	GND
40	ENABKL	41	GND	42	-SHFCLK
43	VDDM	44	VDDM		

CN2: Flat Panel Connector for XVGA

Pin	Description	Pin	Description	Pin	Description
1	GND	2	GND	3	P24
4	P25	5	P26	6	P27
7	P28	8	P29	9	GND
10	GND	11	P30	12	P31
13	P32	14	P33	15	P34
16	P35	17	VDDM	18	VDDM
19	+12VM	20	+12VM		

2.1.4.4 Flat Panel Connector Pin Description

Name	Description
P0~P35	Flat panel data output
ENABKL	Activity Indicator and Enable Backlight outputs
SHFCLK	Shift clock. Pixel clock for flat panel data
M	M signal for panel AC drive control
LP	Latch pulse. Flat panel equivalent of HSYNC
FLM	First line marker. Flat panel equivalent of VSYNC
+12VM	+12V power controlled by chipset
ENAVEE / ENAVDD	Power sequencing controls for panel LCD bias volt
VDDM	3.3V or 5V power controlled by chipset and selected by JP1

Flat Panel Interface Pins for Color DSTN and Color TFT LCD (Twister-T VT8606)

Pin	STN			DSTN
	8-bit	16-bit	24-bit	8-bit
LP	LP	LP	HSYNC	HSYNC
FLM	FP	FP	VSYNC	VSYNC
SHFCLK	XCK	XCK	CK	CK
M	DE	DE	DE	DE
ENAVDD	ENAVDD	ENAVDD	ENAVDD	ENAVDD
ENABLK	ENABLK	ENABLK	ENABLK	ENABLK
P0	R0	R0	R0	LR0
P1	G0	G0	G0	
P2	B0	B0	B0	LG0
P3	R1	R1	R1	
P4	G1	G1	G1	LB0
P5	B1	B1	B1	
P6	R2	R2	R2	LR1
P7	G2	G2	G2	
P8		B2	B2	
P9		R3	R3	
P10		G3	G3	
P11		B3	B3	
P12		R4	R4	
P13		G4	G4	
P14		B4	B4	
P15		R5	R5	
P!6			G5	
P17			B5	
P18			R6	UR0
P19			G6	
P20			B6	UG0
P21			R7	
P22			G7	UB0
P23			B7	
P24				UR1

Pin	DSTN		TFT	
	16-bit	24-bit	9-bit	2X9-bit
LP	LP	LP	HSYNC	HSYNC
FLM	FP	FP	VSYNC	VSYNC
SHFCLK	XCK	XCK	CK	CK
M	DE	DE	DE	DE
ENAVDD	ENAVDD	ENAVDD	ENAVDD	ENAVDD
ENABLK	ENABLK	ENABLK	ENABLK	ENABLK
P0		LB3		
P1		LB2		
P2	LB1	LB1		
P3	LB0	LB0		
P4		UB3		
P5		UB2		
P6	UB1	UB1	R0	R00
P7	UB0	UB0		R10
P8		LG3	R1	R01
P9		LG2		R11
P10	LG1	LG1	R2	R02
P11	LG0	LG0		R12
P12		UG3		
P13		UG2		
P14	UG1	UG1		
P15	UG0	UG0		
P!6		LR3		
P17		LR2		
P18	LR1	LR1	G0	G00
P19	LR0	LR0		G10
P20		UR3	G1	G01
P21		UR2		G11
P22	UR1	UR1	G2	G02
P23	UR0	UR0		G12
P30			B0	B00
P31				B10
P32			B1	B01
P33				B11
P34			B2	B02
P35				B12

Pin	TFT		TFT	
	12-bit	2X12-bit	15-bit	2X15-bit
LP	LP	LP	HSYNC	HSYNC
FLM	FP	FP	VSYNC	VSYNC
SHFCLK	XCK	XCK	CK	CK
M	DE	DE	DE	DE
ENAVDD	ENAVDD	ENAVDD	ENAVDD	ENAVDD
ENABLK	ENABLK	ENABLK	ENABLK	ENABLK
P0				
P1				
P2			R0	R00
P3				R10
P4	R0	R00	R1	R01
P5		R10		R11
P6	R1	R01	R2	R02
P7		R11		R12
P8	R2	R02	R3	R03
P9		R12		R13
P10	R3	R03	R4	R04
P11		R13		R14
P12				
P13				
P14			G0	G00
P15				G10
P!6	G0	G00	G1	G01
P17		G10		G11
P18	G1	G01	G2	G02
P19		G11		G12
P20	G2	G02	G3	G03
P21		G12		G13
P22	G3	G03	G4	G04
P23		G13		G14
P24				
P25				
P26			B0	B00
P27				B10

Pin	TFT		TFT	
	12-bit	2X12-bit	15-bit	2X15-bit
P28	B0	B00	B1	B01
P29		B10		B11
P30	B1	B01	B2	B02
P31		B11		B12
P32	B2	B02	B3	B03
P33		B12		B13
P34	B3	B03	B4	B04
P35		B13		B14

Pin	TFT		TFT	
	18-bit	24-bit	2X18-bit	
LP	LP	LP	HSYNC	
FLM	FP	FP	VSYNC	
SHFCLK	XCK	XCK	CK	
M	DE	DE	DE	
ENAVDD	ENAVDD	ENAVDD	ENAVDD	
ENABLK	ENABLK	ENABLK	ENABLK	
P0		B0	R00	
P1		B1	R10	
P2	B0	B2	R01	
P3	B1	B3	R11	
P4	B2	B4	R02	
P5	B3	B5	R12	
P6	B4	B6	R03	
P7	B5	B7	R13	
P8		G0	R04	
P9		G1	R14	
P10	G0	G2	R05	
P11	G1	G3	R15	
P12	G2	G4	G00	
P13	G3	G5	G10	
P14	G4	G6	G01	
P15	G5	G7	G11	
P16		R0	G02	
P17		R1	G12	
P18	R0	R2	G03	
P19	R1	R3	G13	

Pin	TFT		TFT	
	18-bit	24-bit	2X18-bit	
P20	R2	R4	G04	
P21	R3	R5	G14	
P22	R4	R6	G05	
P23	R5	R7	G15	
P24			B00	
P25			B10	
P26			B01	
P27			B11	
P28			B02	
P29			B12	
P30			B03	
P31			B13	
P32			B04	
P33			B14	
P34			B05	
P35			B15	

2.4.2 Floppy Disk Controller

The **SBC82621** provides a 34-pin header type connector, **FDD1**, supporting up to two floppy drives. The floppy drives may be any one of the following types: 5.25" 360KB/1.2MB and 3.5" 720KB/1.44MB/2.88MB. The **FDD1** pin assignment is listed in Appendix B.

2.4.3 Parallel Port Interface

The **SBC82621** onboard **PRT1** is a multi-mode parallel port able to support:

- **Standard mode:** IBM PC/XT, PC/AT and PS/2™ compatible with bi-directional parallel port
- **Enhanced mode:** Enhance parallel port (EPP) compatible with EPP 1.7 and EPP 1.9 (IEEE 1284 compliant)
- **High speed mode:** Microsoft and Hewlett Packard extended capabilities port (ECP) IEEE 1284 compliant

The address select of the onboard parallel port in LPT1 (3BCH) or disabled is done by BIOS CMOS setup.

2.4.4 Serial Port Interface

The serial interface onboard **SBC82621** consists of COM1 port supports RS-232 and COM2 provide RS-232/422/485 connectivity.

2.4.4.1 Serial Ports IRQ Selection

SBC82621 uses two 10-pin connectors for COM2 **(COM2)** and COM1 **(COM1)**. Interrupt Requests on COM1 and COM2 are selected via IRQ4 and IRQ3 respectively. Additionally, both ports can be enabled or disabled via BIOS setting. The RS-232 pin assignments for COM1 and COM2 along with the RS-485 pin assignments for COM2 are in Appendix B.

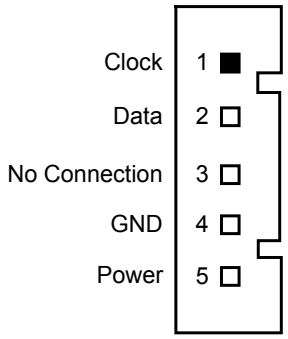
2.4.5 Real Time Clock and CMOS RAM

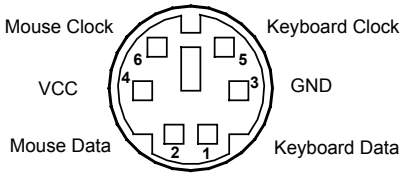
The **SBC82621** contains VT82C686B Integrated Real Time Clock (RTC) and 128 bytes of CMOS RAM. The CMOS RAM stores the system configuration information entered via the SETUP program. A battery, with power lasting 10 years, keeps the stored information on the RTC and CMOS RAM active when system power is turned off.

2.4.6 Keyboard and Mouse Connectors

The **SBC82621** provides a keyboard **(CN9)** and mouse **(CN10)** interface with a 5-pin connector. **CN7** is a DIN connector for PS/2 keyboard and mouse connection.

CN9/CN10



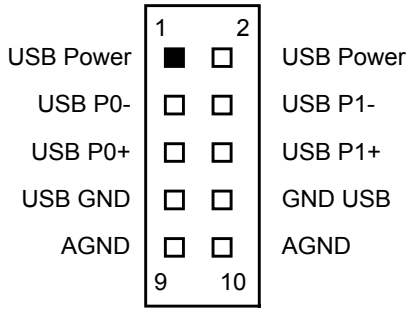


CN7

2.4.7 USB Connector

The Universal Serial Bus (USB) connector on the **SBC82621** is for installation of peripherals supporting the USB interface. **USB1** is the 10-pin USB connector on the **SBC82621**.

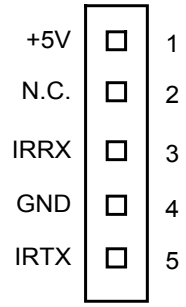
USB1



2.4.8 IrDA Connector

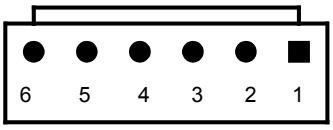
IR1 is a 5-pin IrDA connector for wireless communication.

IR1



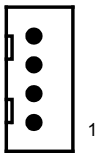
2.4.9 Power Input Connectors

CN8 is the +5V/+12V power input connector of the **SBC82621**. The **SBC82621** needs +5V and +12V for normal operation.



Pin	Description
1	+5V
2	GND
3	+12V
4	SB5V
5	GND
6	+5V

CN4, on the other hand, is the –5V and –12V power input connector of **SBC82621**. The corresponding pin assignment is listed on the table below.

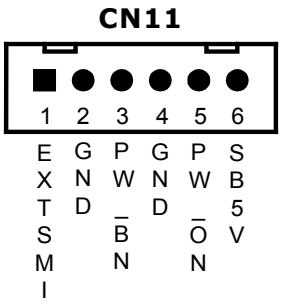


Pin	Description
1	-12V
2	GND
3	GND
4	-5V

2.4.10 ACPI Connector

Advanced Configuration and Power Interface (ACPI) defines a flexible and extensible interface that allows system designers to select appropriate cost/feature trade-offs for power management. The interface enables and supports reliable power management through improved hardware and operating system coordination. The specification enables new power management technology to evolve independently in operating systems and hardware while ensuring that they continue to work together.

CN11 on the **SBC82621** is a 6-pin header connector that provides ACPI interface.



2.4.11 PC/104 Connectors

The PC/104 is an industrial standard. It is a compact form factor with dimensions of 3.6" x 3.8" and is fully compatible with the ISA Bus. The PC/104 interface is able to adapt the off-the-shelf PC/104 modules, such as sound module, fax modem module and multi-I/O module…etc.

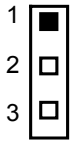
CN5: PC/104 Bus Pin Assignment

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	IOCHCHK	2	GND	3	SD7	4	RESETDRV
5	SD6	6	+5V	7	SD5	8	IRQ9
9	SD4	10	-5V	11	SD3	12	DRQ2
13	SD2	14	-12V	15	SD1	16	ENDXFR
17	SD0	18	+12V	19	IOCHRDY	20	GND
21	AEN	22	SMEMW	23	SA19	24	SMEMR
25	SA18	26	IOW	27	SA17	28	IOR
29	SA16	30	DACK3	31	SA15	32	DRQ3
33	SA14	34	DACK1	35	SA13	36	DRQ1
37	SA12	38	REFRESH	39	SA11	40	SYSCLK
41	SA10	42	IRQ7	43	SA9	44	IRQ6
45	SA8	46	IRQ5	47	SA7	48	IRQ4
49	SA6	50	IRQ3	51	SA5	52	DACK2
53	SA4	54	TC	55	SA3	56	SALE
57	SA2	58	+5V	59	SA1	60	OSC
61	SA0	62	GND	63	GND	64	GND

CN6: PC/104 Bus Pin Assignments

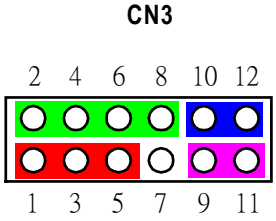
Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	GND	2	GND	3	MEMCS16	4	SBHE
5	IOCS16	6	LA23	7	IRQ10	8	LA22
9	IRQ11	10	LA21	11	IRQ12	12	LA20
13	IRQ15	14	LA19	15	IRQ14	16	LA18
17	DACK0	18	LA17	19	DRQ0	20	MEMR
21	DACK5	22	MEMW	23	DRQ5	24	SD8
25	DACK6	26	SD9	27	DRQ6	28	SD10
29	DACK7	30	SD11	31	DRQ7	32	SD12
33	+5V	34	SD13	35	MASTER	36	SD14
37	GND	38	SD15	39	GND	40	(KEY)

2.4.12 CPU Fan Connector: FAN1 & FAN2



Pin	Description
1	GND
2	+5V
3	SPEED SENSOR

2.4.13 Flat Panel Bezel Connector



- **Power LED**

  This 2-pin connector, designated at Pins 1 and Pin 5 of CN3, connects the system power LED indicator to its respective switch on the case. Pin 1 is +, and pin 5 is assigned as -. The Power LED lights up when the system is powered ON.

- **External Speaker and Internal Buzzer Connector**

  Pins 2, 4, 6, and 8 of CN3 connect to the case-mounted speaker unit or internal buzzer. Short pins 4-6 when connecting the CPU card to an internal buzzer. When connecting an external speaker, set these jumpers to Open and install the speaker cable on pin 8 (+) and pin 2 (-).

- **System Reset Switch**

  Pins 9 & 11 of CN3 connect to the case-mounted reset switch and allow rebooting of your computer instead of turning OFF the power switch. This is a preferred method of rebooting in order to prolong the life of the system's power supply.

- **HDD Activity LED**

  This connector extends to the hard drive activity LED on the control panel. This LED will flash when the HDD is being accessed. Pins 10 & 12 of CN3 connect the hard disk drive and the front panel HDD LED. Pins 10 is -, and pin 12 is assigned as +.

2.4.14 Enhanced IDE Interface Connector

The **SBC82621** includes a PCI bus enhanced IDE controller that can support master/slave mode and post write transaction mechanisms with 64-byte buffer, and master data transaction. This feature, connected via connector IDE1, allows the **SBC82621** to handle 2 IDE drives. Refer to Appendix B for the pinout assignments of IDE1.

Chapter 3
Hardware Description

This chapter gives a detailed explanation of the hardware features onboard the **SBC82621** all-in-one Socket370 CPU cards.

3.1 Microprocessors

The **SBC82621** supports Intel Celeron, Pentium III,Tualatin and VIA Cyrix III CPUs. Systems based on these CPUs can be operated under UNIX, OS/2, Windows XP/NT/2000/98/Me and MS-DOS environments. The system's performance depends on the installed CPU on the board.

3.2 CPU Bus Clock

The **SBC82621** support CPU Bus speeds for 66M, 100M and 133MHz.The CPU Bus Clock is auto detected and generated by a clock generator.

3.3 BIOS

The system BIOS used in **SBC82621** is Award Plug and Play BIOS. The **SBC82621** contains a single 4M bit Flash EPROM.

3.4 System Memory

The **SBC82621** inductrial CPU board supports one 168-pin DIMM (Dual In-Line Memory Module) socket for a maximum memory of 256MB buffer SDRAMs. The memory module can come in sizes of 16MB, 32MB, 64MB, 128MB, 256MB and 512MB.

NOTE: Use SDRAM modules with PC100 or PC133 specifications when running 100MHz CPU bus speed. With 66MHz CPU, SDRAM modules with PC66, PC100 or PC133 specifications can be used. You have to install the Intel Celeron processor before installing the memory modules

3.5 Real Time Clock and CMOS RAM

The **SBC82621** contains VT82C686B Integrated Real Time Clock (RTC) and 128 bytes of CMOS RAM. The CMOS RAM stores the system configuration information entered via the SETUP program. A battery, with power lasting 10 years, keeps the stored information on the RTC and CMOS RAM active when system power is turned off.

3.6 VGA Interface

The Twister-T integrates S3 Graphics '128-bit ProSavage4 graphics accelerator into a single chip. TwisterT brings mainstream graphics performance to the Value PC with leading-edge 2D, 3D and DVD video acceleration into a cost effective package. Based on its capabilities, Twister-T is an ideal solution for the consumer, corporateration users and entry-level professionals. The industry's first integrated AGP 4X solution, TwisterT combines AGP 4X performance with Microsoft Direct-X texture compression and passive 2Kx2K textures to deliver unprecedented 3D.

- **High-Performance 3D Accelerator**
- **128-bit 2D Graphics Engine**
- **DVD Playback and Video conferencing**
- **LCD and Flat Panel Monitor Support**
- **High Screen Resolution CRT Support**

3.7 I/O Port Address Map

The CPU card communicates via I/O ports. It has a total of 1KB port addresses that can be assigned to other devices via I/O expansion cards.

Address	Devices
000-01F	DMA controller #1
020-03F	Interrupt controller #1
040-05F	Timer
060-06F	Keyboard controller
070-07F	Real time clock, NMI
080-09F	DMA page register
0A0-0BF	Interrupt controller #2
0F0	Clear math coprocessor busy signal
0C0-0DF	DMA controller #2
0F1	Reset math coprocessor
0F8-0FF	Math processor
120	Disable watchdog timer operation (read)
121	Enable watchdog timer operation (read)
122	Watchdog
123	Board ID
1F0-1F8	Fixed disk controller
200-207	Game port
300-31F	Prototype card
360-36F	Reserved
378-37F	Parallel port #1
3B0-3BF	MDA video card (including LPT1)
3C0-3CF	EGA card
3D0-3DF	CGA card
3F0-3F7	Floppy disk controller
3F8-3FF	Serial port #1 (COM1)
2F8-2FF	Serial port #2 (COM2)

3.8 Interrupt Controller

The **SBC82621** is a fully PC compatible control board. It consists of 16 ISA interrupt request lines and 4 of the 16 can be either ISA or PCI. The mapping list of the 16 interrupt request lines is shown below.

NMI	Parity check error
IRQ0	System timer output
IRQ1	Keyboard
IRQ2	Interrupt rerouting from IRQ8 through IRQ15
IRQ3	Serial port #2
IRQ4	Serial port #1
IRQ5	Reserved
IRQ6	Floppy disk controller
IRQ7	Parallel port #1
IRQ8	Real time clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	USB
IRQ12	PS/2 Mouse
IRQ13	Math coprocessor
IRQ14	Primary IDE channel
IRQ15	Secondary IDE Channel

Chapter 4
Award BIOS Utility

Chapter 7 describes the different settings available in the Award BIOS that comes with the **SBC82621** CPU card. Also contained here are instructions on how to set up the BIOS configuration.

4.1 BIOS Introduction

The Award BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors in a standard IBM-AT compatible I/O system. The BIOS provides critical low-level support for standard devices such as disk drives, serial and parallel ports. It also adds virus and password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

4.2 BIOS Setup

The Award BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn ON the computer, the Award BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system OFF and back ON again. The following message will appear on the screen:

Press <DEL> to Enter Setup

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

CMOS Setup Utility-Copyright © 1984-2001 Award Software	
▸ Standard CMOS Features	▸ Frequency/Voltage Control
▸ Advanced BIOS Features	Load Fail-Safe Defaults
▸ Advanced Chipset Features	Load Optimized Defaults
▸ Integrated Peripherals	Set Supervisor Password
▸ Power Management Setup	Set User Password
▸ PnP/PCI Configurations	Save & Exit Setup
▸ PC Health Status	Exit Without Saving
Esc : Quit F9 : Menu in BIOS ↑ ↓ → ← : Select Item F10 : Save & Exit Setup	
F6 : SAVE CMOS TO BIOS	F7 : LOAD CMOS FROM BIOS
Time, Date, Hard Disk Type...	

The section below the setup items of the Main Menu displays the control keys for this menu. Another section located at the bottom of the Main Menu, just below the control keys section, displays information on the currently highlighted item in the list.

NOTE: *If you find that your computer cannot boot after making and saving system changes with Setup, the Award BIOS, via its built-in override feature, resets your system to the CMOS default settings.*

We strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your system manufacturer to provide the absolute maximum performance and reliability.

4.2.1 Standard CMOS Setup

"Standard CMOS Setup" allows you to record some basic hardware configurations in your computer system and set the system clock and error handling. If the motherboard is already installed in a working system, you will not need to select this option. You will need to run the Standard CMOS option, however, if you change your system hardware configurations, the onboard battery fails, or the configuration stored in the CMOS memory was lost or damaged.

CMOS Setup Utility-Copyright © 1984-2001 Award Software
Standard CMOS Features

Date (mm:dd:yy)	Fri, Feb 22 2002	Item Help
Time (hh:mm:ss)	16 : 48 : 51	
		Menu Level ▶
▶ IDE Primary Master	Press Enter None	
▶ IDE Primary Slave	Press Enter None	Press [Enter] to enter next page for detail hard drive settings
Drive A	1.44M, 3.5 in.	
Drive B	None	
LCD Type	T1 1024x768 DSTN	
CRT Screen Expansion	Enabled	
Display Type During POST	Default	
Display Type After POST	Default	
Halt On	All, But Keyboard	
Base Memory	640K	
Extended Memory	65472K	
Total Memory	1024K	

↑↓→← : Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

At the bottom of the menu are the control keys for use on this menu. If you need any help in each item field, you can press the <F1> key. It will display the relevant information to help you. The memory display at the lower right-hand side of the menu is read-only. It will adjust automatically according to the memory changed. The following pages describe each item of this menu.

- **Date**

  The date format is:

Day	the day of week, from Sun to Sat, determined by the BIOS, is read only
Month	the month, Jan (1) through Dec (12)
Date	the date, from 1 to 31 (or the maximum allowed in the month), can key in the numerical / function key
Year	the year, from 1994 to 2079

  To set the date, highlight the "Date" field and use the PageUp/ PageDown or +/- keys to set the current time.

- **Time**

  The time format is:

Hour	From 00 to 23
Minute	From 00 to 59
Second	From 00 to 59

  To set the time, highlight the "Time" field and use the <PgUp>/ <PgDn> or +/- keys to set the current time.

- **Drive A / Drive B**

  These fields identify the types of floppy disk drive A or drive B that has been installed in the computer. The available specifications are:

360K, 5.25 in	5.25 inch PC-type standard drive; 360Kb capacity
1.2M, 5.25 in	5.25 inch AT-type high-density drive; 1.2MB capacity
720K, 3.5 in	3.5 inch double-sided drive; 720Kb capacity
1.44M, 3.5 in	3.5 inch double-sided drive; 1.44MB capacity
2.88M, 3.5 in	3.5 inch double-sided drive; 2.88MB capacity

- **LCD Type**

  Although the system chipset already supports VGA and LCD alike, BIOS Features Setup still expands this feature further with the option to set any of the 15 LCD types. The available options are:

■ Type 1/13	1024 x 768	DSTN
■ Type 2	1280 x 1024	TFT
■ Type 3	640 x 480	DSTN
■ Type 4	800 x 600	DSTN
■ Type 5	640 x 480 (16bit)	TFT
■ Type 6	640 x 480 (24bit)	TFT
■ Type 7	1024 x 768	TFT
■ Type 8/9/10	800 x 600	TFT
■ Type 11/12	800 x 600	DSTN
■ Type 14	1280 x 1024	DSTN
■ Type 15	1024 x 600	DSTN

- **CRT Screen Expansion**

  This option allows you to enlarge application screens to full screen scale onto your display. However this option is not inversely compatible, rendering no change when applications screens have resolutions larger than the display resolution. The available options are Enabled and Disabled.

- **Display Type During/After POST**

  This item configures the viewing area for the POST sequence. When configured to the *incorrect display setting* or *Both*, it blankets the POST sequence from being viewed. If you select *Default*, this option is useless and follows the VGA BIOS settings. The available options are CRT Only, LCD Only, Both, and Default.

- **Halt On**

  This field determines whether the system will halt if an error is detected during power up.

No errors	The system boot will halt on any error detected.
All errors	Whenever the BIOS detects a non-fatal error, the system will stop and you will be prompted.
All, But Keyboard	The system boot will not stop for a keyboard error; it will stop for all other errors.
All, But Diskette	The system boot will not stop for a disk error; it will stop for all other errors.
All, But Disk/Key	The system boot will not stop for a keyboard or disk error; it will stop for all other errors.

4.2.2 Advanced BIOS Features

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

CMOS Setup Utility-Copyright © 1984-2001 Award Software
Advanced BIOS Features

Virus Warning	Disabled	Item Help
CPU Internal Cache	Enabled	
External Cache	Enabled	Menu Level ►
CPU L2 Cache ECC Checking	Enabled	Allows you to
Processor Number Feature	Enabled	choose the VIRUS
Quick Power On Self Test	Enabled	Warning feature
First Boot Device	HDD-0	for IDE Hard disk
Second Boot Device	Floppy	boot sector
Third Boot Device	SCSI	protection. If this
Boot Other Device	Enabled	function is enable
Swap Floppy Drive	Disabled	and someone
Boot Up Floppy Seek	Disabled	attempts to write
Boot Up NumLock Status	On	data into this area,
Gate A20 Option	Normal	BIOS will show
Typematic Rate Setting	Disabled	a warning
Typematic Rate (Chars/Sec)	6	message on
Typematic Delay (Msec)	250	screen and alarm
Security Option	Setup	beep
PS/2 Mouse Function Control	Enabled	
OS Select for DRAM >64MB	Non-OS2	
Video BIOS Shadow	Enabled	
C8000-CBFFF	Disabled	
CC000-CFFFF	Disabled	
D0000-D3FFF	Disabled	
D4000-D7FFF	Disabled	
D8000-D8FFF	Disabled	
DC000-DFFFF	Disabled	
Small Logo(EPA) Show	Disabled	

↑↓→← : Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

- **Virus Warning**

  This item protects the boot sector and partition table of your hard disk against accidental modifications. If an attempt is made, the BIOS will halt the system and display a warning message. If this occurs, you can either allow the operation to continue or run an anti-virus program to locate and remove the problem.

  NOTE: *Many disk diagnostic programs, which attempt to access the boot sector table, can cause the virus warning. If you will run such a program, disable the Virus Warning feature.*

- **CPU Internal Cache / External Cache**

  Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPUs from 486-type on up contain internal cache memory, and most, but not all, modern PCs have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU. These items allow you to enable (speed up memory access) or disable the cache function. By default, these are ***Enabled***.

- **CPU L2 Cache ECC Checking**

  When enabled, this allows ECC checking of the CPU's L2 cache. By default, this field is ***Enabled***.

- **Processor Number Feature**

  When a Pentium® III CPU is installed, the system automatically detects it and displays this item.

- **Quick Power On Self Test**

  When enabled, this field speeds up the Power On Self Test (POST) after the system is turned ON. If it is set to *Enabled*, BIOS will skip some items.

- **First/Second/Third Boot Device**

  These items allow the selection of the 1st, 2nd, and 3rd devices that the system will search for during its boot-up sequence. The wide range of selection includes Floppy, LS120, ZIP100, HDD0~3, SCSI, and CDROM.

- **Boot Other Device**

  This item allows the user to enable/disable the boot device not listed on the First/Second/Third boot devices option above. The default setting is ***Enabled***.

- **Swap Floppy Drive**

  This allows you to determine whether to enable Swap Floppy Drive or not. When enabled, the BIOS swaps floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A. By default, this field is set to ***Disabled.***

- **Boot Up Floppy Seek**

  When enabled, the BIOS seeks for number of track (40 or 80) of the installed floppy drive. 360K type has 40 tracks while 760K, 1.2M and 1.44M have 80 tracks. By default, this field is set to ***Enabled.***

- **Boot Up NumLock Status**

  This activates the NumLock function after powering up the system. By default, the system boots up with ***NumLock*** ON.

- **Gate A20 Option**

  This selects how Gate A20 is worked. Gate A20 is a device used to address memory above 1 MB. The default setting is ***Fast.***

- **Typematic Rate Setting**

  When disabled, continually holding down any key on your keyboard will generate only one instance. When enabled, you can set the two typematic controls listed next. By default, this field is set to ***Disabled.***

- **Typematic Rate (Chars/Sec)**

  When the typematic rate is enabled, the system registers repeated keystrokes speeds. You can select speed range from 6 to 30 characters per second. By default, this item is set to ***6.***

- **Typematic Delay (Msec)**

  When typematic rate is enabled, this item allows you to set the time interval between the display of the first and second characters. By default, this item is set to ***250msec***.

- **Security Option**

  This allows you to limit access to the System and Setup. The default value is ***Setup***. When set to *System,* the system prompts for the User Password every boot up. Selecting *Setup* always boots up and prompts for Supervisor Password only when Setup utility is called up.

- **OS Select for DRAM > 64MB**

  This allows system to access more than 64MB of DRAM memory when used with OS/2 depends on certain BIOS calls to access memory. The default setting is ***Non-OS/2***.

- **Video BIOS Shadow**

  This item allows you to change the Video BIOS location from ROM to RAM. Video Shadow will increase the video speed.

- **C8000 - CBFFF Shadow/DC000 - DFFFF Shadow**

  Shadowing ROM reduces available memory between 640KB and 1024KB. These fields determine whether optional ROM is copied to RAM or not.

4.2.3 Advanced Chipset Features

This Setup menu controls the configuration of the motherboard chipset.

CMOS Setup Utility-Copyright © 1984-2001 Award Software Advanced Chipset Features		
DRAM Timing By SPD	Enabled	Item Help
DRAM Clock	Host CLK	
SDRAM Cycle Length	3	Menu Level ►
Bank Interleave	Disabled	Enabled adds a
Memory Hole	Disabled	Parity check to the
P2C/C2P Concurrency	Enabled	boot-up memory
System BIOS Cacheable	Disabled	tests. Select
Video RAM Cacheable	Disabled	Enabled only if the
AGP Aperture Size	64MB	system DRAM
AGP Driving Control	Auto	Contains parity
AGP Driving Value	DA	
AGP Fast Write	Disabled	
OnChip USB	Enabled	
USB Keyboard Support	Disabled	
CPU to PCI Write Buffer	Enabled	
PCI Dynamic Bursting	Enabled	
PCI Master 0 WS Write	Enabled	
PCI Delay Transaction	Enabled	
PCI#2 Access #1 Retry	Enabled	
AGP Master 1 WS Write	Disabled	
AGP Master 1 WS Read	Disabled	
Memory Parity/ECC Check	Disabled	
↑↓→← : Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults		

- **DRAM Timing By SPD**

  This item allows you to select the value in this field, depending on whether the board has paged DRAMs or EDO (extended data output) DRAMs.

- **DRAM Clock**

  This item allows you to select the DRAM clock value, depending on whether the board has paged DRAMs or EDO (extended data output) DRAMs. The available choices are 66 MHz and Host CLK.

- **SDRAM Cycle Length**

  When synchronous DRAM is installed, the number of clock cycles of CAS latency depends on the DRAM timing. Do not reset this field from the default value specified by the system designer. The default setting is ***3***.

- **Memory Hole**

  To improve performance, certain space in memory is reserved for ISA cards. This memory must be mapped into the memory space below 16MB. The available choices are 15M-16M and Disabled.

- **P2C/C2P Concurrency**

  This item allows you to enable/disable the PCI to CPU, CPU to PCI concurrency. By default, this field is set to ***Enabled***.

- **System BIOS Cacheable**

  When enabled, access to the system BIOS ROM addressed at F0000H-FFFFFH is cached, provided that the cache controller is disabled.

- **Video RAM Cacheable**

  Selecting *Enabled* allows caching of the video BIOS ROM at C0000h to C7FFFh, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

- **AGP Aperture Size**

  The field sets aperture size of the graphics. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation. The options available are 4M, 8M, 16M, 32M, 64M, 128M and 256M.

- **OnChip USB**

  This should be enabled if your system has a USB installed on the system board and you wish to use it. Even when so equipped, if you add a higher performance controller, you will need to disable this feature. The available choices are Enabled and Disabled.

- **USB Keyboard Support**

  Select *Enabled* if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard. The options available are Enabled, Disabled.

- **CPU to PCI Write Buffer**

  When this field is *Enabled,* writes from the CPU to the PCI bus are buffered, to compensate for the speed differences between the CPU and the PCI bus. When *Disabled*, the writes are not buffered and the CPU must wait until the write is complete before starting another write cycle.

- **PCI Dynamic Bursting**

  This item allows you to enable/ disable the PCI dynamic bursting function.

- **PCI Master 0 WS Write**

  When *Enabled,* writes to the PCI bus are executed with zero wait states.

- **PCI Delay Transaction**

  The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI specification version 2.1. The default setting is ***Disabled***.

- **PCI#2 Access #1 Retry**

  When disabled, PCI#2 will not be disconnected until access finishes (default). When enabled, PCI#2 will be disconnected if max retries are attempted without success.

- **AGP Master 1 WS Write**

  When *Enabled,* writes to the AGP(Accelerated Graphics Port) are executed with one wait states..

- **AGP Master 1 WS Read**

  When *Enabled,* read to the AGP (Accelerated Graphics Port) are executed with one wait states..

- **Memory Parity/ECC Check**

  This item *enabled* to detect the memory parity and Error Checking & Correcting.

4.2.4 Integrated Peripherals

This option sets your hard disk configuration, mode and port.

CMOS Setup Utility-Copyright © 1984-2001 Award Software Integrated Peripherals		
OnChip IDE Channel0	Enabled	Item Help
Release IRQ15 For OS	Disabled	
IDE Prefetch Mode	Enabled	Menu Level ►
Primary Master PIO	Auto	
Primary Slave PIO	Auto	
Primary Master UDMA	Auto	
Primary Slave UDMA	Auto	
Init Display First	PCI Slot	
IDE HDD Block Mode	Enabled	
Onboard Lan Boot ROM	Disabled	
Onboard FDC Controller	Enabled	
Onboard Serial Port 1	3F8/IRQ4	
Onboard Seiral Port 2	2F8/IRQ3	
UART 2 Mode	Standard	
IR Function Duplex	Half	
TX,RX inverting enable	No, Yes	
Onboard Parallel Port	378/IRQ7	
Onboard Parallel Mode	Normal	
ECP Mode Use DMA	3	
Parallel Port EPP Type	EPP1.9	
↑↓→← : Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults		

- **OnChip IDE Channel0**

  The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select *Enabled* to activate each channel separately.

- **IDE Prefetch Mode**

  The onboard IDE drive interface supports IDE prefetching for faster drive accesses. If you install a primary and/or secondary add-in IDE interface, set this field to *Disabled* if the interface does not support prefetching.

- **Primary Master/Slave PIO**

  The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the two IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device. The options available are Auto, Mode 0, Mode 1, Mode 2, Mode 3, and Mode 4.

- **Primary Master/Slave UDMA**

  Ultra DMA 66/100 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software support Ultra DMA 33/66/100, select Auto to enable BIOS support. The options available are Auto, Mode 0, Mode 1, and Mode 2.

- **Init Display First**

  This item allows you to decide to active whether PCI Slot or AGP first. The options available are PCI Slot, AGP.

- **IDE HDD Block Mode**

  This field allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive.

- **Onboard FDD Controller**

  Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install and-in FDC or the system has no floppy drive, select Disabled in this field. The options available are Enabled, Disabled.

- **Onboard Serial Port 1/Port 2**

  Select an address and corresponding interrupt for the first and second serial ports. The options available are 3F8/IRQ4, 2E8/IRQ3, 3E8/IRQ4, 2F8/IRQ3, Disabled, Auto.

- **UART 2 Mode**

  The second serial port offers these infrared interface modes:

  - IrDA
  - ASKIR IrDA-compliant serial infrared port
  - Normal (default value)

  NOTE: *The UART Mode Select will not appear on the menu once you disable the setting of Onboard Serial Port 2.*

  When UART Mode Select is set as ASKIR or IrDA, the options RxD, TxD Active and IR Transmittion delay will appear.

- **IR Function Duplex**

  This item allows you to select the IR half/full duplex funcion.

- **TX,RX inverting enable**

  This item allows you to enable the TX, RX inverting which depends on different H/W requirement. This field is not recommended to change its default setting for avoiding any error in your system.

- **Onboard Parallel Port**

  This item allows you to determine access onboard parallel port controller with which I/O address. The options available are 378H/IRQ7, 278H/IRQ5, 3BC/IRQ7, Disabled.

- **Onboard Parallel Port Mode**

  Select an operating mode for the onboard parallel (printer) port. Select Normal unless your hardware and software require one of the other modes offered in this field. The options available are EPP1.9, ECP, SPP, ECPEPP1.7, EPP1.7.

- **ECP Mode Use DMA**

  Select a DMA channel for the parallel port for use during ECP mode.

- **Parallel Port EPP Type**

  Select EPP port type 1.7 or 1.9.

4.2.5 Power Management Setup

The Power Management Setup allows you to save energy of your system effectively. It will shut down the hard disk and turn OFF video display after a period of inactivity.

CMOS Setup Utility-Copyright © 1984-2001 Award Software Power Management Setup		
ACPI Function	Enabled	Item Help
Power Management	Press Enter	
PM Control by APM	Yes	Menu Level ►
Video off Option	Suspend -> off	
Video off Method	V/H SYNC+Blank	
MODEM Use IRQ	3	
Soft-off by PWRBTN	Instant-off	
State After Power Failure	Auto	
Wake Up Events	Press Enter	
↑↓→← : Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults		

- **ACPI Function**

  This item allows you to enable/disable the Advanced Configuration and Power Management (ACPI). The options available are Enabled, Disabled.

- **Power Management**

  This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

  - HDD Power Down
  - Doze Mode
  - Suspend Mode

  There are four selections for Power Management, three of which have fixed mode settings.

Disable (default)	No power management. Disables all four modes
Min. Power Saving	Minimum power management. Doze Mode = 1 hr. Standby Mode = 1 hr., Suspend Mode = 1 hr., and HDD Power Down = 15 min.
Max. Power Saving	Maximum power management -- **ONLY AVAILABLE FOR SL CPU'S**. Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min., and HDD Power Down = 1 min.
User Define	Allows you to set each mode individually. When not disabled, each of the ranges is from 1 min. to 1 hr. except for HDD Power Down which ranges from 1 min. to 15 min. and disable.

NOTE: *In order to enable the CPU overheat protection feature, the Power Management field should not be set to Disabled.*

- **PM Control by APM**

  When enabled, an Advanced Power Management device will be activated to enhance the Max. Power Saving mode and stop the CPU internal clock. If Advance Power Management (APM) is installed on your system, selecting Yes gives better power savings. If the Max. Power Saving is not enabled, this will be preset to *No*.

- **Video Off Option**

  When enabled, this feature allows the VGA adapter to operate in a power saving mode.

Always On	Monitor will remain on during power saving modes.
Suspend --> Off	Monitor blanked when the system enters the Suspend mode.
Susp,Stby --> Off	Monitor blanked when the system enters either Suspend or Standby modes.
All Modes --> Off	Monitor blanked when the system enters any power saving mode.

- **Video Off Method**

  This determines the manner in which the monitor is blanked.

V/H SYNC + Blank	This causes the system to turn off the vertical and horizontal synchronization ports and write blanks to the video buffer.
DPMS	Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards to select video power management values.
Blank Screen	This option only writes blanks to the video buffer.

- **Modem Use IRQ**

  This field names the interrupt request (IRQ) line assigned to the modem (if any) on your system. Activity on the selected IRQ always awakens the system. The available choices are 3, 4, 5, 7, 9, 10, 11, and NA. By default, the IRQ is set to *3*.

- **Soft-off by PWRBTN**

  This only works with systems using an ATX power supply. It also allows user to define the type of soft power OFF sequence the system will follow.

Instant-Off (default)	This option follows the conventional manner systems perform when power is turned OFF. Instant-Off is a soft power OFF sequence requiring only the switching of the power supply button to OFF.
Delay 4 Sec.	Upon turning OFF system from the power switch, this option will delay the complete system power OFF sequence by approximately 4 seconds. Within this delay period, system will temporarily enter into Suspend Mode enabling you to restart the system at once.

- **Wake Up Events**

  An input signal on the network 2 awakens the system from a soft-off state.

4.2.6 PNP/PCI Configuration

This option configures the PCI bus system. All PCI bus systems on the system use INT#, thus all installed PCI cards must be set to this value.

CMOS Setup Utility-Copyright © 1984-2001 Award Software PnP/PCI Configurations		
PNP OS Installed	No	Item Help
Reset Configuration Data	Disabled	
		Menu Level ►
Resources Controlled By	Auto (ESCD)	
X IRQ Resources	Press Enter	Select Yes if you are
X DMA Resources	Press Enter	using a Plug and play capable operating
PCI/VGA Palette Snoop	Disabled	system select No if
Assign IRQ For VGA	Enabled	you need the BIOS to
Assign IRQ For USB	Enabled	configure non-boot devices
↑↓→← : Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults		

- **PNP OS Installed**

  This item allows you to determine install PnP OS or not. The options available are Yes and No.

- **Reset Configuration Data**

  Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup or if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system can not boot. The options available are Enabled and Disabled.

- **Resource controlled by**

  The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. The options available are Auto and Manual.

- **IRQ Resources**

  When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt:

  1. Legacy ISA Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).
  2. PCI/ISA PnP Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

  The default value is *"PCI/ISA PnP"*.

- **DMA Resources**

  When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt:

  1. Legacy ISA Devices compliant with the original PC AT bus specification, requiring a specific DMA channel.
  2. PCI/ISA PnP Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

  The default value is *"PCI/ISA PnP"*.

- **PCI/VGA Palette Snoop**

  Some non-standard VGA display cards may not show colors properly. This field allows you to set whether MPEG ISA/VESA VGA Cards can work with PCI/VGA or not. When enabled, a PCI/VGA can work with a MPEG ISA/VESA VGA card. When disabled, a PCI/VGA cannot work with a MPEG ISA/VESA Card.

- **Assign IRQ For USB/VGA**

  Enable/Disable to assign IRQ for USB/VGA. The options available are Enabled, Disabled

4.2.7 PC Health Status

This section is to monitor the current hardware status of core voltages. This is available only if there is hardware monitoring mechanism onboard.

CMOS Setup Utility-Copyright © 1984-2001 Award Software PC Health Status	
Current CPU Temp.	Item Help
Current System Temp.	
Current CPUFAN1 Speed	Menu Level ►
Vcore	
2.5V	
3.3V	
5V	
12V	
↑↓→← : Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults	

- **Current CPU Temp.**
  Show you the current CPU temperature.

- **Current System Temperature**
  These read-only fields reflect the functions of the hardware thermal sensor that monitors the chip blocks and system temperatures to ensure the system is stable.

- **Current CPUFAN1 Speed**
  These optional and read-only fields show the current speeds in RPM (revolution per minute) for the CPU fan and chassis fan as monitored by the hardware monitoring IC.

4.2.8 Frequency/Voltage Control

CMOS Setup Utility-Copyright © 1984-2001 Award Software Frequency/Voltage Control		
Auto Detect DIMM/PCI Clk	Enabled	Item Help
Spread Spectrum	[Disabled]	
CPU Host/PCI Clock	Default	Menu Level ►
↑↓→← : Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults		

- **Auto Detect DIMM/PCI Clk**

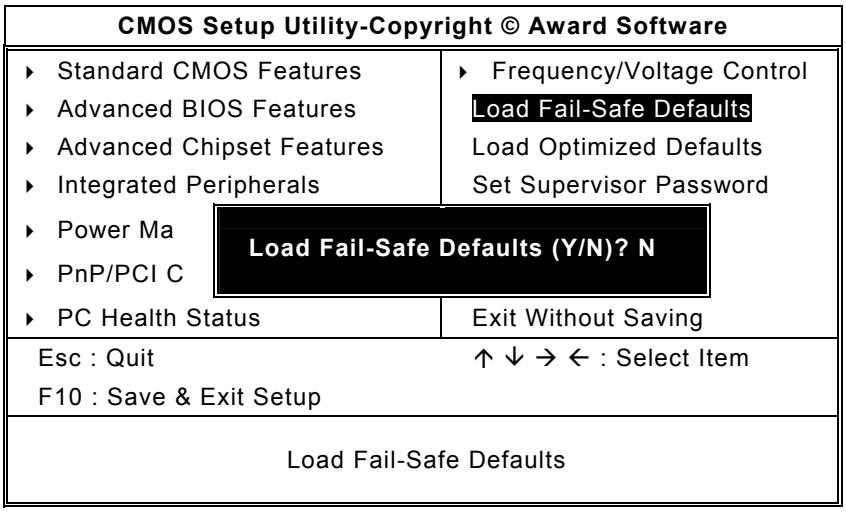
  This item automatically detects the clock speeds of the system memory installed as well as the PCI interface. The options available are Enabled and Disabled. The default setting is ***Enabled***.

- **Speed Spectrum**

  This item directly relates to the EMI performance of the whole system. When enabled, all system clocks run at slower speeds thereby decreasing the electromagnetic interference to the surrounding environment. Disabling this item improves the system performance but simultaneously increase the EMI. The default setting is ***Disabled***.

4.2.9 Load Fail Safe Defaults

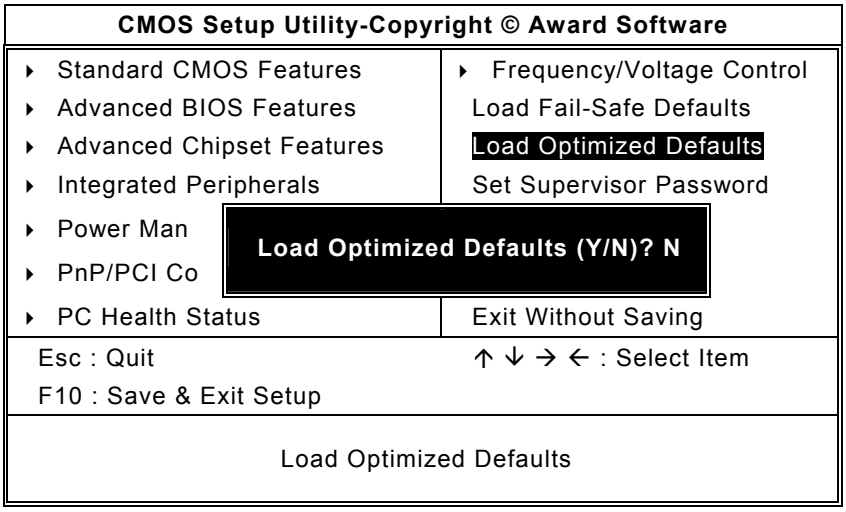
This option allows you to load the troubleshooting default values permanently stored in the BIOS ROM. These default settings are non-optimal and disable all high-performance features.



To load BIOS defaults value to CMOS SRAM, enter "Y". If not, enter "N".

4.2.10 Load Optimized Defaults

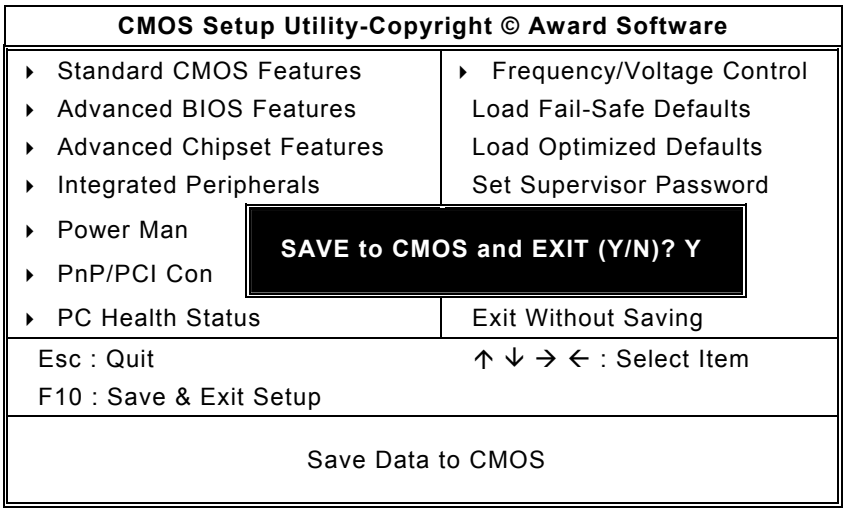
This option allows you to load the default values to your system configuration. These default settings are optimal and enable all high performance features.



To load SETUP defaults value to CMOS SRAM, enter "Y". If not, enter "N".

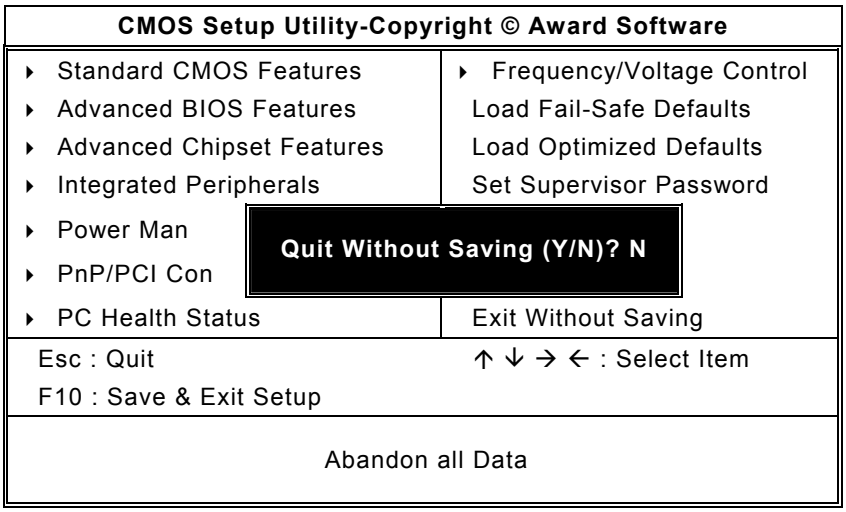
4.2.11 Save & Exit Setup

This allows you to determine whether or not to accept the modifications. Typing "Y" quits the setup utility and saves all changes into the CMOS memory. Typing "N" brigs you back to Setup utility.



4.2.12 Exit Without Saving

Select this option to exit the Setup utility without saving the changes you have made in this session. Typing "Y" will quit the Setup utility without saving the modifications. Typing "N" will return you to Setup utility.



Appendix A
Watchdog Timer

Using the Watchdog Function

The **SBC82621** CPU card uses version 2.0 of the watchdog timer. This onboard WDT generates either a system reset or non-maskable interrupt (NMI), depending on the settings made on jumper **JP3** of **SBC82621**. Follow the steps below to enable and program the watchdog function of **SBC82621**.

Start

↓

Un-Lock WDT	:	**OUT 120H 0AH ; enter WDT function** **OUT 120H 0BH ; enable WDT function**

↓

Set multiple (1~4)	:	**OUT 120 0NH ; N=1,2,3 or 4**

↓

Set base timer (0~F)	:	**OUT 121 0MH ; M=0,1,2,...F**

↓

WDT counting

↓

re-set timer	:	**OUT 121 0MH ; M=0,1,2,...F**

↓

IF No re-set timer	:	**WDT time-out, generate RESET or NMI**

↓

IF to disable WDT	:	**OUT 120 00H ; Can be disable at any time**

M	N			
	1	2	3	4
0	0.5 sec.	5 secs.	50 secs.	100 secs.
1	1 sec.	10 secs.	100 secs.	200 secs.
2	1.5 secs.	15 secs.	150 secs.	300 secs.
3	2 secs.	20 secs.	200 secs.	400 secs.
4	2.5 secs.	25 secs.	250 secs.	500 secs.
5	3 secs.	30 secs.	300 secs.	600 secs.
6	3.5 secs.	35 secs.	350 secs.	700 secs.
7	4 secs.	40 secs.	400 secs.	800 secs.
8	4.5 secs.	45 secs.	450 secs.	900 secs.
9	5 secs.	50 secs.	500 secs.	1000 secs.
A	5.5 secs.	55 secs.	550 secs.	1100 secs.
B	6 secs.	60 secs.	600 secs.	1200 secs.
C	6.5 secs.	65 secs.	650 secs.	1300 secs.
D	7 secs.	70 secs.	700 secs.	1400 secs.
E	7.5 secs.	75 secs.	750 secs.	1500 secs.
F	8 secs.	80 secs.	800 secs.	1600 secs.

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