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B&R COMPACT PLC
USER'S MANUAL

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Published by: Bernecker und Rainer Industrie-Elektronik GmbH.
Model No.: MABRCOMP1-0E

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1. GENERAL INFORMATION

The MINI/MULTICONTROL family is offered by B&R as control system which can be adapted to all customer specific wishes because of its modular structure and 100% software compatibility.

To enhance this list, B&R has now expanded the product palette with a new Compact PLC. The compact is basically a controller which settles into the family just under the MINICONTROL. Again, 100% software compatibility to the MINICONTROL was called for. Therefore, if in the future an upgrade is required, the MINICONTROL can be implemented without losing your software.

Even though the Compact PLC is priced so low, because we have kept the previous modularity all in one unit, the Compact PLC is in concept and construction able to be used universally.

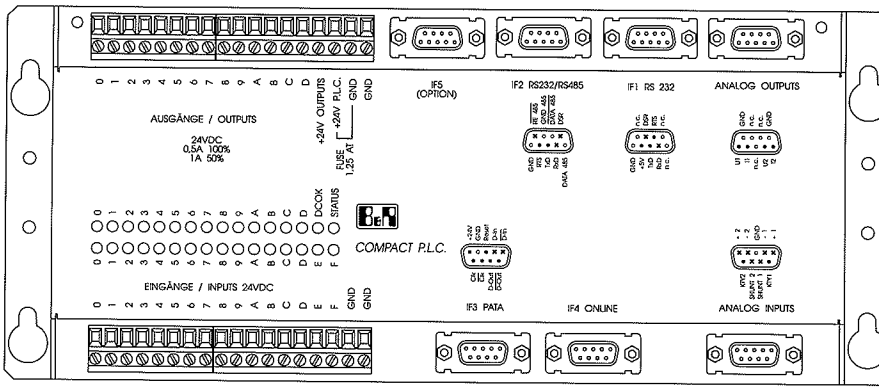
Construction

- Digital Inputs/Outputs
- Relay expansion card
- Analog Inputs (voltage, current and temperature)
- Analog Outputs (voltage and current)
- Event counter
- Interrupt input
- Reference input
- Channels A and B for positioning applications
- 2 serial interfaces
- CAN Bus (BRCOMP2-0)
- B&R standard PATA interface (for MINICONTROL operator interface panel)
- SSI interface für connection of absolute encoders
- B&R on-line interface
- 16 Kbytes EEPROM application memory
- 16 Kbytes additional EEPROM
- RS485 Network (B&R MININET)
- Operator panels: MINICONTROL Operator Interface Panel
  Compact MMI P120 and MMI P121
  and other products from the PANELWARE family

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2. MODEL NUMBER

2.1 B&R COMPACT PLC



Compact PLC, with 6303 processor, 16 Kbytes application memory, approx. 4 msec / K instructions, 16 digital inputs, 14 digital outputs, 2 analog inputs, 2 analog outputs, channels A and B for positioning tasks, reference input, event counter, interrupt input, B&R on-line interface, RS232 interface (not galvanically isolated), RS232/RS485 interface (RS485 galvanically isolated), PATA/SSI interface,

without CAN Bus	**BRCOMP**
with CAN Bus on IF5	**BRCOMP**

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2.2 RELAY EXPANSION CARD

A relay expansion card is available for the Compact Control which adds an additional 16 relay outputs to the 14 transistor outputs (O 060 - O 06F).

The relay expansion card is described in section "15. Relay Expansion Card for BRCOMP".

2.3 STANDARD SOFTWARE

A diskette with the most important standard software has been put together especially for the Compact Control. The following software is saved on the diskette:

- Standard Utility Programs (standard software package 1)
- Operator Panel Software
- B&R MININET
- Positioning

Language	Model Number
German	SWSPSBRC01-0
English	SWPLCBRC01-0

2.4 TERMINAL BLOCKS

A set of PHOENIX terminal blocks can be ordered (BRTB0218-0) as an accessory. Contained in delivery:

Amount	Terminal Blocks
2	8 Pin
2	10 Pin

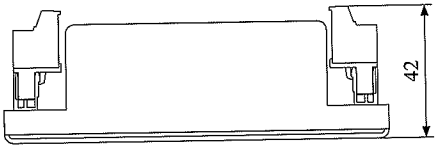
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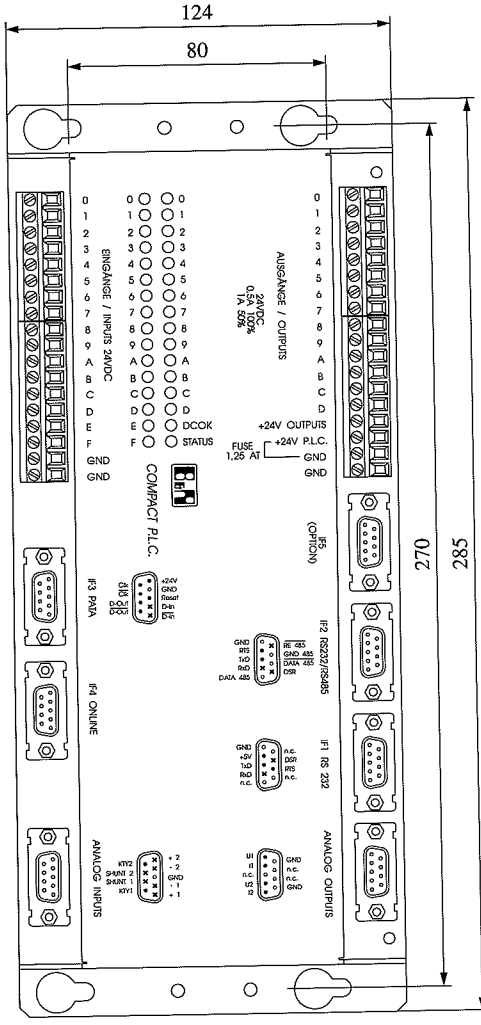
3. TECHNICAL DATA

Processor	6303
Processing time	approx. 4 msec / K instructions
User program memory	16 Kbytes RAM/EEPROM
Expansion memory	16 Kbytes EEPROM (for data)
Status-LED	Red
Number of registers Non-volotile Volotile	7168 7148 20
Number of flags Non-volotile Volotile	800 300 500
Time/date	Real-time clock
Software timers	64
Clock pulses	10 msec, 100 msec, 1 sec, 10 sec
Digital inputs	16 of which four can be used as counter inputs
Digital outputs	14
Analog inputs	2
Analog outputs	2
Serial interface IF1 IF2 IF3 IF4 IF5	 RS232 RS232/RS485 (RS485 galvanically isolated) PATA (MINICONTROL operator interface panel or relay expansion card) SSI (connecting absolute encoders) B&R on-line interface CAN Bus (BRCOMP2-0)
Supply voltage	24 VDC ±25 %
Max. power consumption without operator panels at 18 V at 24 V at 30 V	 6.0 W 6.5 W 7.5 W
Fuse	T 1.25 A / 250 V
Soft and Hardware watchdogs	YES
Battery monitor	YES
Operating temperature	5 to 55 °C
Relative humidity	30 - 95 % non-condensing

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4. MEASUREMENTS





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5. INSTALLATION MOUNTING

5.1 INSTALLATION GUIDELINES

Make sure that devices that create heavy electromagnetic disturbances (e.g. frequency converter, transformer, motor controller etc.) are at a sufficient distance. The distance from these devices to PLC should be as large as possible. If necessary, they are to be separated with a magnetic shieldi partition (VACOPERM[a] 70).

5.2 THERE ARE TWO INSTALLATION POSSIBILITIES

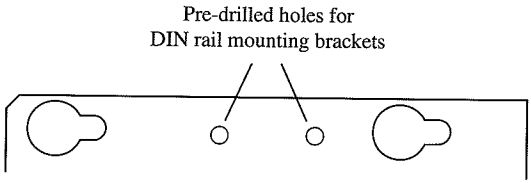
5.2.1 Directly to Control Cabinet Wall

The Compact PLC can be mounted horizontally or vertically. If it should be mounted vertically, that the digital inputs/outputs are at the top (see drawing on the next page).
The chassis should be screwed firmly to the wall of the cabinet using the four screw holes provid vertical mounting.

M5 screws are to used in mounting the Compact PLC (if M5 screws are not available, use appro replacement screws) (hole dimensions: 80 * 270 mm or 3.14 * 10.62 inches).

5.2.2 Rail Mount

For mounting the unit to a standard mounting rail (DIN EN 50022-35) two mounting brackets are provided in the delivery which must be screwed onto the Compact PLC.



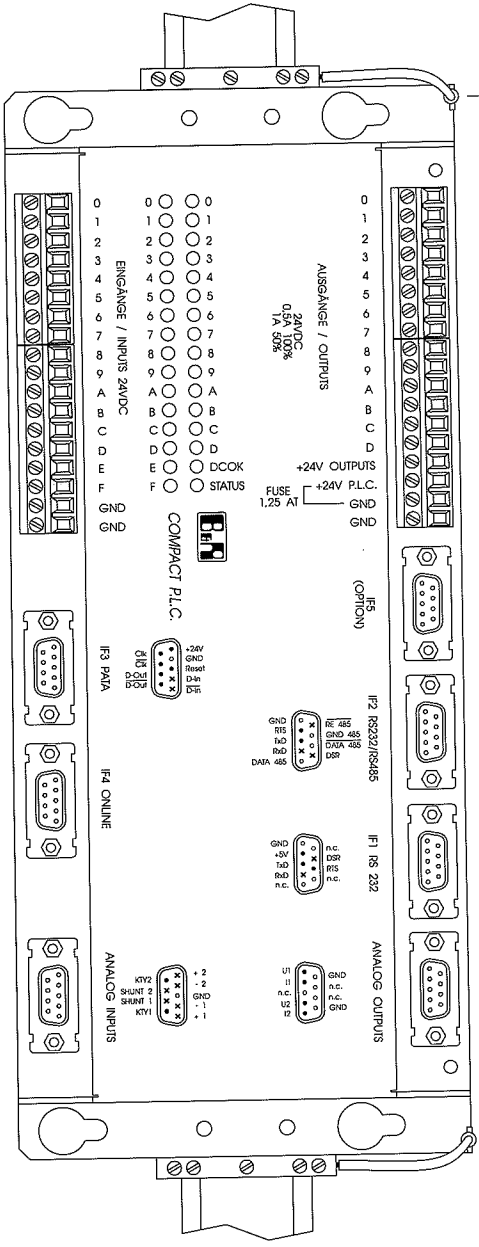
Fastening the Compact PLC to the DIN rail.

Cable clamps should be fastened to the left and right of the Compact PLC. The unit is to be groun with the attachment provided (see drawing on the next page).

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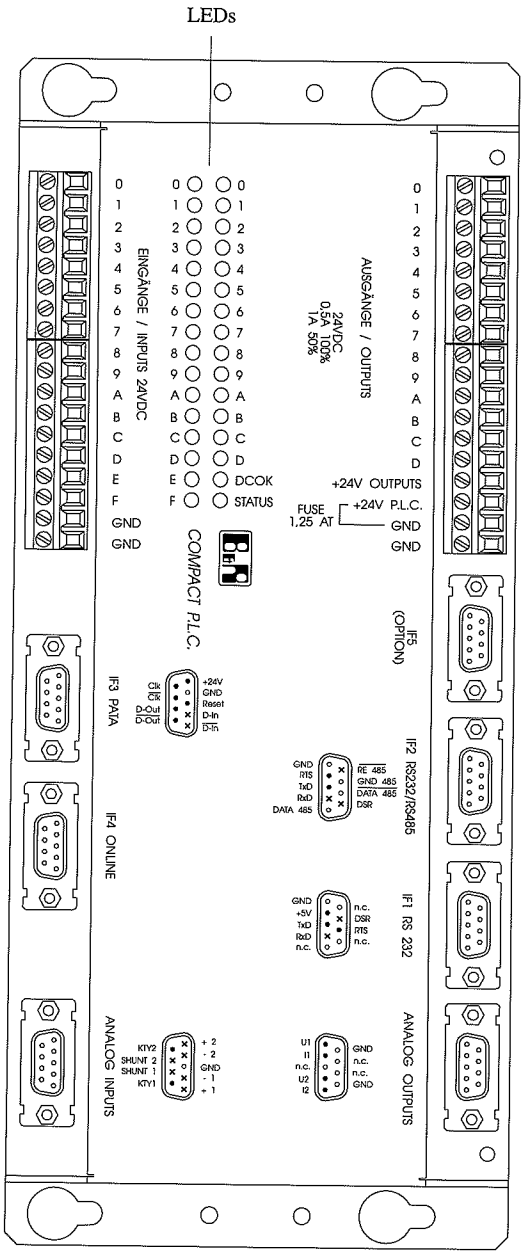
NOTE: The DIN rail must also be grounded.

The width of the mounting plates which are attached to the unit provide enough space between the Compact PLC and neighboring modules for ventilation.



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6. DESCRIPTION OF COMPONENTS



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7. POWER SUPPLY

The LED DCOK indicates that the control is being supplied with power. There are two different ways to supply the Compact PLC:

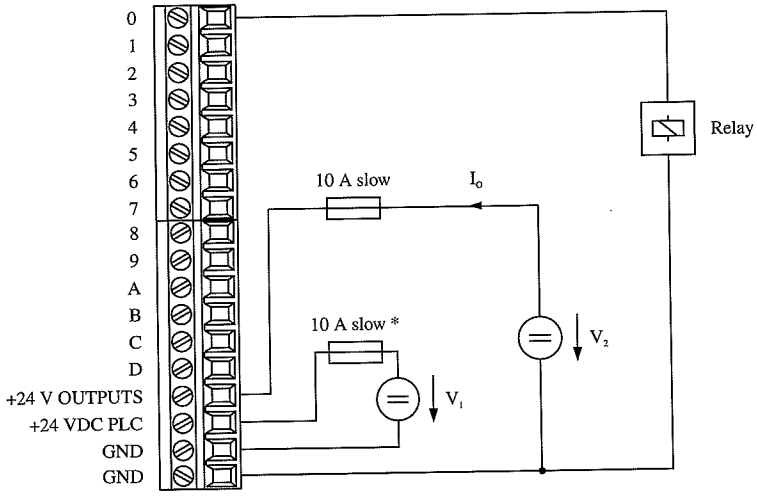
- One power supply: - Combinational supply for inputs and outputs
- Two power supplies: - One for the control
  - One for the digital outputs

One Power Supply

A single Compact PLC supply is standard (For wiring see section "11. Digital Outputs").

Two Power Supplies

Control and outputs are supplied separately.



V_1 ... 24 VDC / 1A
V_2 ... 24 VDC / I_O
I_O ... Total current of all outputs

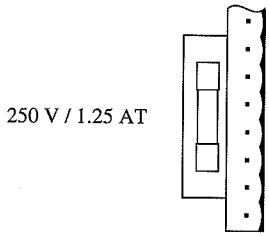
* 10 A fuse (slow) for protecting the connector in case of a short circuit or reverse poles.

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8. FUSE

The Compact PLC is protected with a 250 V / 1.25 AT fuse. The fuse compartment can be found the terminal block for the digital outputs.

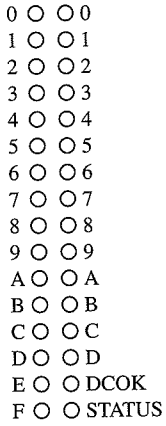
NOTE: The digital outputs are supplied separately. The supply must be fed through a sep fuse (see section "7. Voltage Supply" and "11. Digital Outputs").



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9. LEDs

32 LEDs inform the user of digital input status, digital output status, power supply and the CPU activity.

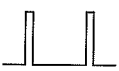
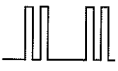


LEDs for	Description
Digital inputs	The green LEDs (0 - F) on the left-hand side of the unit indicate the status of the digital inputs. Off ... Input = "0" On ... Input = "1"
Digital outputs	The orange LEDs (0 - D) indicate the status of the digital outputs. Off ... Output = "0" On ... Output = "1"
Supply	The orange LED DCOK indicates, whether power is being supplied or not. Off ... No supply On ... Supply voltage OK.

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Status-LED

The Compact PLC is equipped with a red status LED which is used to indicate the various opera states.

LED-Status	Operating status
HI / LO 	User program is running in RAM
HI / LO 	CPU in HALT status
HI / LO 	On-line unplugged during PROM programming
HI / LO	Error during user program execution
HI / LO	User program is running in PROM

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10. DIGITAL INPUTS

The digital inputs convert the binary signals of the process in binary values 0 and 1. States of the inputs are indicated by means of the green LEDs.

The Compact PLC is equipped with 16 digital inputs (I 040 - I 04F). Inputs I 04C - I 04F can also be used for special tasks:

- Event counter
- Interrupt input
- Reference input
- Incremental encoder (channels A and B) for positioning tasks

The functions are explained in more detail in section "14. Counter Inputs and Interrupt Input".

10.1 TECHNICAL DATA

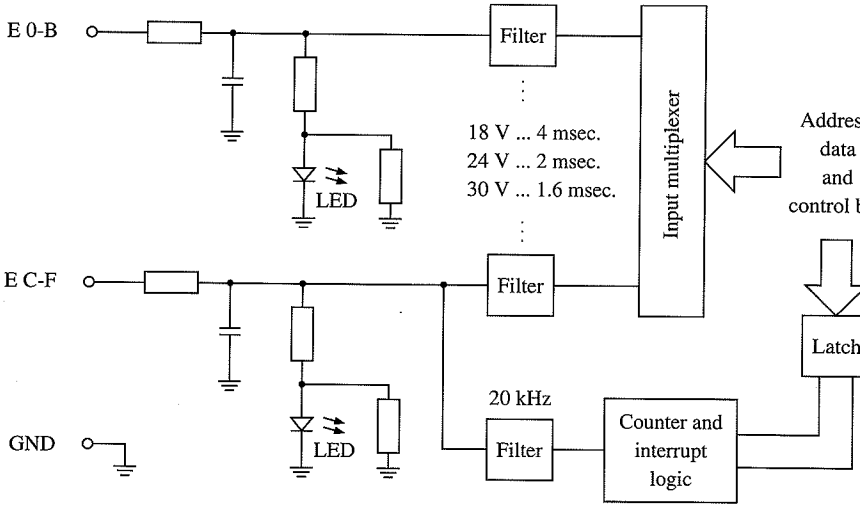
Amount	16
Revision	Type 1 conforming to IEC 1131-2
Status display	16 green LEDs
Electrical isolation Input ↔ PLC Input ↔ Input	 NO NO
Input voltage [1] Minimal Nominal Maximal	 15 VDC 24 VDC 30 VDC
Input resistance	4 kΩ
Switching threshold log. 0 → 1 log. 1 → 0	 Min. 15 VDC Max. 5 VDC
Input current at 24 VDC	Approx. 5 mA
Switch delay inputs 0 - F (log. 0 → 1, log. 1 → 0)	18 V: Max. 4 msec. 24 V: Max. 2 msec. 30 V: Max. 1.6 msec.
Input frequency inputs C - F	Max. 20 kHz
Update of input data by CPU	Automatically with any change
Maximum peak voltage	500 V for 50 µsec, max. every 100 msec [2]

[1] If using inputs C - F as counter inputs, the input voltage should be 24 VDC ± 10 %, so that the maximum input frequency of 20 kHz can be reached.

[2] Standard pulse 1.2/50 (IEC 60-2)

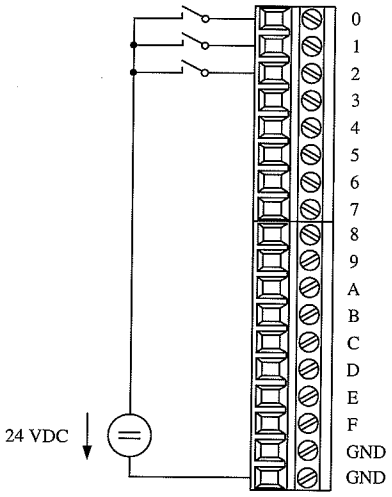
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10.2 INPUT CIRCUIT



Counter and interrupt logic is described in section "14. Counter Inputs and Interrupt Input".

10.3 DIGITAL INPUT WIRING



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11. DIGITAL OUTPUTS

Digital outputs are for controlling external loads (Relays, Motors, Magnetic valves, etc.). The status of the outputs is indicated with orange LEDs.

The Compact PLC is equipped with 14 transistor outputs (O 050 - O 05D).

11.1 TECHNICAL DATA

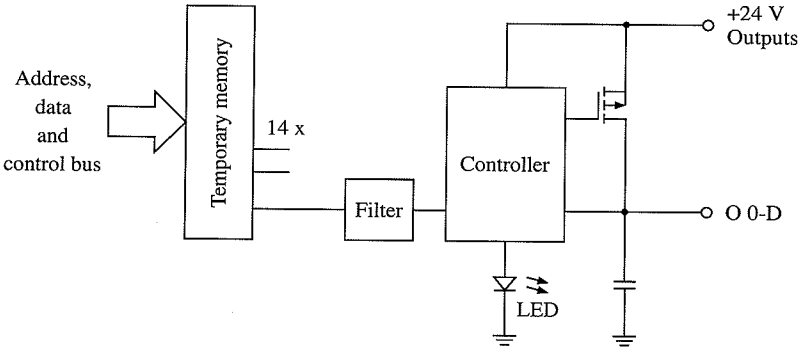
Amount	14
Status display	14 orange LEDs
Electrical isolation Output ↔ PLC Output ↔ Output	 NO NO
Supply voltage Minimal Nominal Maximal	 18 VDC 24 VDC 30 VDC
Switching current 50 % Simultaneousness 100 % Simultaneousness	 1.0 A[1)] 0.5 A
Switching delay log. 0 → 1 log. 1 → 0	 Approx. 200 µsec. Approx. 200 µsec.
Residual voltage	< 1 V at 1 A
Protection circuit [2)]	Internal
Short circuit proof	YES
Overload protection	Automatic shut-off by thermal overload

[1)] **NOTE:** If current flows at 50 % simultaneousness the maximum allowed environmental temperature is of 40 °C.

[2)] In some circumstances an external protection circuit may be required (see section "11.4 Switching Resistive-Inductive Loads").

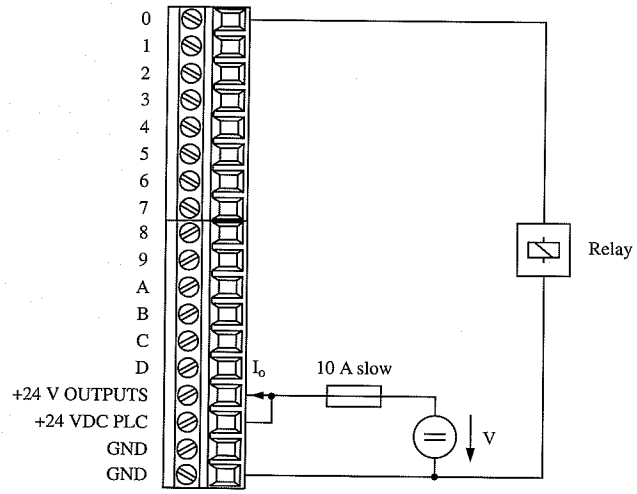
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11.2 OUTPUT CIRCUIT



11.3 WIRING

Another wiring diagram is shown in section "7. Power Supply".



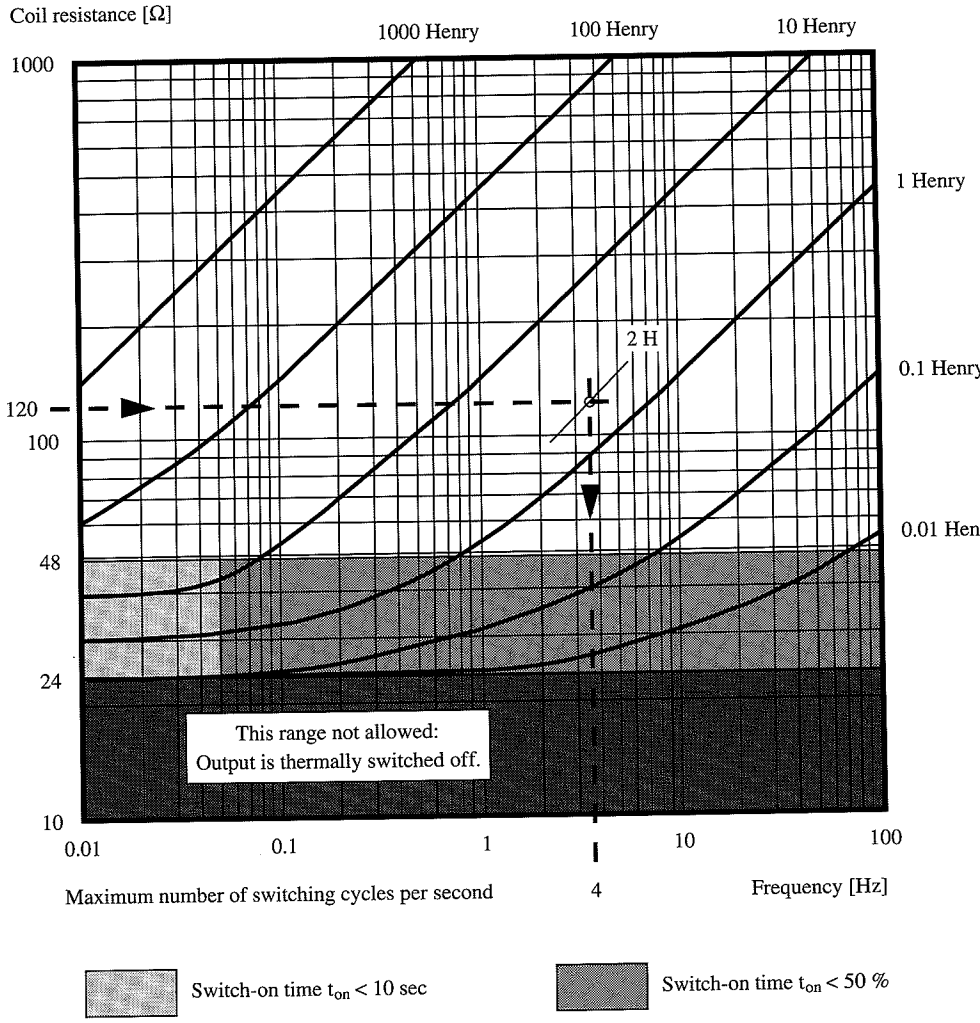
V ... 24 VDC / 1 A + I_O

I_O ... Total current of all outputs

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11.4 SWITCHING RESISTIVE-INDUCTIVE LOAD

When switching resistive-inductive loads, attention must be paid to coil resistance and to coil inductivity.
The diagram shown below indicates the maximum number of switching cycles per second in connectio with the coil resistance and coil inductivity. All outputs are switched simultaneously (0.5 A at 24 V).



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If the coil resistance is less than 24 Ω, the thermal protection unit takes over and switches the ou
off.

At a coil resistance of between 24 Ω and 48 Ω the switch-on tiem should be paid attention to. D
ing on the switching frequency, it may not be longer than 10 seconds or not longer than the swit
time. Continued operation is not possible in this range!
If, for example, one switching cycle per second is executed, the switch-on time may not be long
0.5 sec.

Example With which maximum switching frequency can a magnetic valve be switched w
following coil data?

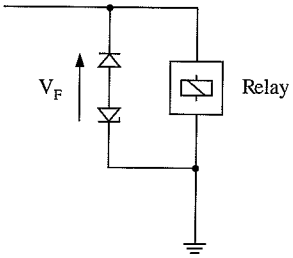
Inductivity:	2 H
Coil resistance:	120 Ω

Find your coil resistance on the Y axis and follow the horizontal line to the right
you reach the intersecting parameter curve for 2 H (see diagram). At this intersec
the vertical line to the x axis can be found. Follow this line to the x axis and read
maximum switching frequency (pay attention to the logarithmic scale).
The magnetic valve can be operated at a maximum switching frequency of 4 Hz.

Operation with a higher switching frequency is not allowed and can lead to a the
shutdown of the output.
If a higher switching frequency is required, an external protection circuit must be
implemented. Most manufacturers of relays and magnetic valves provide protect
circuits for the respective elements.

The inverse voltage V_F must be ≤ 8 V.

Example of a protection circuit



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12. ANALOG INPUTS

With analog inputs, measurement values (current, voltage, resistance or temperature) are converted to numerical values which can be processed by the PLC.

The B&R Compact Control is equipped with two analog inputs. One of the following signals can be selected with software for each channel. The selection is made by entering a mode number (0 - 9).

Measurement	Mode	Input Signal	Software Filter Resolution at			Value
			10 Hz / 50 Hz ±14 Bit	250 Hz ±12 Bit	1 kHz ±8 Bit	
Voltage	0	±10 V	±0.610 mV	±2.441 mV	±39.06 mV	±32767
	1	±2.5 V	±0.152 mV	±0.610 mV	±9.76 mV	±32767
Current	2	0 - 20 mA	1.221 µA	4.883 µA	78.12 µA	0 - 32767

Measurement	Mode	Input Signal	Resolution	Value
Temperature	3	KTY10 (-50 °C to +150 °C)	0.01 °C	-5000 to +15000
	4	KTY10 (-58 F to +302 F)	0.01 F	-5800 to +30200
reserved	5	--	--	
	6	--	--	
	7	--	--	
Resistance	8	Resistance measurement (0 - 65000 Ω) [1]	1 Ω	0 - 65000
	9	Resistance measurement (0 - 4500 Ω) [1]	0.1 Ω	0 - 45000

[1] Resistance Measurement

The resistance measurement can only be made with the standard function block AINJ (see section "12.7 AINJ - Analog Input Compact Control"). The resolution Ω/bit can be seen on the diagrams on the following pages.

Temperature

Temperature measurement with sensors such as NTC, PTC, PT1000 etc. is possible with the resistan measurement (see section "12.7 AINJ - Analog Input Compact PLC").

Utilities: ALIN, TLIN for nonlinear characteristic curves
SCAL, TSCL for linear characteristic curves

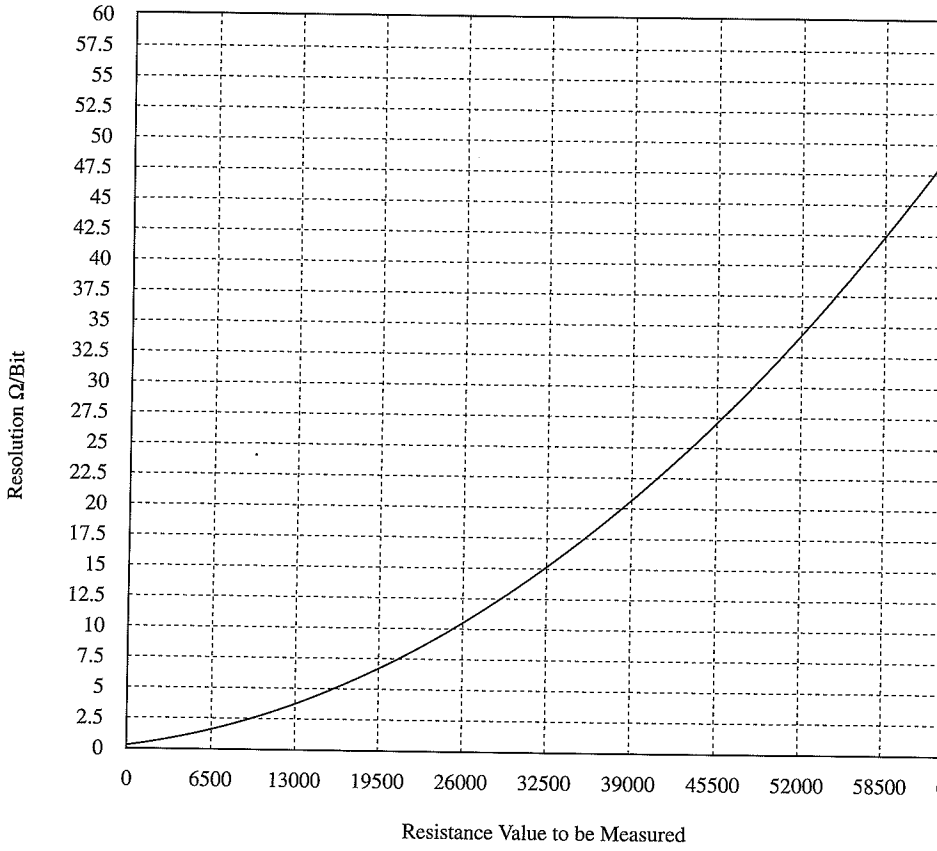
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Diagram for Resistance Measurements

The resolution Ω/bit for a certain resistance value can be read from the following diagrams.

1) Resistance measurement 0 - 65000 Ω:

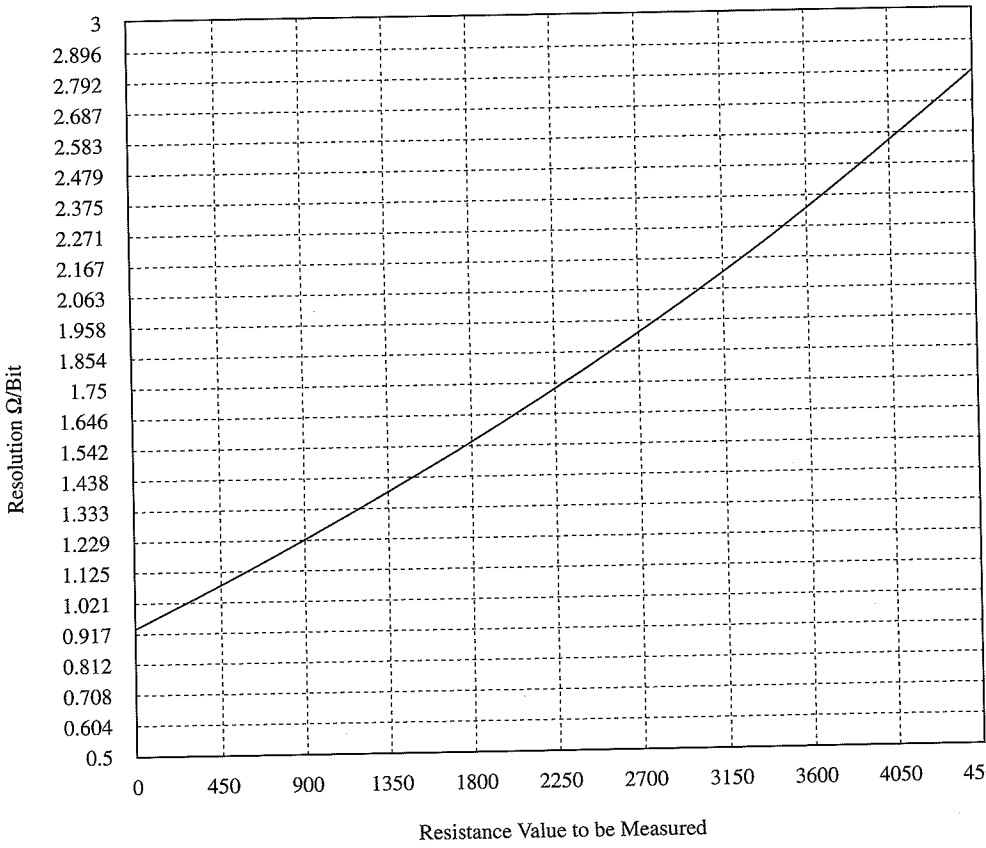
Mode: 8



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2) Resistance Measurement 0 - 4500 Ω:

Mode: 9



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12.1 TECHNICAL DATA

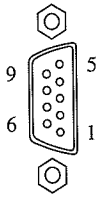
Amount	2
Galvanic isolation	Differential inputs, not galvanically isolated
Common mode voltage	±12 V
Input resistance	min. 10 MΩ
Dielectric strength	±30 V max.
Resolution A/D converter	16 Bit
Addressing	Operating system
Precision at 25 °C	Software compensation to ±0.01 % (10 Hz Notch)
Temperature drift	±10 V range: ±0.03 % / °C ±0.9 LSB / °C [1)] ±2.5 V range: ±0.02 % / °C ±3.5 LSB / °C
Hardware filter Cutoff frequency Rolloff Step response	 Approx. 110 Hz Approx. 20 dB/Dec. 63 % in 1.4 msec
Software filter Cutoff frequency (1. Notch)	 10 Hz, 50 Hz, 250 Hz, 1 kHz, software selectable
Conversion times	302 msec (10 Hz), 62 msec (50 Hz), 16.2 msec (250 Hz), 4.1 msec (1
Calibration times	902 msec (10 Hz), 183 msec (50 Hz), 48 msec (250 Hz), 11,7 msec (1
Damping 1st order notch	>100 dB
Operating mode	Trigger (a calibration is performed after every notch frequency change and after a reset. After a reset a notch frequency of 50 Hz is set automatically again)
Input voltage	±10 V / ±2.5 V software selectable
Precision voltage input	appr. ±14 bit (10 Hz & 50 Hz), appr. ±12 bit (250 Hz), appr. ±8 bit (1 k
Current measurement	an internal shunt must be used (124 Ω)
Precision for 0 - 20 mA	appr. 14 bit (10 Hz & 50 Hz), appr. 12 bit (250 Hz), appr. 8 bit (1 kH
KTY10 Temperature sensor Range of measurement Linearization Resolution	 -50 to +150 °C Hardware to ±0.3 °C from -10 to +110 °C 0.01 °C

[1)] LSB ... Least Significant Bit

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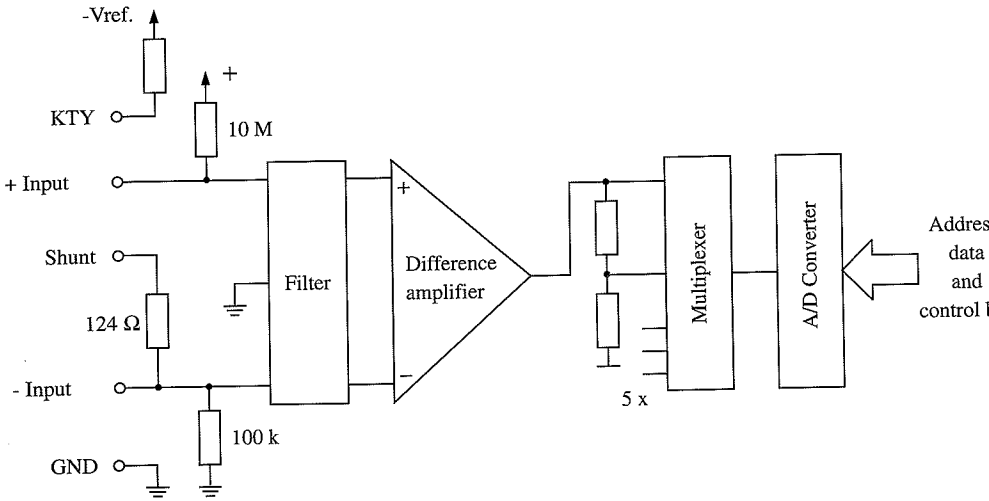
12.2 PIN-OUTS

9 pin D-type (female)



Pin	Assignment
1	+ Input 1
2	- Input 1
3	GND
4	- Input 2
5	+ Input 2
6	KTY 1
7	Shunt 1
8	Shunt 2
9	KTY 2

12.3 INPUT CIRCUIT

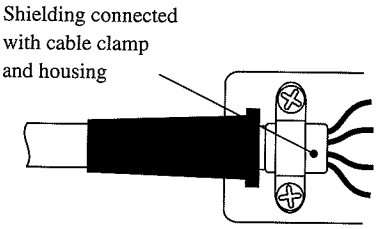


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12.4 SHIELD GROUNDING

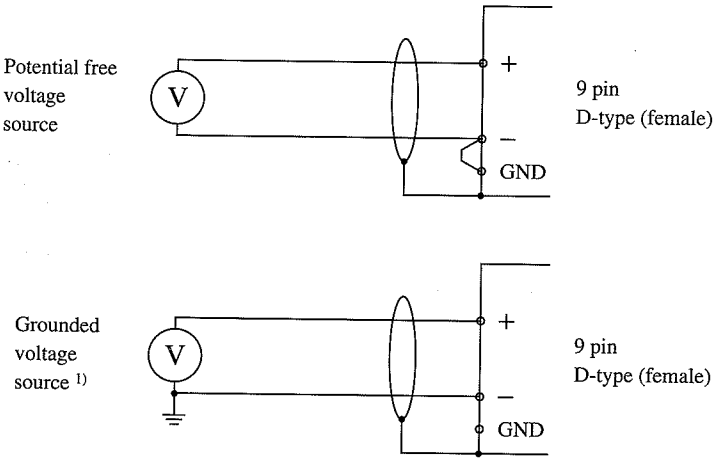
Metal screws or a metallic connector housing are the easiest and most efficient methods of diver
any possible disturbances to the housing of the Compact PLC.

The cable shielding should be in direct contact with the connector housing.



12.5 WIRING

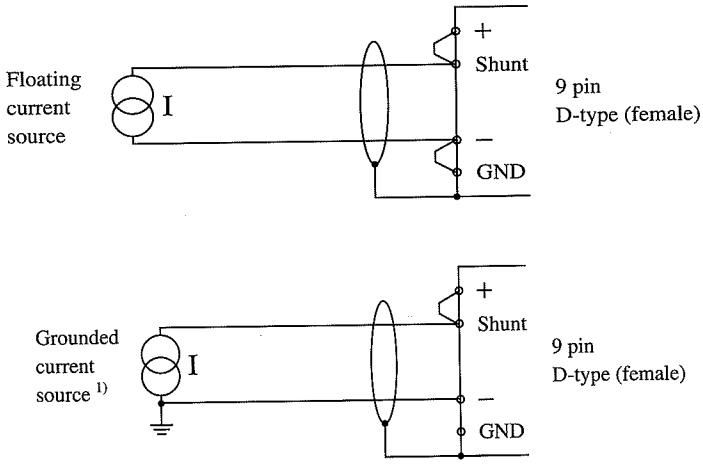
Voltage source



1) No voltage dropout monitoring is possible for this connection.

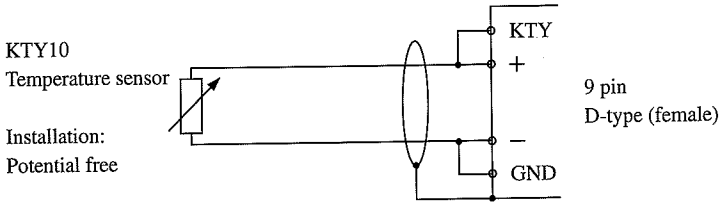
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Current source



KTY10 sensor

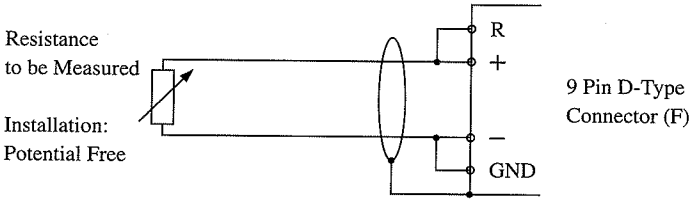
The KTY sensors are semiconductor temperature sensors. The KTY10 series has a nominal resistance of 2000 Ω at 25 °C (e.g. KTY10-6, KTY11-6, KTY13-6, KTY16-6 and KTY19-6).



1) No current dropout monitoring is possible for this connection.

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Resistance measurement with NTC, PTC, PT1000 etc.



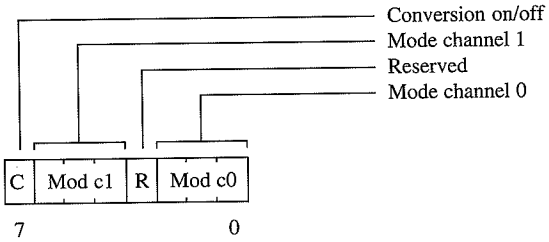
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12.6 SOFTWARE OPERATION

The initialization of the analog input is handled through registers R 1000 - R 1003. The analog value is either converted in the END routine or by an STL call. The converted values are then stored in registers R 1004 - R 1007.

The initialization can either be done with commands in STL or with the help of the AINJ function block (see section 12.7).

Register R 1000

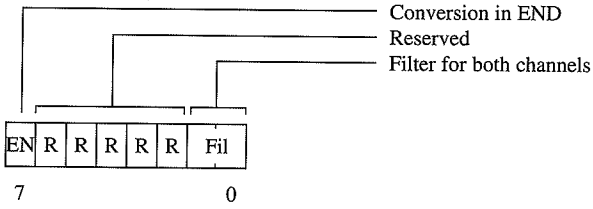


Conversion on/off	Switches the analog conversion on/off. If it is switched off, registers R 1004 - R 1007 contain a value of 0. 0 ... Conversion off 1 ... Conversion on
Mode channel 1	Bits 4 - 6 are used to set the mode for channel 1.
Reserved	Reserved for later use.
Mode channel 0	Bits 0 - 2 are used to set the mode for channel 0. The same modes can be set as for channel 1.

Mode	Signal
0	±10 V
1	±2.5 V
2	0 - 20 mA
3	KTY10 (Temperature in °C)
4	KTY10 (Temperature in F)

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Register R 1001



Conversion in END	Defines whether the conversion should be done during the END routine execution or not. If th conversion is not done during the END routine, the analog conversion routine must be started an STL call (see Analog Conversion). 0 ... Conversion in the END routine 1 ... Conversion with STL call
Reserved	Reserved for later use.
Filter for both channels	Defines the filter for both channels.

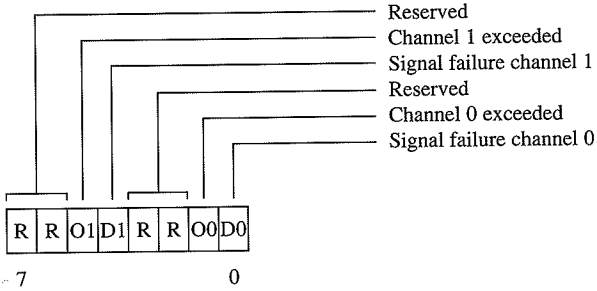
Filter	Frequency	Conversion time
0	10 Hz	302 msec.
1	50 Hz	62 msec.
2	250 Hz	16.2 msec.
3	1000 Hz	4.1 msec.

Register R 1002

Conversion frequency channel 1	Defines the conversion frequency of channel 1 (0 - 255). 0 ... Channel 1 is never converted 1 ... Channel 1 is always converted to channel 0 2 ... Channel 1 is converted to double channel 0 : ... : : ... : 255 ... Channel 1 is converted to 255 times channel 0

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Register R 1003



Reserved	Reserved for later use.
Channel 1 exceeded	1 ... Range exceeded for channel 1
Signal failure channel 1	1 ... Signal failure channel 1
Reserved	Reserved for later use.
Channel 0 exceeded	1 ... Range exceeded for channel 0
Signal failure channel 0	1 ... Signal failure channel 0

Registers R 1004 - R 1007

Destination memory

In registers R 1004 - R 1007, the converted values are stored.

Memory	Channel
R 1004&	0
R 1006&	1

Value range:

Signal	Value
±10 V	-32768 to +32767
±2.5 V	-32768 to +32767
0 - 20 mA	0 to 32767
-50.00 to +150.00 °C	-5000 to +15000
-58.00 to +302.00 F	-5800 to +30200

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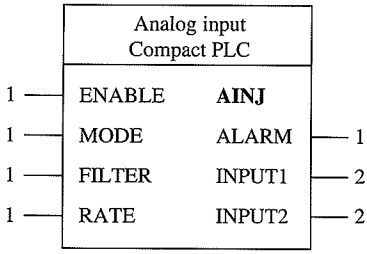
12.7 AINJ - ANALOG INPUT COMPACT PLC

The function block is used for initializing the analog inputs. The converted values and the alarm range exceeding and Signal failures are sent to outputs.

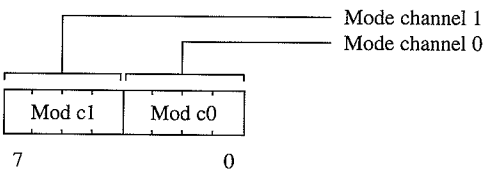
NOTE: The analog conversion is always done in the END routine.

AINJ

Function block length: 84 lines
First Scan: No



Inputs/Outputs	Description	Address t
ENABLE	If the ENABLE input is set to 1, the function block is executed.	R, F,
MODE	Channel mode setting.	R, #

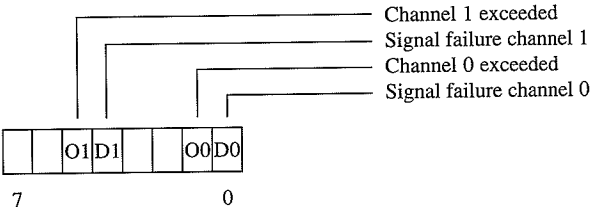


Mode	Signal
0	±10 V
1	±2.5 V
2	0 - 20 mA
3	KTY10 (Temperature in °C)
4	KTY10 (Temperature in F)
5	reserved
6	reserved
7	reserved
8	Resistance measurement (0 - 65000 Ω) [1]
9	Resistance measurement (0 - 4500 Ω) [1]

[1] Version 1.30 and higher

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<table>
<tr><th>Inputs/Outputs</th><th>Description</th><th>Address types</th></tr>
<tr><td>FILTER</td><td>Defines the filter for both channels.
<table><tr><th>Filter</th><th>Frequency</th><th>Conversion time</th><th>Resolution</th></tr><tr><td>0</td><td>10 Hz</td><td>302 msec.</td><td>±14 bit</td></tr><tr><td>1</td><td>50 Hz</td><td>62 msec.</td><td>±14 bit</td></tr><tr><td>2</td><td>250 Hz</td><td>16.2 msec.</td><td>±12 bit</td></tr><tr><td>3</td><td>1000 Hz</td><td>4.1 msec.</td><td>±8 bit</td></tr></table></td><td>R, #</td></tr>
<tr><td>RATE</td><td>Defines the conversion time of channel 1 (0 - 255).

0 ... Channel 1 is never converted
1 ... Channel 1 is always converted to channel 0
2 ... Channel 1 is converted to double channel 0
: ... :
: ... :
255 ... Channel 1 is converted to 255 times channel 0</td><td>R, #</td></tr>
<tr><td>ALARM</td><td>indicates a signal failure or an exceed on a channel.

</td><td>R</td></tr>
<tr><td>INPUT0</td><td>Contains the converted value of channel 0.

Value range:
<table><tr><th>Signal</th><th>Value</th></tr><tr><td>±10 V</td><td>-32768 to +32767</td></tr><tr><td>±2.5 V</td><td>-32768 to +32767</td></tr><tr><td>0 - 20 mA</td><td>0 to 32767</td></tr><tr><td>-50.00 to +150.00 °C</td><td>-5000 to +15000</td></tr><tr><td>-58.00 to +302.00 F</td><td>-5800 to +30200</td></tr><tr><td>0 - 65000 Ω</td><td>0 to 65000</td></tr><tr><td>0 - 4500 Ω</td><td>0 to 4500</td></tr></table></td><td>R</td></tr>
</table>

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<table>
<tr><th>Inputs/Outputs</th><th>Description</th><th>Address</th></tr>
<tr><td>INPUT1</td><td>Contains the converted value from channel 1.

Value range:
<table>
<tr><th>Signal</th><th>Value</th></tr>
<tr><td>±10 V</td><td>-32768 to +32767</td></tr>
<tr><td>±2.5 V</td><td>-32768 to +32767</td></tr>
<tr><td>0 - 20 mA</td><td>0 to 32767</td></tr>
<tr><td>-50.00 to +150.00 °C</td><td>-5000 to +15000</td></tr>
<tr><td>-58.00 to +302.00 F</td><td>-5800 to +30200</td></tr>
<tr><td>0 - 65000 Ω</td><td>0 to 65000</td></tr>
<tr><td>0 - 4500 Ω</td><td>0 to 4500</td></tr>
</table>
</td><td>R</td></tr>
</table>

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12.8 ANALOG CONVERSION

NOTE: The values in registers R 1004 - R 1007 are zero for the first program cycle.

If bit 7 of R 1000 (Mode register) is not set, no analog conversion is performed (R 1004 - R 1007 = 0).

1) Conversion in the END routine

Software	Conversion
FBK	The conversion is always done during the END routine.
STL	If bit 7 of register R 1001 is set, the conversion is done in the END routine.

2) Direct Jump to Pointer in Operating System

Software	Conversion
FBK	This call is not possible when using the AINJ function block.

STL	Instead of the conversion being done in the END routine, you can jump directly from the program to a pointer in the operating system, which references the analog conversion routine (Pointer: $C10E).
	
	Analysis of converted channels: Carry = 0 ... Conversion ended
	Accu B ... Converted channel
	
	Example
	`LDD # $C10E`
	`XGDX`
	`JSR X 000`
	`BCS BUSY`
	`LDX# R 1004` `Analysis of the converted channel`
	`ASLB` `Accu B: converted channel number (0/1)`
	`ABX`
	`LDD X 000`
	`...`
	`...`
	`BUSY RTS`

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3) Channel Refresh Time (with conversion in END routine)

a) Program cycle time is less than channel conversion time (depends on the filter)

Refresh time$_{max}$ = Number of channels * (Channel conversion time + Program cycle time

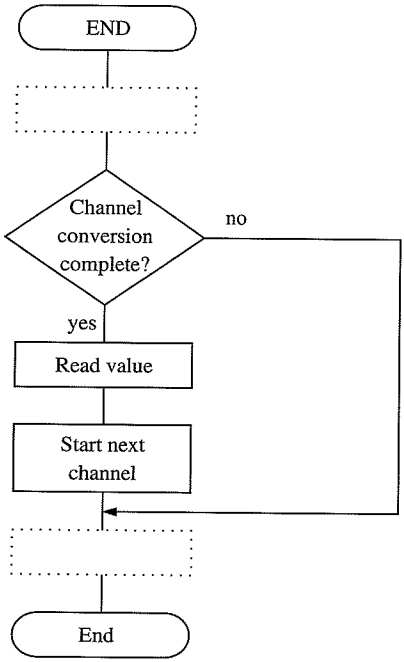
b) Program cycle time is longer than the channel conversion time (depends on the filter)

Refresh time = Number of channels * Program cycle time (one channel per cycle)

4) END Routine

If the analog conversion is executed in the END routine, the routine controls whether the conver a channel is finished. If "yes", the value is read and the conversion of the next channel is started. "no", the analog conversion part of the program is skipped.

Flow chart:



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13. ANALOG OUTPUTS

Analog outputs are utilized for converting internal numerical values from the PLC into current and voltage.

13.1 TECHNICAL DATA

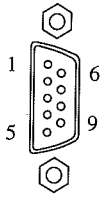
Amount	2
Revision	Short circuit protected
Addressing	Through the operating system
Voltage output	±10 V / 10 mA
Current output	0 - 20 mA, load 50 Ω (400 Ω max.)
Resolution D/A conversion	12 bit
Offset at 25 °C	Software compensation to ±1 LSB[1)]
Offset drift	±0.02 % of full scale / °C (±0.8 LSB/°C)[1)]
Gain error at 25 °C	Software compensation to ±0.5 %
Gain drift	±0.02 %/°C
Gain error load	0.01 %/Ω
Linearity	±1 LSB[1)]
Response time constant	< 1 msec
Maximum output level at reset (or before initialization)	±50 mV or -0.3 mA

[1)] LSB ... Least Significant Bit

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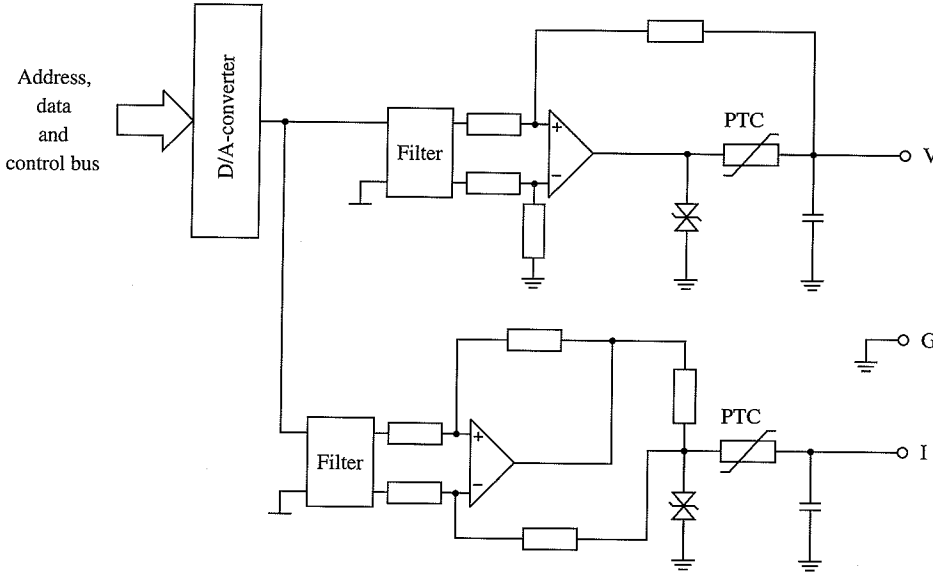
13.2 PIN-OUTS

9 pin D-type (female)



Pin	Assignment
1	V output 1
2	I output 1
3	n.c.
4	V output 2
5	I output 2
6	GND
7	n.c.
8	n.c.
9	GND

13.3 OUTPUT CIRCUIT

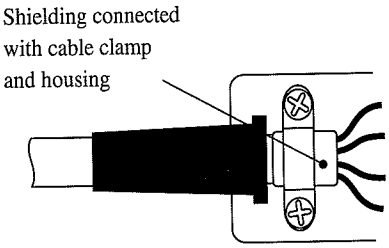


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13.4 GROUNDING YOUR CABLE SHIELDING

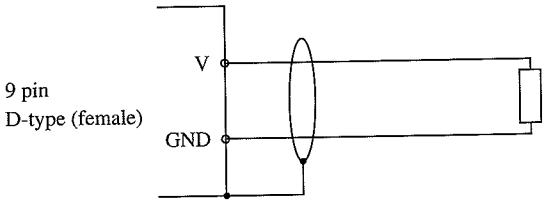
Metal screws or a metallic connector housing are the easiest and most efficient methods of diverting any possible disturbances to the housing of the Compact PLC.

The cable shielding should be in direct contact with the connector housing.

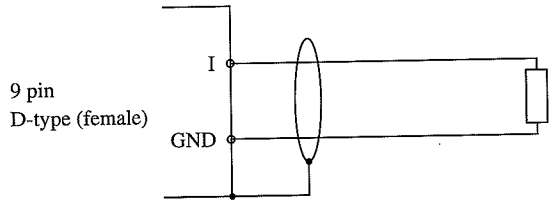


13.5 WIRING

Voltage output



Current output



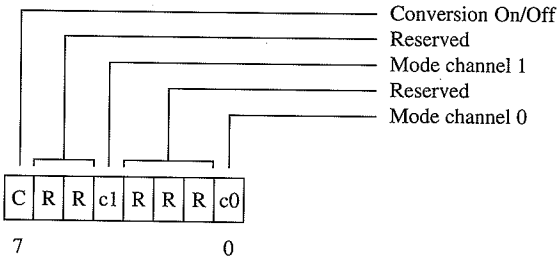
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13.6 SOFTWARE OPERATION

The initialization of the analog outputs is done with the register R 1009. The values to be conve stored in registers R 1010 - R 1013.

The initialization can either be done with commands in STL or with the help of the AOTF funct block (see section 13.7).

Register R 1009



Conversion On/Off	Switches the analog conversion on/off. If it is switched off, the analog outputs are 0 (the conte registers R 1010 - R 1013 are retained). 0 ... Conversion off 1 ... Conversion on
Reserved	Reserved for later use.
Mode channel 1	Bit 4 is used to set the mode for channel 1.
Reserved	Reserved for later use.
Mode channel 0	Bit 4 is used to set the mode for channel 0.

Mode	Signal
0	±10 V
1	0 - 20 mA

Mode	Signal
0	±10 V
1	0 - 20 mA

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Registers R 1010 - R 1013

Source registers	In registers R 1010 - R 1013, the values to be converted are stored.

Registers	Channel
R 1010&	0
R 1012&	1

Value range:

Signal	Value
±10 V	-32768 to +32767
0 - 20 mA	0 to 32767

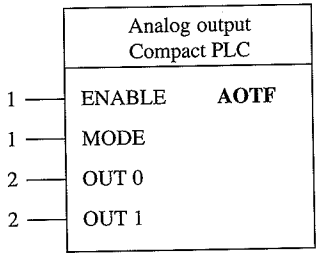
13.7 AOTF - ANALOG OUTPUT COMPACT PLC

This function block is used to initialize the analog outputs. The digital values to be converted are given to the function block through inputs OUT 0 and OUT 1.

NOTE: The analog conversion is only done with a value change. The value comparison is done in a system interrupt. After a power on or a reset (SW or HW), the outputs are set to 0.

AOTF

Function block length: 14 lines
First Scan: No



Inputs/Outputs	Description	Address types
ENABLE	If the ENABLE input is set to 1, the function block is executed.	R, F, #
MODE	Sets the modes for the channels.	R, #

Channel	Bit
0	0
1	4

Mode	Signal
0	±10 V
1	0 - 20 mA

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<table>
<tr><th>Inputs/Outputs</th><th>Description</th><th>Addres</th></tr>
<tr><td>OUT0</td><td>Contains the values to be converted from channel 0.
Value range:
<table>
<tr><th>Signal</th><th>Value</th></tr>
<tr><td>±10 V</td><td>-32768 to +32767</td></tr>
<tr><td>0 - 20 mA</td><td>0 to 32767</td></tr>
</table></td><td>R</td></tr>
<tr><td>OUT1</td><td>Contains the values to be converted from channel 1.
Value range:
<table>
<tr><th>Signal</th><th>Value</th></tr>
<tr><td>±10 V</td><td>-32768 to +32767</td></tr>
<tr><td>0 - 20 mA</td><td>0 to 32767</td></tr>
</table></td><td>R</td></tr>
</table>

13.8 ANALOG CONVERSION

The analog conversion is only done with a value change. After a power on or a reset (SW or HW registers R 1010 - R 1013 and therefore the outputs as well, are set to 0.

1) Value comparison in system interrupt

The value comparison is done in a system interrupt. Only one channel is checked per system int i.e., the fastest update time per channel is 20 msec.

2) Direct jump to pointer in operating system

In addition to the value comparison in the system interrupt, a pointer can be jumped to directly f program. This pointer references the analog conversion routine (Pointer: $C111). Shorter update are accomplished in this way. One channel is checked per call.

Example:
```
LDD   # $C111     Address of the operating system routine
XGDX
JSR   X 000       Operating system routine call
```

3) Checking a single channel

This method is used if only one analog output is required. As in point 2 you make a jump to a po the operating system which references the analog conversion routine (Pointer: $C120). The chan number is sent to Accu B.

Example:
```
LDD   # $C120     Address of the operating system routine
XGDX
LDAB  Channel number (0/1)
JSR   X 000       Operating system routine call
```


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14. COUNTER INPUTS AND INTERRUPT INPUT

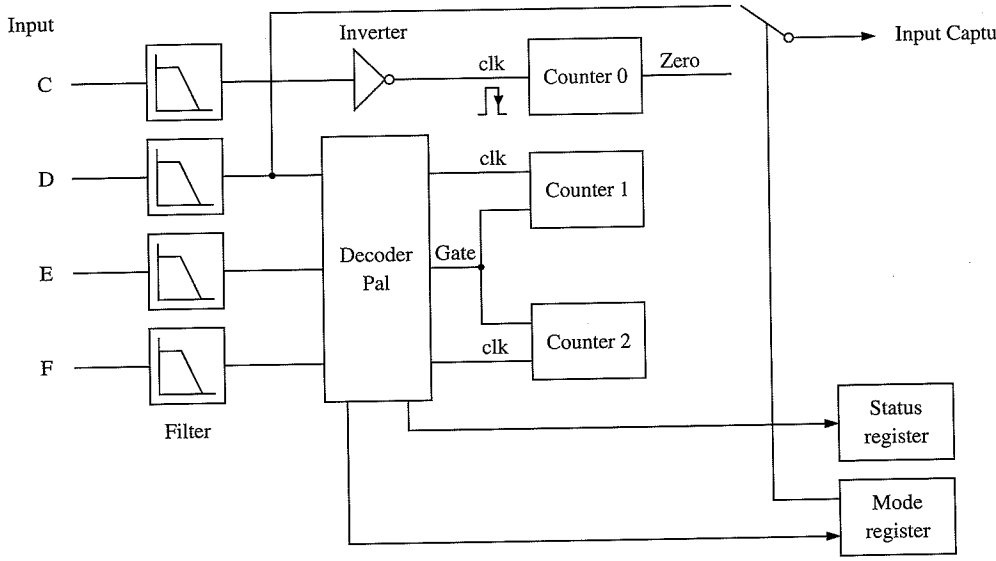
The Compact PLC is equipped with 16 digital inputs. Inputs C - F can also be used for special assignments:

- Event counter
- Interrupt input
- Reference input
- Incremental encoder (Channels A and B) for positioning tasks

The software for the operation of the inputs is saved on the standard software diskette for the Compact Control.

To follow is a description of the input functions, once in graphic format (an overview) and once in tabl form.

Overview of Functions



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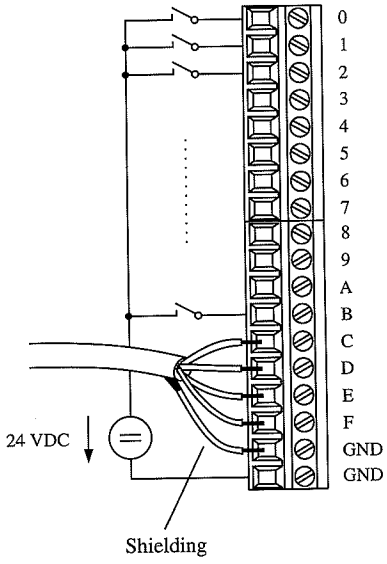
Input Functions

Input	Function
C	Decrements with every negative edge of counter 0. Counter 0 can be used in two ways. The definition is d through the MODE function block input or in the mode register (see section "14.6.3 Mode Register"). 1) Event counter ... Counter with 4 bytes (0 - 4 294 967 295) 2) HW counter ... Counter with 2 bytes (0 - 65535) The hardware counter can be used for generating interrupts. The interrupt is executed if the counter rea value of 0 (see also section "14.5 Interrupt Mode").
D	This is used as a reference pulse input or an interrupt input. The definition is done through the MODE fun block input or in the mode register (see section "14.6.3 Mode Register"). 1) Reference pulse input: Used to set the counter to a predetermined value (minimum pulse duration: 50 µsec). 2) Interrupt input The use of input D as an interrupt input is described in section "14.5 Interrupt Mode".
E	Decrements counter 1 or is used as input A for two channel counting. The definition is done through the M function block input or in the mode register (see section "14.6.3 Mode Register"). 1) Event counter ... Counter with 4 bytes (0 - 4 294 967 295) 2) Input A For positioning tasks, a two channel counting with quadruple evaluation can be executed. The first cha connected to input E.
F	Decrements counter 2 or is used as input B for two channel counting. The definition is done through the M function block input or in the mode register (see section "14.6.3 Mode Register"). 1) Event counter ... Counter with 4 bytes (0 - 4 294 967 295) 2) Input B For positioning tasks, a two channel counting with quadruple evaluation can be executed. The second c is connected to input F.

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14.1 WIRING

Wiring schematic with up to twelve digital inputs, three counter inputs and an interrupt input:



14.2 USING THE COUNTERS

The counters can be operated with the CMDC function block or the CMDD function block or by calling operating system routines from the STL.
These two methods can also be combined with each other.

The software for the operation of the inputs is saved on the standard software diskette for the Compact Control.

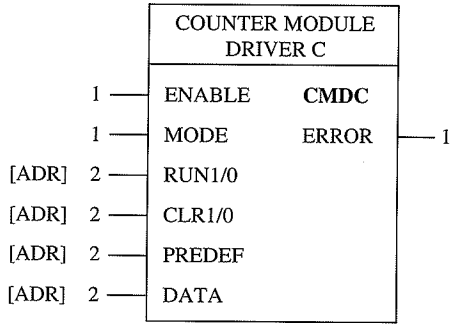
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14.3 CMDC - COUNTER MODULE DRIVER (BRCOMP)

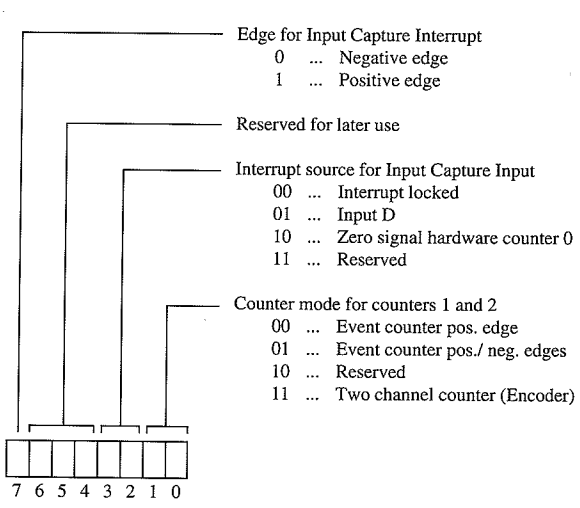
When using this function block, preselected values and new counter states are taken or updated next END (program end).

CMDC

Function block length: 120 lines
First Scan: Yes



Inputs/Outputs	Description	Address
ENABLE	If the ENABLE input is set to 1, the function block is executed.	R, F,
MODE	Sets the counter operating mode.	R, #



Event counter 0 always responds to the positive edge. This setting cannot be changed.
If the zero signal from counter 0 is selected as the interrupt source, bit 7 must be set for the positive edge. Otherwise no interrupt is executed.
Bit 7 will only change if the status of bits 0 - 3 changes.
If counter 0 is used as the interrupt source, the preset value for counter 0 may only be a value in between 3 and 65535 (see section "14.6.8 Calling Operating System Routines", point 3 for the transfer of preset values).

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Inputs/Outputs	Description	Address types
RUN1/0	The start address of a 4 byte long range of memory is attached to this input. Every counter can be stopped or restarted again with this range of memory. Memory assignment / Memory status 1st byte ... Counter 0 — 0 ... Stopped 2nd byte ... Counter 1 — 1 ... Continue 3rd byte ... Counter 2 4th byte ... Encoder position This memory can naturally only be used sensibly if the proper operating status mode is also set. E.g.: Setting the fourth byte is useless if two channel counter mode is not selected.	[ADR] R, [ADR] F
CLR1/0	The start address of a 4 byte long range of memory is attached to this input. Every counter can be set to the preset value with this memory. Assigning the Memory / Memory status 1st byte ... Counter 0 — 0 ... Continue 2nd byte ... Counter 1 — 1 ... Set to preset value 3rd byte ... Counter 2 4th byte ... Encoder position This memory can naturally only be used sensibly if the proper operating status mode is also set. E.g.: Setting the fourth byte is useless if two channel counter mode is not selected.	[ADR] R, [ADR] F
PREDEF	The start address of a 16 byte range of registers is attached to this input. This memory contains the preset values of the counter. Bytes 1 - 4 ... Preset value counter 0 Bytes 5 - 8 ... Preset value counter 1 Bytes 9 - 12 ... Preset value counter 2 Bytes 13 - 16 ... Preset value encoder position This memory can naturally only be used sensibly if the proper operating status mode is also set. E.g.: Setting registers 13 - 16 is useless if two channel counter mode is not selected.	[ADR] R
DATA	The start address of an 18 byte range of registers is attached to this input. This memory contains the counter states of the counters Bytes 1 - 4 ... Counter status counter 0 Bytes 5 - 8 ... Counter status counter 1 Bytes 9 - 12 ... Counter status counter 2 Bytes 13 - 16 ... Counter status encoder position Bytes 17 - 18 ... Counter status counter 0 - Hardware counter This memory can naturally only be used sensibly if the proper operating status mode is also set. E.g.: Reading registers 13 - 16 is useless if two channel counter mode is not selected.	[ADR] R
ERROR	This output indicates that an input is either not connected or is connected incorrectly.	R, F

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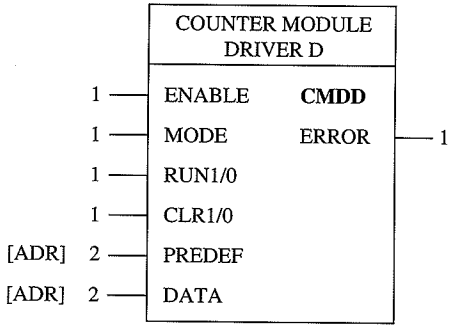
14.4 CMDD - COUNTER 0 MODULE DRIVER (BRCOMP)

The hardware counter can only be predefined if the counter is not selected as interrupt source. A hardware counter is predefined, it must be defined as interrupt source.
The actual value of the hardware counter only changes to the predefined value after the next edg the counter input.

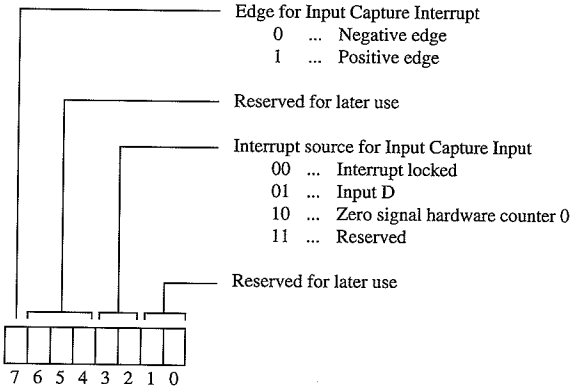
The hardware counter cannot be stopped.

CMDD

Function block length: 90 lines
First Scan: Yes



Inputs/Outputs	Description	Address
ENABLE	If the ENABLE input is set to 1, the function block is executed.	R, F,
MODE	Sets the operating mode of the 0 counter.	R, #



Event counter 0 always responds to the positive edge. This setting cannot be changed.
If the zero signal from counter 0 is selected as the interrupt source, bit 7 must be set for the positive edge. Otherwise no interrupt is executed.
Bit 7 will only change if the status of bits 0 - 3 changes.
If counter 0 is used as the interrupt source, the preset value for counter 0 may only be a value in between 3 and 65535.

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Inputs/Outputs	Description	Address types
RUN1/0	Stop or free counter 0. 0 ... stop 1 ... continue counting Naturally, the memory can only be used in manner that makes sense if the correct operating mode is set. e.g. Setting the memory only has no effect if hardware counter 0 is selected as interrupt source.	R, F
CLR1/0	Setting the counter to a predefined value. 0 ... continue counting 1 ... set to predefined value	R, F
PREDEF	The start address of a 4 byte long register area is connected to this input. The memory contains the predefined value for the counter 0. If the 0 hardware counter is used as the interrupt source, the predefined value for the 0 hardware counter can only lie between 3 and 65535. Offset 0 ... HHB predefined value for counter 0 1 ... HB predefined value for counter 0 Offset 2 ... MB predefined value for counter 0 or hardware counter 3 ... LB predefined value for counter 0 or hardware counter	[ADR] R
DATA	The start address of a 6 byte long register area is connected to this input. The memory contains the position of the counter. Offset 0 ... HHB position of the counter 0 1 ... HB position of the counter 0 2 ... MB position of the counter 0 3 ... LB position of the counter 0 Offset 4 ... HB position of the hardware counter 5 ... LB position of the hardware counter	[ADR] R
ERROR	This output indicates if an input is not connected or is incorrectly connected.	R, F

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14.5 INTERRUPT MODE

An interrupt source for the generation of an interrupt can be defined in the mode register or wit
MODE function block input.
Interrupts are only enabled or locked when the next END (program end) is executed and not aft
definition of the mode register or during the execution of the function block.
By calling the operating system routine, the interrupt is immediately enabled or locked.

1. Input D is used as Interrupt Source

Depending on the definition, the positive or negative edge activates an interrupt on this input. T
interrupt is repeated for every respective event on input D.

For function block CMDC, the edge definition is done with the MODE input. By calling an ope
system routine from the STL the initialization is done in the initialization register $2122.

2. Hardware Counter 0 is used as Interrupt Source

The interrupt is executed if hardware counter 0 has counted from the preset value to 0. Since the
hardware counter only has a 16 bit range, only preset values are sent into the 2 byte numerical r
The valid value range is from 3 to 65535 (see section "14.6.8 Calling Operating System Routine
point 3 for the transfer of preset values).

Hardware counter 0 counts down to 0 and carries on the count again from 65535. The next time
reached an interrupt is executed.
If the procedure should be started from a certain value, hardware counter 0 must be loaded with
preset value after every time zero is reached.

Interrupt Routines

With a One-time write operation (e.g. First Scan), registers R 0968 and R 0969 are assigned wit
address of the interrupt program.

```
...
LDXL   INTR
STX    R 0968
...
```

Interrupt routine INTR is written as a subprogram in STL and closed with RTS.

```
INTR   LDAA   I 043
       ...
       ...
       RTS
```

NOTE: Ladder diagrams cannot be used as interrupt routines, since all ladder diagrams ir
program use the same temporary memory which could lead to incorrect assignme

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14.6 OPERATION IN STL

Utilizing the three counters and the reference or interrupt input can also be done in STL. The settings are made in the END routine.

If the settings must be used immediately, operating system routines can be called. This is done with a pointer in the operating system. The pointer refers to the address of the routine.

Actual values and preset values of the counter sit at operating system addresses. The counter initialization is done with three registers (control register, mode register and initialization register).

14.6.1 Counter Operating System Addresses

Actual value

Addresses	Actual value	Range
$2100 - $2103	Counter 0	0 - 4 294 967 295
$2104 - $2107	Counter 1	0 - 4 294 967 295
$2108 - $210B	Counter 2	0 - 4 294 967 295
$210C - $210F	2 channel counter (Encoder)	0 - 4 294 967 295
$2123 - $2124	Hardware counter 0	0 - 65535

Preset values

Addresses	Preset values	Range
$2110 - $2113	Counter 0	0 - 4 294 967 295 [1]
$2114 - $2117	Counter 1	0 - 4 294 967 295
$2118 - $211B	Counter 2	0 - 4 294 967 295
$211C - $211F	2 channel counter (Encoder)	0 - 4 294 967 295

[1] If counter 0 is used as a hardware counter, the preset value is between 3 and 65535 (2 byte counter).

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14.6.2 Control Register $2120

Bit	Function
0	Enable counter 0
1	Enable counter 1
2	Enable counter 2
3	Enable 2 channel counter (Encoder)
4	Clear counter 0
5	Clear counter 1
6	Clear counter 2
7	Clear 2 channel counter (Encoder)

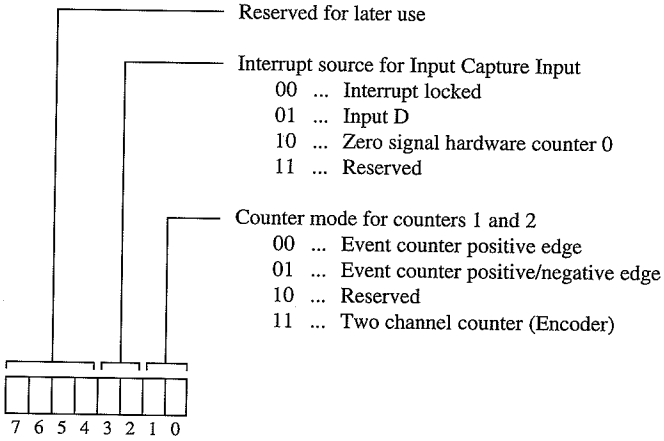
Enable Counter

These bits can be used to individually stop ev
counter and enable it again.

Clear Counter

These bits may only be set for one program c
bit 0 in the initialization register ($2122) is se
respective counter is set to the preset value du
the END routine execution.
For the operating system routines "Load coun
with preset value" these bits do not have to be

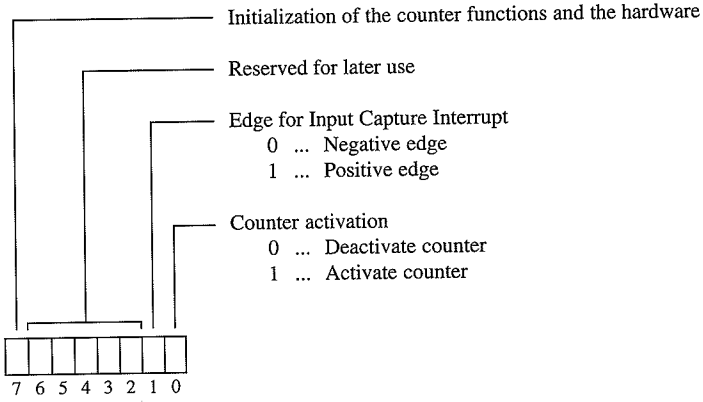
14.6.3 Mode Register $2121



Event counter 0 always responds to the positive edge. This setting cannot be changed.
If hardware counter 0 is used as the interrupt source, the preset value for the hardware counter 0 c
only be between 3 and 65535.

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14.6.4 Initialization Register $2122



If the zero signal from hardware counter 0 is selected as the interrupt source, bit 1 must be set on the positive edge. Otherwise no interrupt is executed.
Changing bit 1 is only accepted if bits 0 - 3 of the mode register are changed.

14.6.5 Addresses of Operating System Routines

Address	Actual value
$C114	Set mode register
$C117	Activate reference pulse
$C11A	Read reference pulse
$C11D	Activate interrupt source zero signal hardware counter 0
$C123	Load counter 0 with preset value
$C126	Load counter 1 with preset value
$C129	Load counter 2 with preset value
$C12C	Load 2 channel counter (encoder) with preset value
$C12F	Read counter 0
$C132	Read counters 1 and 2
$C135	Read two channel counter (encoder)
$C138	Enable Input Capture Interrupt
$C13B	Disable Input Capture Interrupt
$C13E	End referencing
$C141	Initialize counter

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14.6.6 Function of the Counter

Bit 0 must be set in initialization register ($2122), in order to activate the counter and the genera
the Input Capture Interrupt.

The counter functions can be collected or be set for each counter individually (control register $

In the control register ($2120), every individual channel (depending on the operating system mo
be enabled or stopped. Enabled counters decrement the respective actual value range ($2100 - $
of the counter status. This is a 4 byte value (0 - 4 294 967 295). When 0 is reached, it starts decr
ing again from the maximum count.

If hardware counter 0 is used as the interrupt source, the counting range is between 0 and 65535
(Preset value: 3 - 65535).

In the control register ($2120), every individual channel (depending on the operating system mo
be set to the preset value. This must be entered previously in the respective memory location
($2110 - $211F).

The preset value of the counter can be changed at any time. The counter can be set to the preset
any time as well.

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14.6.7 Counter Initialization

Setting the counter mode, the interrupt source and activating the counter are done with the mode register and the initialization register. The operating mode can also be changed at any time during operation.

In order to put the settings to use, bit 7 in the initialization register ($2122) must be set. The initialization is executed and bit 7 is cleared again in the END routine.
For later changes to the Input Capture Edge, bit 7 must not be set (see section "14.6.8 Calling Operatin System Routines", Point 1).

NOTE: After a power-on or a reset, no functions are enabled.

Example Initialization register $2122:
Activate counter
Negative edge for Input Capture Interrupt
Set bit 7 for initialization

Mode register $2121:
Counters 1 and 2 as event counters with positive edge
Interrupt source for Input Capture is input D

The program segment shown below is only executed one time during the first program cycle. The defined initialization is executed in the END routine.

```
LDD   # $2122           Initialization register
XGDX
LDAA  # %10000001       neg. edge Capture Interrupt, Counter act.
STAA  X 000
LDD   # $2121           Mode register
XGDX
LDAA  # %00000100       Interrupt Input D, Counter pos. edge
STAA  X 000
```


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14.6.8 Calling Operating System Routines

1) Setting the Mode Register

No call parameters, no response data

NOTE: Calling the operating system routine may be done one program cycle after the in
tion at the earliest.

Example Initialization register $2122:

Positive edge for Input Capture Interrupt

- Must be positive, if hardware counter 0 is used as the interrupt so
- A change in this bit is only accepted if bits 0 - 3 in the mode regi
also changed.

Mode register $2121:

Counters 1 and 2 as event counters with positive/negative edge
interrupt source for Input Capture is hardware counter 0

The setting is accepted immediately after the operating system routine is called.

```
LDD   # $2121          Mode register
XGDX
LDAA  # %00001001      Counter pos/neg edge, Int HW-counter
LDAB  # %00000011      Positive Edge Capture Interrupt
STD   X 000
LDD   # $C114          Addr of the OS routine: "Set Mode regi
XGDX
JSR   X 000            Operating system routine call
```


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2) Reference Pulse

Before the call "Read reference pulse", the function "Activate reference pulse" must be called first. Reference bit 0 is set to 0.
When the reference pulse occurs the reference bit is set to 1. This remains 1 until the function "Activate reference pulse" is called again.

Activate Reference Pulse:

No call parameters, no response data

```
LDD   # $C117          Activate reference pulse call
XGDX
JSR   X 000
```

Read Reference Pulse:

No call parameters, response data in accu A, bit 0

```
LDD   # $C11A          Read reference pulse call
XGDX
JSR   X 000
BITA  # 001           Bit 0 in Accu A set ?
BEQ   LABL
```

3) Activate Interrupt Source Zero Signal Counter 0

Transfer preset value to accumulator D, no response data

```
LDD   # $C11D          Activate interrupt source call
XGDX
LDD   # 10500         E.g. preset value = 10500 pulses
JSR   X 000
```

For the call of this function, the required changes are executed in the mode register ($2121) and in the initialization register ($2122). The counter is written to directly with the transfer value in accumulator D.

NOTE: If this function is used in conjunction with the CMDC function block, it must be coordinated with the register connected to the MODE input. Otherwise the operating mode will be changed again during the END routine.

```
LDAA  # % 100010xx
STAA  R xxxx
LDD   # $C11D          Activate interrupt source call
XGDX
...
```


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4) Changing the Preset Value of Counter x

The preset values of the counter are stored in addresses $2110 - $211F. In order to change the v
the procedure in the following example must be followed.

Example The preset value of counter 0 is changed. The value sits in registers R 2000 - R 2

```
LDD   #$2110          Start address preset value counter 0
XGDX
LDD   R 2000          Higher Word preset value
STD   X 000
LDD   R 2002          Lower Word preset value
STD   X 002
```

5) Load Counter x with Preset Value

The preset values of the counters are stored at addresses $2110 - $211F. The pointers to the oper
system routines sit at the following addresses:

Address	Actual value
$C123	Load counter 0 with preset value
$C126	Load counter 1 with preset value
$C129	Load counter 2 with preset value
$C12C	Load 2 channel counter (Encoder) with preset value

NOTE: The corresponding bits (4 - 7) in the control register **must not** be set .

In order to change the values, the following procedure must be followed:

```
LDD   # $xxxx         Address of the pointer to OS routine
XGDX
JSR   X 000
```


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6) Read Counter x

The actual values of the counters are stored at addresses $2100 - $210F. The pointers to the operating system routines sit at the following addresses:

Address	Actual value
$C12F	Read counter 0
$C132	Read counters 1 and 2
$C135	Read 2 channel counter (Encoder)

NOTE: The corresponding bits (0 - 3) in the control register **must be set.**

In order to read the values, follow the procedure shown below:

```
LDD    # $xxxx          Address of pointer to OS routine
XGDX
JSR    X 000
```

7) Copy Actual Value to Registers

The actual values of the counters are stored at addresses $2100 - $210F. In order to copy the values to registers, the procedure shown in the example below must be followed.

Example The actual value of counter 0 will be copied to registers R 3000 - R 3003.

```
LDD    #$2100          Start address Actual value Counter 0
XGDX
LDD    X 000           Higher Word Actual value
STD    R 3000
LDD    X 002           Lower Word Actual value
STD    R 3002
```


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8) Hardware Counter 0

The actual value of hardware counter 0 is stored at addresses $2123 and $2124. It is read by usi
"Load Counter 0" function (see point 6).

Because of hardware limitations, the status of the 4 byte counter 0 in the memory range $2100 -
cannot be synchronized with the hardware counter.
The effect only occurs if **"Zero Signal Counter 0 as Interrupt Source"** is set. By setting the c
to different preset values during operation, differentiation between real positioning changes, ove
or new start values can no longer be made.
This is not the case for any of the other operating modes.

Addresses $2123 and $2124 always indicate the pulse remaining until the interrupt.

NOTE: If the counter is read with the preset value, the preset value is not accepted imme
The next pulse decrements the old counter state one more time.

Example

3000	Load with preset value (e.g. with 5000)
2999	The next pulse decrements the old counter state
5000	The preset value is accepted
4999	The second pulse decrements starting from the preset value
:	

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15. RELAY EXPANSION CARD FOR BRCOMP

15.1 GENERAL INFORMATION

A relay expansion card is available for the Compact PLC which adds 16 additional relay outputs to the 14 transistor outputs that already exist (O 060 - O 06F).

The Compact PLC and the relay expansion card can be mounted either beside each other or piggyback (one on top of the other).
The connection to the controller is made with the cable BRKA08-0 via the PATA interface. The cable must be ordered separately.

The DOUC function block transfers the output states to the relay expansion card.

15.2 RELAY GROUPS

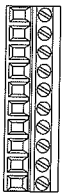
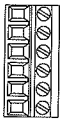
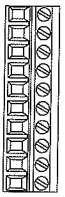
Group	Outputs	Type
1	4	N.O.
2	4	N.O.
3	2	N.O.
4	2	N.O.
5	1	N.O.
6	1	N.O.
7	1	Switching
8	1	Switching

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15.3 TECHNICAL DATA

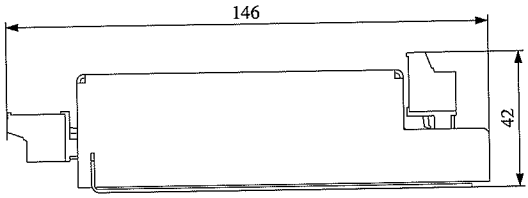
Number	16
Type	Relay
Number of Groups	8
Switching Voltage	5 - 240 VAC, 50/60 Hz 5 - 30 VDC
Switching Current per Output per Group	 max. 3 A max. 6 A
Switching Delay log. 0 → 1 log. 1 → 0	 approx. 10 msec approx. 15 msec
Protection Circuit	external from user
Switching Play mechanical electrical	 $> 2 \times 10^7$ $> 1 \times 10^5$
Relay Supply	24 VDC ±15 %, max. 400 mA
Operating Temperature	0 to 55 °C
Relative Humidity	0 - 95 % non-condensing

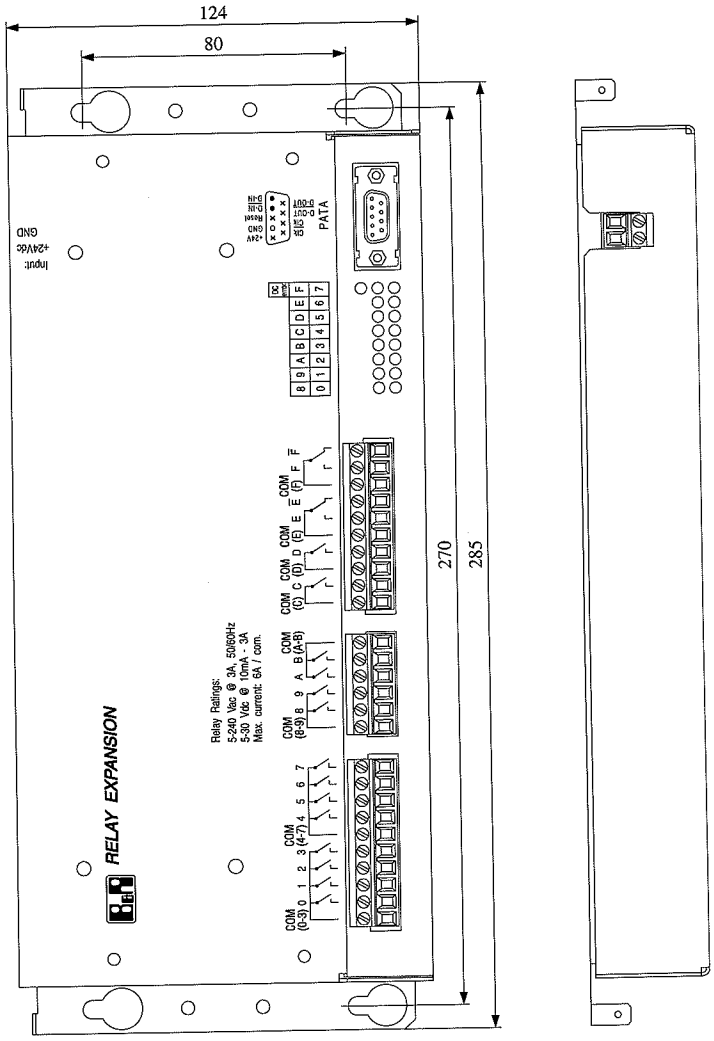
15.4 PIN ASSIGNMENTS

Terminal Block	Pin	Assignment
	1	GND (O 060 - O 063)
1	2	Output 0
2	3	Output 1
3	4	Output 2
4	5	Output 3
5	6	GND (O 064 - O 067)
6	7	Output 4
7	8	Output 5
8	9	Output 6
9	10	Output 7
10		
	11	GND (O 068 - O 069)
11	12	Output 8
12	13	Output 9
13	14	GND (O 06A - O 06B)
14	15	Output A
15	16	Output B
16		
	17	GND (O 06C)
17	18	Output C
18	19	GND (O 06D)
19	20	Output D
20		
21	21	GND (O 06E)
22	22	Output E - N.O.
23	23	Output E - N.C.
24		
25	24	GND (O 06F)
26	25	Output F - N.O.
	26	Output F - N.C.

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15.5 MEASUREMENTS





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15.6 INSTALLATION GUIDELINES

The relay expansion card can be mounted either horizontally or vertically. The distance to the neighboring module caused by the fastening bracket is enough to ensure sufficient air circulatio

The area under the relay expansion card is to be kept below the maximum operating temperatur 55 °C. A fan is not required to cool the housing.

15.7 MOUNTING

Two Possibilities

- directly on the back panel of the enclosure
- on mounting rail

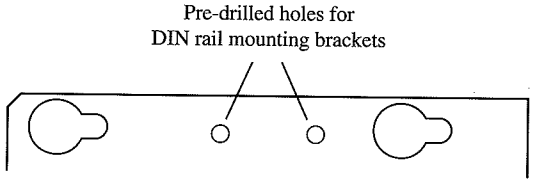
Directly on the Back Panel of the Enclosure

The chassis is to be screwed onto the back panel of the enclosure with the four mounting holes n sure there is good contact with the back panel.

M5 screws are to be used (distance between holes: 80 * 270 mm).

On Mounting Rail

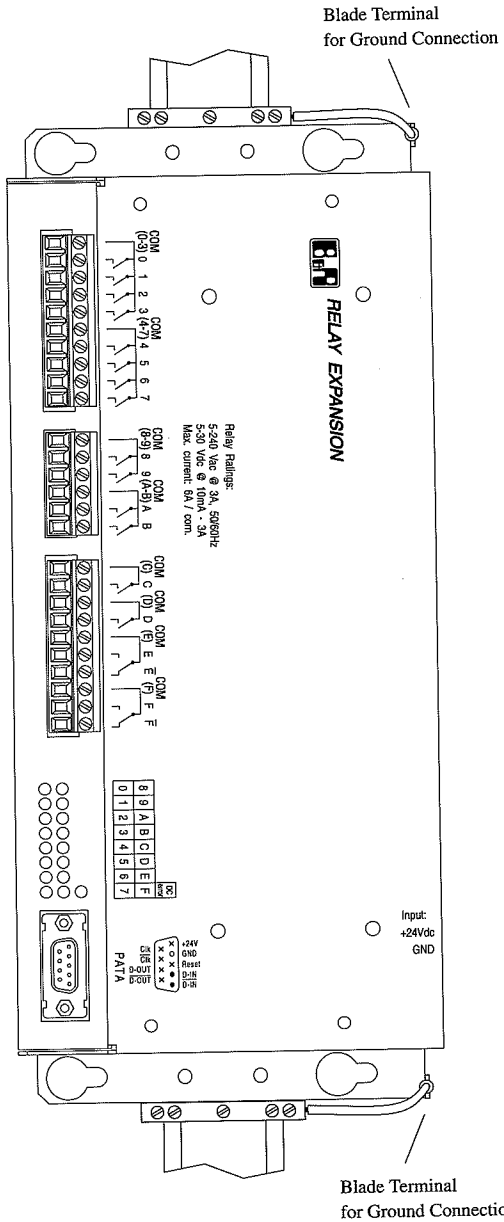
In order to mount the chassis on mounting rail (DIN EN 50022-35), the two accompanying mou rail fasteners (type: KSA10) must be screwed to the relay expansion card.



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Install relay expansion card on the mounting rail. The mounting rail must be grounded!

Install a grounding clamp left and right of the relay expansion card. Ground the relay expansion card with the blade terminal provided.



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15.8 COMPACT PLC AND RELAY EXPANSION CARD

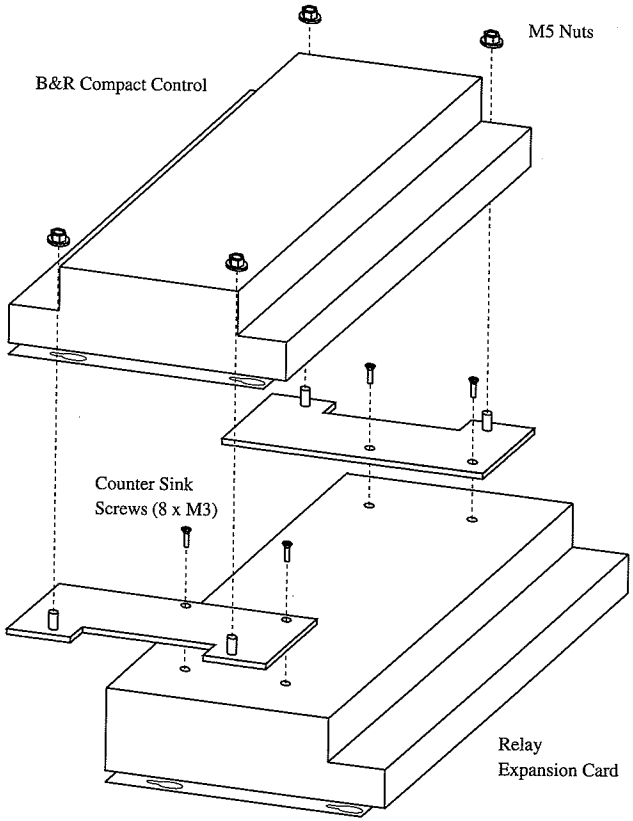
The Compact PLC and the relay expansion card can be mounted either beside each other or pigg
(one on top of the other).

1. Beside Each Other

If the two housings are mounted next to each other, please follow installation and mounting inst
given.

2. Piggyback

With this type of installation, the relay expansion card is first mounted either directly on the bac
of the enclosure or on the mounting rail (see instructions). Then the Compact PLC is fastened to
relay expansion card with the two mounting plates.
The mounting plates are included with the delivery of the relay expansion card.

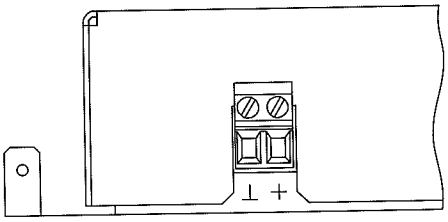


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15.9 CONNECTION TO THE COMPACT PLC

The connection to the Compact PLC is made with the cable BRKA08-0 via the PATA interface. The cable must be ordered separately.

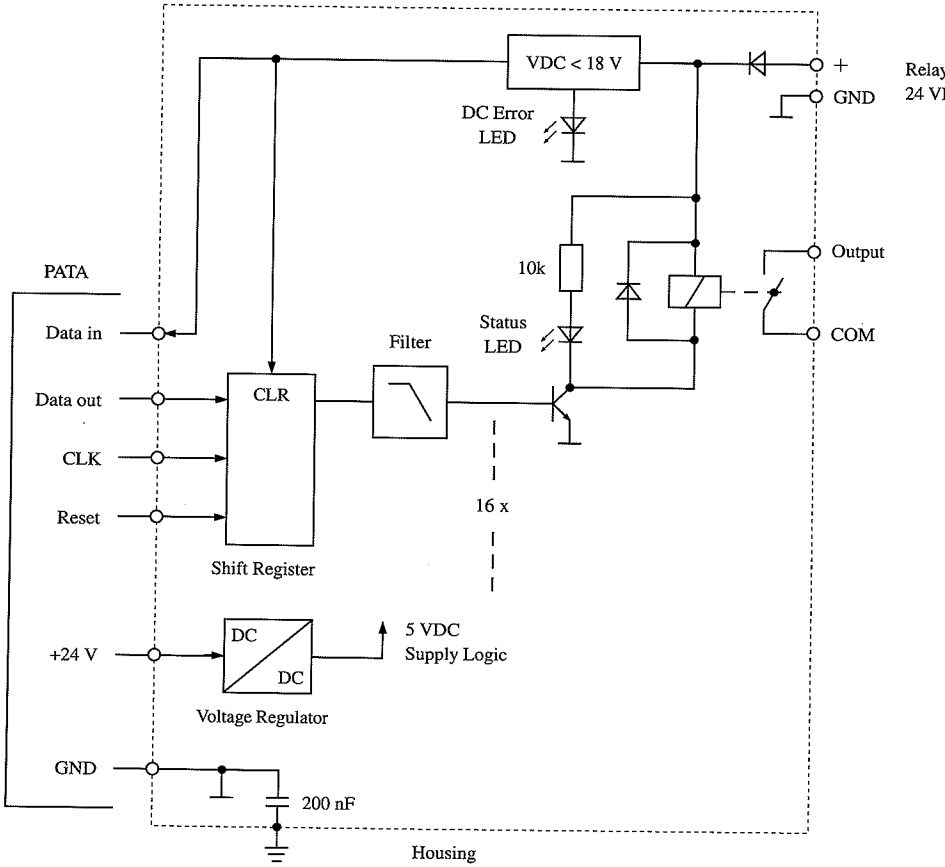
15.10 RELAY SUPPLY



\+ +24 VDC ±15 %, max. 400 mA
⊥ GND

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15.11 SWITCHING CIRCUIT



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16. IF1 - RS232 INTERFACE

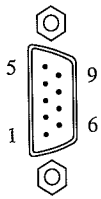
16.1 TECHNICAL DATA

Interface	RS232
Galvanic isolation	NO
Connection	9 pin D-type (male)
Max. distance	15 m, shielded cable
Handshake lines [1]	DSR, RTS
Baudrate	300 - 19200 Baud
Data format Data bits Parity Configuration	 5 to 8 yes / no / even / odd software
Supply for Compact MMI P120 and MMI P121	+5 V / 500 mA

[1] The DTR signal can be created from the RTS with the appropriate interface software (see section "18. Using Interfaces IF1 and IF2").

16.2 PIN-OUTS

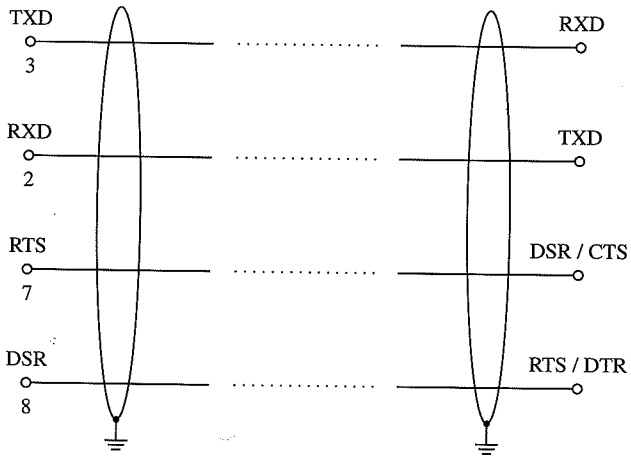
9 pin D-type (male)



Pin	Assignment
1	
2	RXD
3	TXD
4	+5 V / 500 mA
5	GND
6	
7	RTS
8	DSR
9	

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16.3 WIRING



16.4 GROUNDING AND SHIELDING

Shielded cable must be used for interface connections. The cable shielding must be grounded at
ends.

16.5 SOFTWARE OPERATION

The software functionality of the interface is described in section "18. Using Interfaces IF1 and I

16.6 COMPACT MMI P120 AND MMI P121

Interface panels Compact MMI P120 and MMI P121 are available for the Compact PLC. These
connected to the IF1 interface (connecting cable: BRKACOMP1-0). Supply is through pin 4.

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17. IF2 - RS232/RS485 INTERFACE

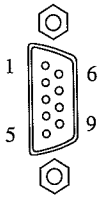
17.1 TECHNICAL DATA

Interface	RS232	RS485
Galvanic isolation	NO	YES
Max. distance	15 m, Shielded Cable	1200 m, Shielded Twisted Pair
Handshake lines [1]	DSR, RTS	
Connection	9 pin D-type (female)	
Baudrate	300 - 19200 Baud	
Data format Data bits Parity Configuration	5 to 8 yes / no / even / odd software	

[1] The DTR signal can be created from the RTS with the appropriate interface software (see section "18. Using Interfaces IF1 and IF2").

17.2 PIN-OUTS

9 pin D-type (female)



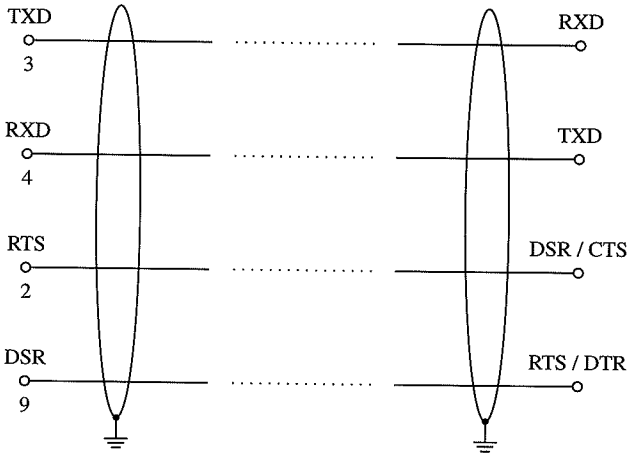
Pin	RS232	RS485
1	GND	
2	RTS	
3	TXD	
4	RXD	
5		DATA
6		$\overline{\text{Enable}}$
7		GND [2]
8		$\overline{\text{DATA}}$
9	DSR	

[2] Pin 6 ($\overline{\text{Enable}}$) must be connected with GND on pin 7 during RS485 operation. This should be take into consideration when cabling with standard cable (standard: connection Pin 6 with Pin 1).

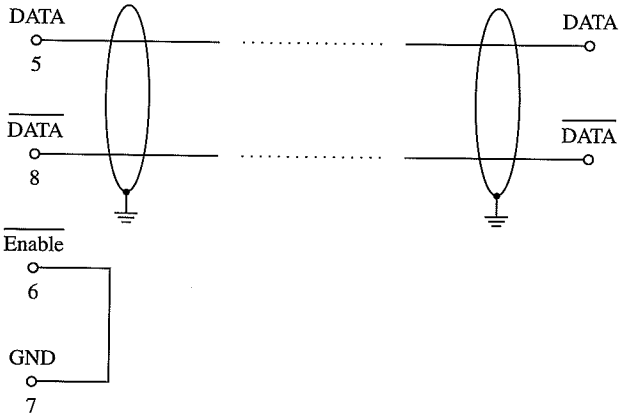
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17.3 WIRING

RS232 interface



RS485 interface



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17.4 GROUNDING AND SHIELDING

Shielded cable must be used for interface connections. The shielding must be grounded on both ends.

17.5 SOFTWARE OPERATION

The software functionality of the interface is described in section "18. Using Interfaces IF1 and IF2".

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18. USING INTERFACES IF1 AND IF2

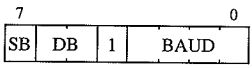
Operating the user interfaces is done with the following registers:

Register	IF1	IF2
Data register	P 100	P 300
Status register	P 101	P 301
Command register	P 102	P 302
Program register	P 103	P 303

Initialization

The program register and the command register are written to with certain preset values during t initialization. This defines the baudrate, data format, parity etc. The initialization is only execute time immediately after switching on the PLC or after a reset.

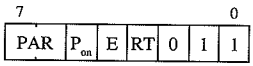
Program register



P 103 / P 303

SB	Stopbits	0	... 1 Stopbit
		1	... if DB=5 and no parity ... 1.5 Stopbi
			if DB=8 and parity ... 1 Stopbit
			in all other cases ... 2 Stopbits
DB	Databits	00	... 8 Databits 10 ... 6 Databits
		01	... 7 Databits 11 ... 5 Databits
BAUD	Baudrate	0110	... 300 1010 ... 2400 1101 ...
		0111	... 600 1011 ... 3600 1110 ...
		1000	... 1200 1100 ... 4800 1111 ...
		1001	... 1800

Command register



P 102 / P 302

PAR	Parity	00	... Parity odd
		01	... Parity even
		10	... Parity bit set during send
		11	... Parity bit cleared during send
P_{on}	Parity on/off	0	... No parity checking, Parity bit not genera
		1	... Parity checking active
E	Echo Mode	0	... Echo Mode off
		1	... Echo Mode on, RT must be 0
RT	RTS line	0	... RTS high, not ready to send (-12
		1	... RTS low, ready to send (+12

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Example Initializing user interface IF1:

Baudrate = 9600, 8 Databits, 1 Stopbit, Parity off, Echo Mode off

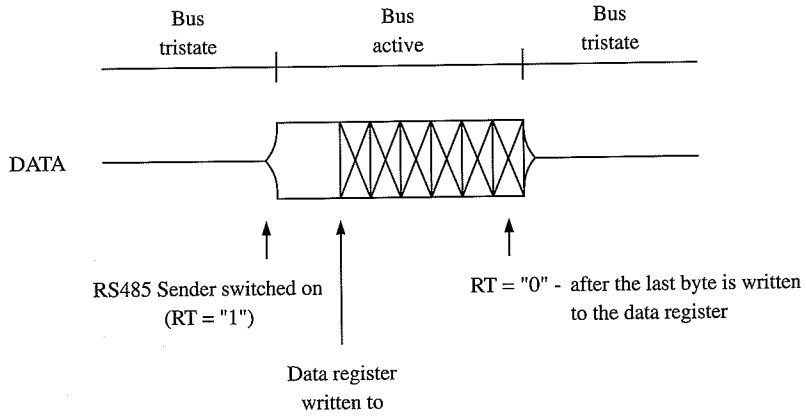
```
LDAB  # %00011110      9600 Baud, 8 Databits, 1 Stopbit
LDAA  # %00001011      Parity off, Echo Mode off
STD   P 102            Program register & command register
```

The RT Bit

RS485 interface - Bus connection:

In order to switch on the RS485 sender, the RT bit must first be set to 1. After writing the last byte to be transmitted to the data register, the RT bit must be reset again. Switching the bus to tristate (high resistance state) is now done automatically after the last byte is sent.
The bus remains active until the character is completely sent (maximum RTS delay is 5 µsec.).

If there is no active sender which also means that the bus is in a state of high resistance, there is a possibility of undefined characters being received.



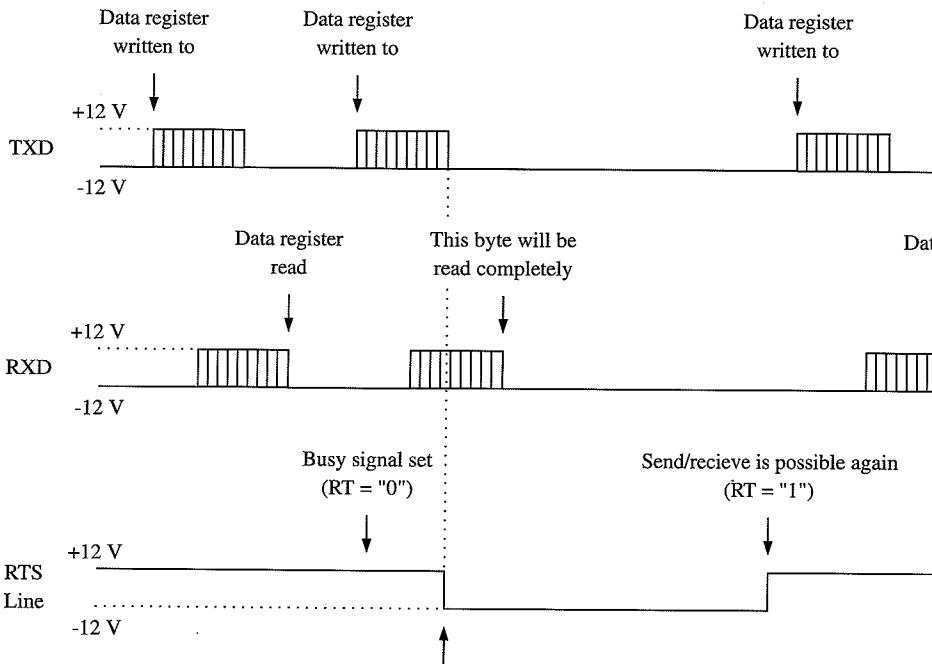
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RS232 Interface - Point to Point:

The RT bit is normally set for RS232 communication. If the user wants to set a busy signal, the can be set to "0".

NOTE: If the RT bit is "0", this sender is also inactive!

The following diagram shows signals in an RS232 communication.



NOTE: The originating sender is also inactive.

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