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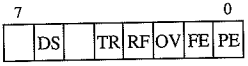
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Status Register

The status register delivers information about the status of the serial interface and about possible errors. The status of the status register must be checked for every send or receive procedure.

Status register



P 101 / P 301

DS	DSR Line Status	0 ... DSR low - Other station ready 1 ... DSR high - Other station not ready
TR	Transmit ready	0 ... Transmitter sends frame (character) 1 ... Send register empty. Sender ready to send a frame
RF	Receive frame	0 ... No frame (character) received 1 ... Frame received
OV	Overrun error	0 ... No error 1 ... Error. The receiver was not properly read before a new frame (character) was received
FE	Framing error	0 ... No error 1 ... Error. Stopbit not recognized.
PE	Parity error	0 ... No error 1 ... Parity test error

Data Register

The data register has two different functions:

- Frames to be received are read from the data register
- Frames to be sent are written to the data register

Data register



P 100 / P 300

DATA Data to be sent or received

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Outputting a Character

Before writing the character to be output to the data register, the transmitter (sender) must first l
checked for whether it is ready to send a character or not (Bit 4 must be 1 in the status register).

```
LDAB   P 101              Status register
BITB   # %00010000        Transmitter ready ?
BLS    NO                 Branch, if transmitter not ready
LDAA   x xxx              Frame (character) to be output
STAA   P 100              Data register
```

Reading a Character

Whether a character has been received or not is determined by checking bit 3 in the status regist
bit 3 = 1, a character has been received. Bits 0 through 2 in the status register indicate whether t
mission errors have occurred (parity error, overrun error or framing error). If one of these error l
set, the received character is invalid.
The data register must also be read if an error has occurred, since the error message must be ack
edged through it.

```
        LDAB   P 101              Status register
        BITB   # %00001000        Frame (character) received ?
        BLS    NO                 Branch, if no character received
        LDAA   P 100              Read data register
        BITB   # %00000111        Transmission error ?
        BLS    FAIL               Branch, if transmission error
        :                         Check received character

FAIL    :
```


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18.1 USING INTERFACE INTERRUPTS

The interface module triggers the following interrupts:

a) Send Interrupt: If the transmitter is ready to send a character.

b) Receive Interrupt: If a character is received (also if an error occurs).

In order to acknowledge the interrupt, the interrupt routine must:

a) Send Interrupt: write to the data register.

b) Receive Interrupt: read from the status register.

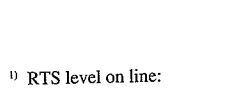
IRQ Vector

The interrupt vector is stored in registers R 0976 and R 0977. Before the interrupt is enabled, the vecto must be set to the address of the user interrupt routine. This definition is done in the initialization routine.

Enabling

Both interrupts are enabled or disabled in command registers (P 102 or P 302). DTR must be active (bit 0 = 1) in order to trigger interrupts.

Command register



P 102 / P 302

[1] RTS level on line:

High ... -12 V
Low ... +12 V

PAR Parity
00 ... Parity odd
01 ... Parity even
10 ... Parity bit set during transmission
11 ... Parity bit cleared during transmission

P_{on} Parity on/off
0 ... No parity test, parity bit not generated
1 ... Parity test active

E Echo Mode
0 ... Echo Mode off
1 ... Echo Mode on, TIC must be 00 or 01

TIC Transmitter Interrupt Control
Send interrupt and handshake line RTS control

00 ... RTS high [1], Send interrupt disabled (Sender off)
01 ... RTS low, Send interrupt enabled (Sender on)
10 ... RTS low, Send interrupt disabled (Sender on)
11 ... RTS low, Send interrupt disabled
(Break on TXD = +12 V)

I IRD - Interrupt Request Disabled (Receive interrupt control)

0 ... Receive interrupt enabled
1 ... Receive interrupt disabled

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Example 1) Enabling the receive interrupt:

```
LDAA   # %00001001
STAA   P 102          Command register
```

2) Enabling the send interrupt:

```
LDAA   # %00000111
STAA   P 102          Command register
```

3) Enabling the send and receive interrupts:

```
LDAA   # %00000101
STAA   P 102          Command register
```

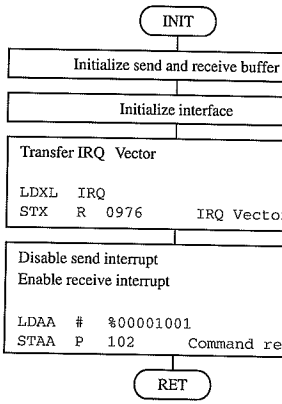
Interrupt Utilization

These two interrupts can be separately enabled or disabled in command registers. They both dea
the same vector however. In order to use the receive and the send interrupts simultaneously, it m
determined whether the interrupt is initiated by the receiver or the sender.
This is done by reading the RF "Receive Frame" bit in the status register (bit 3). If the bit is 0, th
interrupt has been initiated by the sender.

NOTE: If both interfaces (IF1 and IF2) operate with interface interrupts, the status regist
both interfaces must be evaluated in an interrupt routine.

Application Example

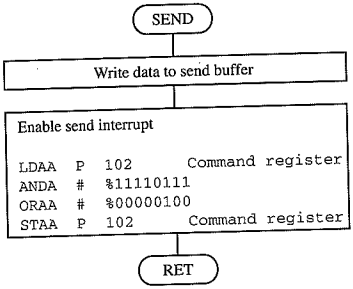
In this example, send and receive interrupts are used at the same time. Initialization takes place in the "INIT" subroutine.

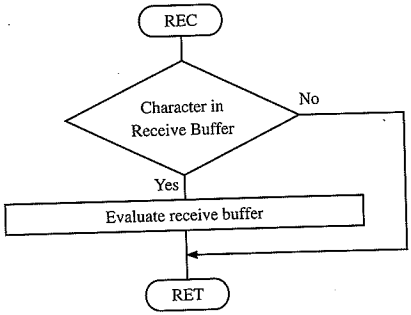


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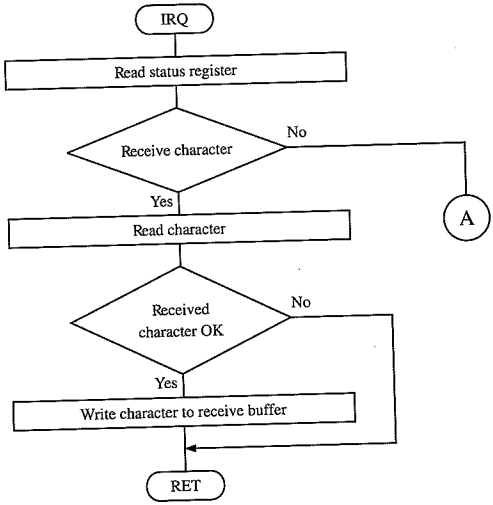
Data is written in a send buffer and the send interrupt is triggered in the "SEND" subroutine.

A check is made by the in the "REC" subroutine to see if a character is in the receive buffer. If a character is received, it is evaluated.





The interrupt routine "IRQ" is divided into two sections. In one section, the received characters are checked and written to the receive buffer. In the other section of the routine, a character from the send buffer is written to the data register.

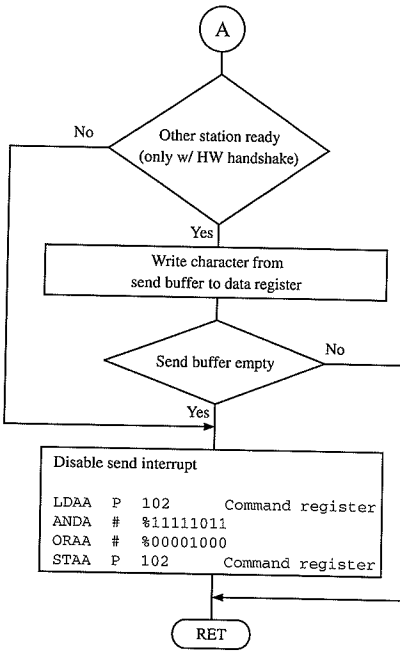


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NOTE:

If the other station isn't ready, the send interrupt will be disabled. A re-enable is done with the "SEND" subroutine.

By disabling the interrupt, the application program is no longer disrupted by continuous interrupt calls.



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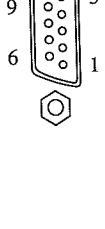
19. IF3 - PATA/SSI INTERFACE

The IF3 interface is a modified RS422 interface. A MINICONTROL operator panel or a relay expansion card can be connected to the IF3 interface (PATA interface).

It is also set up as an SSI interface for connecting absolute encoder systems.

Pin-outs

9 pin D-type (female)



Pin	Assignment
1	$\overline{\text{DATA IN}}$
2	DATA IN
3	Reset
4	GND
5	+24 V
6	$\overline{\text{DATA OUT}}$
7	DATA OUT
8	$\overline{\text{CLK}}$
9	CLK

Shielding and Grounding

For interface connections, shielded cables must always be used. This shielding must always be grounded at both ends.

PATA Interface

Software operation for the MINICONTROL operator panels is described in the "Operator Interface Panel User's Manual" (MATERMINAL-E).

For MINICONTROL operator panel control, the standard software package SWPLCSTD02-0 (Rev. 00.31 or higher) is available from B&R. However, the operator panel software for the Compact Control is saved on the standard software diskette SWPLCBRC01-0.
Panel operation is done with function blocks and table parameter definitions.

Important addresses:

Address	Description
E 05F	Serial key code
A 05E	Serial dislay data
A 05F	Reset signal

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SSI Interface

The following conditions must be met in order to connect absolute encoders to the SSI interface

- Only absolute encoders with a monoflop time between 20 µsec and 260 µsec can be
- Absolute encoders with a maximum 24 Bit (AG24) or 32 Bit (AG32) can be read.

The function blocks AG24 and AG32 are provided for the operation. They are contained in the s software package 4 SWPLCPOS01-0 (rev. 00.32 or higher).

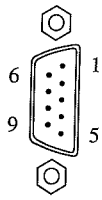
20. IF4 - B&R ONLINE INTERFACE

For communication with the programming device, the Compact PLC uses an on-line interface. T line interface is a TTY interface which runs at 62.5 kBaud and is only used for on-line operation the programming device.

The connection to the programming device is made with an online cable (BRKAOL-0).

Pin-outs

9 Pin D-Type
Connector (M)



Pin	Assignment
1	TXD
2	Reserved
3	RXD RET
4	Reset RET
5	Reserved
6	TXD RET
7	RXD
8	Reset
9	Reserved

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21. IF5 - CAN BUS

21.1 CHARACTERISTICS OF THE CAN BUS

- Field bus
- Low cost
- High resistance to disturbance because of differential signal
- Bus structure
- Open system
- Fast data transfer for small data packets (up to 8 bytes)
- Error recognition via CRC (Cyclic Redundancy Check) and frame check -> hamming distance 6
- Predictable transfer time for high priority messages (real time behavior)
- Simple use

21.2 B&R AND CAN

The controller used by B&R conforms to the CAN Bus Specification 2.0B. In this way, the protocols Standard CAN and Extended CAN can be operated on one bus.

The B&R software supports the Standard CAN Identifier (11 bit) at the time being.

21.3 BUS LENGTH AND CABLE TYPE

The cable type to be used is highly dependent on the bus length required and the number of nodes. The bus length is determined mainly from the bit rate.

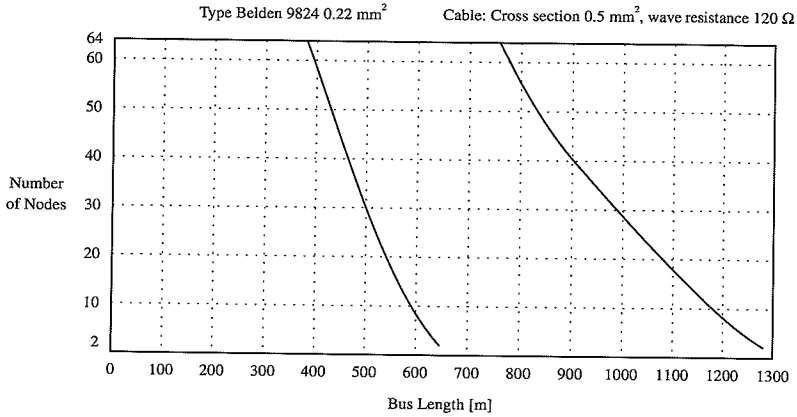
The table on the next page contains some values for the maximum bus length in relation to the transfer rate and the synchronization jump width (SJW). The fourth column contains the permissible oscillator tolerance.

The synchronization jump width (SJW) is the factor that determines how close the controller can synchronized. The larger the synchronization jump width, the smaller the bus length.

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Bit Rate [kBit/sec]	Synchronization Jump Width (SJW)	Bus Length [m]	Permissible Osc. Toler
500	0	67	0.121
	1	56	0.242
	2	33	0.363
	3	10	0.485
250	0	215	0.121
	1	192	0.242
	2	147	0.363
	3	101	0.485
125	0	510	0.121
	1	465	0.242
	2	374	0.363
	3	283	0.485
100	0	658	0.121
	1	601	0.242
	2	488	0.363
	3	374	0.485
50	0	1397 [1)]	0.121
	1	1284 [1)]	0.242
	2	1056 [1)]	0.363
	3	829	0.485
20	0	3613 [1)]	0.121
	1	3329 [1)]	0.242
	2	2761 [1)]	0.363
	3	2193 [1)]	0.485
10	0	7306 [1)]	0.121
	1	6738 [1)]	0.242
	2	5602 [1)]	0.363
	3	4456 [1)]	0.485

Relationship between number of nodes and bus length for certain cable types:



[1)] According to CiA (CAN in Automation), the maximum bus length is 1000 m.

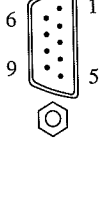
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21.4 CONNECTOR PIN ASSIGNMENTS

The Compact Control **BRCOMP2-0** (operating system version 4.1) is equipped with a CAN Bus interface that conforms to ISO-DIS 11898. The pin assignments of the connector conform to CiA DS 102-1.

Pin Assignments

9 Pin D-Type
Connector (M)



Pin	Assignment
1	
2	CAN L
3	CAN GND
4	
5	
6	
7	CAN H
8	
9	

21.5 WIRING

The wiring is done in the form of a bus structure. Both bus ends are to be terminated with a termination resistance. A node can be connected to the bus with a branch line. The length of the branch line may not exceed 30 cm.
A four conductor twisted pair cable is to be used for the bus cable.

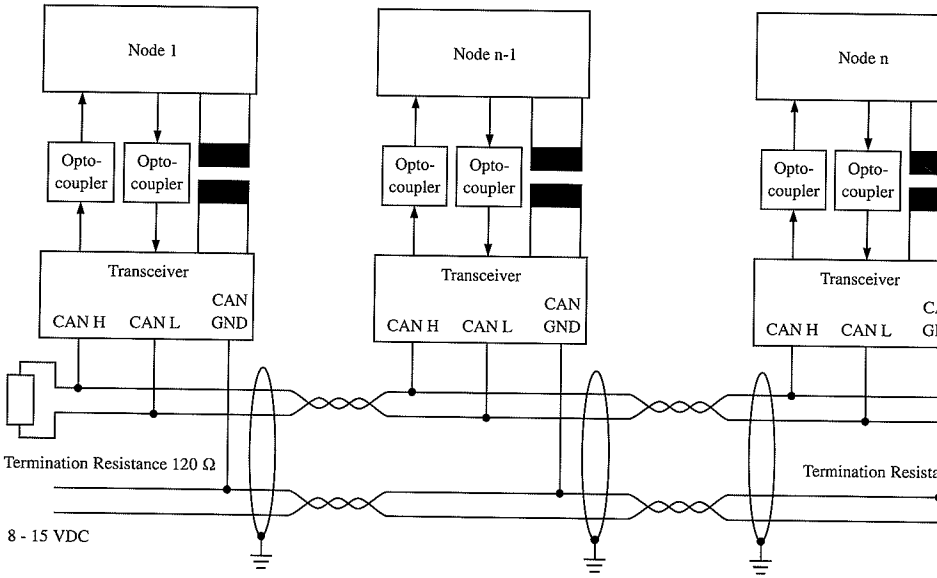
CAN Signal

CAN H	...	CAN High
CAN L	...	CAN Low
CAN GND	...	CAN Ground
CAN+	...	CAN Supply 8 - 15 V

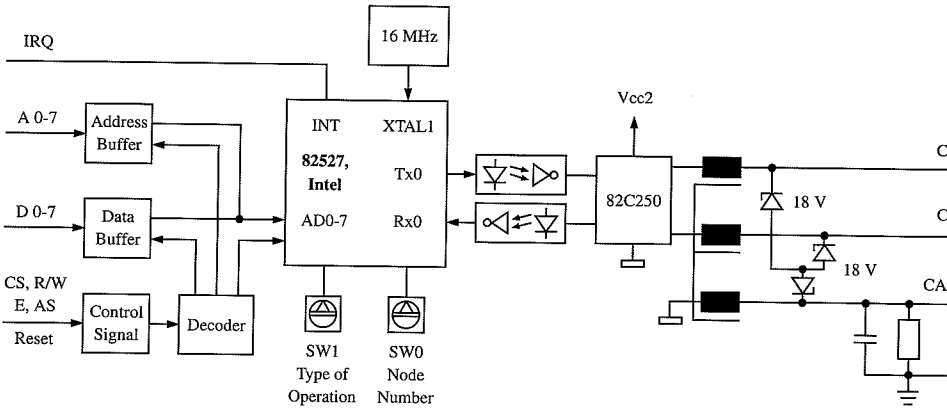
All of the CAN interfaces from B&R are supplied internally, CAN+ is not connected.

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21.5.1 Wiring Principle



21.5.2 Block Diagram of a Node



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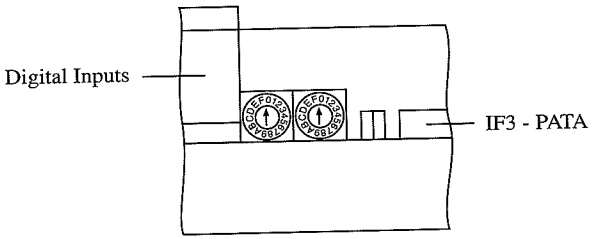
21.6 OPERATING THE CAN BUS

The CAN bus is operated with the function blocks CNSW and CNCS. The function blocks are available as standard software (on 3.5" diskettes).

Language	Model Number
German	SWSPSCAN01-0
English	SWPLCCAN01-0

21.6.1 CNSW - CAN Node Switch

The function block reads the switch settings of both hex switches (between the digital inputs and IF3 - PATA) and provides this information to the CAN Client/Server function block CNCS. Additionally, all switch settings are output directly as values between 0 - 15. The CNSW function block eases the use of the same program for different client stations.



21.6.2 CNCS - CAN Client/Server

The function block allows the communication a standard CAN net (11 bit ID) via CAL/CMS services for transmitting object data. Layer or network management services and identifier distribution services are supported.
That means that CAL is a LMT/NMT/DBT slave of class 0 with static CAN ID distribution. The communication takes place via the CMS protocol for variables and for uncontrolled events.
The Client/Server services for "Read-Only Access, Basic Variable" are not implemented. Of the CMS data types, only integer as byte multiples are supported.

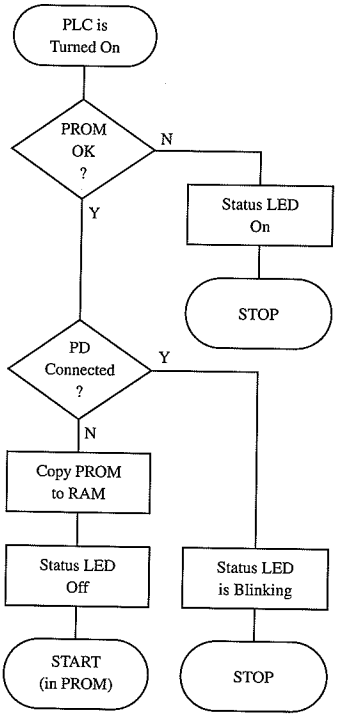
Transfer data (max. 8 bytes) is transferred on the bus in increasing byte order (LSB to MSB) (Little Endian).

Abbreviations

CAL	...	CAN Application Layer
CMS	...	CAN based Message Specification
LMT	...	Layer Management
NMT	...	Network Management
DBT	...	Communication Object Distributor

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22. POWER-ON SEQUENCE



23. COMMAND SET

A 6303 processor (Hitachi) is implemented in the Compact PLC. This is the same processor whic used in the MINICONTROL CPU. Therefore giving full software compatibility to the next size c system.

A complete description of the 6303 processor command set is provided in the "STL Instructions" booklet (MAAWLKB-E).

This booklet contains the following useful information:

- B&R and MOTOROLA Mnemonics
- Descriptions for all instructions
- The possible types of addressing and opcodes
- The possible address codes
- Instruction lengths and executions times
- Changed Flags

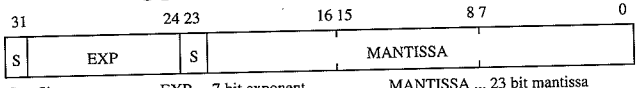
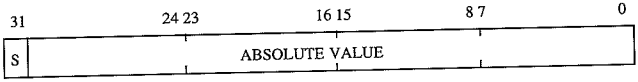
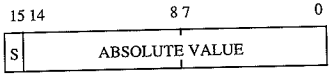
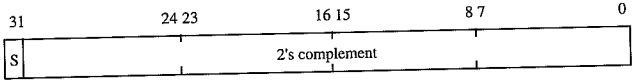
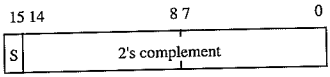
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24. MATHEMATIC ROUTINES

The CPU of the Compact PLC is equipped with fast floating point mathematic routines. These routines are components of the operating system. They are called by means of statement list instruction mnemonics.
In addition to the basic mathematics addition, subtraction, multiplication, division and square root numerous conversion and utility programs available (e.g. for comparing and copying). Numbers are represented in standard 4 byte IEEE format. A detailed description of these mathematic routines can be found in the MAAWLKB-E booklet.

NOTE: Mathematic routines may not be used in the interrupt routines.

Number Formats

Format	Range
IEEE-Floating point format  S ... Sign EXP ... 7 bit exponent MANTISSA ... 23 bit mantissa	$-9.22 * 10^{18}$ to $-9.22 * 10^{-18}$ and $9.22 * 10^{-18}$ to $9.22 * 10^{18}$
Absolute with sign, long 	$\pm 2.15 * 10^9$
Absolute with sign, short 	±32767
Integer, long 	$\pm 2.15 * 10^9$
Integer, short 	-32768 to +32767

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Instr.	Function	Source or Operands	Destination or Result	Execution time in µsec.	Possible Error Messages										
					1	2	3	4	5	6	7	8	9	10	11
MADD	OP1 := OP1 + OP2	OP1, OP2	OP1	209/690	●	●				●	●				
MSUB	OP1 := OP1 - OP2	OP1, OP2	OP1	219/700	●	●				●	●				
MMUL	OP1 := OP1 * OP2	OP1, OP2	OP1	209/803	●	●				●	●				
MDIV	OP1 := OP1 / OP2	OP1, OP2	OP1	190/1980	●	●	●			●	●				
MSQR	OP1 := SQR(OP1)	OP1	OP1	71/8065	●	●				●	●	●			
MSGN	OP1 := OP1 * (-1)	OP1	OP1	85/85											
MCOP	OP2 := OP1	OP1	OP2	46/46											
MEXG	OP1 ↔ OP2	OP1, OP2	OP2, OP1	76/76											
LAL1	Load OP1, abs. with sign 4 byte	(X)	OP1	190/339					●						
LAL2	Load OP2, abs. with sign 4 byte	(X)	OP2	190/339					●						
LAW1	Load OP1, abs. with sign 2 byte	AD	OP1	83/250											
LAW2	Load OP2, abs. with sign 2 byte	AD	OP2	83/250											
LIL1	Load OP1, int. 4 byte	(X)	OP1	197/381					●						
LIL2	Load OP2, int. 4 byte	(X)	OP2	194/378					●						
LIW1	Load OP1, int. 2 byte	AD	OP1	87/260											
LIW2	Load OP2, int. 2 byte	AD	OP2	84/257											
LF1	Load OP1, IEEE	(X)	OP1	88/125	●					●	●				
LF2	Load OP2, IEEE	(X)	OP2	88/125	●					●	●				
CAF	ASCII - IEEE	(X)	OP1	280/2140	●					●	●		●		
SAW	Store OP1, abs. with sign 2 byte	OP1	AD	158/373				●							
SAL	Store OP1, abs. with sign 4 byte	OP1	(X)	169/408				●							
SIW	Store OP1, int. 2 byte	OP1	AD	158/380				●							
SIL	Store OP1, int. 4 byte	OP1	(X)	172/424				●							
SFX	Store OP1, IEEE	OP1	(X)	43/43											
CFA	OP1 - ASCII	OP1	(X)	352/7310	●			●		●	●				
CFA0	OP1 - ASCII with leading zeros	OP1	(X)	310/7190	●			●		●	●				
CFEA	OP1 - ASCII with exp.	OP1	(X)	570/7140	●					●	●				
SFM1	Store OP1 in memory 1	OP1	MEM1	60/60											
SFM2	Store OP1 in memory 2	OP1	MEM2	60/60											
SFM3	Store OP1 in memory 3	OP1	MEM3	60/60											
RFM1	Load OP2 from memory 1	MEM1	OP2	56/56											
RFM2	Load OP2 from memory 2	MEM2	OP2	56/56											
RFM3	Load OP2 from memory 3	MEM3	OP2	56/56											
FM2B	Multiplication 2 x 2 byte	(X) int. 2 byte, AD	(R1048, 1049) 4 byte	115/191											
FM3B	Multiplication 3 x 2 byte	(X) int. 3 byte, AD	(R1048, 1049) 5 byte	156/270											
FM4B	Multiplication 4 x 2 byte	(X) int. 4 byte, AD	(R1048, 1049) 6 byte	192/344											
CBCD	Binary - BCD	(AD) abs. 3 byte	(X) BCD 3 byte	192/1180				●							
CBIN	BCD - Binary	(AD) BCD 3 byte	(X) abs. 3 byte	112/223											
CIA	Binary - ASCII	(R1048, 1049)	(X)	380/2020				●							
CIA0	Binary - ASCII with leading zeros	(R1048, 1049)	(X)	310/1960				●							
CBPP	Binary - physical (parameters)	(X)	(R1048, 1049)	2500/6700	●					●	●				
CBPQ	Binary - physical (fast)	AD, (X)	AD, OP1	780/1700	●					●	●				
CPBQ	Physical - binary (fast)	AD, (X)	AD, OP1	780/1500	●					●	●				
CBP	Binary - physical	(R1046, 1047), (X)	(R1048, 1049), AD, OP1	3400/8300	●					●	●				
CPB	Physical - binary	(R1046, 1047), (X)	(R1048, 1049), AD, OP1	3400/8300	●					●	●				
CIM	Inch - metric	(R1046, 1047), AD	(X), AD	307/472											
CMI	Metric - Inch	(R1046, 1047), AD	(X), AD	307/472											
FCOP	Copy data block	(X), AD	(R1048, 1049)												
FSMB	Load memory area with byte values	(X), AD, R1052	(X)	48 + L * 12											
FSMW	Load memory area with word values	(X), AD, R1052	(X)	48 + L * 14											
FCLR	Clear memory area	(X), AD	(X)	48 + L * 12											
MCMP	Compare OP1 with OP2	OP1, OP2		201/223											●
MHIL	If OP1 > OP2 then OP1 := OP2	OP1, OP2	OP1	215/271											●
MLOL	If OP1 < OP2 then OP1 := OP2	OP1, OP2	OP1	215/271											●

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Error Messages

The error messages in the table (see previous page) which are marked with ●, are possible for the respective function on the same line. If an error occurs during the execution of a routine, the Carry Flag is set and the error number is put into register R 1024.

Error number	Description
1	Range overflow during computation
2	Range underflow during computation
3	Division by 0
4	Range overflow during number format conversion
5	Trimming of Lower Significant Byte (LSB) while loading 4 Byte Mantissa
6	Range overflow while loading numbers
7	Range underflow while loading numbers
8	Negative operand for square root computation
9	Invalid character for string conversion routine
10	Not used
11	Invalid command (trap error set off)
12	Number out of range
13	Exponent error in metric-inch or inch-metric conversion
14	Data overflow in metric-inch or inch-metric conversion

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Operands and Registers

Registers	Function
R 1024	Error number
R 1025	Reserved
R 1026 to R 1029	Operand 1 (OP1)
R 1030 to R 1033	Operand 2 (OP2)
R 1034 to R 1037	Interim memory 1 (MEM1)
R 1038 to R 1041	Interim memory 2 (MEM2)
R 1042 to R 1045	Interim memory 3 (MEM3)
R 1046 to R 1047	Source address
R 1048 to R 1049	Destination address
R 1050 to R 1051	Length
R 1052 to R 1053	Data

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25. SYSTEM REGISTERS AND FLAGS

Several registers and flags are reserved for the operating system. These may not be used or may only be partially utilized by application programs:

Registers:	R 0800 to R 1499
Flags:	F 800 to F 999

Flag addresses beginning at F 800, which are used for operating system functions are entered with the addresses S Dxx or T Dxx:

Addresses	Entered as [1]
F 800	S D00
F 801	S D01
:	:
F 899	S D99
F 900	T D00
F 901	T D01
:	:
F 999	T D99

[1] The programming device permits the entry of the F address, but after [↵] is pressed, the address is automatically converted to S Dxx or T Dxx format.

Enter:	F 820
After [↵] is modified to:	S D20

Enter:	F 980
After [↵] is modified to:	T D80

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The registers and flags which can be used in limited form by applications programs are describe below:

Permitted Access		Address(es)	Function
Read	Write		
		R 0800 to R 0863	Pre-multiplexer for software timers
●		R 0899	First scan register
		R 0900 to R 0963	Counter for software timers
●	●	R 0968, R 0969	HW counter interrupt or interrupt input vector
		R 0972, R 0973	Timer interrupt vector
		R 0974, R 0975	Timer interrupt time
●	●	R 0976, R 0977	IRQ vector
		R 0978, R 0979	Trap vector
●	●	R 0980 to R 0987	Real-time clock
●	●	R 0990	Breakpoint special function
		R 0991 to R 0993	Counter / Multiplexer
		R 0998, R 0999	Run-time watchdog
●	●	R 1000 to R 1013	Analog inputs / analog outputs
●	●	R 1024 to R 1053	Operands and memories for math routines
		R 1054 to R 1499	Reserved for standard function blocks
●	●	S D00 to S D63	Start flags for software timers
●	●	S D85, S D86	Control bits for real-time clock
●		T D00 to T D63	Software times
●		T D64	First Scan Flag
●		T D80 to T D83	Time cycles
●		T D90 to T D93	Time pulses
●		T D99	Battery test

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26. FIRST SCAN FLAG

The first scan flag is a flag (T D64), which is set to 1 automatically during the first program cycle and otherwise is 0. The first scan flag is used for program initialization. Register R 0899 also provides the first scan functions:

T D64	First Scan Flag (1 = first program cycle)
R 0899	First Scan Register (1 = first program cycle)

Example

```
INIT  LDAA  Z D64       First Scan
      BEQ   INIR        Branch, if already initialized
      :
      :                 Initialization
      :
INIR  RTS
```

In the ladder diagram the first scan flag can be connected to the enable input of function blocks which are supposed to be executed only once during the program's first cycle.

NOTE: The B&R PROgramming SYStem command "XFER" allows programs to be downloaded to the CPU without interrupting the application program running in the RAM of the CPU.
The user must switch to the new program manually with a command from the programming device. In this case neither the first scan flag or the first scan register are set during the first program cycle of the new program!

Since the First Scan flag and register are not set, caution is bid when using interrupt routines or B&R MININET.
The address of the interrupt routine is not updated after a program change, if the definition is made in the initialization routine.

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27. LITHIUM BATTERY

The Compact PLC is provided with a lithium battery. This is required in order to provide back-u the SRAM and the real-time clock.

NOTE: Lithium batteries fall into the catagory of hazardous waiste. Please be sure to fol guidelines for disposal that are valid for your area.

Buffer Life

3 years at 70 °C
6 years at 40 °C

NOTE: Take note that the temperature within the housing of the unit can sometimes be u 20 °C above the surrounding temperature.

Power Monitor

The state of the battery can checked with bit 1 of the Inport Address $3480 (see section "34. Inp Address $3480") (hardware monitoring).

0 ... Battery OK (Voltage > 2.55 V)
1 ... Battery dead (Voltage < 2.45 V)

The bit status can be placed on an output. If you are using an operating panel, a respective messa also be output.

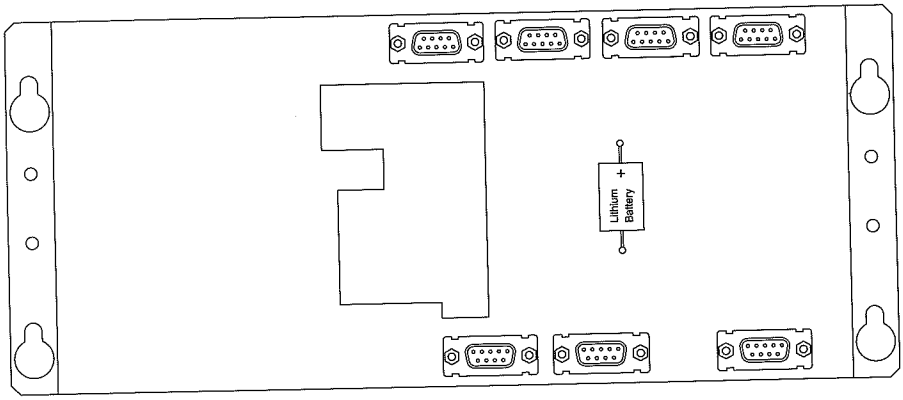
For reasons of compatibility, the state of the battery can also be checked with the register T D99. However, this method should not be used since it is software monitoring!

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Changing the Battery

To change the battery, all power must be switched off.

NOTE: Data stored in RAM and the clock time is lost. By using the B&R PROgramming SYStem "UPDL" command the data can be saved however.

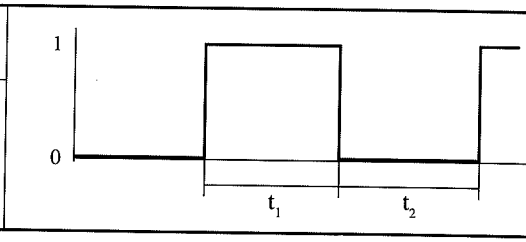


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28. TIME CYCLES

Time cycles are flags which are generated by the operating system:

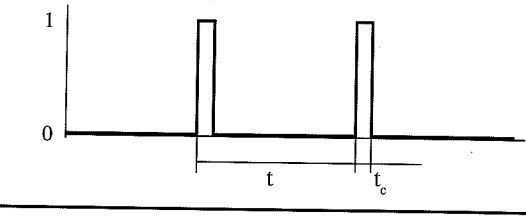
Address	t_1	t_2
T D80	10 msec	10 msec
T D81	40 msec	60 msec
T D82	0.4 sec	0.6 sec
T D83	4 sec	6 sec



29. TIME PULSES

Time pulses are flags which are automatically set to 1 for the length of one program cycle by the operating system.

Address	t
T D90	10 msec
T D91	100 msec
T D92	1 sec
T D93	10 sec



t_c ... Program cycle

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30. REAL-TIME CLOCK

If the PLC is switched off, the real-time clock keeps running (buffered by the lithium battery).

Time registers (all specifications in BCD):

R 0980	1/100 Seconds ($00 to $99)
R 0981	Seconds ($00 to $59)
R 0982	Minutes ($00 to $59)
R 0983	Hours ($00 to $23)
R 0984	Day ($01 to $31)
R 0985	Month ($01 to $12)
R 0986	Year ($00 to $99)
R 0987	Day of the week (0 to 6)

Control of the real-time clock is done by means of two memory locations:

S D85	Clock ON/OFF (1 = ON)
S D86	Set clock ON/OFF (0 = Set clock ON)

To set the real-time clock (the clock must be switched on, i.e. S D85 must be 1):

- Set clock ON (clear S D86)
- Load clock time registers R 0980 to R 0987 with time/date
- S D86 is set automatically at the end of the next program cycle

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31. SOFTWARE TIMERS

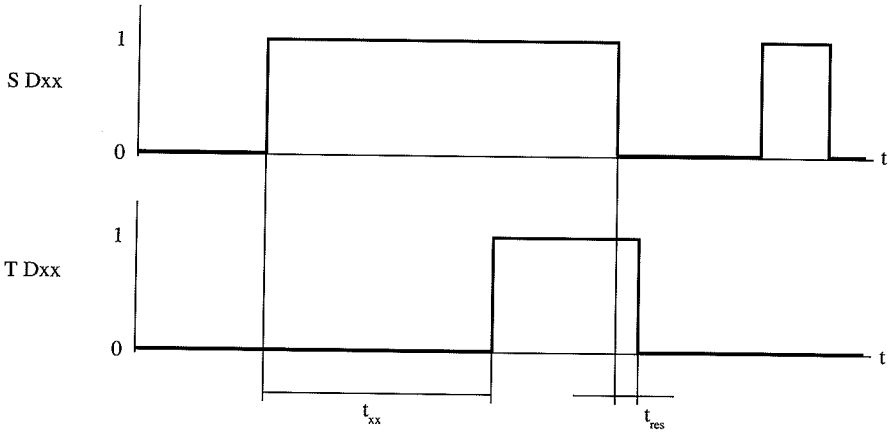
The CPU of the Compact PLC has 64 timers that work on an On-Delay. Every software timer c of the following addresses:

S Dxx — Starts the software timer. By writing a 1 to this flag, the software timer xx (xx = 63) is started. This flag can also be read (e.g., to determine whether a certain sof timer has been started or not).

T Dxx — Result. If this flag contains 1, then the associated software timer has elapsed. Th read-only flag. It is reset when the S Dxx start flag is cleared.

Txx n"nn — Time definition. The Txx instruction defines the duration of the software timer i seconds and 100ths of seconds. This instruction must always be executed; thus it usually placed at the beginning of an application program.

Time Sequence



After the software timer xx has been started by writing 1 to the start flag S Dxx and the elapse of time t_{xx} set in the time definition Txx, the timer flag T Dxx is also set to 1.

After the start flag S Dxx has been reset, timer flag T Dxx is reset in the next program scan by th definition Txx. In the worst case the reset time t_{res} can be one program cycle long.

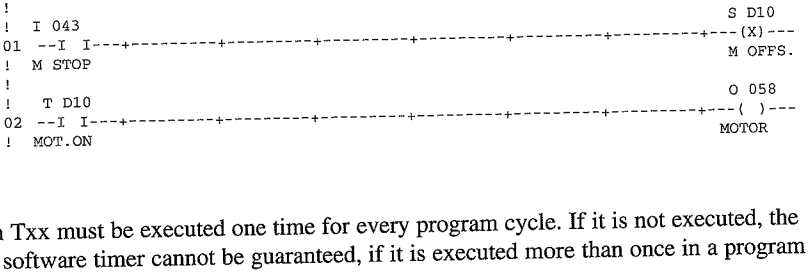
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Example 5.5 seconds after pressing a key (I 042) an motor (O 058) is to be started. Another key (I 043) is used to stop the motor:

```
0000        T10          5"50        Time definition
0001        LDAA    N    I 042       START key
0002        PRS          F 100       Pos. edge of I 042
0003        EORA         F 100       Pos. edge of I 042
0004        RST          F 100       Pos. edge of I 042
0005        PRS          S D10       Start Motor offset
0006        LDAA         I 043       STOP key
0007        RST          S D10       Start Motor offset
0008        LDAA         T D10       Motor offset
0009        STAA         O 058       Motor
0010        END
```

The same program example can also be done in ladder diagram:

```
0000        T10          5"50        Time definition
0001        JSR          LAD1        Ladder diagram call
0002        END
```

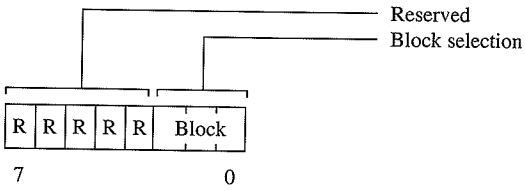


Time definition Txx must be executed one time for every program cycle. If it is not executed, the function of the software timer cannot be guaranteed, if it is executed more than once in a program cycle, then the time is incorrect.

Each software timer occupies one register between R 0800 and R 863 which serves a pre-scalar and another register from R 0900 to R 0963 which serves as a counter. The time definition Txx is a software interrupt that takes approximately 0.5 msec (note that there will be an effect on the program scan when numerous software timers are used!).

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32. INPORT/OUTPORT ADDRESS $3400



Reserved	Reserved for later use.
Block selection	With the bits 0 - 3, the desired 2 Kbyte memory area in the additional EEPROM can be selecte 0 ... Block 0 1 ... Block 1 : : : : 7 ... Block 7 For a more detailed description see section "33. Additional User EEPROM".

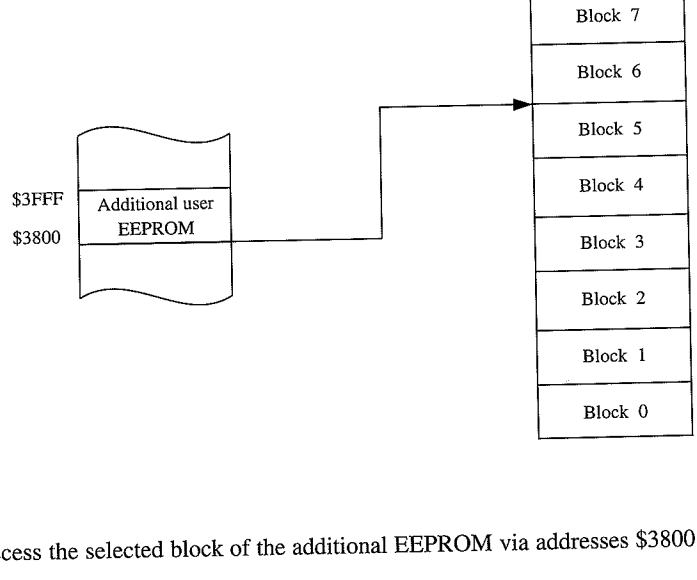
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33. ADDITIONAL USER EEPROM

The user is provided with 16 Kbytes of additional EEPROM memory. It is split up into 8 blocks of 2 Kbytes each. The desired block is defined with the first 3 bits of the Inport/Outport byte (address $3400).

Example Definition of block 6 of the additional EEPROM.

```
LDD   # $3400          Load accu. D with $3400
XGDX                   Set index register to address $3400
LDAA  X 000            Load contents to accu. A
ANDA  # %11111000      Clear bits 0 to 2
ORAA  # 006            Define block 6
STAA  X 000            Store accu. A to address $3400
```



The user can access the selected block of the additional EEPROM via addresses $3800 to $3FFF.

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33.1 READING DATA

To read data from a block, the STL macro DFEE is used

Send parameters:	Source	...	Block number in R 0881 Offset to address $3800 in R 0882&
	Destination	...	Index register
	Data length	...	In accumulator D
Return parameters:	No error:		
	Carry = 0	...	Data transfer OK
	Error:		
	Carry = 1	...	The sum of Offset and Data length is outside of the valid range (> $3FFF)
Used registers:	R 0866&	...	Source address
	R 0868&	...	Destination address
	R 0884&	...	Current data length

```
DFEE  STD   R 0884 DATA 04          Current data length
      STX   R 0868 & DEST 0
      LDD   R 0882 DATA 02          Offset
      ANDA  # %00000111             Limited to 2 Kbytes / Block
      ADDD  # $3800                 Start address EEPROM-Block
      STD   R 0866 & SOURCE 0
      ADDD  R 0884 DATA 04          Current data length
      SUBD  # $3FFF
      BMI   DFE0
*----------------------
      SEC                           Data outside of valid range
      RTS
*----------------------
DFE0  LDD   # $3400                 Inport/Outport Address
      XGDX
      LDAA  R 0881 DATA 01
      ANDA  # %00001111            Block number limited to 0 ... F
      STAA  R 0881 DATA 01
      LDAA  X 000
      ANDA  # %11110000
      ORAA  R 0881 DATA 01
      STAA  X 000                   Select block
*---
```


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```
        LDD   R 0884 DATA 04          Current data length
        LSRD
        BCC   DFE1                    No odd data lengths
        STD   R 0884 DATA 04          Current data length
        LDX   R 0866 & SOURCE 0
        LDAA  X 000                   Read first byte
        INX
        STX   R 0866 & SOURCE
        LDX   R 0868 & DEST 0
        STAA  X 000                   Store first byte
        INX
        STX   R 0868 & DEST 0
        LDD   R 0884 DATA 04          Current data length
*---
DFE1    STD   R 0884 DATA 04          Current data length
        BEQ   DFE2                    Finished
        LDX   R 0866 & SOURCE 0
        LDD   X 000                   Read data
        INX
        INX
        STX   R 0866 & SOURCE 0
        LDX   R 0868 & DEST 0
        STX   X 000                   Store data
        INX
        INX
        STX   R 0868 & DEST 0
        LDD   R 0884 DATA 04          Current data length
        SUBD  # 00001
        JMP   DFE1                    Not all data copied
*----------------------
DFE2    CLC                           Data transfer OK
        RTS
```

Example Starting at address $3A00, 50 bytes are read from block 4. The data is stored from R 2000 onward.

```
        LDAA  # 004                   Block number 4
        STAA  R 0881 DATA 00
        LDD   # $0200                 Offset to $3800 (Source adr. = $3A00
        STD   R 0882 DATA 01
        LDX#  R 2000 Dest.addr.
        LDD   # 00050                 Data length
        JSR   DFEE                    Read data from additional EEPROM
        BCC   OK
        :                             ERROR Check
        :
```


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33.2 WRITING DATA

When writing data to an EEPROM, remember that there is a slight delay in comparison to writi
flag or register.

To write data to a block, the STL macro DTEE is used

The STL macro DTEE is used for programming parameter data which does not change while a
is in operation.

NOTE: If the application program is running in the EEPROM, the additional EEPROM
be programmed.

If data is programmed in the EEPROM, the rest of the program is not processed!
For writing to the EEPROM during a program cycle, the function block MCEE
used. This is stored on the "Utility.01" diskette of standard software package 1
(SWPLCSTD01-0 Rev. 00.30 or higher).

Send parameters:

Source	...	Index register
Destination	...	Block number in R 0881
		Offset to address $3800 in R 0882&
Data length	...	In accumulator D

Return parameters:

No error:

Carry = 0	...	Data transfer OK
R 0881	...	Block number of the next free byte
R 0882&	...	Offset to $3800 of the next free byte

Error:

Carry = 1	...	Data transfer faulty
Accu. A	...	Error number:
		1 - Data length greater than free memo
		2 - EEPROM defect
R 0881	...	Block number of the defect memory location
R 0882&	...	Offset to $3800 of the defect memory location

Used registers:

R 0880	...	Run-time counter
R 0884&	...	Current data length
R 0886&	...	Source pointer

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```
DTEE  STD   R 0884 DATA 04          Current data length
      STX   R 0866 & SOURCE 0
      LDD   R 0882 DATA 02          Offset
      ANDA  # %00000111             Limit to 2 Kbytes / Block
      ADDD  # $3800                 Start address of EEPROM block
      STD   R 0882 DATA 02
      ADDD  R 0884 DATA 04
      SUBD  # $3FFF
      BLS   DTE5
*-----------------------
      LDAA  # 001                   ERROR ... Data length greater than
      SEC                                     free memory
      RTS
*-----------------------
DTE5  LDAA  R 0998 CYCLE TIME COUNTER
      STAA  R 0886 DATA 06
DTE3  LDAA  R 0886 DATA 06
      STAA  R 0998 CYCLE TIME COUNTER
*
      LDD   # $3400                 Inport/Outport Address
      DXR
      LDAA  R 0881 DATA 01
      ANDA  # %00001111             Limit block number to 0 ... F
      STAA  R 0881 DATA 01
      LDAA  X 000
      ANDA  # %11110000
      ORAA  R 0881 DATA 01
      STAA  X 000                   Block selection
*
      LDX   R 0866 & SOURCE 0
      LDAA  X 000                   Read data
      LDX   R 0882 DATA 02
      STAA  X 000                   Store current copy data
*---
      PSHA
      LDD   # 01500
DTE0  SUBD  # 00001                 Wait state
      BNE   DTE0
      CBA
*---
      CLR   R 0880 DATA 00          Reset run-time counter
DTE1  LDAB  X 000                   Compare EEPROM data with current
      CBA                           copy data
      BEQ   DTE2
      INC   R 0880 DATA 00          Increase run-time counter
      LDAB  R 0880 DATA 00
      CMPB  # 200                   Compare with run-time MAX
      BCS   DTE1
*-----------------------
      LDAA  # 002
      SEC                           ERROR ... EEPROM defect
      RTS
*-----------------------
```


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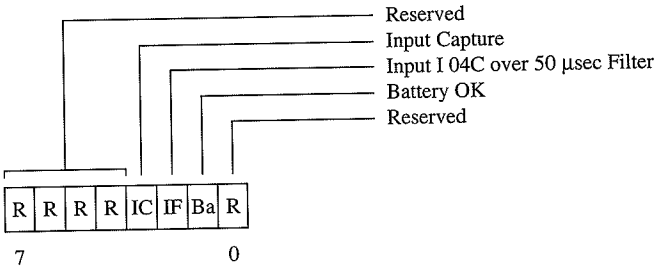
```
DTE2  LDD   R 0882 DATA 02          Increase MEM address pointer
      ADDD  # 00001
      STD   R 0882 DATA 02
      LDX   R 0866 & SOURCE 0
      INX
      STX   R 0866 & SOURCE 0
      LDD   R 0884 DATA 04          Current data length
      SUBD  # 00001                 All data copied ?
      STD   R 0884 DATA 04
      BEQ   DTE4
      JMP   DTE3
DTE4  CLC                           Data transfer OK
      RET
```

Example Starting at address $3B00, 40 bytes are written to block 7. The data to be written stored in the memory starting from R 2500.

```
LDAA  # 007                       Block number 7
STAA  R 0881 DATA 00
LDD   # $0300                     Offset to $3800 (dest. = $3B00)
STD   R 0882 DATA 01
LDX#  R 2500 Source address
LDD   # 00040                     Data length
JSR   DTEE                        Write data to additional EEPROM
BCC   OK
:                                 ERROR evaluation
:
```


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34. INPORT ADDRESS $3480



Reserved	Reserved for later use.
Input Capture	The interrupt source for the Input Capture Input is determined with the mode register $2121 (see section "14.6.3 Mode Register $2121"). This bit indicates the status of input I 04D or the zero signal of hardware counter 0.
Input I 04C	Input I 04C is read through a 50 µsec filter (fast input).
Battery OK	This bit is used for monitoring the lithium battery. The state of the battery is checked using hardware monitoring. 0 ... Battery dead (Voltage < 2.45 V) 1 ... Battery OK (Voltage > 2.55 V)
Reserved	Reserved for later use.

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35. WATCHDOG

35.1 SOFTWARE WATCHDOG

The software watchdog monitors the maximum permitted program cycle time of 100 msec. If a program cycle has not ended when this time elapses, the application program is stopped and a s reset is executed (all outputs are reset).
A run-time error is indicated in the debugger of the programming device and through the status

35.2 HARDWARE WATCHDOG

The CPU of the Compact PLC has a hardware watchdog, which can bring the system to a secure of operation even if the CPU fails completely.

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36. TIMER INTERRUPT ROUTINES

Independent of the length of an application program, an interrupt is triggered every 10 msec and the timer interrupt routine is called. This operating system function is used for security and diagnostic functions as well as the generation of software timers, clock functions, time cycles and time pulses.

The timer interrupt vector (the address of the timer interrupt routine) sits at R 0972&. The timer interrupt time is stored in R 0974& (units µsec.). Neither the timer interrupt vector nor the timer interrupt time may be changed by the application program.

In addition to the operating system functions, the user can have one or two program segments executed on a time basis (user timer interrupt routines). The timer interrupt handlers $US1 and $US2 are used for this purpose with parameters:

AA	Desired time interval in msec.
R	Start address of user timer interrupt routine

Call `JSR $US1` or `JSR $US2`

The user timer interrupt routine is terminated with RTS. Independent of the time interval chosen for the user timer interrupt routine, the operating system timer interrupt routine is executed every 10 msec.

NOTE: Timer interrupt routines are not executed if the PLC is in HALT state.

Calling lengthy timer interrupt routines too often can extend the program scan time and cause disturbance in the system. The sum of the execution times of the two user timer interrupt routines must not exceed 300 µsec.

Operating system math routines must not be used in timer interrupt routines.

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To switch off an active timer interrupt routine, load the AA with 0 and call the interrupt handler or $US2) again.

Example Every 3 msec a descending counter is to be read and compared to 10 000. If the falls below this value, a flag is to be set. The timer interrupt handler $US1 is onl once in the initialization:

```
INIT  LDAA  T D64       First Scan
      BEQ   INIR
      LDAA  # 003       3 msec
      LDXL  TEST        Address of the interrupt routine
      JSR   $US1
INIR  RTS

TEST  JSR   READ        Read counter state
      SUBD  # 10000     Compare with 10,000
      BCC   TESR
      SET   O 040       Counter low !
TESR  RTS
```


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37. ERROR MESSAGES

The CPU is equipped with extensive security and diagnostic functions (e.g. Program checksum tests at Power-on). In the event of an error the application program is stopped, the status LED is switched on and a software reset is executed. All digital outputs are reset, all analog outputs are set to 0 V or 0 mA. If a programming system is connected, an appropriate error message is displayed in the debugger (e.g. RUNTIME ERROR).

The following table provides a summary of all possible errors on the Compact PLC:

Message	Description/Cause	Solution
Transmission error during download	An error occurred while downloading a program from the programming device to the PLC. **Possible causes:** The Online link between the programming device and the PLC is affected by electromagnetic disturbance.	Perform the download again.
Checksum error after RUN	An application program downloaded with RUN is indicated as having the wrong checksum in the RAM of the PLC. **Cause:** Program memory defect.	Download the program again; if the error occurs repeatedly, replace the EE32 module.
Checksum error	The checksum of the application program is incorrect after a power-on or reset. **Possible causes:** For PROM programs the PROM memory is defective, for RAM programs either the battery is low or dead or there is a software problem which overwrites the application program.	Download the application program again. If the error occurs repeatedly, check the battery, examine the application program for errors, or replace the application program memory module.
Runtime error	The permissible program cycle time of 100 msec was exceeded. **Possible causes:** Software error, too many program loops, an endless loop.	Check program again and correct errors.
Pointer error	During the checksum test at power-on, it was determined that the operating system vectors are incorrect. **Possible causes:** see "Checksum error".	See "Checksum error".

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Message	Description/Cause	Solution
Communication error	An error occurred during communication between the programming device and the PLC (RUN, debug). **Possible causes:** The Online link between the programming device and the PLC is affected by electromagnetic disturbance.	Perform the download again.
Stack pointer error	At the end of a program scan (END) the stack pointer is incorrect. **Possible causes:** Error in the application program (subroutine not terminated with RTS, error in use of system stack for data storage).	Correct program error.
Trap error	Unknown processor instruction. **Possible causes:** Error in the application program (e.g., indexed jump to data region)	Correct program error.

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