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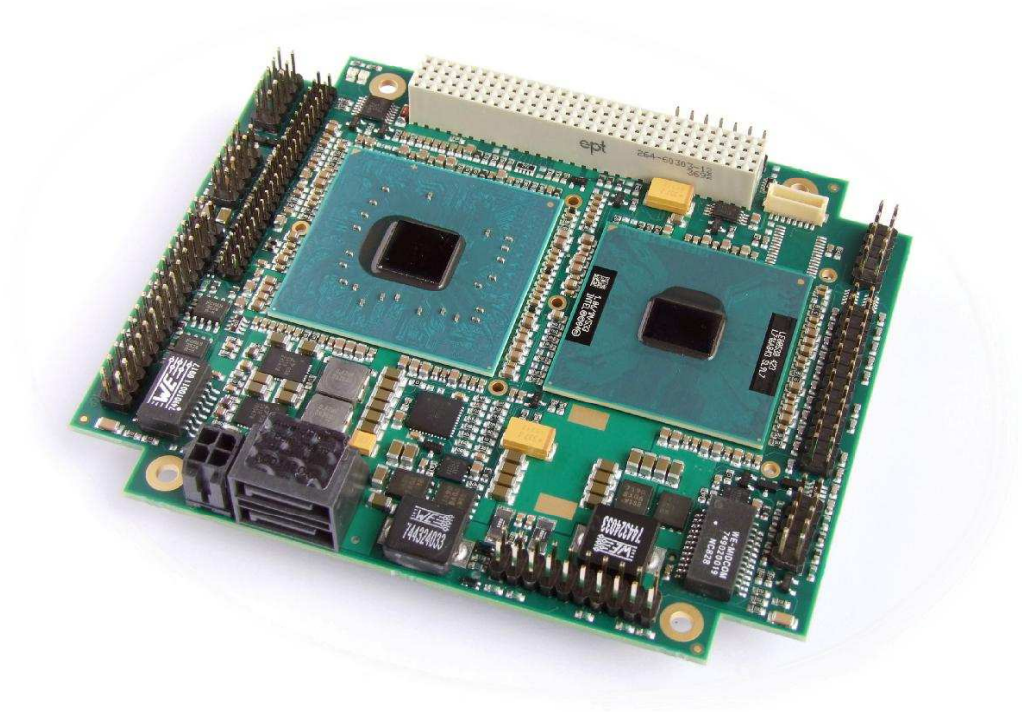
Find the *Beckhoff CB4051-0008* at our website: *Click HERE*

BECKHOFF

CB4051

Manual

rev 1.4



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0 History

Version	Changes
0.1	first preliminary release
0.2	adopted new name for form factor: "PCI-104" from www.pc104.org, updated block diagram
0.3	numbering of USB and SATA starts at 1 in block diagram and pinout tables
0.4	updated annex (PCI and SMB devices), minor changes
1.0	- added connector map - updated block diagram - updated temperature ranges - several small changes
1.1	updated contact details, minor changes
1.2	new photographs (board rev. G4), minor changes
1.3	minor changes
1.4	updated block diagram: BIOS connected via SPI, added note concerning PS_ON, minor changes



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1 Introduction

1.1 Notes on the Documentation

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards. It is essential that the following notes and explanations are followed when installing and commissioning these components.

1.1.1 Liability Conditions

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.
The documentation has been prepared with care. The products described are, however, constantly under development. For that reason the documentation is not in every case checked for consistency with performance data, standards or other characteristics. None of the statements of this manual represents a guarantee (Garantie) in the meaning of § 443 BGB of the German Civil Code or a statement about the contractually expected fitness for a particular purpose in the meaning of § 434 par. 1 sentence 1 BGB. In the event that it contains technical or editorial errors, we retain the right to make alterations at any time and without warning. No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

1.1.2 Copyright

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1.2 Safety Instructions

Please consider the following safety instructions and descriptions. Product specific safety instructions are to be found on the following pages or in the areas mounting, wiring, commissioning etc.

1.2.1 Disclaimer

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH.

1.2.2 Description of Safety Symbols

The following safety symbols are used in this documentation. They are intended to alert the reader to the associated safety instructions.



ACUTE RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is immediate danger to life and health of individuals!



RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is danger to life and health of individuals!



HAZARD TO INDIVIDUALS, ENVIRONMENT, DEVICES, OR DATA!

If you do not adhere to the safety advise next to this symbol, there is obvious hazard to individuals, to environment, to materials, or to data.



NOTE OR POINTER

This symbol indicates information that contributes to better understanding.

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1.3 Essential Safety Measures

1.3.1 Operator's Obligation to Exercise Diligence

The operator must ensure that

- the product is only used for its intended purpose
- the product is only operated in sound condition and in working order
- the instruction manual is in good condition and complete, and always available for reference at the location where the products are used
- the product is only used by suitably qualified and authorised personnel
- the personnel is instructed regularly about relevant occupational safety and environmental protection aspects
- the operating personnel is familiar with the operating manual and in particular the safety notes contained herein

1.3.2 National Regulations Depending on the Machine Type

Depending on the type of machine and plant in which the product is used, national regulations governing the controllers of such machines will apply, and must be observed by the operator. These regulations cover, amongst other things, the intervals between inspections of the controller. The operator must initiate such inspections in good time.

1.3.3 Operator Requirements

- Read the operating instructions

All users of the product must have read the operating instructions for the system they work with.

- System know-how

All users must be familiar with all accessible functions of the product.

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1.4 Functional Range

NOTE

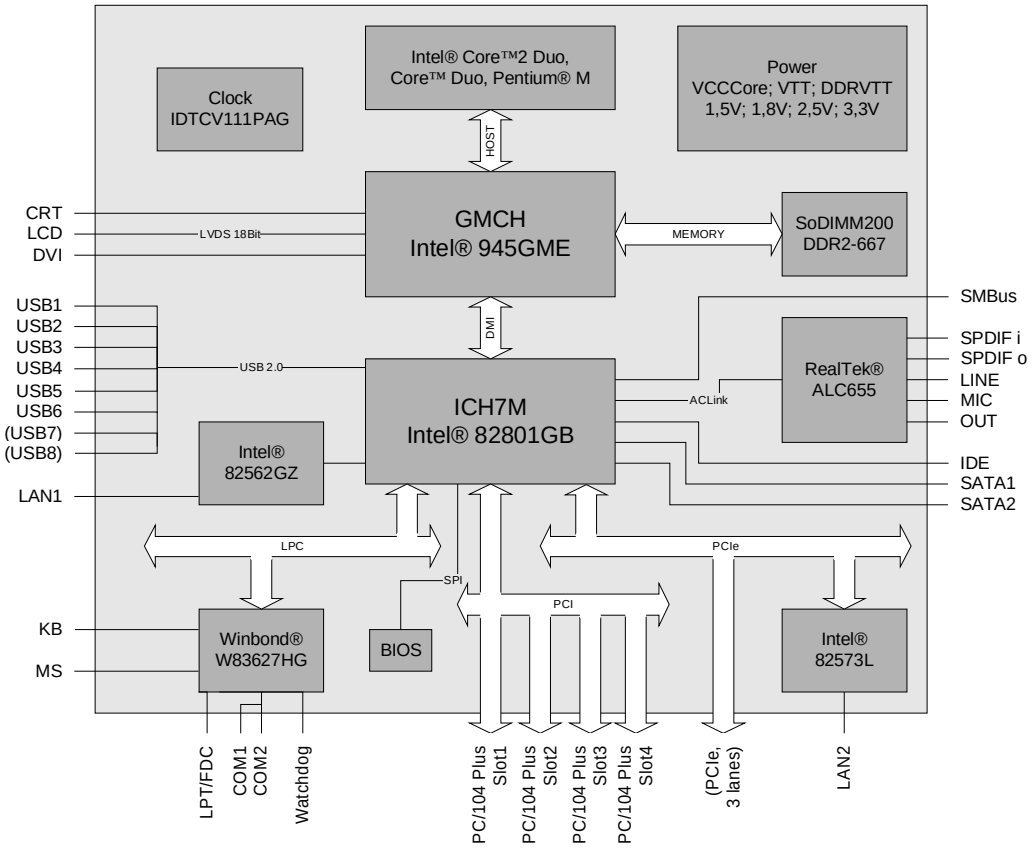
The descriptions contained in the present documentation represent a detailed and extensive product description. As far as the described motherboard was acquired as an integral component of an Industrial PC from Beckhoff Automation GmbH, this product description shall be applied only in limited scope. Only the contractually agreed specifications of the corresponding Industrial PC from Beckhoff Automation GmbH shall be relevant. Due to several models of Industrial PCs, variations in the component placement of the motherboards are possible. Support and service benefits for the built-in motherboard will be rendered by Beckhoff Automation GmbH exclusively as specified in the product description (inclusive operation system) of the particular Industrial PC.

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2 Overview

2.1 Features

The CB4051 is a highly complex PCI-104-board with the functionalities of a motherboard. Equipped with an Intel® Celeron® M, an Intel® Core™ Duo, or an Intel® Core™2 Duo processor, it can accommodate up to 2 GByte RAM (DDR2-667) via SO-DIMM200. It also provides a PCI bus (via PC/104-Plus) and additional peripheral devices such as two serial interfaces, Gigabit-LAN, one IDE and two SATA interfaces, audio in and out, eight USB channels and CRT and TFT support. As an option a PCIe connector can be provided.



- o Processor Intel® Celeron® M, Intel® Core™ Duo, Intel® Core™2 Duo
- o Chipset Intel® 945GM(E) and Intel® ICH7
- o SO-DIMM200 socket for one DDR2-667 module of up to 2 GByte
- o Two serial interfaces COM1 and COM2
- o LAN-interface Ethernet 10/100 (Base-T)
- o LAN-interface Ethernet 10/100/1000 (Base-T)
- o IDE-interface
- o Two SATA-interfaces
- o PS2 keyboard / mouse interface
- o LPT interface
- o Eight USB 2.0 interfaces
- o AWARD® BIOS 6.10

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- CRT connection
- TFT connection, LVDS 18Bit
- AC97 compatible sound controller with SPDIF in and out
- RTC with external CMOS battery
- 5V single supply voltage
- PCI bus via PC/104-Plus
- PCIe connector (option), 3 lanes
- Size: 96 mm x 90 (115,5) mm

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2.2 Specifications and Documents

In making this manual and for further reading of technical documentation the following documents, specifications and web-pages were used and are recommended.

- PC/104™ specification
  Version 2.5
  www.pc104.org
- PC/104-Plus™ specification
  Version 2.0
  www.pc104.org
- PCI-104™ specification
  Version 1.0
  www.pc104.org
- PCI specification
  Version 2.3 resp. 3.0
  www.pcisig.com
- PCI-Express specification
  Version 1.1
  www.pcisig.com
- ACPI specification
  Version 3.0
  www.acpi.info
- ATA/ATAPI specification
  Version 7 Rev. 1
  www.t13.org
- USB specifications
  www.usb.org
- SM-Bus specification
  Version 2.0
  www.smbus.org
- Intel® chip set description
  Mobile Intel 945 Express Chipset Family Datasheet
  www.intel.com
- Intel® chip descriptions
  Celeron® M, Core™ Duo/Solo, Core2™ Duo
  www.intel.com
- Winbond® chip description
  W83627HG Datasheet
  www.winbond-usa.com or www.winbond.com.tw
- Intel® chip description
  82562GZ Datasheet
  www.intel.com
- Intel® chip description
  82573E Datasheet
  www.intel.com
- IDT® chip description
  IDTCV111i Datasheet
  www.idt.com

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3 Detailed Description

3.1 Power Supply

The power supply of the hardware module is effected via the power connector. The board only requires an operating voltage of 5 volt ± 5%.

3.2 CPU

The board can be ordered with one of the following processors employed:Intel® Celeron® M, Intel® Core™ Duo, and Intel® Core™ 2 Duo. The package type allows a maximum die temperature of 100 degrees Celsius and accords highest possible security even in rough environment.
The processor includes a second level cache of up to 4 MByte, depending on which model is used. Furthermore the processors offer many features known from the desktop range such as MMX2, serial number, loadable microcode etc.

3.3 Memory

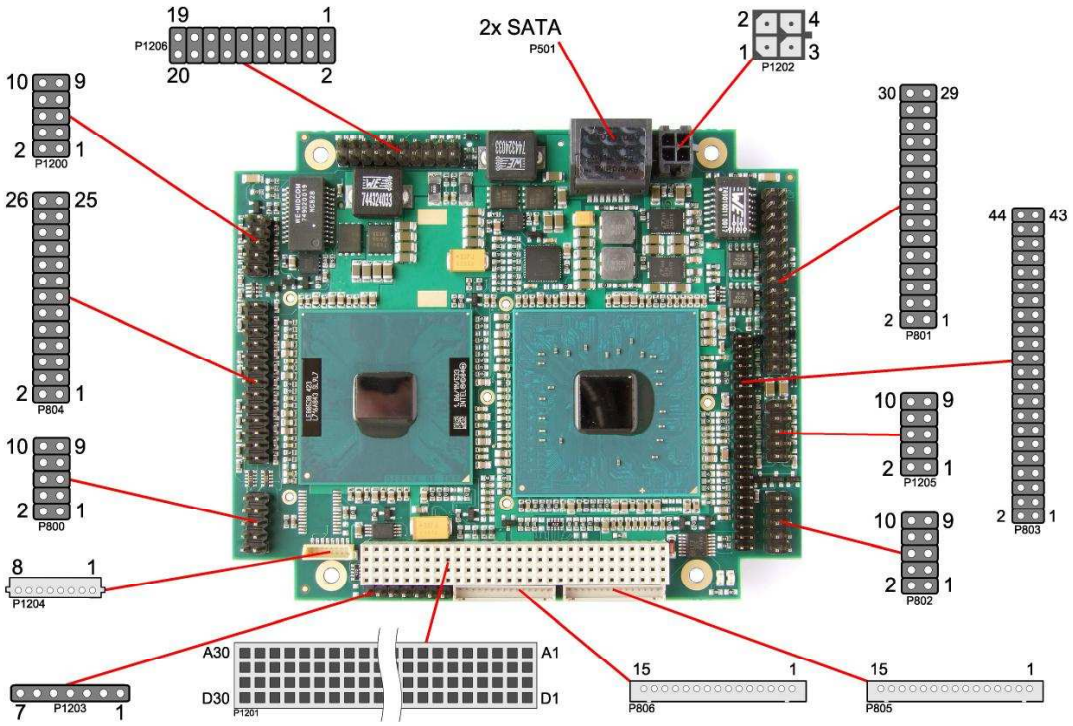
There is one conventional SO-DIMM200 socket available to equip the board with memory. For mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your sales representative for recommended memory modules.
With currently available SO-DIMM200 modules a memory extension up to 2 GByte is possible (DDR2-667).

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4 Connectors

4.1 Connector Map

Please use the connector map below for quick reference. Only connectors on the component side are shown. For more information on each connector refer to the table below.



Ref-No.	Function	Page
P501	"SATA Interfaces"	p. 28
P502*	"PCIe" (option)	n/a
U600*	"Memory"	p. 17
P800	"Serial Interface COM1"	p. 31
P801	"USB 1 to 4, LAN, Sound"	p. 25
P802	"Serial Interface COM2"	p. 32
P803	"IDE Interface"	p. 29
P804	"Parallel Interface LPT"	p. 30
P805/6	"LCD"	p. 23
P1200	"System"	p. 16
P1201	"PC/104-Plus Bus"	p. 20
P1202	"Power Supply"	p. 15
P1203	"SMBus"	p. 33
P1204	"Monitoring Functions"	p. 34
P1205	"VGA"	p. 22
P1206	"USB 5 and 6, LAN2"	p. 27

* not in the picture above (cf. bottom side of board)

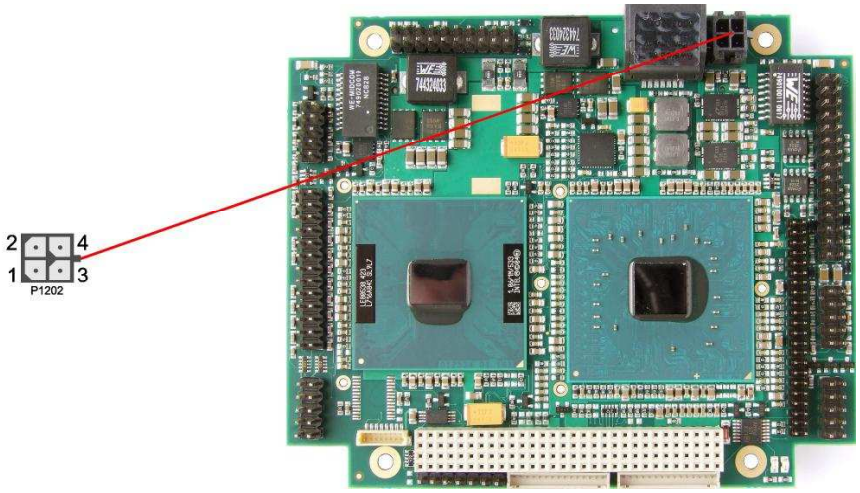
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4.2 Power Supply

The power supply is effected via a 2x2pin connector (Molex PS 43045-04xx, mating connector: Molex PS 43025-04xx).
The board only requires an operating voltage of 5 volt ± 5%. 3.3V output to the PC/104-Plus bus is the only off-board supply available.
Should additional voltages be needed for PC/104-Plus expansion cards, these must be provided externally by connecting the respective pins on the PC/104-Plus connector (see below).
For maximum current availability, it is recommended to use both this power connector and the PC/104-Plus connector for power supply.

CAUTION

The CB4051 includes circuitry that will notify an intelligent power supply to shut down if the processor reaches a critical temperature. This is achieved by deasserting the (low-active) PS_ON# signal found on the SM-Bus connector. When PS_ON# is pulled high, it can signal an intelligent power supply to shut down if PS_ON# is connected to the power supply's PS_ON input. If PS_ON# is not otherwise connected, the CB4051 can be damaged beyond repair if a thermal shutdown event occurs. In rare instances, if power is not shut down, the board will continue to heat up until failure occurs.



Description	Name	Pin		Name	Description
5 volt supply	VCC	1	2	VCC	5 volt supply
ground	GND	3	4	GND	ground

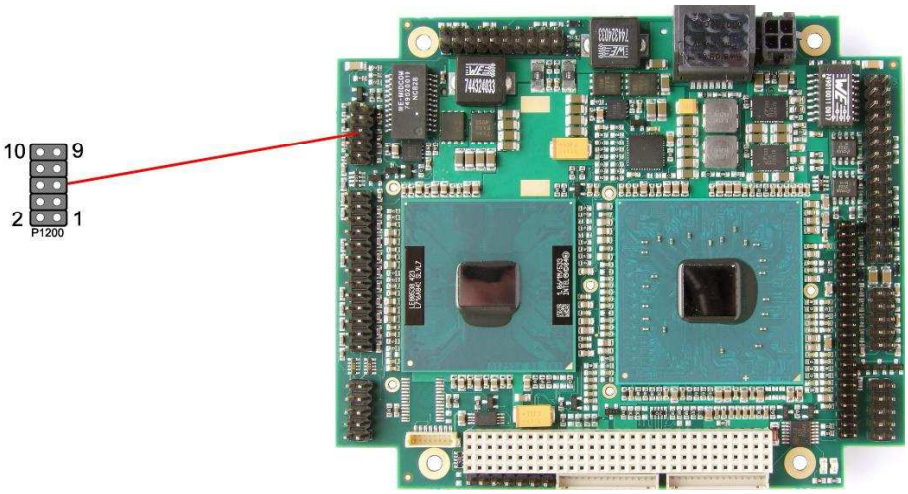
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4.3 System

The system connector, which has the main functions that are necessary to start the board, is provided via a standard IDC socket connector with a spacing of 2.54 mm.
This connector supports the following interfaces: PS/2 keyboard, PS/2 mouse, speaker, external RTC-battery and reset of the board.

NOTE

For "Real Time Clock" an external battery (3.3V) must be connected. Connect "+" to VBAT and "-" to GND.

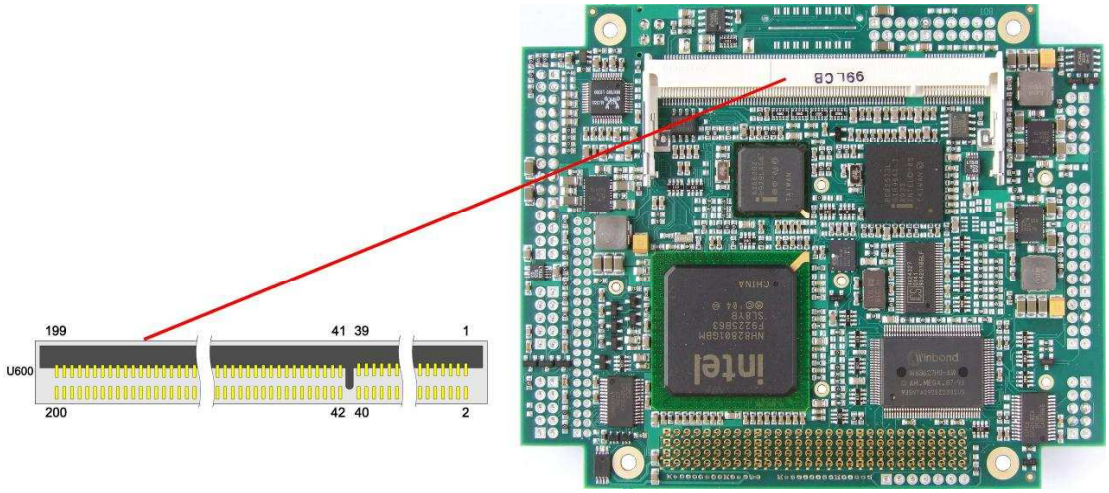


Description	Name	Pin		Name	Description
speaker to 5 volt	SPEAKER	1	2	GND	ground
reset to ground	RESET#	3	4	KLOCK#	keyboard lock
keyboard Data	KDAT	5	6	KCLK	keyboard clock
mouse data	MDAT	7	8	MCLK	mouse clock
CMOS battery ≥ 3 volt	VBAT	9	10	VCC	5 volt supply

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4.4 Memory

There is one conventional SO-DIMM200 socket available to equip the board with memory (DDR2-667). It is located on the bottom side of the board. For mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your sales representative for recommended memory modules. With currently available SO-DIMM modules a memory extension up to 2 GByte is possible. The timing parameters for different memory modules are automatically set by BIOS.



Description	Name	Pin		Name	Description
memory reference current	REF	1	2	GND	ground
ground	GND	3	4	DQ4	data 4
data 0	DQ0	5	6	DQ5	data 5
data 1	DQ1	7	8	GND	ground
ground	GND	9	10	DQM0	data mask 0
data strobe 0 -	DQS0#	11	12	GND	ground
data strobe 0 +	DQS0	13	14	DQ6	data 6
ground	GND	15	16	DQ7	data 7
data 2	DQ2	17	18	GND	ground
data 3	DQ3	19	20	DQ12	data 12
ground	GND	21	22	DQ13	data 13
data 8	DQ8	23	24	GND	ground
data 9	DQ9	25	26	DQM1	data mask 1
ground	GND	27	28	GND	ground
data strobe 1 -	DQS1#	29	30	CK0	clock 0 +
data strobe 1 +	DQS1	31	32	CK0#	clock 0 -
ground	GND	33	34	GND	ground
data 10	DQ10	35	36	DQ14	data 14
data 11	DQ11	37	38	DQ15	data 15
ground	GND	39	40	GND	ground
ground	GND	41	42	GND	ground
data 16	DQ16	43	44	DQ20	data 20
data 17	DQ17	45	46	DQ21	data 21
ground	GND	47	48	GND	ground
data strobe 2 -	DQS2#	49	50	N/C	reserved
data strobe 2 +	DQS2	51	52	DQM2	data mask 2

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Description	Name	Pin		Name	Description
ground	GND	53	54	GND	ground
data 18	DQ18	55	56	DQ22	data 22
data 19	DQ19	57	58	DQ23	data 23
ground	GND	59	60	GND	ground
data 24	DQ24	61	62	DQ28	data 28
data 25	DQ25	63	64	DQ29	data 29
ground	GND	65	66	GND	ground
data mask 3	DQM3	67	68	DQS3#	data strobe 3 -
reserved	N/C	69	70	DQS3	data strobe 3 +
ground	GND	71	72	GND	ground
data 26	DQ26	73	74	DQ30	data 30
data 27	DQ27	75	76	DQ31	data 31
ground	GND	77	78	GND	ground
clock enables 0	CKE0	79	80	CKE1	clock enables 1
1.8 volt supply	1.8V	81	82	1.8V	1.8 volt supply
reserved	N/C	83	84	N/C	reserved
SDRAM bank 2	BA2	85	86	N/C	reserved
1.8 volt supply	1.8V	87	88	1.8V	1.8 volt supply
address 12	A12	89	90	A11	address 11
address 9	A9	91	92	A7	address 7
address 8	A8	93	94	A6	address 6
1.8 volt supply	1.8V	95	96	1.8V	1.8 volt supply
address 5	A5	97	98	A4	address 4
address 3	A3	99	100	A12	address 2
address 1	A1	101	102	A0	address 0
1.8 volt supply	1.8V	103	104	1.8V	1.8 volt supply
address 10	A10	105	106	BA1	SDRAM bank 1
SDRAM bank 0	BA0	107	108	RAS#	row address strobe
write enable	WE#	109	110	S0#	chip select 0
1.8 volt supply	1.8V	111	112	1.8V	1.8 volt supply
column address strobe	CAS#	113	114	ODT0	on die termination 0
chip select 1	S1#	115	116	A13	address 13
1.8 volt supply	1.8V	117	118	1.8V	1.8 volt supply
on die termination 1	ODT1	119	120	N/C	reserved
ground	GND	121	122	GND	ground
data 32	DQ32	123	124	DQ36	data 36
data 33	DQ33	125	126	DQ37	data 37
ground	GND	127	128	GND	ground
data strobe 4 -	DQS4#	129	130	DQM4	data mask 4
data strobe 4 +	DQS4	131	132	GND	ground
ground	GND	133	134	DQ38	data 38
data 34	DQ34	135	136	DQ39	data 39
data 35	DQ35	137	138	GND	ground
ground	GND	139	140	DQ44	data 44
data 40	DQ40	141	142	DQ45	data 45
data 41	DQ41	143	144	GND	ground
ground	GND	145	146	DQS5#	data strobe 5 -
data mask 5	DQM5	147	148	DQS5	data strobe 5 +
ground	GND	149	150	GND	ground
data 42	DQ42	151	152	DQ46	data 46
data 43	DQ43	153	154	DQ47	data 47
ground	GND	155	156	GND	ground
data 48	DQ48	157	158	DQ52	data 52
data 49	DQ49	159	160	DQ53	data 53
ground	GND	161	162	GND	ground

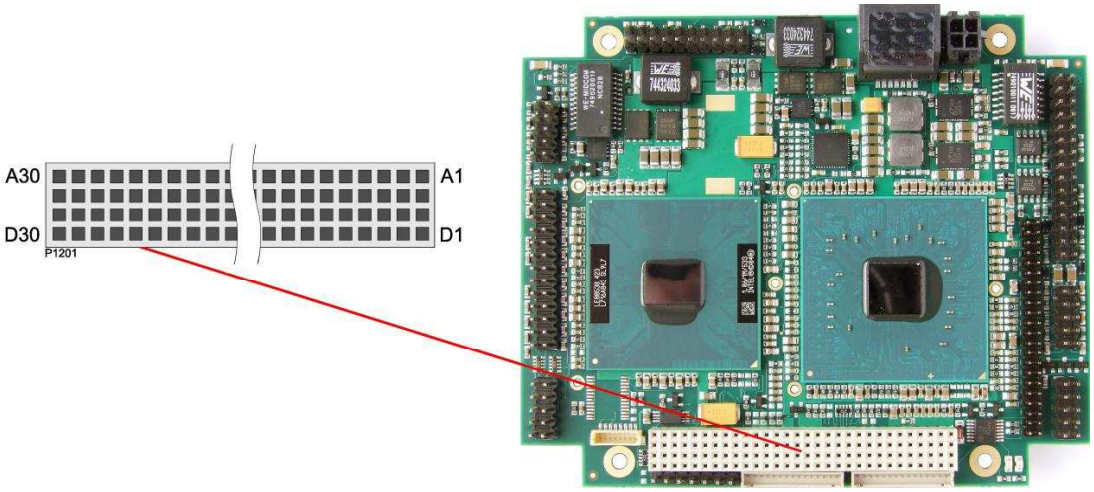
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Description	Name	Pin		Name	Description
test	TEST	163	164	CK1	clock 1 +
ground	GND	165	166	CK1#	clock 1 -
data strobe 6 -	DQS6#	167	168	GND	ground
data strobe 6	DQS6	169	170	DQM6	data mask 6
ground	GND	171	172	GND	ground
data 50	DQ50	173	174	DQ54	data 54
data 51	DQ51	175	176	DQ55	data 55
ground	GND	177	178	GND	ground
data 56	DQ56	179	180	DQ60	data 60
data 57	DQ57	181	182	DQ61	data 61
ground	GND	183	184	GND	ground
data mask 7	DQM7	185	186	DQS7#	data strobe 7 -
ground	GND	187	188	DQS7	data strobe 7 +
data 58	DQ58	189	190	GND	ground
data 59	DQ59	191	192	DQ62	data 62
ground	GND	193	194	DQ63	data 63
SMBus data	SDA	195	196	GND	ground
SMBus clock	SCL	197	198	SA0	SPD address
3.3 volt supply	3.3V	199	200	SA1	SPD address

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4.5 PC/104-Plus Bus

Expansion cards can be connected to the board using the PCI connector first introduced with the PC/104-Plus standard. A maximum of four PC/104-Plus cards are supported.
The interrupt routing and the IDSEL signals for the expansion cards are specified in the PC/104-Plus specification (see "Specifications and Documents", p. 12).



Description	Name	Pin		Name	Description
ground	GND	A1	B1	N/C	reserved
5 volt - IO buffer power	VCCIO	A2	B2	AD2	PCI – address/data 2
PCI – address/data 5	AD5	A3	B3	GND	ground
PCI – com/byte enable 0	CBE0#	A4	B4	AD7	PCI – address/data 7
ground	GND	A5	B5	AD9	PCI – address/data 9
PCI – address/data 11	AD11	A6	B6	VCCIO	5 volt - IO buffer power
PCI – address/data 14	AD14	A7	B7	AD13	PCI – address/data 13
3.3 volt supply	3.3V	A8	B8	CBE1#	PCI – com/byte enable 1
PCI – system error	SERR#	A9	B9	GND	ground
ground	GND	A10	B10	PERR#	PCI – parity error
PCI – stop	stop#	A11	B11	3.3V	3.3 volt supply
3.3 volt supply	3.3V	A12	B12	TRDY#	PCI – target ready
PCI – frame	FRAME#	A13	B13	GND	ground
ground	GND	A14	B14	AD16	PCI – address/data 16
PCI – address/data 18	AD18	A15	B15	3.3V	3.3 volt supply
PCI – address/data 21	AD21	A16	B16	AD20	PCI – address/data 20
3.3 volt supply	3.3V	A17	B17	AD23	PCI – address/data 23
PCI – ID select slot 1	IDSEL0	A18	B18	GND	ground
PCI – address/data 24	AD24	A19	B19	CBE3#	PCI – com/byte enable 3
ground	GND	A20	B20	AD26	PCI – address/data 26
PCI – address/data 29	AD29	A21	B21	VCC	5 volt supply
5 volt supply	VCC	A22	B22	AD30	PCI – address/data 30
PCI – bus request slot 1	REQ0#	A23	B23	GND	ground
ground	GND	A24	B24	REQ2#	PCI – bus request slot 3
PCI – bus grant slot 4	GNT1#	A25	B25	VCCIO	5 volt - IO buffer power
5 volt supply	VCC	A26	B26	CLK0	PCI – clock slot 1
PCI – clock slot 3	CLK2	A27	B27	VCC	5 volt supply

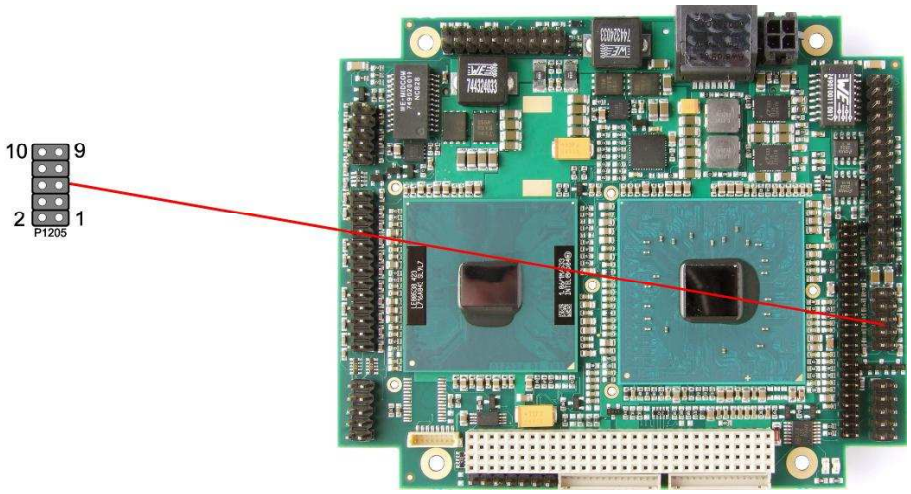
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Description	Name	Pin		Name	Description
ground	GND	A28	B28	INTD#	PCI – interrupt D
12V supply	12V	A29	B29	INTA#	PCI – interrupt A
-12V supply	-12V	A30	B30	REQ3#	PCI – bus request slot 4
5 volt supply	VCC	C1	D1	AD0	PCI – address/data 0
PCI – address/data 1	AD1	C2	D2	VCC	5 volt supply
PCI – address/data 4	AD4	C3	D3	AD3	PCI – address/data 3
ground	GND	C4	D4	AD6	PCI – address/data 6
PCI – address/data 8	AD8	C5	D5	GND	ground
PCI – address/data 10	AD10	C6	D6	M66EN	PCI – 66MHz enable
ground	GND	C7	D7	AD12	PCI – address/data 12
PCI – address/data 15	AD15	C8	D8	3.3V	3.3 volt supply
reserved	N/C	C9	D9	PAR	PCI – parity bit
3.3 volt supply	3.3V	C10	D10	N/C	reserved
PCI – lock	LOCK#	C11	D11	GND	ground
ground	GND	C12	D12	DEVSEL#	PCI – device select
PCI – initiator ready	IRDY#	C13	D13	3.3V	3.3 volt supply
3.3 volt supply	3.3V	C14	D14	CBE2#	PCI – com/byte enable 2
PCI – address/data 17	AD17	C15	D15	GND	ground
ground	GND	C16	D16	AD19	PCI – address/data 19
PCI – address/data 22	AD22	C17	D17	3.3V	3.3 volt supply
PCI – ID select slot 2	IDSEL1	C18	D18	IDSEL2	PCI – ID select slot 3
5 volt - IO buffer power	VCCIO	C19	D19	IDSEL3	PCI – ID select slot 4
PCI – address/data 25	AD25	C20	D20	GND	ground
PCI – address/data 28	AD28	C21	D21	AD27	PCI – address/data 27
ground	GND	C22	D22	AD31	PCI – address/data 31
PCI – bus request slot 2	REQ1#	C23	D23	VCCIO	5 volt - IO buffer power
5 volt supply	VCC	C24	D24	GNT0#	PCI – bus grant slot 1
PCI – bus grant slot 3	GNT2#	C25	D25	GND	ground
ground	GND	C26	D26	CLK1	PCI – clock slot 2
PCI – clock slot 4	CLK3	C27	D27	GND	ground
5 volt supply	VCC	C28	D28	RST#	PCI – reset
PCI – interrupt B	INTB#	C29	D29	INTC#	PCI – interrupt C
PCI – bus grant slot 4	GNT3#	C30	D30	GND	ground

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4.6 VGA

The CRT-VGA signals are provided by a standard IDC socket connector with a spacing of 2.54 mm. This interface allows the connection of a standard VGA-monitor. I2C communication is supported.

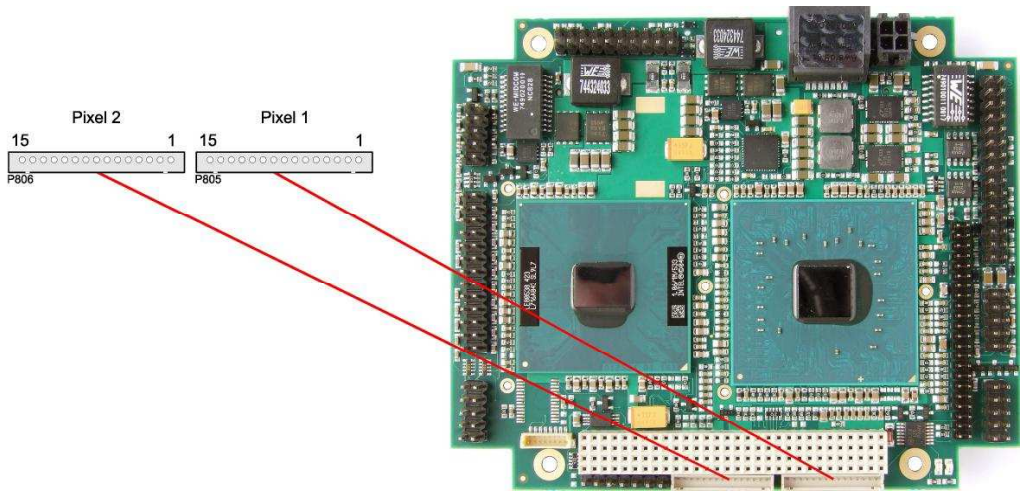


Description	Name	Pin		Name	Description
analog red	RED	1	2	GND	ground
analog green	GREEN	3	4	DDDA	DD data
analog blue	BLUE	5	6	DDCK	DD clock
vertikal sync	VSYNC	7	8	GND	ground
horizontal sync	HSYNC	9	10	GND	ground

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4.7 LCD

The LCD is connected via two 15 pin connectors (Hirose DF13-15P-DAS, mating connector: DF13-15S-xxx). The power supply for the display is also provided through these connectors. The CB4051 board only supports displays with LVDS interface. For displays with digital interface an extra receiver board is available. There is no support for DSTN displays.
With the LVDS interface it is possible to trigger LVDS displays with a maximum of 18 Bit colour depth and one or two pixels per clock. For single pixel displays only one connector is necessary. However, if you want to read the display's EDID data the second connector must be connected.
The display type can be chosen over the BIOS setup. Please contact your sales representative regarding an appropriate cable to connect your display.



The following table shows the pin description for the first bit ("even" pixel).

Pin	Name	Description
1	GND	ground
2	GND	ground
3	TXO00#	LVDS even data 0 -
4	TXO00	LVDS even data 0 +
5	TXO01#	LVDS even data 1 -
6	TXO01	LVDS even data 1 +
7	TXO02#	LVDS even data 2 -
8	TXO02	LVDS even data 2 +
9	TXO0C#	LVDS even clock -
10	TXO0C	LVDS even clock +
11	TXO03#	LVDS even data 3 -
12	TXO03	LVDS even data 3 +
13	BL_VCC	switched 5 volt for backlight
14	FP_3.3V	switched 3.3 volt for display
15	FP_3.3V	switched 3.3 volt for display

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The following table shows the pin description for the second bit ("odd" pixel). This connector will only be used if a display with two pixels per clockcycle is to be connected.

Pin	Name	Description
1	GND	ground
2	GND	ground
3	TXO10#	LVDS odd data 0 -
4	TXO10	LVDS odd data 0 +
5	TXO11#	LVDS odd data 1 -
6	TXO11	LVDS odd data 1 +
7	TXO12#	LVDS odd data 2 -
8	TXO12	LVDS odd data 2 +
9	TXO1C#	LVDS odd clock -
10	TXO1C	LVDS odd clock +
11	TXO13#	LVDS odd data 3 -
12	TXO13	LVDS odd data 3 +
13	DDC_CLK	EDID clock for LCD
14	DDC_DAT	EDID data for LCD
15	VCC	5 volt supply

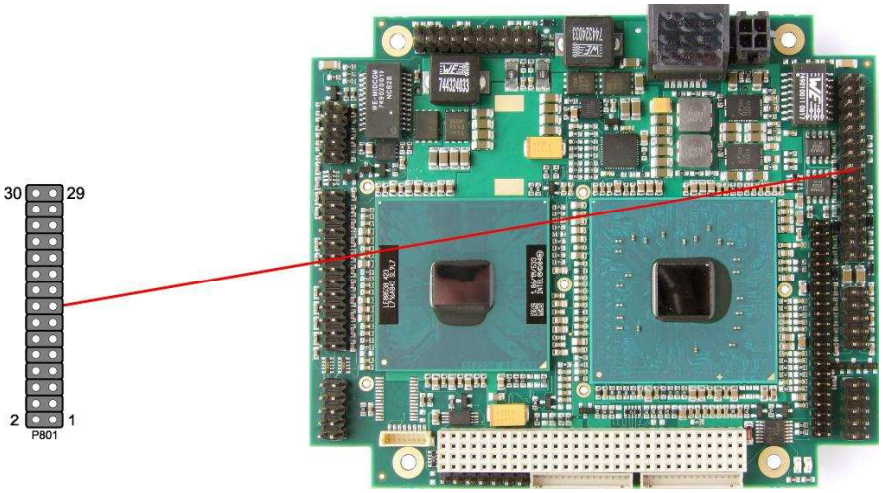
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4.8 USB 1 to 4, LAN, Sound

USB 1-4, LAN and sound are provided via a standard IDC socket connector with a spacing of 2.54 mm. Necessary settings can be accomplished in BIOS setup.
All USB-channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with an USB keyboard without enabling USB keyboard support. Running a USB supporting OS (such as Microsoft® Windows®) with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronically resettable fuse.
The LAN-interface on this connector supports 10BaseT and 100BaseT compatible network components with automatic bandwidth selection. Additional outputs are provided for status LEDs. Auto-negotiate and auto-cross functionality is available, PXE and RPL are available on request.
AC'97 - 2.3 compatible audio I/O is available on this connector. There are two ways to use these signals. Default functionality is the familiar audio in, audio out, and microphone (2-channel mode). OS dependent device drivers can switch these signals to support an 5.1 output; thus in this mode no audio input signals are available. In 2-channel mode LOUT is the only active audio output. Moth MIC inputs are available. In 6-channel mode the speaker outputs are: LOUT to Front, AUXA to Surround, MIC1 to Center and MIC2 to LFE (Sub).
The signals "SPDIFI" and "SPDIFO" provide digital input and output. If a transformation to a coaxial or optical connector is necessary this must be performed externally.

CAUTION

The same IDC socket connector supports all three devices and is not "keyed"! Misconnected support cables may short two devices together and damage the board. Please check diagrams before installing any connecting cables to ensure proper connection.



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Description	Name	Pin		Name	Description
5 volt for USB1	USB1 VCC	1	2	USB2 VCC	5 volt for USB2
USB- channel 1	USB1#	3	4	USB2#	USB- channel 2
USB+ channel 1	USB1	5	6	USB2	USB+ channel 2
ground	GND	7	8	GND	ground
USB+ channel 3	USB3	9	10	USB4	USB+ channel 4
USB- channel 3	USB3#	11	12	USB4#	USB- channel 4
5 volt for USB3	USB3 VCC	13	14	USB4 VCC	5 volt for USB4
LAN activity	ACTLED	15	16	SPEEDLED	LAN 10/100 speed
LAN RX+	LANRX	17	18	LANTX	LAN TX+
LAN RX-	LANRX#	19	20	LANTX#	LAN TX-
digital output SPDIF	SPDIFO	21	22	3.3V	3.3 volt supply
digital input SPDIF	SPDIFI	23	24	S_AGND	analog ground sound
sound output right / frond output right	LOUT_R / FRONT_R	25	26	LOUT_L / FRONT_L	sound output left / frond output left
AUX input right / rear output right	AUXA_R / REAR_R	27	28	AUXA_L / REAR_L	AUX input left / rear output left
microphone input 1 / center output	MIC1 / CENTER	29	30	MIC2 / LFE	microphone input 2 / LFE output



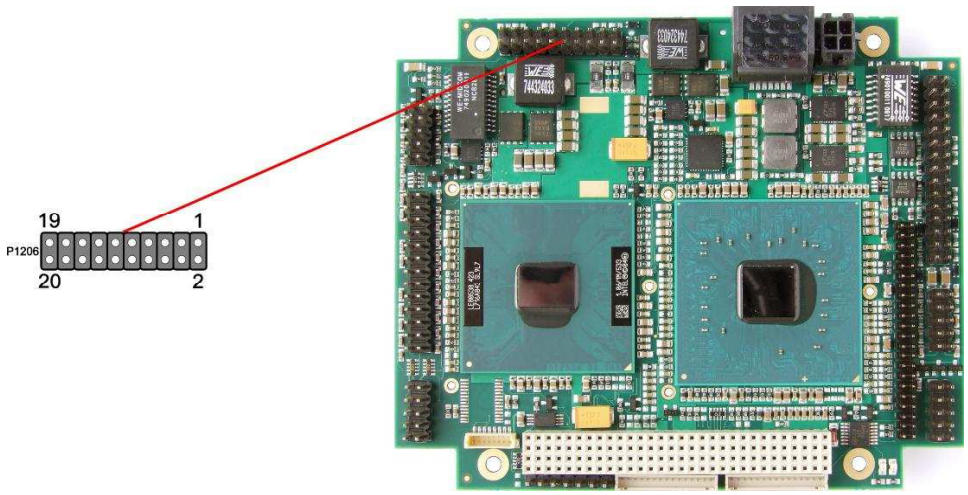
CAUTION

Please keep in mind that both USB 2.0 and 100Mbit LAN require twisted and shielded cables to reliably maintain full speed data rates.

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4.9 USB 5 and 6, LAN2

USB channels 5 and 6 are combined with LAN2 into one standard IDC socket connector with a spacing onf 2.54 mm. All required settings can be accomplished in BIOS setup.
The USB channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with a USB keyboard without enabling USB keyboard support. Running Windows with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronical fuse.
The LAN-interface supports 10BaseT, 100BaseT, and 1000BaseT compatible net components with automatic bandwidth selection. Additional signals are provided for status LEDs.



Description	Name	Pin		Name	Description
5V for USB5	USB5 VCC	1	2	USB6 VCC	5V for USB6
USB- channel 5	USB5#	3	4	USB6#	USB- channel 6
USB+ channel 5	USB5	5	6	USB6	USB+ channel 6
ground	GND	7	8	GND	ground
LAN active LED	ACTLED2	9	10	LILED2	LAN link LED
LAN 1 +	LAN1	11	12	LAN0	LAN 0 +
LAN 1 -	LAN1#	13	14	LAN0#	LAN 0 -
LAN 3 +	LAN3	15	16	LAN2	LAN 2 +
LAN 3 -	LAN3#	17	18	LAN2#	LAN 2-
LAN link 100 LED	SPEED100	19	20	3.3V	3.3 volt supply

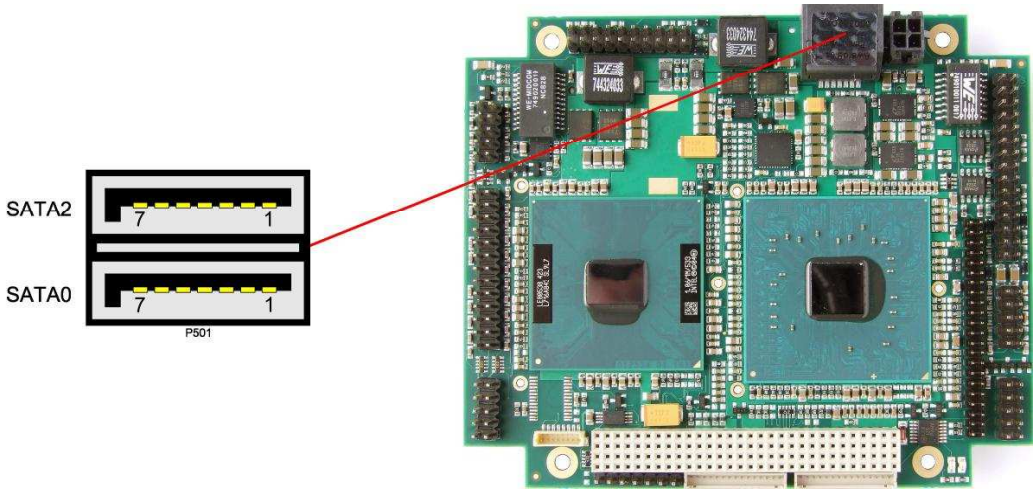
NOTE

LAN LEDs are most commonly connected in the following way: Pins 9 and 20 are connected to a conventional LED while pins 10 and 19 are connected to a bi-color LED. The latter indicates "link" and "link100" each in a different color. In rare cases it can be desirable to have one separate LED for each of the three signals "active", "link", and "link 100". For this non-standard solution to work you need to add a 330Ohm resistor to the LILED2 line.

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4.10 SATA Interfaces

The CB4051 provides two SATA interfaces allowing transfer rates of up to 3 GBit per second. These interfaces are made available via two 7 pin connectors.
The required settings are made in the BIOS setup.



Pin	Name	Description
1	GND	ground
2	SATA1TX	SATA1 transmit +
3	SATA1TX#	SATA1 transmit -
4	GND	ground
5	SATA1RX	SATA1 receive +
6	SATA1RX#	SATA1 receive -
7	GND	ground

Pin	Name	Description
1	GND	ground
2	SATA2TX	SATA2 transmit +
3	SATA2TX#	SATA2 transmit -
4	GND	ground
5	SATA2RX	SATA2 receive +
6	SATA2RX#	SATA2 receive -
7	GND	ground

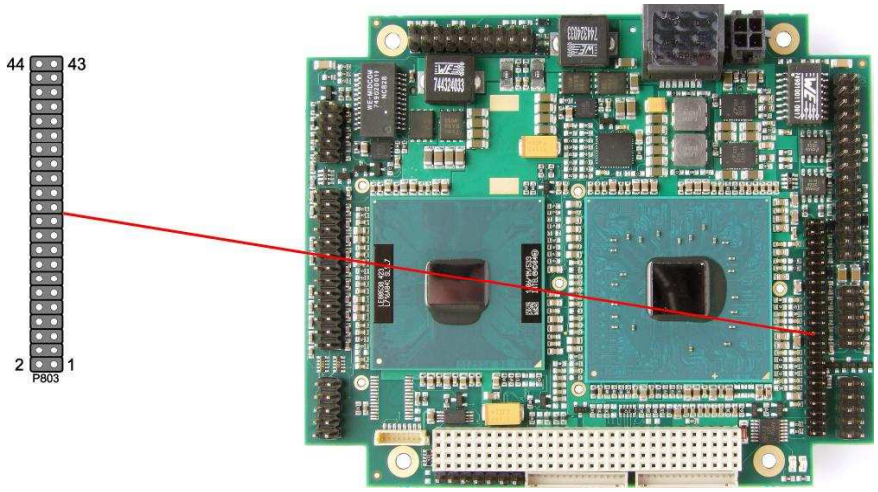
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4.11 IDE Interface

The primary IDE interface is a standard IDC socket connector with a spacing of 2 mm. All commercial IDE devices are supported but an adapter to connect may be necessary.
The required settings are made in the BIOS setup.

CAUTION

Pins are not keyed! Please be sure to connect the cable properly, otherwise you risk damaging the IDE interface, the CPU and the drive, voiding respective warranties.



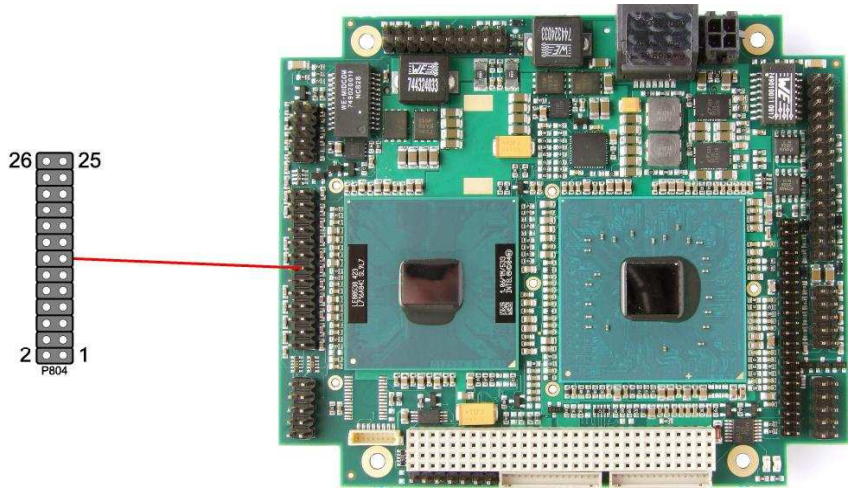
Pinout for primary IDE

Description	Name	Pin		Name	Description
reset	PRST#	1	2	GND	ground
data bit 7	PDD7	3	4	PDD8	data bit 8
data bit 6	PDD6	5	6	PDD9	data bit 9
data bit 5	PDD5	7	8	PDD10	data bit 10
data bit 4	PDD4	9	10	PDD11	data bit 11
data bit 3	PDD3	11	12	PDD12	data bit 12
data bit 2	PDD2	13	14	PDD13	data bit 13
data bit 1	PDD1	15	16	PDD14	data bit 14
data bit 0	PDD0	17	18	PDD15	data bit 15
ground	GND	19	20	N/C	reserved
DMA request signal	PDDREQ	21	22	GND	ground
write signal	PDIOW#	23	24	GND	ground
read signal	PDIOR#	25	26	GND	ground
ready signal	PDRDY	27	28	N/C	reserved
DMA acknowledge signal	PDDACK#	29	30	GND	ground
interrupt signal	PDIRQ	31	32	N/C	reserved
address bit 1	PDA1	33	34	PDMA66EN	enable UDMA66
address bit 0	PDA0	35	36	PDA2	address bit 2
chip select signal 0	PDSC0#	37	38	PDCS1#	chip select signal 1
reserved	N/C	39	40	GND	ground
supply HDD 5V	VCC	41	42	VCC	supply HDD 5V
ground	GND	43	44	N/C	reserved

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4.12 Parallel Interface LPT

The parallel interface is a standard IDC socket connector with a spacing of 2.54 mm. The port address and the interrupt are set via the BIOS setup.
The parallel port may be selected in BIOS-setup to interface to a standard PC floppy drive, but a special cable is required for such operation. Please contact your sales representative for such a cable.



Pinout LPT interface (FDC signals in brackets):

Description	Name	Pin		Name	Description
strobe	STB#	1	2	AFD# (DRVDEN0)	automatic line feed (drive density 0)
LPT data 0 (Index)	PD0 (IDX#)	3	4	ERR# (HDSL#)	error (head select)
LPT data 1 (track 0)	PD1 (TR0#)	5	6	INIT# (DIR#)	init (direction)
LPT data 2 (write protect)	PD2 (WPRT#)	7	8	SLIN# (STP#)	select input (step)
LPT data 3 (read data)	PD3 (RDATA#)	9	10	GND	ground
LPT data 4 (disk change)	PD4 (DC#)	11	12	GND	ground
LPT data 5	PD5	13	14	GND	ground
LPT data 6 (motor 0)	PD6 (MT0#)	15	16	GND	ground
LPT data 7 (drive select 0)	PD7 (DR0#)	17	18	GND	ground
acknowledge (drive select 1)	ACK# (DR1#)	19	20	GND	ground
busy (motor 1)	BUSY (MT1#)	21	22	GND	ground
paper end (write data)	PE (WD#)	23	24	GND	ground
select printer (write enable)	SLCT (WG#)	25	26	VCC	5 volt supply

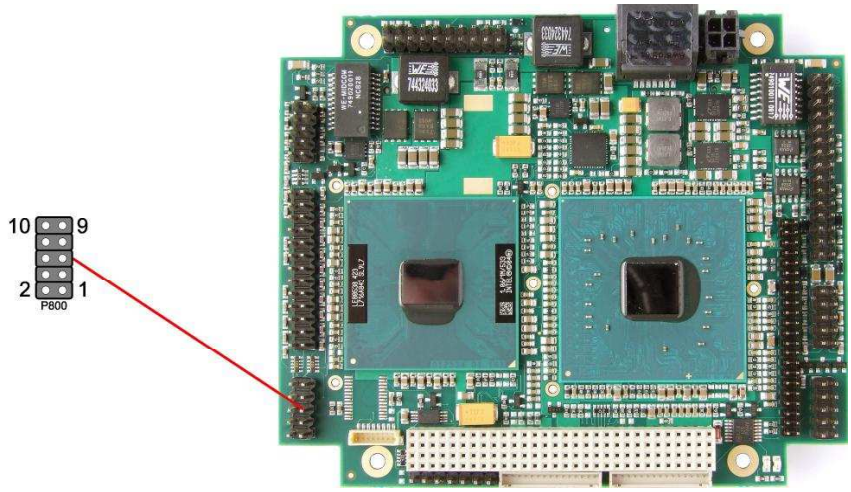
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4.13 Serial Interface COM1

The serial interface is a standard IDC socket connector with a spacing of 2.54 mm. Signals default to RS232 but can be ordered as TTL level too.
The port address and the interrupt are set via the BIOS setup.

CAUTION

COM 1 & 2 cables are not the same pin orientation and you may damage the COM interface and CPU attached if you use the incorrect COM cable.



Description	Name	Pin		Name	Description
data carrier detect	DCD	1	2	DSR	data set ready
receive data	RXD	3	4	RTS	request to send
transmit data	TXD	5	6	CTS	clear to send
data terminal ready	DTR	7	8	RI	ring indicator
ground	GND	9	10	VCC	5 volt supply

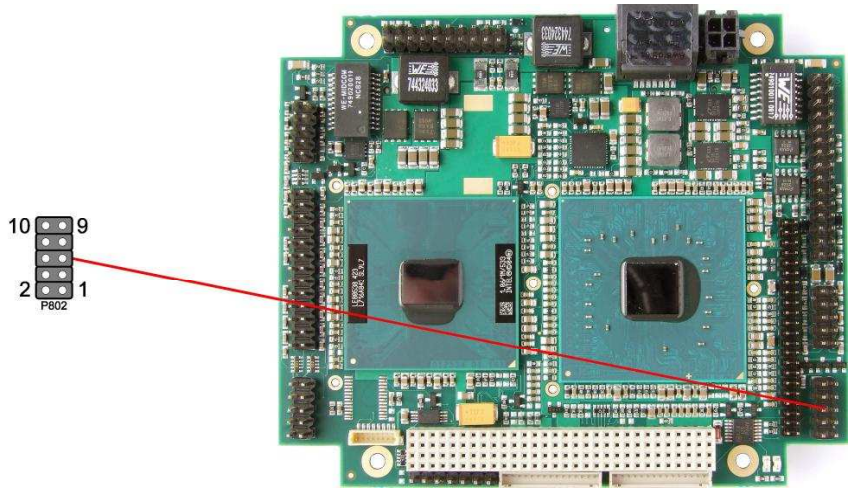
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4.14 Serial Interface COM2

The serial interface is a standard IDC socket connector with a spacing of 2.54 mm. Signals default to RS232 but can be ordered as TTL level too.
The port address and the interrupt are set via the BIOS setup.

CAUTION

COM 1 & 2 cables are not the same pin orientation and you may damage the COM interface and CPU attached if you use the incorrect COM cable.

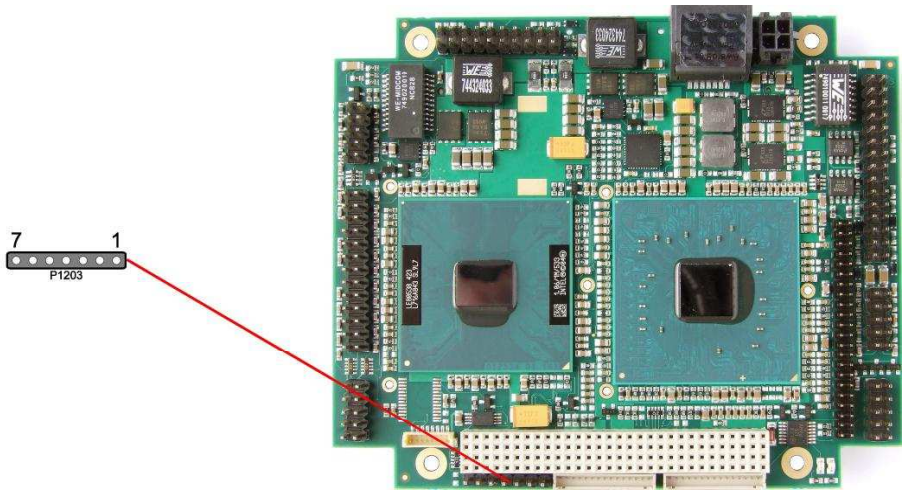


Description	Name	Pin		Name	Description
data carrier detect	DCD	1	2	DSR	data set ready
receive data	RXD	3	4	RTS	request to send
transmit data	TXD	5	6	CTS	clear to send
data terminal ready	DTR	7	8	RI	ring indicator
ground	GND	9	10	VCC	5 volt supply

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4.15 SMBus

The CB4051 can communicate with external devices via the SMBus protocol. The signals for this protocol are available through a standard IDC socket connector with a spacing of 2.54 mm. A 3.3 volt power supply is also available for these SMBus devices. Additionally, you can use this connector to access the PWRBTN# and PS_ON# signals used for power control. If PWRBTN# is held low for four seconds an unconditional hardware power-down event will occur. In the off state S5 both SMBALRT# and PWRBTN# will generate a power-on event if asserted.

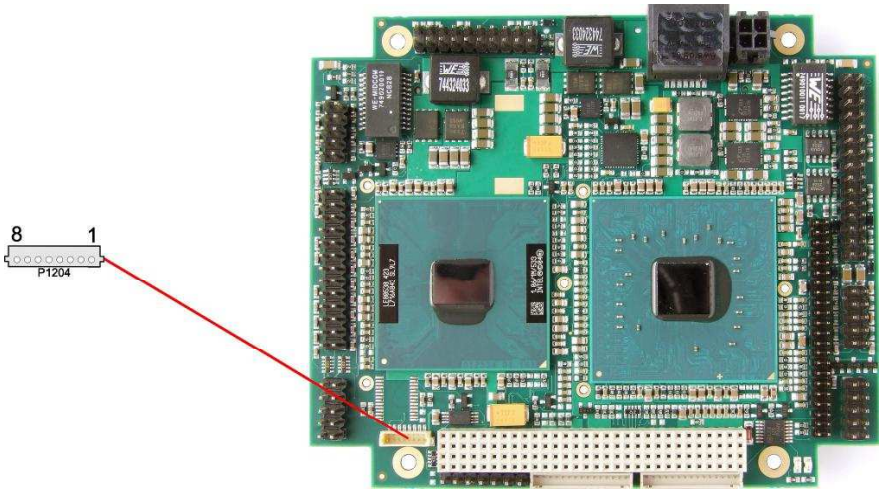


Pin	Name	Description
1	3.3V	3.3 volt supply
2	CS-SMB-CLK	SMBus clock
3	CS-SMB-DAT	SMBus data
4	SMB-ALERT#	SMBus alert
5	PWRBTN#	power button
6	PS_ON#	power supply on
7	GND	ground

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4.16 Monitoring Functions

Some more monitoring functions, e. g. concerning the status of the fan or of other devices connected over SMBus (e. g. temperature sensor), are accessible via an 8 pin connector (JST BM08B-SRSS-TB, mating connector: SHR-08V-S(-B)).



Pin	Name	Description
1	3.3V	3.3 volt supply
2	CS-SMB-CLK	SMBus clock
3	CS-SMB-DAT	SMBus data
4	GND	ground
5	FANON1	5 volt supply (switched)
6	FANCTRL1	fan 1 monitoring signal
7	VCC	5 volt supply
8	FANCTRL3	fan 3 monitoring signal

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5 BIOS Settings

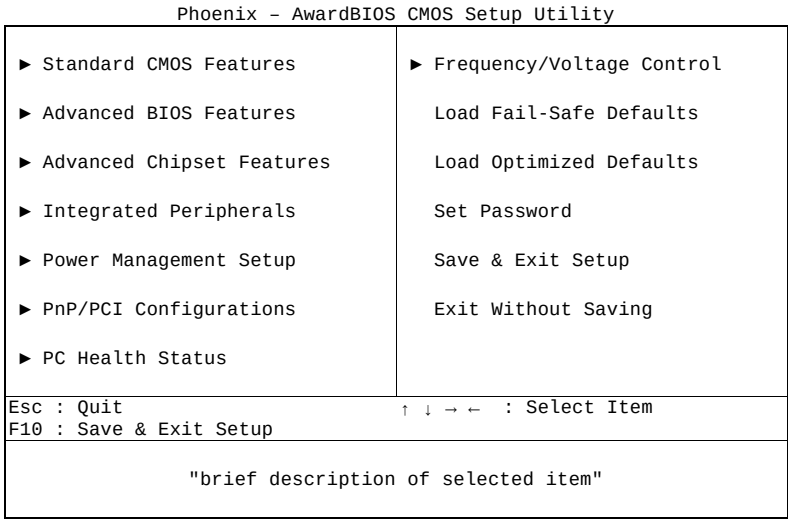
5.1 Remarks for Setup Use

In a setup page, standard values for its setup entries can be loaded. Fail-safe defaults are loaded with F6 and optimized defaults are loaded with F7. These standard values are independent of the fact that a board has successfully booted with a setup setting before.
This is different if these defaults are called from the Top Menu. Once a setup setting was saved, which subsequently leads to a successful boot process, those values are loaded as default for all setup items afterwards.
See also the chapters “Load Fail-Safe Defaults" (5.10) and “Load Optimized Defaults” (5.11).

NOTE

BIOS features and setup options are subject to change without further notice. The settings displayed in the screenshots on the following pages are meant to be examples only. Neither do they represent the recommended settings nor the default settings. What the appropriate settings are depends entirely on the particular application scenario in which the board is used.

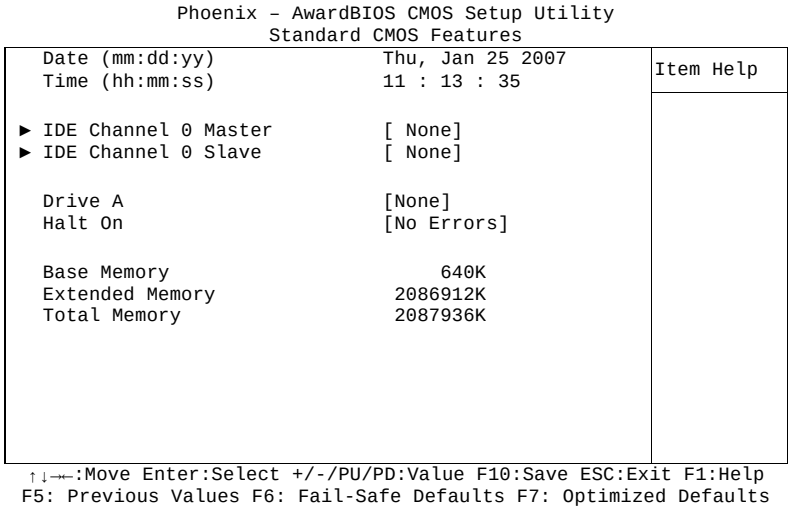
5.2 Top Level Menu



The sign „►“ in front of an item means that there is a sub menu.
The „x“ sign in front of an item means, that the item is disabled but can be enabled by changing or selecting some other item (usually somewhere above the disabled item on the same screen).
Use the arrow buttons to navigate from one item to another. For selecting an item press Enter which will open either a sub menu or a dialog screen.

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5.3 Standard CMOS Features



- **Date (mm:dd:yy)**
  Options: mm: month
  dd: day
  yy: year

- **Time (hh:mm:ss)**
  Options: hh: hours
  mm: minutes
  ss: seconds

- **IDE Channel 0 Master**
  Sub menu: see "IDE Channel 0 Master/Slave" (p. 37)

- **IDE Channel 0 Slave**
  Sub menu: see "IDE Channel 0 Master/Slave" (p. 37)

- **Drive A**
  Options: None / 360K, 5.25 in. / 1.2M, 5.25 in. / 720K, 3.5 in. / 1.44M, 3.5 in. / 2.88M, 3.5 in.

- **Halt On**
  Options: All Errors / No Errors / All, But Keyboard / All, But Diskette / All, But Disk/Key

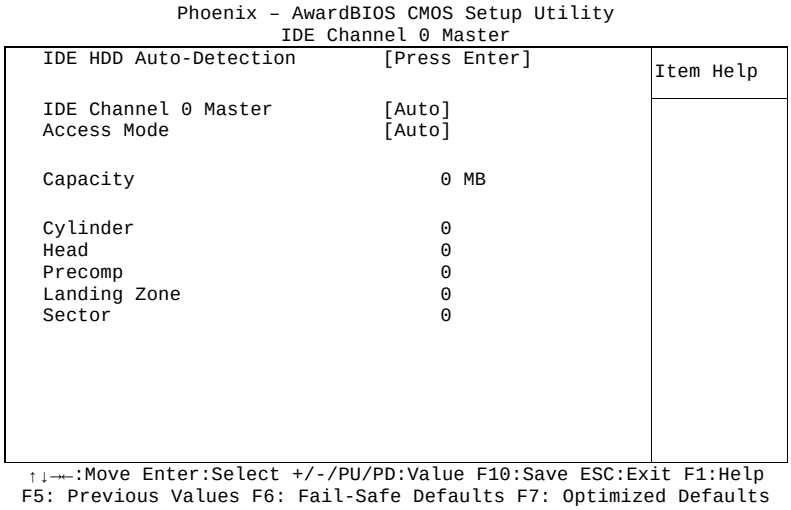
- **Base Memory**
  Options: none

- **Extended Memory**
  Options: none

- **Total Memory**
  Options: none

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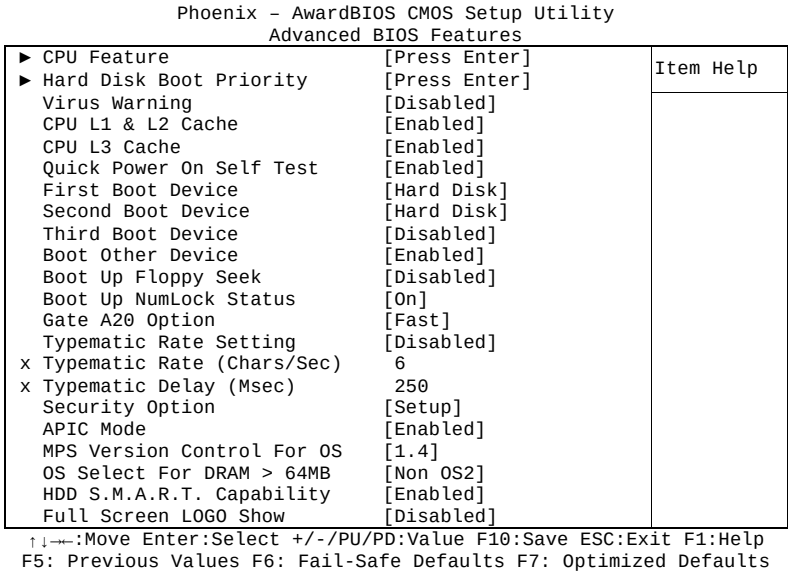
5.3.1 IDE Channel 0 Master/Slave



- **IDE HDD Auto-Detection**
  Options: none
- **IDE Channel 0 Master**
  Options: None / Auto / Manual
- **Access Mode**
  Options: CHS / LBA / Large / Auto
- **Capacity**
  Options: none
- **Cylinder**
  Options: none
- **Head**
  Options: none
- **Precomp**
  Options: none
- **Landing Zone**
  Options: none
- **Sector**
  Options: none

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5.4 Advanced BIOS Features



- **CPU Feature**
  Sub menu: see "CPU Feature" (p. 40)

- **Hard Disk Boot Priority**
  Sub menu: see "Hard Disk Boot Priority" (p. 41)

- **Virus Warning**
  Options: Enabled / Disabled

- **CPU L1 & L2 Cache**
  Options: Enabled / Disabled

- **CPU L3 Cache**
  Options: Enabled / Disabled

- **Quick Power On Self Test**
  Options: Enabled / Disabled

- **First Boot Device**
  Options: Floppy / LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / LAN / Disabled

- **Second Boot Device**
  Options: Floppy / LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / LAN / Disabled

- **Third Boot Device**
  Options: Floppy / LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / LAN / Disabled

- **Boot Other Device**
  Options: Enabled / Disabled

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- **Boot Up Floppy Seek**
  Options: Enabled / Disabled

- **Boot Up NumLock Status**
  Options: Off / On

- **Gate A20 Option**
  Options: Normal / Fast

- **Typematic Rate Setting**
  Options: Enabled / Disabled

- **Typematic Rate (Chars/Sec)**
  Options: 6 / 8 / 10 / 12 / 15 / 20 / 24 / 30

- **Typematic Delay (Msec)**
  Options: 250 / 500 / 750 / 1000

- **Security Option**
  Options: Setup / System

- **APIC Mode**
  Options: Enabled / Disabled

- **MPS Version Control For OS**
  Options: 1.1 / 1.4

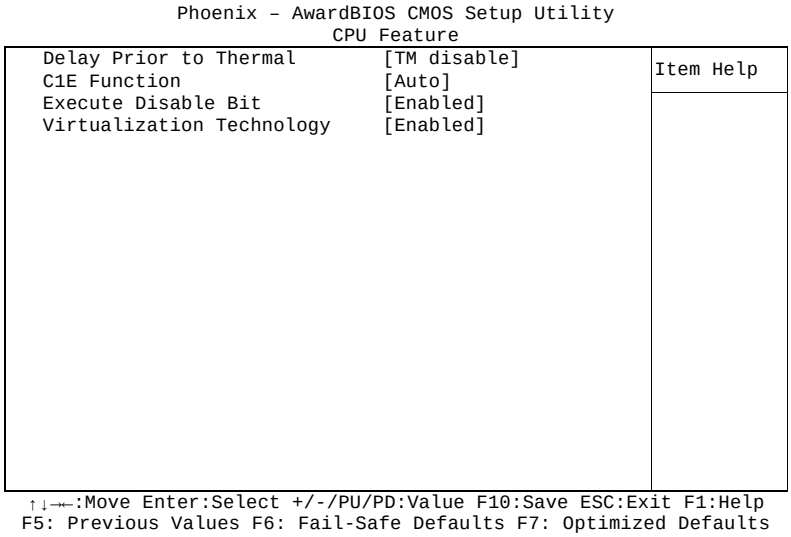
- **OS Select For DRAM > 64MB**
  Options: Non-OS2 / OS2

- **HDD S.M.A.R.T. Capability**
  Options: Enabled / Disabled

- **Full Screen LOGO Show**
  Options: Enabled / Disabled

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5.4.1 CPU Feature



- **Delay Prior to Thermal**
  Options: 4 Min / 8 Min / 16 Min / 32 Min / TM disable

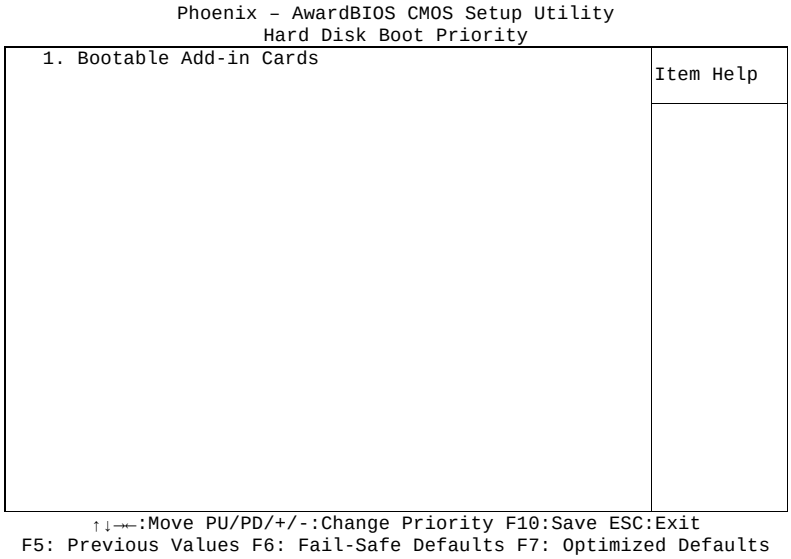
- **C1E Function**
  Options: Auto / Disabled

- **Execute Disable Bit**
  Options: Enabled / Disabled

- **Virtualization Technology**
  Options: Enabled / Disabled

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5.4.2 Hard Disk Boot Priority

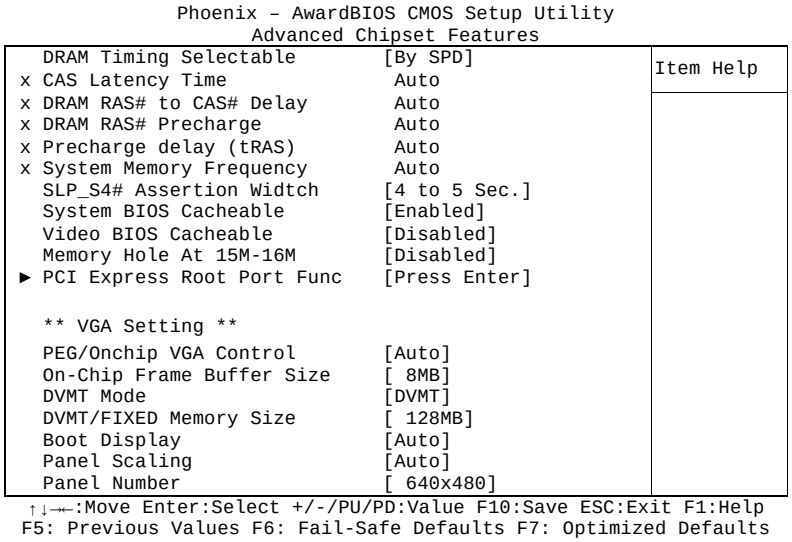


- **[list of available devices]**
  Options: this dialog allows you to set the order in which the available bootable devices shall be accessed for an attempt to boot.

- **Attention!**
  in this sub menu the buttons <Page Up>, <Page Down>, <+> and <-> have a different function than in the rest of the setup: They serve to move the items of the list up or down.

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5.5 Advanced Chipset Features



- **DRAM Timing Selectable**
  Options: By SPD / Manual

- **CAS Latency Time**
  Options: 5 / 4 / 3 / 6 / Auto

- **DRAM RAS# to CAS# Delay**
  Options: 2 / 3 / 4 / 5 / 6 / Auto

- **DRAM RAS# Precharge**
  Options: 2 / 3 / 4 / 5 / 6 / Auto

- **Precharge delay (tRAS)**
  Options: Auto / 4 / 5 / 6 / 7 / 8 / 10 / 11 / 12 / 13 / 14 / 15

- **System Memory Frequency**
  Options: Auto / 533MHz / 667MHz

- **SLP_S4# Assertion Width**
  Options: 4 to 5 Sec. / 3 to 4 Sec. / 2 to 3 Sec. / 1 to 2 Sec.

- **System BIOS Cacheable**
  Options: Enabled / Disabled

- **Video BIOS Cacheable**
  Options: Enabled / Disabled

- **Memory Hole At 15M-16M**
  Options: Enabled / Disabled

- **PCI Express Root Port Func**
  Sub menu: see "PCI Express Root Port Function" (p. 44)

- **PEG/Onchip VGA Control**
  Options: Onchip VGA / PEG Port / Auto

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- **On-Chip Frame Buffer Size**
  Options: 1MB / 8MB

- **DVMT Mode**
  Options: FIXED / DVMT / BOTH

- **DVMT/FIXED Memory Size**
  Options: 64MB / 128MB / 224MB

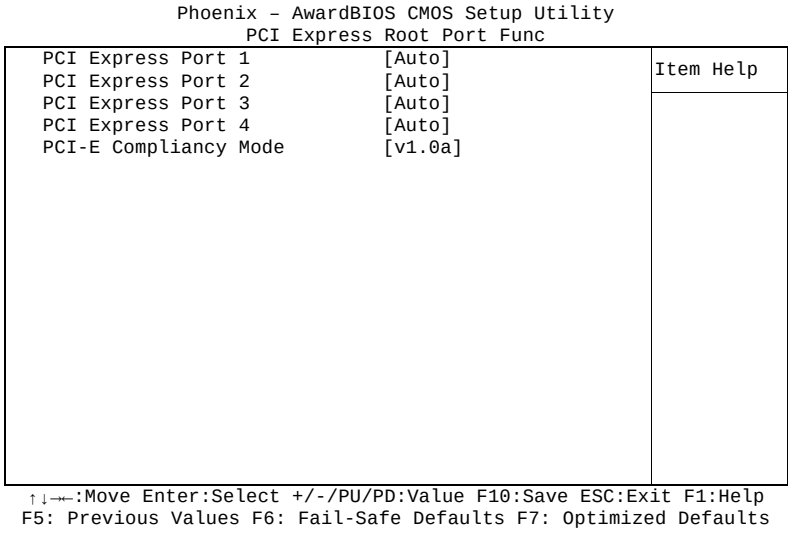
- **Boot Display**
  Options: Auto / CRT / TV / EFP / LFP

- **Panel Scaling**
  Options: Auto / On / Off

- **Panel Number**
  Options: 640x480 / 800x600 / 1024x768 / 1280x1024 / 1400x1050 / 1600x1200 / 1280x768 / 1680x1050 / 1920x1200 / 1280x800 / 1440x900

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5.5.1 PCI Express Root Port Function



- **PCI Express Port 1**
  Options: Auto / Enabled / Disabled

- **PCI Express Port 2**
  Options: Auto / Enabled / Disabled

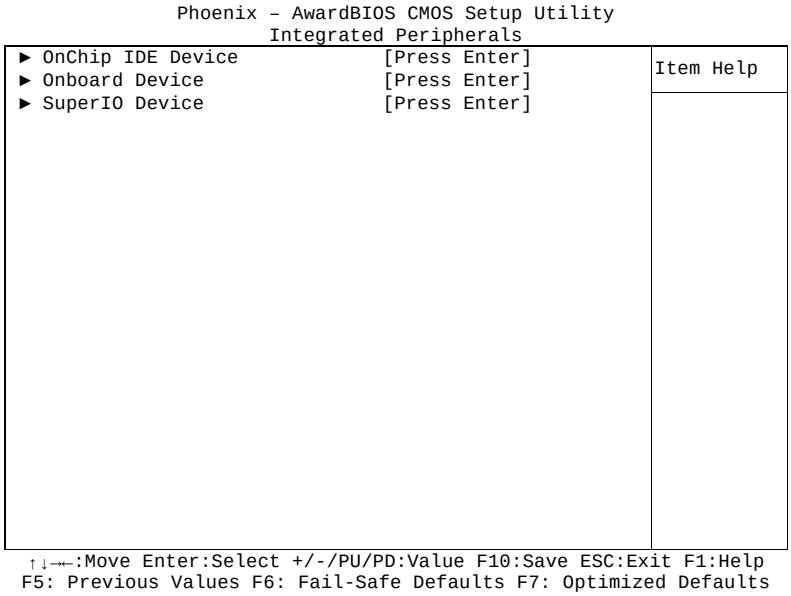
- **PCI Express Port 3**
  Options: Auto / Enabled / Disabled

- **PCI Express Port 4**
  Options: Auto / Enabled / Disabled

- **PCI-E Compliancy Mode**
  Options: v1.0a / v1.0

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5.6 Integrated Peripherals



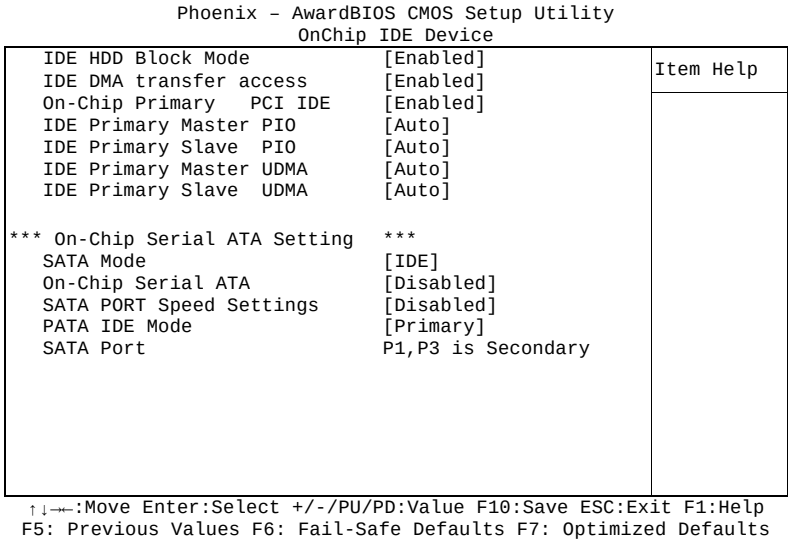
- **OnChip IDE Device**
  Sub menu: see "OnChip IDE Devices" (p. 46)

- **Onboard Device**
  Sub menu: see "Onboard Devices" (p. 47)

- **SuperIO Device**
  Sub menu: see "SuperIO Devices" (p. 48)

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5.6.1 OnChip IDE Devices



- **IDE HDD Block Mode**
  Options: Enabled / Disabled

- **IDE DMA transfer access**
  Options: Enabled / Disabled

- **On-Chip Primary PCI IDE**
  Options: Enabled / Disabled

- **IDE Primary Master PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- **IDE Primary Slave PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- **IDE Primary Master UDMA**
  Options: Disabled / Auto

- **IDE Primary Slave UDMA**
  Options: Disabled / Auto

- **SATA Mode**
  Options: IDE / RAID / AHCI

- **On-Chip Serial ATA**
  Options: Disabled / Auto / Combined Mode / Enhanced Mode / SATA Only

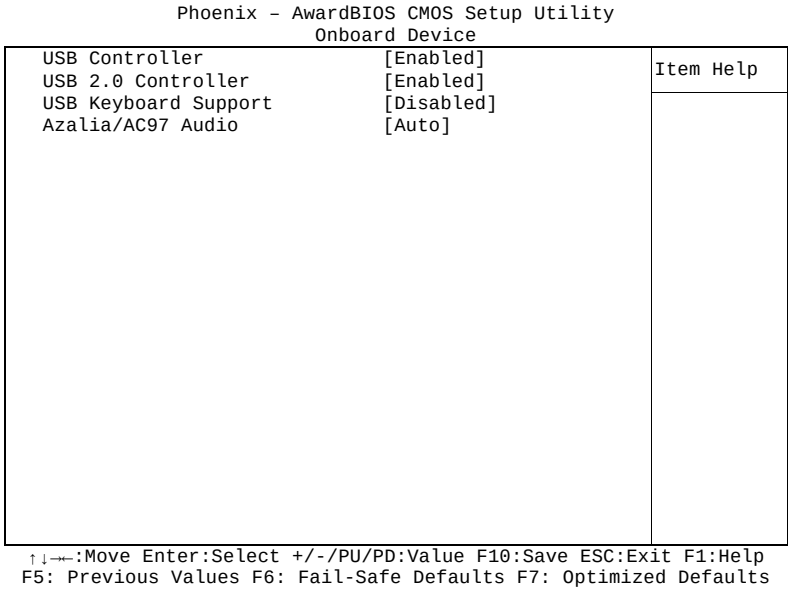
- **SATA PORT Speed Settings**
  Options: Disabled / Force GEN I / Force GEN II

- **PATA IDE Mode**
  Options: none

- **SATA Port**
  Options: none

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5.6.2 Onboard Devices



- **USB Controller**
  Options: Enabled / Disabled

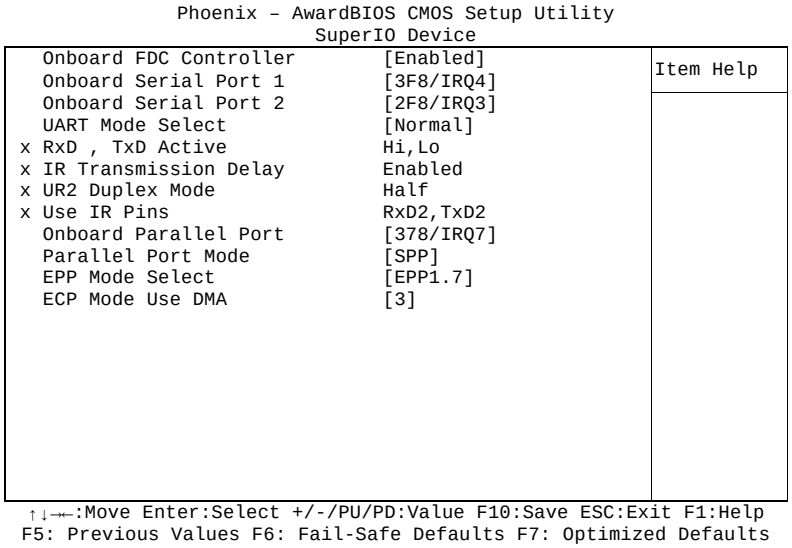
- **USB 2.0 Controller**
  Options: Enabled / Disabled

- **USB Keyboard Support**
  Options: Enabled / Disabled

- **Azalia/AC97 Audio Select**
  Options: Auto / Azalia / AC97 Audio and Modem / AC97 Audio only / AC97 Modem only / All Disabled

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5.6.3 SuperIO Devices



- **Onboard FDC Controller**
  Options: Enabled / Disabled

- **Onboard Serial Port 1**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / Auto

- **Onboard Serial Port 2**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / Auto

- **UART Mode Select**
  Options: IrDA / ASKIR / Normal

- **RxD , TxD Active**
  Options: Hi,Hi / Hi,Lo / Lo,Hi / Lo,Lo

- **IR Transmission Delay**
  Options: Enabled / Disabled

- **UR2 Duplex Mode**
  Options: Full / Half

- **Use IR Pins**
  Options: RxD2,TxD2 / IR-Rx2Tx2

- **Onboard Parallel Port**
  Options: Disabled / 378/IRQ7 / 278/IRQ5 / 3BC/IRQ7

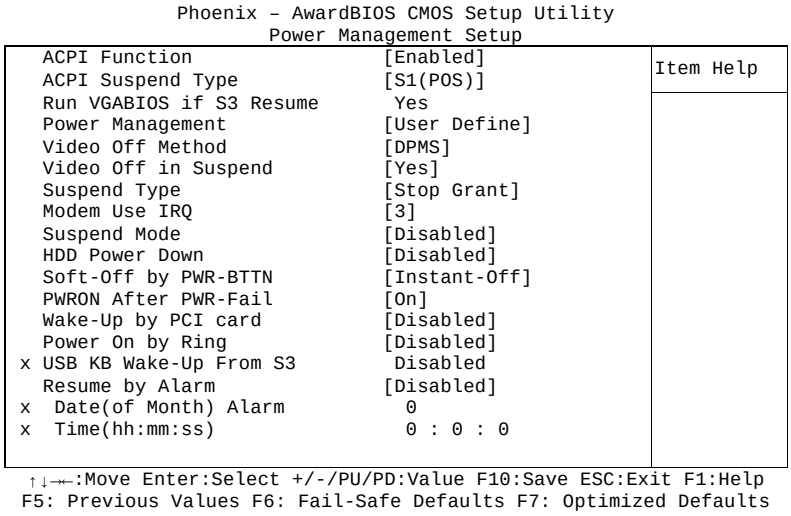
- **Parallel Port Mode**
  Options: SPP / EPP / ECP / ECP+EPP / Normal

- **EPP Mode Select**
  Options: EPP1.9 / EPP1.7

- **ECP Mode Use DMA**
  Options: 1 / 3

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5.7 Power Management Setup



- **ACPI function**
  Options: Enabled / Disabled

- **ACPI Suspend Type**
  Options: S1(POS) / S3(STR) / S1&S3

- **Run VGABIOS if S3 Resume**
  Options: Auto / Yes / No

- **Power Management**
  Options: User Define / Min Saving / Max Saving

- **Video Off Method**
  Options: Blank Screen / V/H SYNC+Blank / DPMS

- **Video Off In Suspend**
  Options: No / Yes

- **Suspend Type**
  Options: Stop Grant / PwrOn Suspend

- **MODEM Use IRQ**
  Options: NA / 3 / 4 / 5 / 7 / 9 / 10 / 11

- **Suspend Mode**
  Options: Disabled / 1 Min / 2 Min / 4 Min / 8 Min / 12Min / 20 Min / 30 Min / 40 Min / 1 Hour

- **HDD Power Down**
  Options: Disabled / 1 Min ... 15 Min

- **Soft-Off by PWR-BTTN**
  Options: Instant-Off / Delay 4 Sec

- **PWRON After PWR-Fail**
  Options: Former Sts / On / Off

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- **Wake Up by PCI Card**
  Options: Enabled / Disabled

- **Power-On by Ring**
  Options: Enabled / Disabled

- **USB KB Wake Up From S3**
  Options: Enabled / Disabled

- **Resume by Alarm**
  Options: Enabled / Disabled

- **Date(of Month) Alarm**
  Options: 1 / ... / 31

- **Time (hh:mm:ss) Alarm**
  Options: [hh], [mm] und [ss] eintragen

- **Primary IDE 0**
  Options: Enabled / Disabled

- **Primary IDE 1**
  Options: Enabled / Disabled

- **Secondary IDE 0**
  Options: Enabled / Disabled

- **Secondary IDE 1**
  Options: Enabled / Disabled

- **FDD,COM,LPT Port**
  Options: Enabled / Disabled

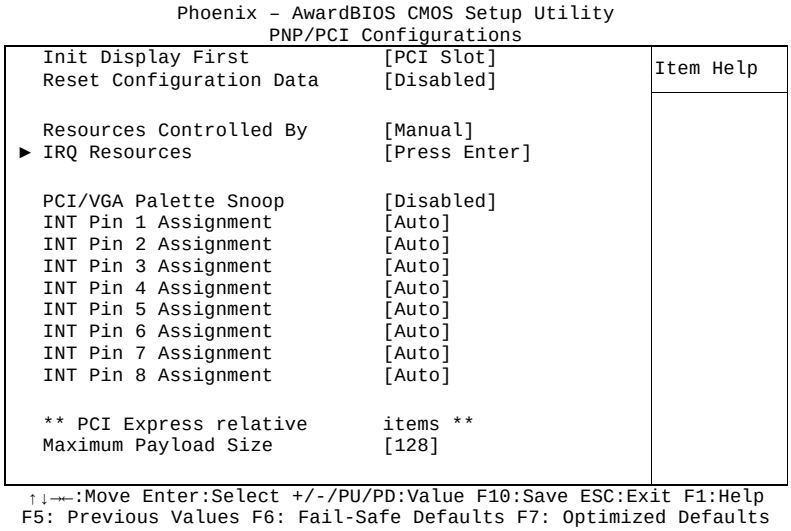
- **PCI PIRQ[A-D]#**
  Options: Enabled / Disabled

- **HPET Support**
  Options: Enabled / Disabled

- **HPET Mode**
  Options: 32-bit mode / 64-bit mode

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5.8 PnP/PCI Configuration



- **Init Display First**
  Options: PCI Slot / Onboard

- **Reset Configuration Data**
  Options: Enabled / Disabled

- **Resources Controlled By**
  Options: Auto(ESCD) / Manual

- **IRQ Resources**
  Sub menu: see "IRQ Resources" (p. 53)

- **PCI/VGA Palette Snoop**
  Options: Enabled / Disabled

- **INT Pin 1 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 2 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 3 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 4 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 5 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 6 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 7 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

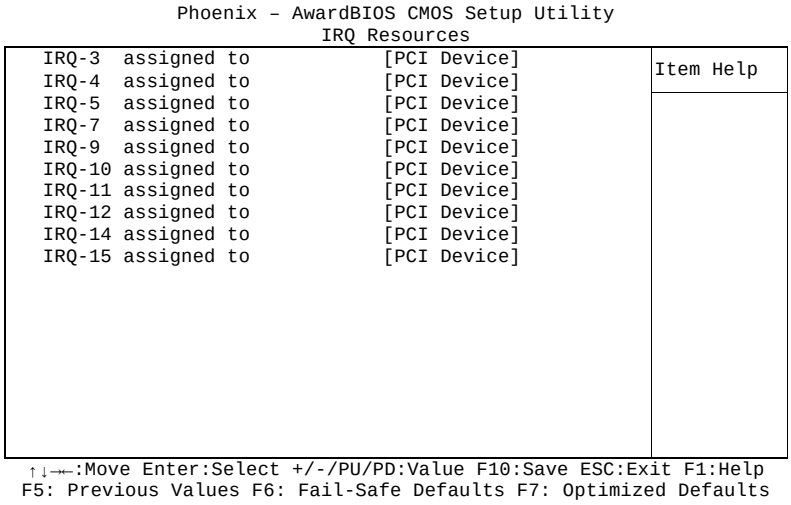
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- **INT Pin 8 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **Maximum Payload Size**
  Options: 128 / 256 / 512 / 1024 / 2048 / 4096
  (Note: The Intel® 945GM and SCH US15W chipsets only support an MPL of 128B)

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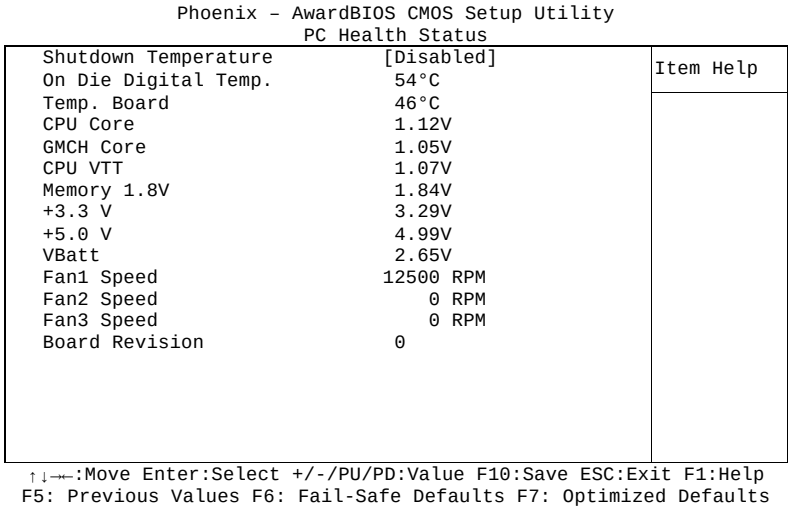
5.8.1 IRQ Resources



- **IRQ-3 assigned to**
  Options: PCI Device / Reserved
- **IRQ-4 assigned to**
  Options: PCI Device / Reserved
- **IRQ-5 assigned to**
  Options: PCI Device / Reserved
- **IRQ-7 assigned to**
  Options: PCI Device / Reserved
- **IRQ-9 assigned to**
  Options: PCI Device / Reserved
- **IRQ-10 assigned to**
  Options: PCI Device / Reserved
- **IRQ-11 assigned to**
  Options: PCI Device / Reserved
- **IRQ-12 assigned to**
  Options: PCI Device / Reserved
- **IRQ-14 assigned to**
  Options: PCI Device / Reserved
- **IRQ-15 assigned to**
  Options: PCI Device / Reserved

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5.9 PC Health Status



- **Shutdown Temperature**
  Options: 60°C/140°F / 65°C/149°F / 70°C/158°C / Disabled

- **On Die Digital Temp.**
  Options: none

- **Temp. Board**
  Options: none

- **CPU Core**
  Options: none

- **GMCH Core**
  Options: none

- **CPU VTT**
  Options: none

- **Memory 1.8 V**
  Options: none

- **+3.3 V**
  Options: none

- **+5.0 V**
  Options: none

- **VBatt**
  Options: none

- **Fan1 Speed**
  Options: none

- **Fan2 Speed**
  Options: none

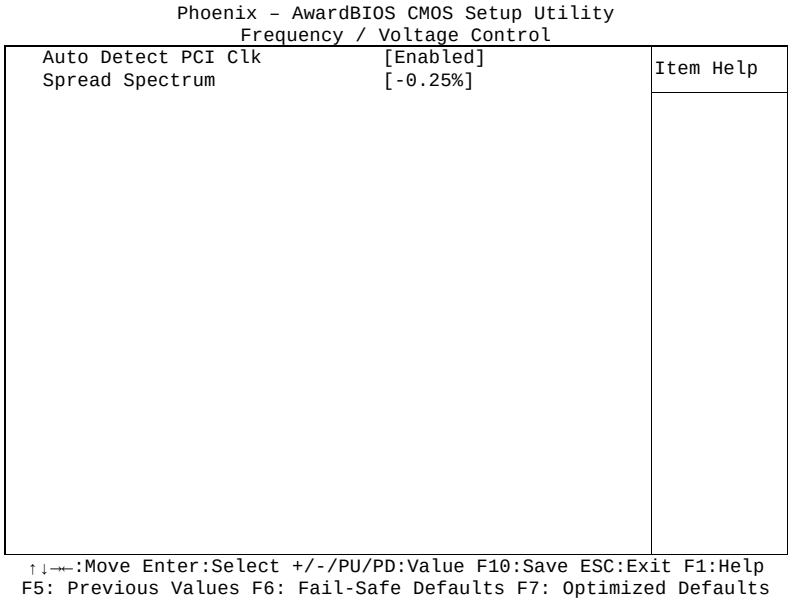
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- **Fan3 Speed**
  Options: none

- **Board Revision**
  Options: none

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5.10 Frequency/Voltage Control



- **Auto Detect PCI Clk**
  Options: Enabled / Disabled

- **Spread Spectrum**
  Options: -0.25% / -0.5% / -0.75% / -1% / +-0.125% / +-0.25% / +-0.375% / +-0.5%

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5.11 Load Fail-Safe Defaults

If this option is chosen, the last working setup is loaded from flash. Working means that the setup setting has already led to a successful boot process.
At the first setting of the BIOS setup, safe values are loaded which lets the board boot. This status is reached again, if the board is reprogrammed with the corresponding flash-program and the required parameters.

5.12 Load Optimized Defaults

This option applies like described under “Remarks for Setup Use” (5.1).
At first start of the BIOS, optimized values are loaded from the setup, which are supposed to make the board boot. This status is achieved again, if the board is reprogrammed using the flash program with the required parameters.

5.13 Set Password

Here you can enter a password to protect the BIOS settings against unauthorized changes. Use this option with care! Forgotten or lost passwords are a frequent problem.

5.14 Save & Exit Setup

Settings are saved and the board is restarted.

5.15 Exit Without Saving

This option leaves the setup without saving any changes.

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6 BIOS update

If a BIOS update becomes necessary, the program “AWDFLASH.EXE” of the company Phoenix is used for this. It is important, that the program is started from a DOS environment without a virtual memory manager such as for example “EMM386.EXE”. In case such a memory manager is loaded, the program will stop with an error message.
The system must not be interrupted during the flash process, otherwise the update is stopped and the BIOS is destroyed afterwards.
The program should be started as follows:

```
awdflash [biosfilename] /sn /cc /cd /cp
```

/sn	Do not save the current BIOS
/cc	Clear the CMOS
/cd	Clear the DMI information
/cp	Clear the PnP information

The erasure of CMOS, DMI and PnP is strongly recommended. This ensures, that the new BIOS works correctly and that all chipset registers, which were saved in the setup, are reinitialized through the BIOS.
A complete description of all valid parameters is shown with the parameter “/?”.
In order to make the updating process run automatically, the parameter “/py” must be added. This parameter bypasses all security checks during programming.



CAUTION

Updating the BIOS in an improper way can render the board unusable. Therefore, you should only update the BIOS if you really need the changes/corrections which come with the new BIOS version.



CAUTION

Before you proceed to update the BIOS you need to make absolutely sure that you have the right BIOS file which was issued for the exact board and exact board revision that you wish to update. If you try to update the BIOS using the wrong file the board will not start up again.

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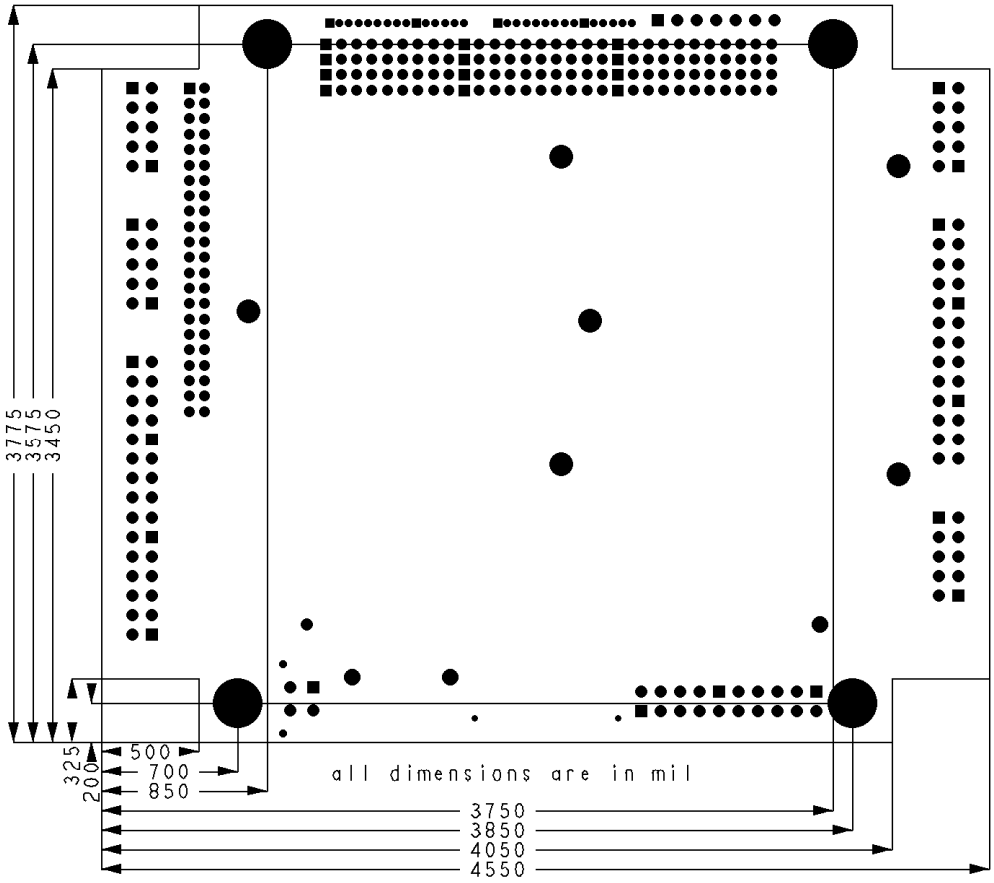
7 Mechanical Drawing

7.1 PCB: Mounting Holes

A true dimensioned drawing can be found in the PC/104 specification.

NOTE

All dimensions are in mil (1 mil = 0,0254 mm)

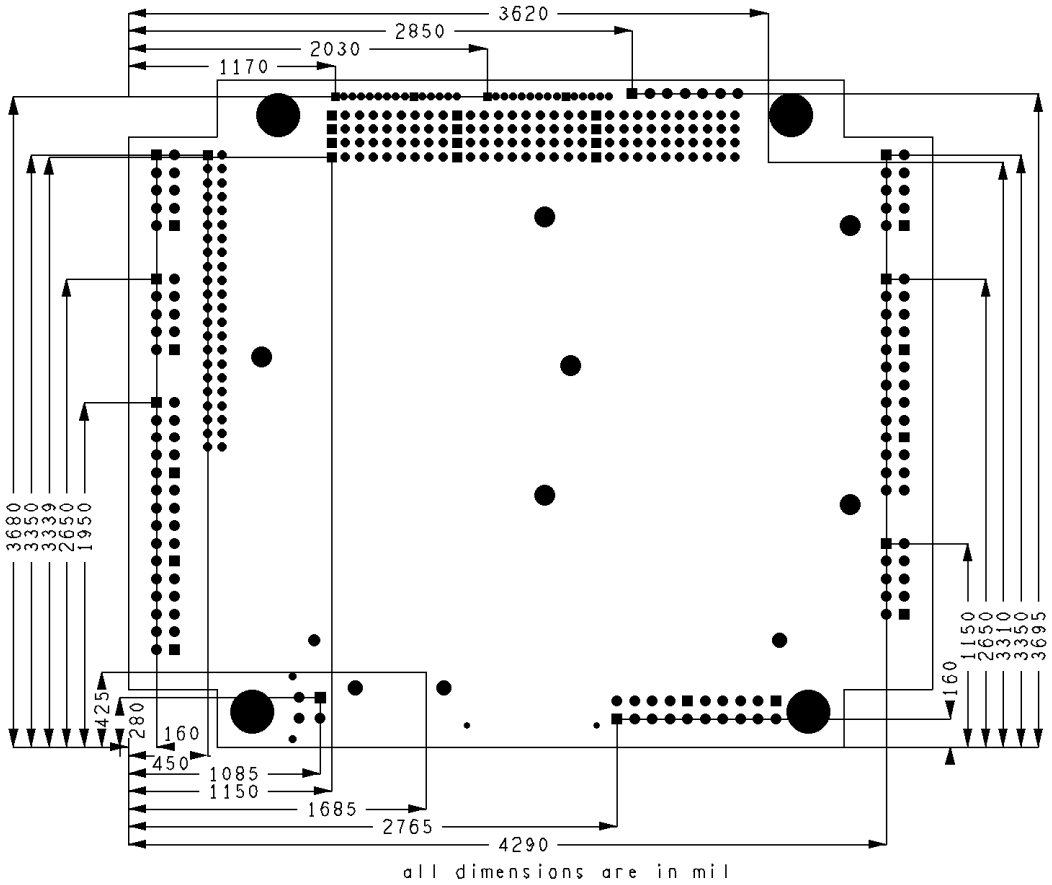


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7.2 PCB: Pin 1 Dimensions

NOTE

All dimensions are in mil (1 mil = 0,0254 mm)

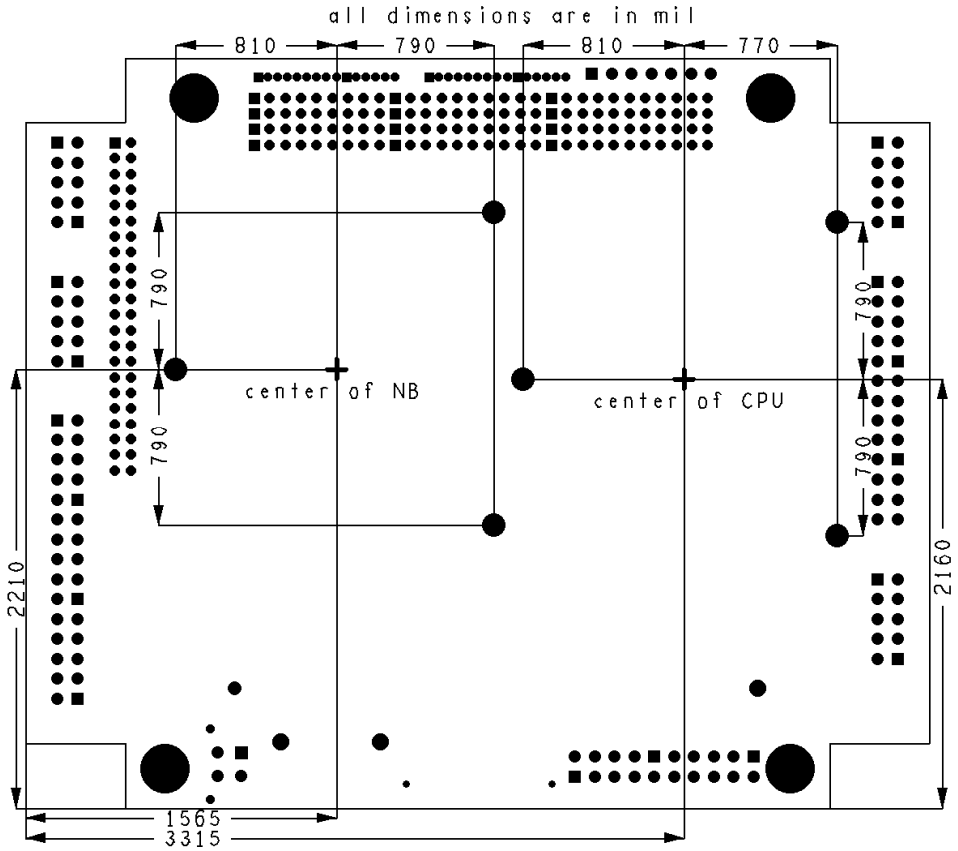


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7.3 PCB: Heat Sink

NOTE

All dimensions are in mil (1 mil = 0,0254 mm)



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8 Technical Data

8.1 Electrical Data

Power Supply:

Board:	5 Volt +/- 5%
RTC:	>= 3 Volt

Electric Power Consumption:

Board:	2,6A idle, 4.1A full (Celeron M 440, 25°C)
RTC:	<= 10µA

8.2 Environmental Conditions

Temperature Range:

Operating:	0°C to +60°C (extended temperature on request)
Storage:	-25°C up to +85°C
Shipping:	-25°C up to +85°C, for packaged boards

Temperature Changes:

Operating:	0.5°C per minute, 7.5°C per 30 minutes
Storage:	1.0°C per minute
Shipping:	1.0°C per minute, for packaged boards

Relative Humidity:

Operating:	5% up to 85% (non condensing)
Storage:	5% up to 95% (non condensing)
Shipping:	5% up to 100% (non condensing), for packaged boards

Shock:

Operating:	150m/s^2, 6ms
Storage:	400m/s^2, 6ms
Shipping:	400m/s^2, 6ms, for packaged boards

Vibration:

Operating:	10 up to 58Hz, 0.075mm amplitude 58 up to 500Hz, 10m/s^2
Storage:	5 up to 9Hz, 3.5mm amplitude 9 up to 500Hz, 10m/s^2
Shipping:	5 up to 9Hz, 3.5mm amplitude 9 up to 500Hz, 10m/s^2, for packaged boards



CAUTION

Shock and vibration figures pertain to the motherboard alone and do not include additional components such as heat sinks, memory modules, cables etc.

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8.3 Thermal Specifications

The board is specified to operate in an environmental temperature range from 0°C to +60°C (extended temperature on request). Maximum die temperature is 100°C. To keep the processor under this threshold an appropriate cooling solution needs to be applied. This solution has to take typical and maximum power consumption into account. The maximum power consumption may be twice as high and should be used as a basis for the cooling concept. Additional controllers may also affect the cooling concept. The power consumption of such components may be comparable to the consumption of the processor.
The board design includes thermal solution mounting points that will provide the best possible thermal interface between die and solution. Since we take thermal solutions seriously we have several advanced, aggressive cooling solutions in our product portfolio. Please contact your sales representative to order or discuss your thermal solution needs.



CAUTION

The end customer has the responsibility to ensure that the die temperature of the processor does not exceed 100°C. Permanent overheating may destroy the board!
In case the temperature exceeds 100°C the environmental temperature must be reduced. Under certain circumstances sufficient air circulation must be provided.



CAUTION

The CB4051 includes circuitry that will notify an intelligent power supply to shut down if the processor reaches a critical temperature. This is achieved by deasserting the (low-active) PS_ON# signal found on the SM-Bus connector. When PS_ON# is pulled high, it can signal an intelligent power supply to shut down if PS_ON# is connected to the power supply's PS_ON input. If PS_ON# is not otherwise connected, the CB4051 can be damaged beyond repair if a thermal shutdown event occurs. In rare instances, if power is not shut down, the board will continue to heat up until failure occurs.

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9.2 Beckhoff Headquarters

Beckhoff Automation GmbH
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33415 Verl
Germany

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fax: +49(0)5246/963-198
e-mail: info@beckhoff.com
web: www.beckhoff.com

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I Annex: Post-Codes

Code	Description
01h	The Xgroup-program code is written in the random access memory from address 1000:0 onwards.
03h	Initialise Variable/Routine "Superio_Early_Init".
05h	1. Cancel display 2. Cancel CMOS error flag
07h	1. Cancel 8042 (keyboard controller) Interface Register 2. Initialising and self testing of 8042 (keyboard controller)
08h	1. Test of special keyboard controllers (Winbond 977 super I/O Chip-series). 2. Enabling of the keyboard-interface register
0Ah	1. Disabling of the PS/2 mouse interface (optional). 2. Auto-detection of the connectors for Keyboard and mouse, optional: swap of PS/2 mouse ports and PS/2 interfaces.
0Eh	Test of the F000h-memory segment (Read/Write ability). In case of an error a signal will come out of the loud speakers.
10h	Auto-detection of the flash-rom-type and loading of the suitable Read/Write program into the run time memory segment F000 (it is required for ESCD-data & the DMI-pool-support).
12h	Interface-test of the CMOS RAM-logic (walking 1's"-algorithm). Setting of the power status of the real-time-clock (RTC), afterwards test of register overflow.
14h	Initialising of the chip-set with default values. They can be modified through a software (MODBIN) by the OEM-customer.
16h	Initialise Variable/Routine "Early_Init_Onboard_Generator".
18h	CPU auto-detection (manufacturer, SMI type (Cyrix or Intel), CPU-class (586 or 686).
1Bh	Initialising if the interrupt pointer table. If nothing else is pretended, the hardware interrupts will point on "SPURIOUS_INT_HDLR and the software interrupts will point on SPURIOUS_soft_HDLR.
1Dh	Initialise Variable/Routine EARLY_PM_INIT.
1Fh	Load the keyboard table (Notebooks)
21h	Initialising of the hardware power management (HPM) (Notebooks)
23h	1. Test the validity of the RTC-values (Example: "5Ah" is an invalid value for an RTC-minute). 2. Load the CMOS-values into the BIOS Stack. Default-values are loaded if CMOS-checksum errors occur. 3. Preparing of the BIOS 'resource map' for the PCI & plug and play configuration. If ESCD is valid, take into consideration the ESCD's legacy information. 4. Initialise the onboard clock generator. Clock circuit at non-used PCI- and DIMM slots. 5. First initialising of PCI-devices: assign PCI-bus numbers - alot memory- & I/O resources - search for functional VGA-controllers and VGA-BIOS and copy the latter into memory segment C000:0 (Video ROM Shadow).
27h	Initialise cache memory for INT 09
29h	1. Program the CPU (internal MTRR at P6 and PII) for the first memory address range (0-640K). 2. Initialising of the APIC at CPUs of the Pentium-class. 3. Program the chip-set according to the settings of the CMOS-set-up (Example: Onboard IDE-controller). 4. Measuring of the CPU clock speed. 5. Initialise the video BIOS.
2Dh	1. Initialise the "Multi-Language"-function of the BIOS 2. Soft copy, e.g. Award-Logo, CPU-type and CPU clock speed…
33h	Keyboard-reset (except super I/O chips of the Winbond 977 series)
3Ch	Test the 8254 (timer device)
3Eh	Test the interrupt Mask bits of IRQ-channel 1 of the interrupt controller 8259.
40h	Test the interrupt Mask bits of IRQ-channel 2 of the interrupt controller 8259
43h	Testing the function of the interrupt controller (8259).
47h	Initialise EISA slot (if existent).

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Code	Description
49h	1. Determination of the entire memory size by revising the last 32-Bit double word of each 64k memory segment. 2. Program “write allocation” at AMD K5-CPUs.
4Eh	1. Program MTRR at M1 CPUs 2. Initialise level 2-cache at CPUs of the class P6 and set the “cacheable range” of the random access memory. 3. Initialise APIC at CPUs of the class P6. 4. Only for multiprocessor systems (MP platform): Setting of the “cacheable range” on the respective smallest value (for the case of non-identical values).
50h	Initialise USB interface
52h	Testing of the entire random access memory and deleting of the extended memory (put on “0”)
55h	Only for multi processor systems (MP platform): Indicate the number of CPUs.
57h	1. Indicate the plug and play logo 2. First ISA plug and play initialising – CSN-assignment for each identified ISA plug and play device.
59h	Initialise TrendMicro anti virus program code.
5Bh	(Optional:) Indication of the possibility to start AWDFLASH.EXE (Flash ROM programming) from the hard disk.
5Dh	1. Initialise Variable/Routine Init_Onboard_Super_IO. 2. Initialise Variable/Routine Init_Onbaord_AUDIO.
60h	Release for starting the CMOS set-up (this means that before this step of POST, users are not able to access the BIOS set-up).
65h	Initialising of the PS/2 mouse.
67h	Information concerning the size of random access memory for function call (INT 15h with AX-Reg. = E820h).
69h	Enable level 2 cache
6Bh	Programming of the chip set register according to the BIOS set-up and auto-detection table.
6Dh	1. Assignment of resources for all ISA plug and play devices. 2. Assignment of the port address for onboard COM-ports (only if an automatic junction has been defined in the setup).
6Fh	1. Initialising of the floppy controller 2. Programming of all relevant registers and variables (floppy and floppy controller).
73h	Optional feature: Call of AWDFLASH.EXE if: - the AWDFLASH program was found on a disk in the floppy drive. - the shortcut ALT+F2 was pressed.
75h	Detection and installation of the IDE drives: HDD, LS120, ZIP, CDROM…
77h	Detection of parallel and serial ports.
7Ah	Co-processor is detected and enabled.
7Fh	1. Switch over to the text mode, the logo output is supported. - Indication of possibly emerged errors. Waiting for keyboard entry. - No errors emerged, respective F1 key was pressed (continue): Deleting of the EPA- or own logo.
82h	1. Call the pointer to the “chip set power management”. 2. Load the text font of the EPA-logo (not if a complete picture is displayed) 3. If a password is set, it is asked here.
83h	Saving of the data in the stack, back to CMOS.
84h	Initialising of ISA plug and play boot drives (also Boot-ROMs)
85h	1. Final initialising of the USB-host. 2. At network PCs (Boot-ROM): Construction of a SYSID structure table 3. Backspace the scope presentation into the text mode 4. Initialise the ACPI table (top of memory). 5. Initialise and link ROMs on ISA cards 6. Assignment of PCI-IRQs 7. Initialising of the advanced power management (APM) 8. Set back the IRQ-register.

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Code	Description
93h	Reading in of the hard disk boot sector for the inspection through the internal anti virus program (trend anti virus code)
94h	1. Enabling of level 2 cache 2. Setting of the clock speed during the boot process 3. Final initialising of the chip set. 4. Final initialising of the power management. 5. Erase the onscreen and display the overview table (rectangular box). 6. Program “write allocation” at K6 CPUs (AMD) 7. Program “write combining” at P6 CPUs (INTEL)
95h	1. Program the changeover of summer-and winter-time 2. Update settings of keyboard-LED and keyboard repeat rates
96h	1. Multi processor system: generate MP-table 2. Generate and update ESCD-table 3. Correct century settings in the CMOS (20xx or 19xx) 4. Synchronise the DOS-system timer with CMOS-time 5. Generate an MSIRQ-Routing table..
C0h	Chip set initialising: - Cut off shadow RAM - Cut off L2 cache (apron 7 or older) - Initialise chip set register
C1h	Memory detection: Auto detection of DRAM size, type and error correction (ECC or none) Auto detection of L2 cache size (apron 7 or older)
C3h	Unpacking of the packed BIOS program codes into the random access memory.
C5h	Copying of the BIOS program code into the shadow RAM (segments E000 & F000) via chipset hook.
CFh	Testing of the CMOS read/write functionality
FFh	Boot trial over boot-loader-routine (software-interrupt INT 19h)

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II Annex: Resources

A IO Range

The used resources depend on setup settings.
The given values are ranges, witch are fixed by AT compatibility. Other IO ranges are used, which are dynamically adjusted by Plug & Play BIOS while booting.

Address	Function
0-FF	Reserved IO area of the board
170-17F	IDE2
1F0-1F7	IDE1
278-27F	LPT2
2E8-2EF	COM4
2F8-2FF	COM2
370-377	FDC2
378-37F	LPT1
3BC-3BF	LPT3
3E8-3EF	COM3
3F0-3F7	FDC1
3F8-3FF	COM1

B Memory Range

The used resources depend on setup settings.
If the USB boot function or legacy support is enabled, the BIOS uses 16KByte RAM in the range from A0000-FFFFF. If the entire range is clogged through option ROMs, these functions do not work any more.

Address	Function
A0000-BFFFF	VGA-RAM
C0000-CFFFF	VGA-Bios
E0000-EFFFF	System-BIOS while booting
F0000-FFFFF	System-BIOS

C Interrupt

The used resources depend on setup settings.
The listed interrupts and their use are given through AT compatibility.
If interrupts must exclusively be available on the ISA side, they have to be reserved through the BIOS setup. The exclusivity is not given and not possible on the PCI side.

Address	Function
IRQ0	Timer
IRQ1	PS/2 Keyboard
IRQ2 (9)	(COM3)
IRQ3	COM1
IRQ4	COM2
IRQ5	(COM4)
IRQ6	FDC
IRQ7	LPT1
IRQ8	RTC
IRQ9	
IRQ10	
IRQ11	

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Address	Function
IRQ12	PS/2 Mouse
IRQ13	FPU
IRQ14	IDE Primary
IRQ15	(IDE Secondary)

D PCI Devices

All listed PCI devices exist on the board. Some PCI devices or functions of devices may be disabled in the BIOS setup. Once a device is disabled other devices may get PCI bus numbers different from the ones listed in the table.

AD	INTA	REQ	PCI	Dev.	Fkt.	Controller / Slot
16	-	-	0	0	0	Host Bridge (GMCH) ID27A0
18	A	-	0	2	0	VGA Graphics (GMCH) ID27A2
12	(A)	-	0	28	0	PCI Express Port 1 (ICH)
12	(B)	-	0	28	1	PCI Express Port 2 (ICH)
12	(C)	-	0	28	2	PCI Express Port 3 (ICH)
12	(D)	-	0	28	3	PCI Express Port 4 (ICH)
12	(A)	-	0	28	4	PCI Express Port 5 (ICH)
12	(B)	-	0	28	5	PCI Express Port 6 (ICH)
13	(A)	-	0	29	0	USB UHCI Controller #1 (ICH) ID27C8
13	(B)	-	0	29	1	USB UHCI Controller #2 (ICH) ID27C9
13	(C)	-	0	29	2	USB UHCI Controller #3 (ICH) ID27CA
13	(D)	-	0	29	3	USB UHCI Controller #4 (ICH) ID27CB
13	(A)	-	0	29	7	USB 2.0 EHCI Controller (ICH) ID27CC
14	-	-	0	30	0	PCI-to-PCI Bridge (ICH) ID244E
14	(A)	-	0	30	2	AC '97 Audio Controller (ICH) ID27DE
14	(B)	-	0	30	3	AC '97 Modem Controller (ICH)
15	-	-	0	31	0	LPC Controller (ICH) ID27B8
15	(A)	-	0	31	1	IDE Controller (ICH) ID27DF
15	(B)	-	0	31	2	SATA Controller (ICH)
15	(B)	-	0	31	3	SMBus Controller (ICH) ID27DA
20	A	0	m	4		External Slot 1
21	B	1	m	5		External Slot 2
22	C	2	m	6		External Slot 3
23	D	3	m	7		External Slot 4
24	(E)	-	n	8	0	LAN Intel 82562GZ (ICH) ID27DC

E SMB Devices

Address	Function
10-11	Standard slave address
60-61	Reserviert by BIOS
88-89	BIOS defined slave address
A0-A1	DIMM 1
A2-AF	Reserved by BIOS
D2-D3	IDTCV111PAG

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