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The R64

Hardware Reference Manual

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Preface

Chapter P

P.1 Purpose

This Hardware Reference Manual is intended for anyone installing or using the R64 and the R64e camera interfaces. The purpose of this manual is two-fold. First, this manual completely describes how the board works. Second, it is a reference manual describing in detail what all of the board's registers do.

P.1.1 Support Services

BitFlow, Inc. provides both sales and technical support for the R64 family of product.

P.1.2 Technical Support

Our web site is www.bitflow.com.

Technical support is available at 781-932-2900 from 9:00 AM to 6:00 PM Eastern Standard Time, Monday through Friday.

For technical support by email (support@bitflow.com) or by FAX (781-933-9965), please include the following:

Product name
Camera type and mode being used
Software revision number
Computer CPU type, PCI chipset, bus speed
Operating system
Example code (if applicable)

P.1.3 Sales Support

Contact your local BitFlow Sales Representative, Dealer, or Distributor for information about how BitFlow can help you solve your most demanding camera interfacing problems. Refer to the BitFlow, Inc. website (www.bitflow.com) for a list of North American and International sales representatives.

P.1.4 Conventions

Table P-1 shos the conventions that are used for numerical notation in this manual.

Table P-1 Base Abbreviations

Base	Designator	Example
Binary	b	1010b
Decimal	None	4223
Hexidecimal	h	12fah

Table P-2 shows the numerical abbreviations that are used in this manual.

Table P-2 Numeric Abbreviations

Abbreviation	Value	Example
K	1024	256K
M	1048576	1M

General Description and Architecture

Chapter 1

1.1 The R64 family

There are two models in the R64 family. The first is the PCI Version, part number R64-PCI-CL, which has a 64-bit PCI interface. The second is the PCI Express version, part number R64-PCE-CL, which has a x8 PCI Express interface. The two boards are identical except for their interfaces. For most of this manual, both boards will be refered to as the R64-CL, or simply the R64.

1.2 General Description

The R64-PCI-CL is a 64-bit, 66 MHz digital frame grabber. Its PCI interface can run in a 32 bit slot or a 64 bit slot. The PCI clock can be up to 66Mhz. The R64 will run in PCI-X slots, however, the bus frequency will be 66 MHz. The R64-CL's DMA engine will transfer data over the PCI bus with zero wait states.

THe R64-PCE-CL is a x8 PCI Express board. It can work in any PCI Express slot that it can fit it. Usually this means an x8 or x16 slot. However, some mother boards have x4 slots with x8 connectors. The R64e will work in these slots, although performance my be somewhat reduced.

Figure 1-1 shows the block diagram of the R64-CL with its main blocks.

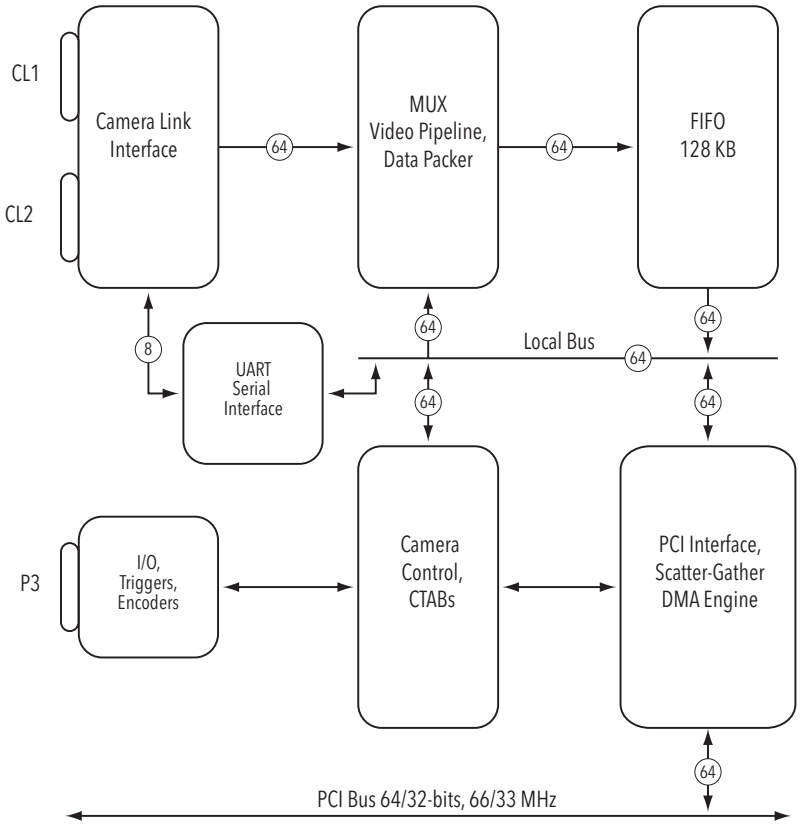


Figure 1-1 R64-CL Block Diagram

The R64-CL is offered in two models: the R64-CL-F, the full model and the R64-CL-D, the dual model.

The R64-CL-F model implements the Camera Link full configuration, i.e. it can accept a single camera putting out up to 64 bits of data.

The R64-CL-D model implements two Camera Link base configurations. It can accept two cameras, each one in base configuration. This model can also accept a single base or medium configuration camera.

The R64-CL can accept input data at up to 80 Mhz.

The following paragraphs are a short description of each block.

The CL-Input block implements the CL full configuration or the dual base configuration, depending on the model. This block has the Channel Link ICs, the Camera Control drivers and the serial communication tranceivers.

The MUX block packs and assembles the data from the Camera Link(s) before it is pushed into the FIFO. This block re-arranges on-the-fly the data from the camera(s) taps so that the data is written in raster scan format in the host memory.

The DCC (DMA and Camera Controller) implements the DMA engine and the camera controls. The camera is controlled by a CTAB (Control Table). The scatter-gather DMA engine is controlled by linked list called QTAB (Quad Table). This list resides in the host memory.

The FIFO block, 128 Kilobytes deep, decouples the camera from the DMA engine. It is implemented with dual ported memories, DPM.

There is an on-board UART, as required by the CL specification. In the dual model, the same UART services both cameras.

The IO connector block has transmitters/receivers to communicate with external industrial equipment (triggers, encoders, light strobes etc.).

CL1 and CL2 are the two Camera Link connectors. CL1 is the main Camera Link connector. It carries data bits 0-23, Camera Controls and serial data port. CL2 is the auxiliary connector. It carries data bits 24-63, for the full model. For the dual model, CL2 carries data bits 0-23, Camera Controls and serial data port.

P3 is the IO connector. It carries a variety of signals that can interface to industrial equipment. These signals can be brought out of the PC through a flat cable.

The purpose of the ID switches is to be able to identify multiple boards in the same PC. The setting of those switches can be read by the software.

1.3 The R64-CL Models

Connector CL1 is the Camera Link main connector. In the full model, data bits 0-23, the Camera Controls and the serial port are assigned to this connector. CL2 is the secondary Camera Link connector. In the full model this connector carries data bits 24-63. Figure 1-2 shows the CL input of the full model. The physical locations of the connectors can be seen in Figure 3-1 and Figure 3-2.

Figure 1-3 shows the CL input for the dual model. Each connector carries 24 bits of data, camera controls and the serial port transceiver lines. The on-board UART can be switched between the cameras under software control. The Camera Controls to the two cameras are identical.

The dual model can also support one single camera in medium configuration, i.e. up to 48 bits of data. The camera control and the serial communication will be done through P1.

The dual base configurations model requires that the two cameras be identical. Below are the requirements for acquiring from two cameras:

- The two cameras are identical (same spacial format, same bit/pixel).
- The two cameras have same frequency pixel clock (no need to synchronize the two cameras clocks).
- The two cameras have same horizontal frequency.
- Area scan cameras must be capable of accepting an asynchronous vertical reset.
- Line scan cameras must be capable of accepting a line sync signal.
- The two cameras will be in the same acquisition state (both are in GRAB/SNAP/FREEZE).

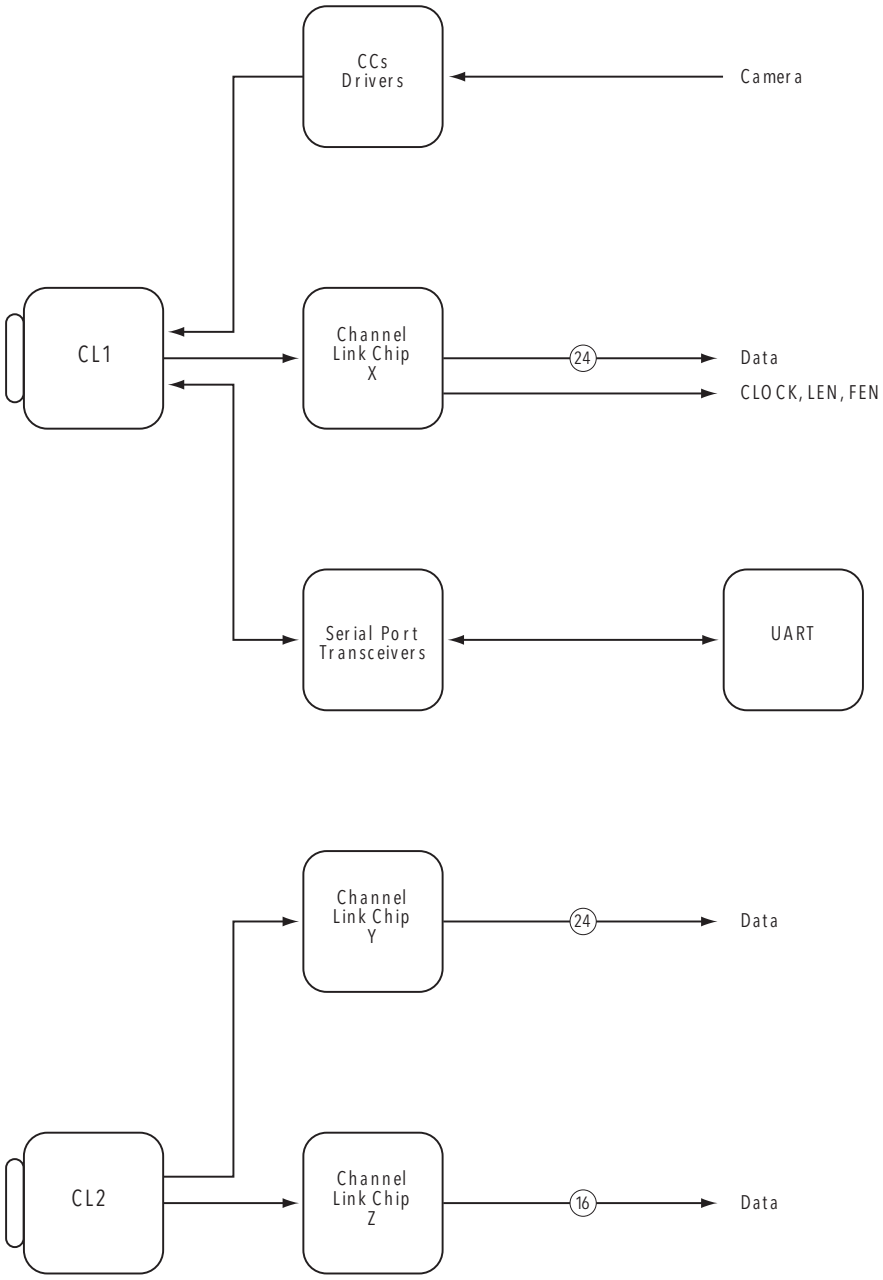


Figure 1-2 R64-CL Full Interface

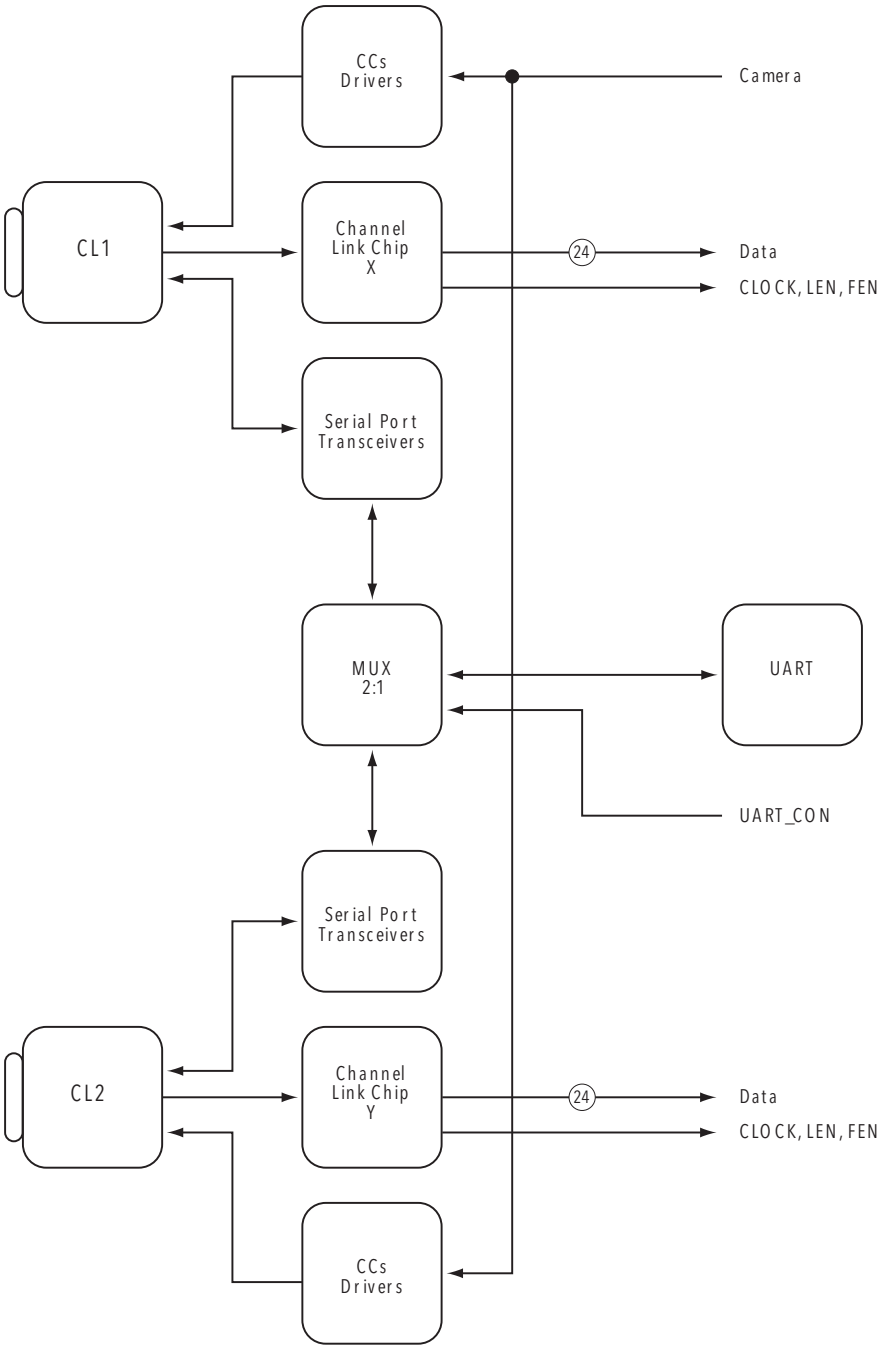


Figure 1-3 R64-CL Dual Interface

1.4 The R64 Flow-Thru Architecture

The MUX block in Figure 1-1 is composed of a chain of sub-blocks that make up the R64-CL Flow-Thru Architecture, FTA. Figure 1-4 shows the structure of the FTA. All the data paths are 64-bit. The implementation of the individual blocks depends on the camera format, i.e. it is specific to the firmware downloaded for each sensor architecture. There is a bitfield, FORMAT, which indicates the currently downloaded firmware.

Below is a description of the individual blocks. For each block are shown the signals that are defined by the user.

Data from the Camera Link is synchronized and assigned to data lanes according to the camera format. The user has no control over these operations. From this block the data goes to a Barrel Shifter.

The Barrel Shifter is composed of four 16-bit barrel shifters. All shifters receive the same command, Left/Right and the amount of shift, up to 15 bits. The main purpose of the Barrel Shifter is for cameras that have more than 8 bits per pixel. The Barrel Shifter can down-shift the data to 8-bit suitable for display. Any camera with up to four taps can be accommodated.

There is a Video Delay Line (not shown) in the data path which can delay the video by up to 8 clocks. This is useful for accurate alignment of the video on the display.

The Video Selector selects the data source: the video from the camera or the on-board generated synthetic video. The various patterns of synthetic video are useful mainly for the on-board Built In Self Test (BIST).

The Mask is a 32-bit mask replicated over the upper and lower 32 bits of the 64-bit data path. The purpose of this mask is to be able to set to zero any bit in the data path (a one will pass the data as is, a zero will set that bit to zero).

The Clip is a clipping mechanism replicated on each one of the eight 8-bit data lanes. If enabled, it will clip the 256 gray levels in each lane according to the formula:

If video > 245 then video = 245
If video <10 then video = 10

This mechanism is useful for displaying gray level data on a VGA that is set in 256-color mode. In this mode the upper and lower 10 gray levels are dedicated to the Windows graphics.

The Assembler will assemble and pack the video data before it is written in the FIFO. This block does the raster scan re-arranging of the data. The packing is dependent on the pixel depth, which is defined in the PIX_DEPTH bitfield in CON10. The DISPLAY bit will force this block to assemble the data as 8-bit pixels, suitable for display. When using this mode, the barrel shifters must be set to down-shift each pixel by the correct amount. A 10-bit camera, for example, would need a 2-bit right shift.

The SWAP bit will swap between odd-even data streams for cameras that supply odd-even pixels.

The amount of data written in the FIFOs is controlled by the Acquisition Window. The vertical and horizontal size of this window is programmed in the ALPF and the ACLP registers respectively (see Section 1.6). The timing of this window is determined by the camera and the acquisition state machine.

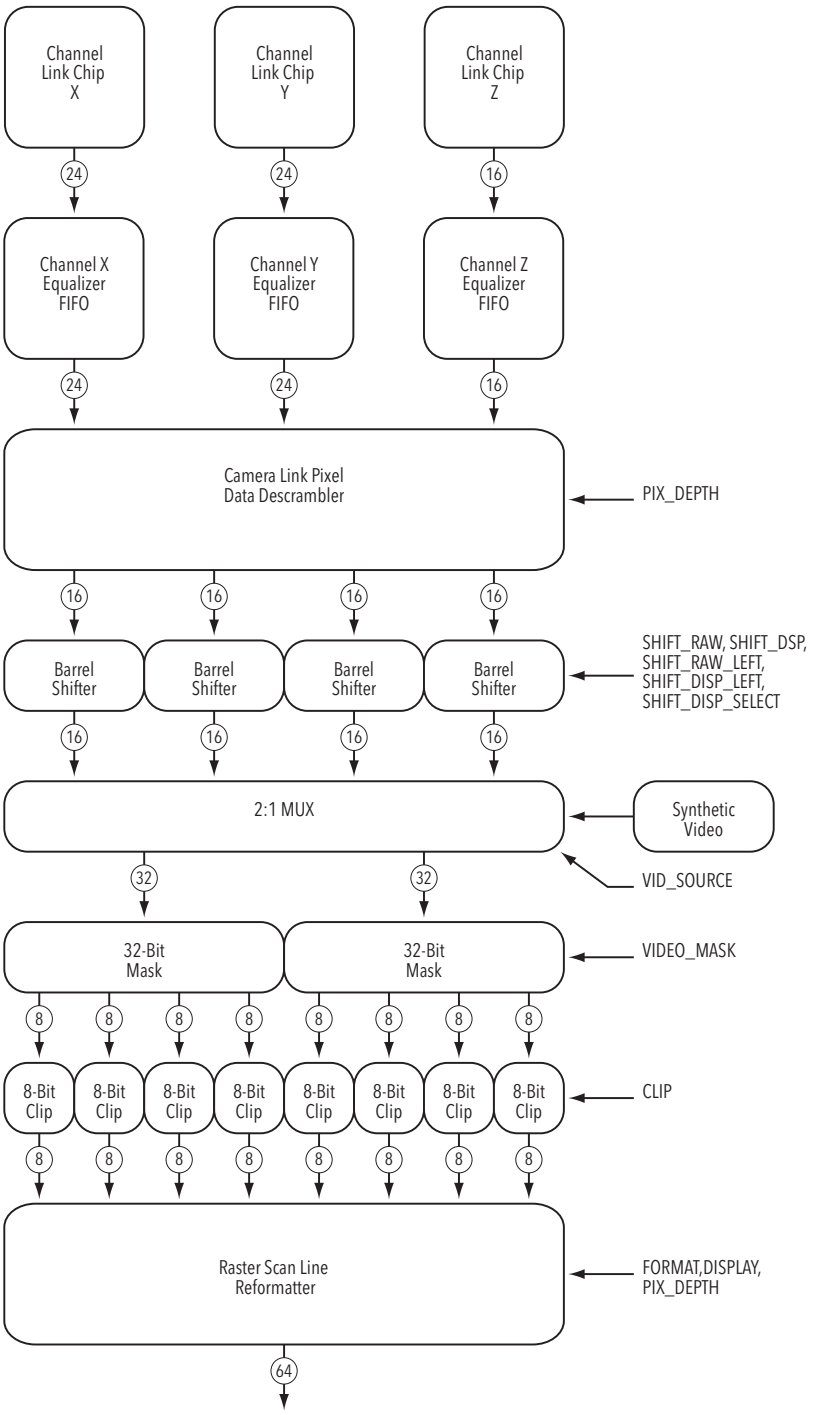


Figure 1-4 R64 Flow Thru Architecture

1.5 Camera Specific Firmware

The R64-CL Flow-Thru architecture is flexible and can be adapted to different cameras architectures. The main intelligence is in the firmware that gets downloaded into the on-board Field Programmable Gate Arrays (FPGAs). This firmware is different for every camera architecture. The firmware is called out in the camera file. On initialization, the R64-CL driver will download into the FPGAs the firmware called-out in the camera file.

The type of the firmware is hard-coded in the FORMAT field in register CON10. The list of the formats is shown in Table 1-1

Table 1-1 Firmware Options

FORMAT	Firmware Name	Format Description
0	MUX	1 tap cameras
1	MUX_2TOEP	2 taps, odd-even pixels
2	MUX_2TOEL	2 taps, odd-even lines
3	MUX_2TS	2 taps, segmented
4	MUX_2TS1RI	2 taps, segmented, right inverted
5	MUX_4TS	4 taps, segmented
6	MUX_4T2S2RIOEP	4 taps, odd-even pixels, right taps inverted
7	MUX_4TQ2RI2BU	4 quads, right quads inverted, bottom quads upside down
8	MUX_2CAM	2 cameras: 1 tap each
9	MUX_2CAM_2TOEP	2 cameras: 2 taps, odd-even pixels
10	MUX_2CAM_2TS1RI	2 cameras: 2 taps, segmented, right-inverted
11	MUX_2CAM_2TS	2 cameras: 2 taps, segmented
12	MUX_2CAM_2TOEL	2 cameras: 2 taps, odd-even lines
13	MUX_8TS	8 taps, segmented
14	MUX_BAY	Bayer decoder, 1 tap 8 bit
15	MUX_BAY_OE	Bayer decoder, 2 taps, odd-even pixels
16	MUX_BAY_2TS	Bayer decoder, 2 taps, segmented
17	MUX_4WI	4 taps, 4-way interleaved

Table 1-1 Firmware Options

FORMAT	Firmware Name	Format Description
18	MUX_2TOEPI	2 taps, odd-even pixels, both inverted
19	MUX_1TI	1 tap, inverted
20	MUX_8WI	8 taps, 8-way interleaved
21	MUX_BAY_2TS_RI	Bayer decoder, 2 taps, segmented, right inverted

1.6 Generation of Acquisition Windows

1.6.1 The Horizontal Active Window, HAW

The Horizontal Active Window (HAW) is a square wave that defines the portion of the line that will be acquired horizontally. HAW can span less than the whole camera line, if we want to acquire only a portion of that line. The size of the HAW is determined by a single number, the Active Clocks Per Line (ACPL). The ACPL is defined as the number of clocks during which the HAW is active. The ACPL field is programmed in CON10. The 17 bits define the maximum HAW as minimum 128K pixels.

The total number of pixels per line that will be acquired can be different than the ACPL. For a dual tap camera that supplies odd-even pixels for example, the total number of pixels acquired will be twice the ACPL, as for every clock the camera supplies two pixels. Note that the ACPL is not a function of the bits per pixel. The relationship between the number of pixels per line and the number of clocks per line is controlled by the firmware currently downloaded to the board. The FORMAT register will indicate which firmware is currently downloaded. Each tap configuration requires a different firmware file be downloaded. The correct firmware is automatically downloaded based on the information contained in the camera configuration file.

The size of the HAW is on an arbitrary boundary. The start in time of the HAW can come from two sources, depending on the setting of the HAW_START bit:

The HSTART bit in the HCTAB, if HAW_START = 1.
The start of LEN, if HAW_START = 0.

In both modes, the start of the HAW can be delayed 0-7 clocks relative to the start function (HSTART or LEN). This is done by the TRIM bits in CON9.

In both modes, the start of the HAW can be advanced 0-7 clocks relative to the start function (HSTART or LEN). This is done by the DELAY bits in CON14.

The HCTAB is the Horizontal Control Table that generates the HSTART, see section on CTABs.

Figure 1-5 shows the controls that generate the HAW.

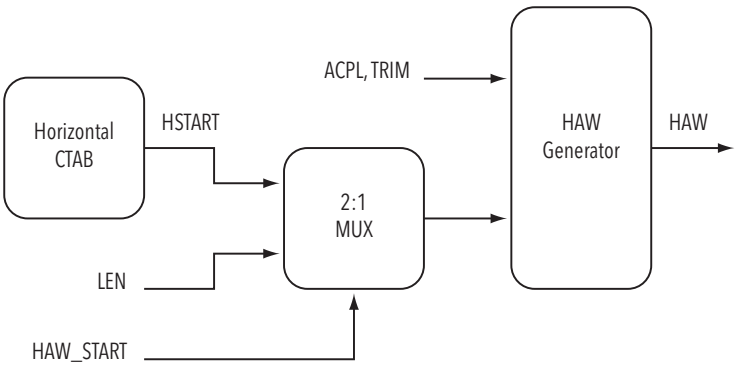


Figure 1-5 Generation of the Horizontal Active Window, HAW

1.6.2 The Vertical Active Window, VAW

The Vertical Active Window (VAW) is a square wave that defines the portion of the frame that will be acquired vertically. VAW can span less than the whole camera frame, if we want to acquire only a portion of that frame. The size of the VAW is determined by a single number, the Active Lines Per Frame (ALPF). The ALPF is defined as the number of HAW periods during which the VAW is active. The ALPF field is programmed in CON17. The 17 bits define the maximum VAW as minimum 128K lines.

The total number of lines per frame that will be acquired can be different than the ALPF. For a dual tap camera that supplies odd-even lines for example, the total number of lines acquired will be twice the ALPF as in the period of one HAW the camera supplies two lines.

The size of the VAW is on an arbitrary boundary. The start in time of the VAW can come from two sources, depending on the setting of the VAW_START bit:

The VSTART bit in the VCTAB, if VAW_START = 1.
The start of FEN, if VAW_START = 0.

Data will be acquired in the window defined by the HAW and the VAW

Figure 1-6 shows the controls that generate the VAW.

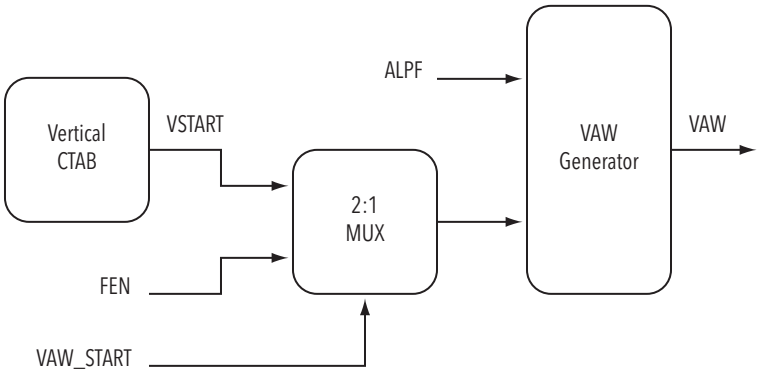


Figure 1-6 Generation of the Vertical Active Window, VAW

1.7 The Control Tables (CTABs)

The CTABs are two memories that are programmed by the host computer and read by the R64's circuitry. The read-out is done in a sequential fashion, i.e. the memories' addresses are scanned sequentially. There is a vertical' memory (VCTAB) and a horizontal' memory (HCTAB). The vertical and horizontal memory each has an associated counter which scans its addresses, VCOUNT and HCOUNT respectively. The concept here is similar to how a CPU runs a program. There is a PC which works it's way through memory, processing each instruction in turn. Each bit in the CTAB corresponds to a different operation. For example, one bit might control the level of a signal going to the camera. In this case the CTABs can be thought of as programmable waveform generators. Another bit might cause an interrupt to occur on the PCI bus, yet another bit might force the HCOUNT to go to zero. The CTABs are fully programmable by software. The details of the CTABs are describe in this section.

1.7.1 Vertical Control Table

Figure 1-7 depicts the structure of the Vertical Control Table (VCTAB). For clarity, the address and data path that allow the host to program the VCTAB are not shown.

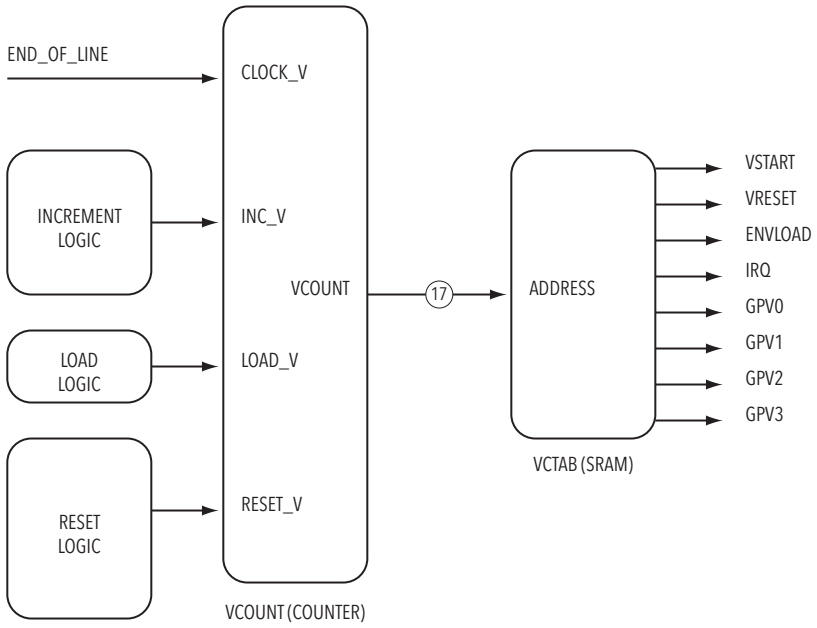


Figure 1-7 Vertical Control Table

The Vertical Control Table is made up of the following blocks:

VCOUNT - a synchronous counter that can be incremented, loaded and reset. The clock that drives VCOUNT is derived from the HCTAB, see below. VCOUNT is 17-bit wide and is connected to the address input of the VCTAB.

Logic for generating INC_V - the increment control signal to the VCOUNT.

Logic for generating LOAD_V - the load control signal to the VCOUNT. When LOAD_V is asserted, VCOUNT is loaded with the value of 8000h (32,768 in decimal).

Logic for generating RESET_V - the reset control signal to the VCOUNT. When RESET_V is asserted, VCOUNT is reset to 0.

Logic for generating CLOCK_V - the clock to the VCOUNT.

VCTAB - a static memory (SRAM) that outputs eight VCTAB control signals. The address of this SRAM is driven by VCOUNT.

If RESET_V and LOAD_V are asserted simultaneous, RESET_V overrides.

As the VCOUNT increments, it scans the addresses of the VCTAB in ascending order. The output of the VCTAB depends on the data that has been written in the VCTAB by the host. If the VCOUNT is free running, it will cyclically scan all the VCTAB's addresses. Any arbitrary cyclic waveform can be implemented by programming the VCTAB with the adequate data.

The LOAD_V and RESET_V will enable the synchronization between external events and the waveforms generated by the VCTAB. LOAD_V and RESET_V will force the VCOUNT to known values, 8000h and 0 respectively.

The INC_V signal will allow for stopping the counter from incrementing. In that case, the output of the VCTAB will be constant. While the VCOUNT is not incrementing, it can still be loaded or reset, see the logic below.

1.7.2 The VCTAB Functions

The functions assigned to the columns in the VCTAB are shown in Table 1-2.

Table 1-2 The VCTAB Functions

Bit	Name	Function
0	VSTART	Start of VAW
1	VRESET	Vertical Reset
2	ENVLOAD	FEN Mask, enable load
3	IRQ	CTAB Interrupt
4	GPV0	General purpose vertical function 0
5	GPV1	General purpose vertical function 1
6	GPV2	General purpose vertical function 2
7	GPV3	General purpose vertical function 3

VSTART defines the start of the Vertical Acquisition Window (VAW), if the start is provided by the VCTAB, see previous section.

VRESET defines the reset of the VCOUNT, in case this function is programmed in the VCTAB.

ENVLOAD enables the FEN to load the VCOUNT. The rationale behind the ENVLOAD column from the VCTAB is that some cameras might not give a FEN, but only two pulses: the start and end of FEN. With the ENVLOAD, we can mask out the unwanted one.

IRQ provides an interrupt to the host, allowing an interrupt to occur at any point on the vertical axis.

GPV are general purpose vertical functions, see usage below.

Note: If a VRESET pulse happens coincident with a LOAD, the LOAD is overriding.

The CLOCK_V Control

CLOCK_V is the clocking of the VCOUNT is generated by the end of the line (horizontal reset).

The INC_V Control

INC_V is the logic for incrementing VCOUNT.

There are only two instances when we want to inhibit the incrementing of VCTAB. The first instance is when VCOUNT reaches 0000h, the “Stop at Zero” case. The other instance is when VCOUNT reaches 7FF0h, the “Vertical Stick” case.

Stop at Zero

Usually, VCOUNT will reach zero because of a RESET_V signal. After VCOUNT is reset, there are programmable options defined by VCNT_RLS_ZERO. Depending on this bitfield, VCOUNT can continue to count or wait at zero till some event occurs, usually the assertion of the TRIGGER.

This operating mode is especially useful for synchronizing cameras to external events. TRIGGER is usually the output of a part-in-place signal. Until this signal is asserted, the VCOUNT waits at address 0000h. After the TRIGGER is asserted, VCOUNT starts counting, i.e., scanning the VCTAB in ascending order. At some address we will program a sync signal to be sent to the camera, usually through GPV0. In response to this sync signal, the camera will give back a frame, and it will assert FEN. The FEN will load address 8000h into VCOUNT. In the VCTAB, we will program the vertical acquisition window to start after address 8000h. At the end of the vertical acquisition window the RESET_V will be asserted, which in turn will reset the VCOUNT. VCOUNT will wait at address 0000h until TRIGGER is asserted.

Vertical Stick

Using the previous example, assume that after we asserted the sync signal to the camera, we expect the camera to give us a frame, i.e., assert FEN. While we expect the camera to assert FEN, VCOUNT is still being incremented. If it takes too long for the camera to respond, VCOUNT will eventually reach and pass beyond 8000h. A vertical

acquisition window will be asserted, even though the camera did not assert FEN. To avoid such a situation, just before address 8000h, when VCOUNT reaches 7FF0h, it will stop. It will stay at 7FF0h until FEN is asserted. Then, VCOUNT will be loaded with 8000h.

The Vertical Stick will occur according to the setting of VCNT_RLS_STK.

The LOAD_V Control

LOAD_V is the logic of loading VCOUNT. In other words, loading VCOUNT means it jump to a new address.

VCOUNT will be loaded with the value 8000h by the rising/falling edge of FEN, if ENVLOAD is asserted. FEN usually marks the start of a valid frame. The start of the vertical acquisition window can be placed starting at address 8000h.

ENVLOAD is a column in the VCTAB. There are cameras that do not assert FEN. Some other type of cameras assert only the start and stop of a frame. In this case, ENVLOAD can mask out the unwanted signals.

Operation on the rising/falling edge of FEN is selected by FENPOL, see CON14

The RESET_V Control

RESET_V is the logic of resetting VCOUNT.

VCOUNT can be reset from different sources, under different conditions. The resetting of the VCOUNT is controlled by the VCNT_RST bitfield.

1.7.3 Horizontal Control Table

The Horizontal Control Table (HCTAB) is 8 bits wide. The function of each bit is show in the following table.

Figure 1-8 depicts the structure of the HCTAB. For clarity, the address and data path that allow the host to program the HCTAB are not shown

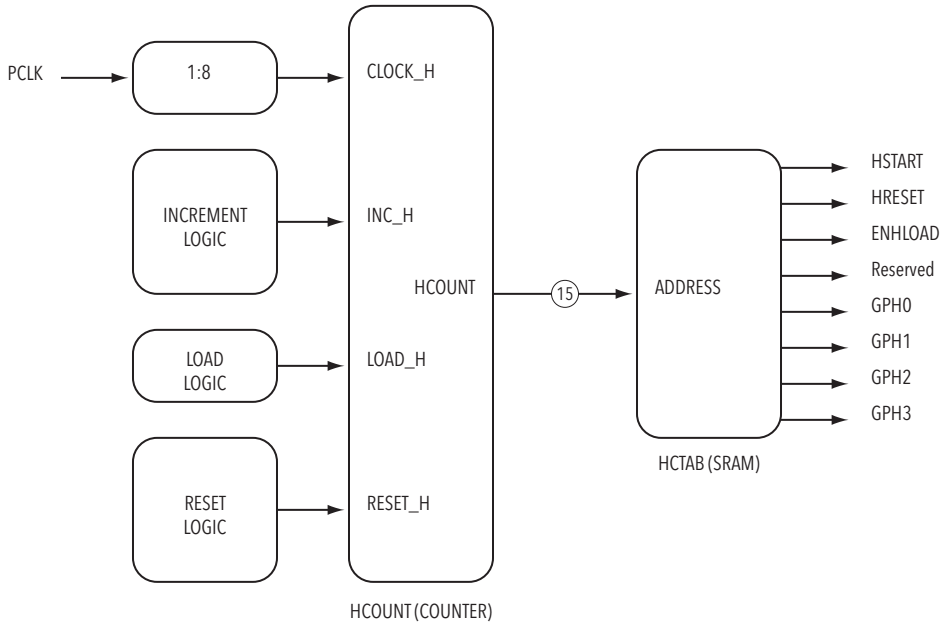


Figure 1-8 Horizontal Control

The Horizontal Control Table is made up of the following blocks:

HCOUNT - a synchronous counter that can be incremented, loaded and reset. The clock that drives HCOUNT is a free running clock, PCLK/8, i.e., the pixel clock divided by eight. HCOUNT is 15 bits wide and is connected to the address input of the HCTAB.

The 15 bit HCOUNT with the PCLK/8 can generate functions up to 256K PCLKs long, on boundaries of 8 PCLKs.

The ACPL is 17 bit, and that can generate an HAW of up to 128K PCLKs.

Logic for generating INC_H - the increment control signal to the HCOUNT.

Logic for generating LOAD_H - the load control signal to the HCOUNT. When LOAD_H is asserted, HCOUNT is loaded with the value of 2000h.

Logic for generating RESET_H - the reset control signal to the HCOUNT. When RESET_H is asserted, HCOUNT is reset to 0.

HCTAB - a static memory (SRAM) that outputs eight HCTAB control signals. The address of this SRAM is driven by HCOUNT.

Logic for generating CLOCK_H - the clock to the HCOUNT. This is a frequency divider. CLOCK_H is PCLK, the pixel clock divided by eight.

Note: If RESET_H and LOAD_H are asserted simultaneously, RESET_H overrides.

As the HCOUNT increments, it scans the address of the HCTAB in ascending order. The output of the HCTAB depends on the data that has been written in the HCTAB by the host. If the HCOUNT is free running, it will cyclically scan all the HCTAB's addresses. Any arbitrary cyclic waveform can be implemented by programming the HCTAB with the adequate data.

The LOAD_H and RESET_H will enable the synchronization between external events and the waveforms generated by the HCTAB. LOAD_H and RESET_H will force the HCOUNT to fixed values, 2000h and 0 respectively.

The INC_H signal will allow for stopping the counter from incrementing. In that case, the output of the HCTAB will be constant. While the HCOUNT is not incrementing, it can still be loaded or reset, see the logic below.

1.7.4 The HCTAB Functions

The functions assigned to the columns in the HCTAB are shown in Table 1-3.

Table 1-3 The HCTAB Functions

HCTAB	Name	Function
D0	HSTART	Start of HAW
D1	HRESET	Reset HCOUNT and increment the VCOUNT
D2	ENHLOAD	LEN Mask, enable horizontal load
D3	reserved	
D4	GPH0	General purpose horizontal function 0
D5	GPH1	General purpose horizontal function 1
D6	GPH2	General purpose horizontal function 2
D7	GPH3	General purpose horizontal function 3

HSTART marks the start of the Horizontal Acquisition Window, HAW. Video will be acquired only while the HAW is active.

HRESET will reset the HCOUNT.

ENHLOAD will allow the loading of the HCOUNT. A location that has 1 will allow the loading of the HCOUNT. A 0 will inhibit the loading of the HCOUNT.

GPH are general purpose horizontal functions. See usage below.

The INC_H Control

INC_H is the logic for incrementing HCOUNT.

There are only two instances when we want to inhibit the incrementing of HCTAB. The first instance is when HCOUNT reaches 0000h, “Stop at Zero” case. The other instance is when HCOUNT reaches 1FF1h, the “Horizontal Stick” case.

The "Stop at Zero" Case

Usually, HCOUNT will reach zero because of a RESET_H signal. After HCOUNT is reset, there are two programmable options:

HCOUNT keeps on counting.
HCOUNT stays at zero until ENCODER is asserted.

The selection between the two options is done by the HCNT_RLS_ZERO bitfield, see next section on camera synchronization.

This operating mode is especially useful for synchronizing line scan cameras to external events. ENCODER is usually the output of an encoder or a tachometer signal. Until this signal is asserted, the HCOUNT waits at address 000oh. After the ENCODER is asserted, HCOUNT starts counting, i.e., scanning the HCTAB in ascending order. At some address we will program a sync signal to be sent to the scan camera, usually through GPH0. In response to this sync signal, the camera will give back a line, and it will assert LEN. The LEN will load address 2000h into HCOUNT. In the HCTAB, we will program the horizontal acquisition window after address 2000h. At the end of the horizontal acquisition window the RESET_H will be asserted, which in turn will reset the HCOUNT. HCOUNT will wait at address 00o0h until ENCODER is asserted.

Horizontal Stick

Using the previous example, assume that after we asserted the sync signal to the camera, we expect the camera to give us a line, i.e., assert LEN. While we expect the camera to assert LEN, HCOUNT is still being incremented. If it takes too long for the camera to respond, HCOUNT will eventually reach and pass beyond 2000h. A horizontal acquisition window will be asserted even though the camera did not assert LEN. To avoid such a situation, just before address 2000h, when HCOUNT reaches 1FF0h, it will stop. It will stay at 1FF0h until LEN is asserted. Then, HCOUNT will be loaded with 2000h.

The LOAD_H Control

LOAD_H is the logic of loading HCOUNT.

HCOUNT will be loaded with the value 2000h by the rising/falling edge of LEN, if ENHLOAD is asserted. LEN usually marks the start of valid data in a line. The Horizontal Acquisition Window can be placed starting at address 2000h.

ENHLOAD is a column in the HCTAB that enables the LEN. There are cameras that do not assert LEN. In that case, the LEN input must be disabled, otherwise its behavior is unpredictable.

Operation on the rising/falling edge of LEN is selected by LENPOL, see CON14.

The RESET_H Control

RESET_H is the logic of reset HCOUNT.

HCOUNT can be reset from several sources, according to HCNT_RST bitfield, see next section on camera synchronization.

Example

Lets look at a simple example to clarify the concept of the HCTAB. Assume we want to program a free running horizontal window of 32 pixels active area. Just before the active area we want to fire a strobe using GPH0. D0 (HSTART) defines the start of the HAW. Bit D1 defines the reset of the HCOUNT. D4, GPH0, is the strobe pulse. The size of the HAW is programmed in ACLP register.

Taking into account that the address counter is clocked by 1/8 the pixel clock, the HCTAB memory map will be as shown in Table 1-4.

Table 1-4 HCTAB Example

HCTAB Address	HRESET	HSTART	GPH0	Comments
0	0	0	0	You got here from address 9
1	0	0	0	
2	0	0	0	
3	0	0	1	Fire the strobe
4	0	1	0	Start Horizontal Acquisition Window
5	0	0	0	Acquire
6	0	0	0	Acquire
7	0	0	0	Acquire
8	0	0	0	Acquire
9	1	0	0	Assert RESET_H
10	0	0	0	

The CT Functions

The CT's are four functions derived from the HCTAB and the VCTAB. Those functions can define an arbitrary horizontal and/or vertical waveform. The definition of the CT's is given below:

CT[0] = GPV[0] AND GPH[0]
CT[1] = GPV[1] AND GPH[1]
CT[2] = GPV[2] AND GPH[2]
CT[3] = GPV[3] AND GPH[3]

Each CT has a vertical and a horizontal component. Both components are programmed in the CTABs. The minimum horizontal pulse is 8 PCLKs. The minimum vertical pulse is one line.

The CT's can be steered to the Camera Controls (on the CL connectors) and to the GPOUTs, on the IO connector.

1.8 Synchronizing Acquisition, Camera, CTABs and External Signals

The R64 is an extremely flexible camera interface. It has been designed to acquire from almost any Camera Link camera and to synchronize with almost all industrial signals. There are two layers of synchronization. The first layer is to synchronize to signals coming from the industrial environment. For example triggers and encoders. The second layer is to synchronize to the camera. This requires both sending signals to the camera (e.g. exposure control) and receiving signals from the camera (e.g. Pixel Clock, Line Enable and Frame Enable). All of these synchronization problems are solved by the R64's Control Tables (CTABs) and Vertical/Horizontal Operations. See previous section for detailed operation on the CTABs.

The Vertical and Horizontal Operations describe different state changes that the board goes through. For example one operation might be to begin acquiring pixels, another might be to reset the VCOUNT back to zero. Generally these state changes are caused by one or more events. There are a number of events, both horizontal and vertical, that the board can react to. These events are tied to operations by a set of programmable bitfields. The details of these events are outlined in this section.

1.8.1 Vertical Operations and Events

The vertical operations are related to the vertical axis of an image (in memory or on the display) or frame timing (of a camera). The operations are mainly commands to VCOUNT and acquisition commands. Each operation can be initiated by some event. The selection of the event that will initiate the specific operation is done by a set of three control bits related to each operation.

Table 1-5 is a list of the vertical operations and their related control bits.

Table 1-5 Vertical Operations

Vertical operation	Control bits
VCOUNT frozen/released from 0000h	VCNT_RLS_ZERO
VCOUNT reset to 0000h	VCNT_RST
VCOUNT load with 8000h	VCNT_LD
VCOUNT frozen/released from 7FF0h	VCNT_RLS_STK
VCOUNT increment	VCNT_INC
Acquire (SNAP, GRAB, CONTINUOUS)	ACQ_CON
FREEZE acquisition	FREEZE_CON
ABORT acquisition	ABORT_CON
START vertical acquisition window	VAW_START

Table 1-6 is a list of the events that initiate the vertical operations:

Table 1-6 Vertical Events

Event description	Event Name
TRIGGER asserted	TRIG_ASRT
TRIGGER de-asserted	TRIG_DASRT
FEN asserted	FEN_ASRT
FEN de-asserted	FEN_DASRT
TRIGGER is HI	TRIG_HI
TRIGGER is LO	TRIG_LO
RESET from VCTAB	RST_VCTAB
RESET from SW	RST_SW
Host writes acquisition command	HOST_WCMD_GRAB/SNAP
Acquisition frame counter reaches programmed value	AQ_COUNT

What follows is a list of each operation and the corresponding events that can be used to cause the operation. Included is the bitfield settings for each operations. It is important to understand that each operation is independent and can be programmed without regard for how the other events are programmed. However, some combinations might not make sense.

VCOUNT Release From Zero

This operation controls the behavior of VCOUNT when it reached zero. See Table 1-7.

Table 1-7 VCNT_RLS_ZERO

Initiator	VCNT_RLS_ZERO	Comments
None	0	Normal operation mode, no stop at 0000h
TRIG_ASRT	1	Edge Mode (aka Letter Mode), always stay at 0000h, release on TRIG_ASRT
TRIG_HI	2	Level Mode (aka Luggage Mode), stay at 0000h if TRIG_LO, release on TRIG_ASRT

VCOUNT Reset To Zero

This operation controls how VCOUNT is reset to zero. See Table 1-8.

Table 1-8 VCNT_RST

Initiator	VCNT_RST	Comments
End_of_VAW	0	Default operation, reset at end of VAW
TRIG_DASRT or End_ of_VAW	1	Triggered termination
RST_VCTAB	2	Reset from VCTAB
FEN asserted or	3	Reset from start of FEN
TRIG_DASRT or RST_ VCTAB	4	Triggered termination
TRIG_DASRT	5	Triggered termination

Note: The VCOUNT is always reset by the RST_SW (sofware reset) and by the HOST_ WCMD_ABORT (host writes ABORT command).

VCOUNT Release From Stick Point (7FF0h)

This operation controls the behavior of VCOUNT when it hits the stick point. The purpose of the stick point is to allow for very long periods of time between frames. The stick point is located at 7ff0h. See Table 1-9.

Table 1-9 VCNT_RLS_STK

Initiator	VCNT_RLS_STK	Comments
None	0	Normal operation mode, no stop at 7FF0h
VLOAD or VRESET	1	Stick at 7FF0h till load (usually FEN) or reset asserted

VCOUNT Load To 8000h

This operation controls how and when VCOUNT loads (jumps to) 8000h. See Table 1-10.

Table 1-10 VCNT_LD

Initiator	VCNT_LD	Comments
None	0	No load
FEN_ASRT and ENV-LOAD	1	Assertion of FEN qualified with ENV-LOAD
FEN_ASRT	2	Assertion of FEN only
TRIG_ASRT	3	Assertion of TRIGGER

Acquisition Command Control

This operations controls how the acquisition commands get initiated. There are two major acquisition commands. The SNAP command, which only acquires one frame. The GRAB command, which continuously acquires frames until a freeze or abort command is issued. In addition, the board has a continuous data mode which is not frame oriented. In continuous data mode, the board will acquire data based only on the clock and data qualifying signals. There are no acquisition commands in this mode. See Table 1-11.

Table 1-11 ACQ_CON

Initiator	ACQ_CON	Comments
HOST_WCMD_GRAB/ SNAP	0	normal, host initiated GRAB/SNAP/ FREEZE
TRIG_ASRT	1	Triggered initiated GRAB/SNAP/ FREEZE
TRIG_ASRT and HOST_ WCMD_GRAB	2	Triggered SNAP
TRIG_HI	3	Continuous data, wo. CTABs

Note: See also Section 1.9 for more details on the how the acquisition commands work.

Freeze Command Control

This operation is used to stop acquisition when the board is in GRAB mode. Acquisition will stop immediately if the board is between frames, or at the end of the current frame, if the board is in the middle of a frame. See Table 1-12.

Table 1-12 FREEZE_CON

Initiator	FREEZE_CON	Comments
HOST_WCMD_ FREEZE	0	Normal, host initiated
AQ_COUNT or HOST_WCMD_ FREEZE	1	Acquisition counter reaches number of frames programmed in the AQ_COUNT register
TRIG_DASRT	2	Trigger de-asserted

Abort Command Control

This operations terminates the current acquisition immediately. This operation will terminate both a SNAP and a GRAB command. If the board is in the middle of a frame, only part of the frame will be acquired. See Table 1-13.

Table 1-13 ABORT_CON

Initiator	ABORT_CON	Comments
HOST_WCMD_ ABORT	0	Normal, host initiated
TRIG_DASRT or HOST_WCMD_ ABORT	1	Abort on falling edge TRIG or host command.

1.8.2 Horizontal Operations and Events

The horizontal operations and events are related to the horizontal axis (of an image in memory or on the display) or line timing (of a camera). The operations are mainly commands to HCOUNT. Each operation can be initiated by some event. The selection of the event that will initiate the specific operation is done by a set of three control bits related to each operation.

Table 1-14 lists the horizontal events.

Table 1-14 Horizontal Operations

Horizontal operation	Control bits
HCOUNT released from zero	HCNT_RLS_ZERO
HCOUNT reset to zero	HCNT_RST
HCOUNT load with 2000h	HCNT_LD
HCOUNT release from 1FF0h	HCNT_RLS7F0
HCOUNT increment	HCNT_INC
Start horizontal active window	HAW_START

The events that can initiate the horizontal operations are listed in Table 1-15.

Table 1-15 Horizontal Events

Event description	Event Name
ENCODER asserted	ENC_ASRT
ENCODER de-asserted	ENC_DASRT
LEN asserted	LEN_ASRT
LEN de-asserted	LEN_DASRT
ENCODER is HI	ENC_HI
ENCODER is LO	ENC_LO
RESET from HCTAB	RST_HCTAB
RESET from SW	RST_SW
FEN asserted	FEN_ASRT

The sections below enumerate all of the horizontal operations and how the various events can initiate them. The control of each operation is independent from all of the others.

HCOUNT Release From Zero

This operation controls the behavior of HCOUNT when it reached zero (see Table 1-16).

Table 1-16 HCNT_RLS_ZERO

Initiator	HCNT_RLS_ ZERO	Comments
None	0	Normal operation mode, no stop at zero
ENC_ASRT	1	One-shot mode, wait for encoder for release

HCOUNT Reset To Zero

This operation controls how HCOUNT is reset to zero (see Table 1-17).

Table 1-17 HCNT_RST

Initiator	HCNT_RST	Comments
END_OF_HAW	0	Default operation, end of HAW
FEN_ASRT or RST_ HCTAB	1	Reset on FEN_ASRT, Random FEN mode
RST_HCTAB	2	Reset from HCTAB

Note: The HCOUNT can always be reset by RST_SW or HOST_WCMD_ABORT

HCOUNT Release From Stick Point (1FF0h)

This operation controls the behavior of HCOUNT when it hits the stick point. The purpose of the stick point is to allow for very long periods of time between lines. The stick point is located at 1ff0h. See Table 1-18.

Table 1-18 HCNT_RLS_STK

Initiator	HCNT_RLS_STK	Comments
None	0	Normal operation mode, no stop at 1FF0h
HLOAD or HRESET	1	Stay at x1FF0 till load (usually LEN) or reset asserted

HCOUNT Load To 2000h

This operation controls how and when HCOUNT loads (jumps to) 2000h (see Table 1-19).

Table 1-19 HCNT_LD

Initiator	HCNT_LD	Comments
None	0	No load
LEN_ASRT	1	Load on LEN assert, qualified with ENH-LOAD column
ENC_ASRT	2	Load on ENCODER assert, qualified with ENHLOAD column

1.9 Acquisition Command and Status

This section describes how the R64 acquisition state machine works. This state machine controls which frames from the camera are acquired and which are ignored. As the commands can be issued asynchronous to the camera's timing, the acquisition state machine will remember the command and execute it starting at the beginning of the frame. That will guarantee that whole frames will be acquired. Note that the acquisition state machine only marks the frames to be acquired. The amount of pixels/line and lines/frame to be acquired in the marked frame is determined by the HAW and VAW, see section Section 1.6.

The acquisition state machine is controlled by the following signals:

AQCMD, the acquisition command bitfield

VACTIVE, the camera's vertical active timing (usually FEN for area scan cameras)..

TRIGGER, the selected trigger.

ACQ_CON, a bitfield that defines special acquisition modes for the state machine.

The current state of the machine can be observed by the AQCMD and AQSTAT bitfields described below.

1.9.1 The Acquisition Bitfields

The acquisition command bits, AQCMD describe the command to be performed in the next frame. The acquisition status bits, AQSTAT, describe the current command that is performed. The four acquisition commands are described in the Table 1-20.

Table 1-20 ACQCMD

AQCMD	Command	Comment
0 (00b)	FREEZE	Stop acquiring at end of current frame
1 (01b)	ABORT	Stop acquiring immediately, unconditionally
2 (10b)	SNAP	Acquire one frame
3 (11b)	GRAB	Acquire continuously

The following list details the behaviors of these bitfields.

- The AQSTAT bits are set at the beginning of the VACTIVE. The last instance a command can be issued is about 4 LCLKs before the start of the VACTIVE.
- For a SNAP command, when the SNAP starts, the AQCMD bits are cleared. Note that for SNAP, the AQCMD bits are written by the host and cleared by the state machine.
- If during a SNAP/GRAB operation another SNAP/GRAB command is issued, it is ignored.

Table 1-11 below describes the acquisition modes for ACQ_CON

Table 1-21 ACQ_CON

ACQ_CON	Mode Description
0 (000b)	Host command performed on next frame
1 (001b)	Host command issued when TRIGGER asserted
2 (010b)	As long as GRAB command is on, a single frame will be SNAPped at every assertion of the TRIGGER.
3 (011b)	Continuous acquisition mode. Host commands are ignored. Data will be acquired continuously as long as the TRIGGER is asserted.

Figure 1-9 shows a timing diagram of the SNAP command, with ACQ_CON = 0. The command is written by the host during the active frame. The acquisition will start at the beginning of the next frame.

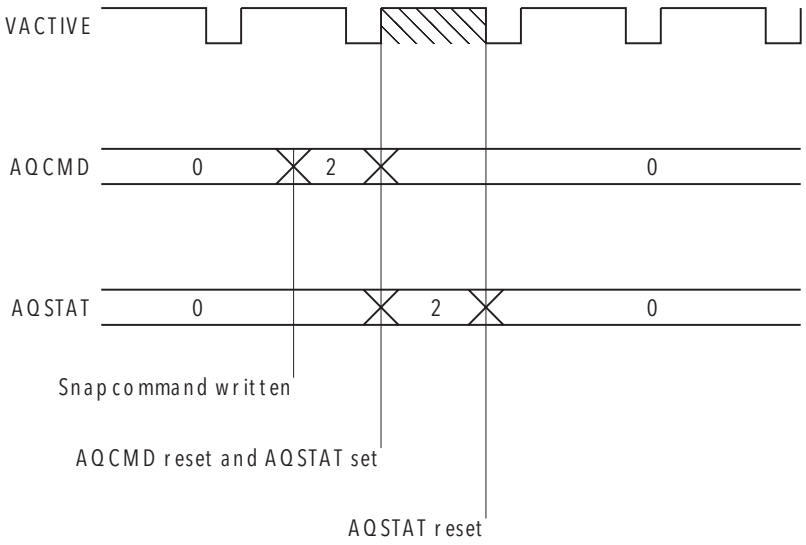


Figure 1-9 Snap Command Timing

Figure 1-10 shows the timing of the GRAB operation with ACQ_CON=0. Figure 1-11 shows the timing of the ABORT operation with ACQ_CON=0. Note that the ABORT command will cut off part of the frame. This command is useful for resetting the board without having to wait for the end of the frame. Figure 1-12 shows a SNAP operation with ACQ_CON=1. In this mode, after the TRIGGER has been asserted and the command executed, the host must write a new command in the AQCMD field. Figure 1-13 shows acquisition in ACQ_CON=2 mode. Here, as long as the GRAB command is on, a frame will be acquired for every assertion of the TRIGGER. In this mode, there is no need for the host to write a new command.

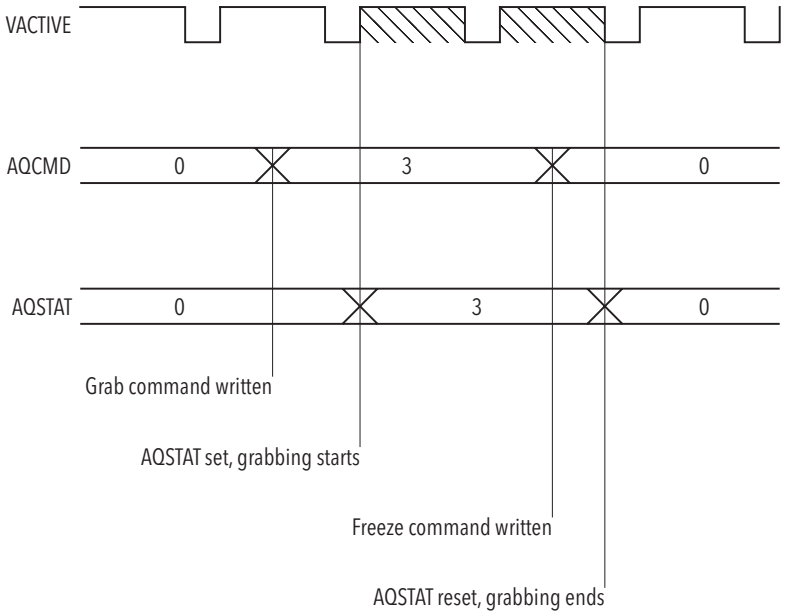


Figure 1-10 Grab Command Timing

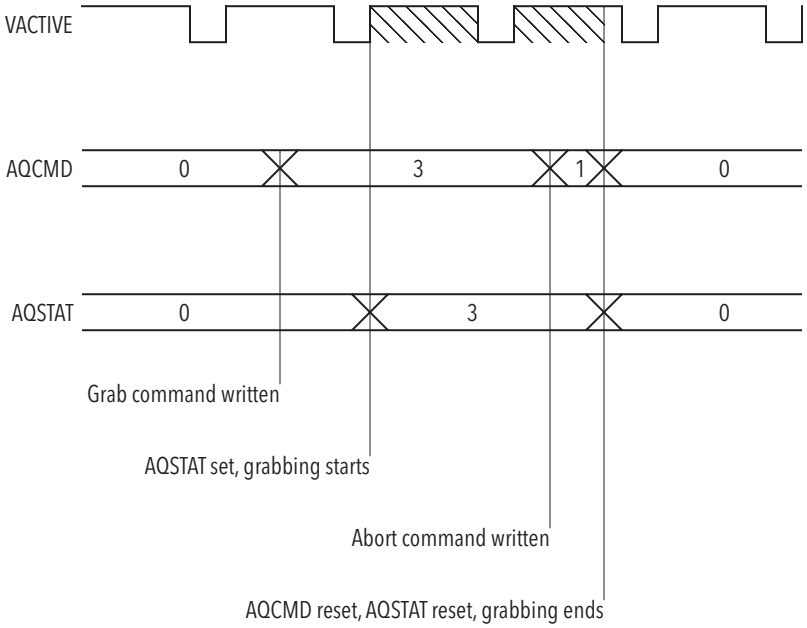


Figure 1-11 Abort Command Timing

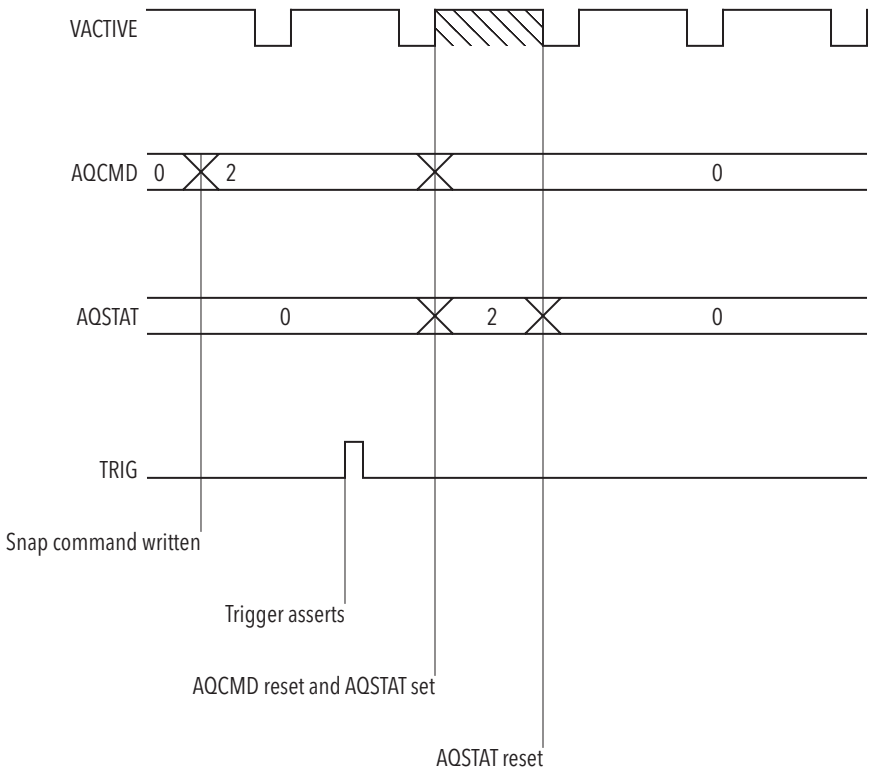


Figure 1-12 Snap Command Timing with ACQ_CON = 2

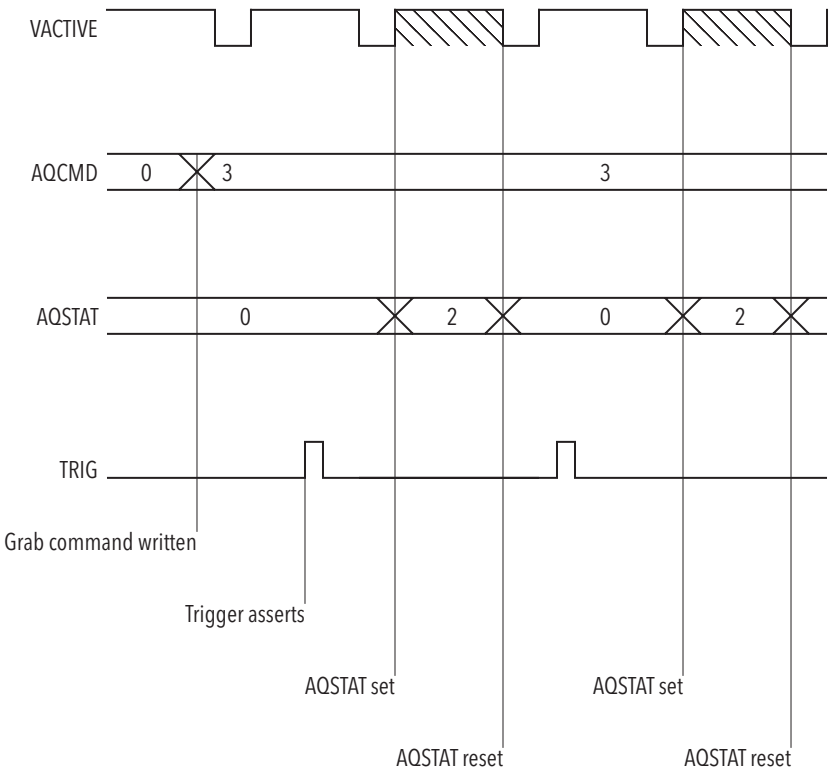


Figure 1-13 Grab Command Timing with ACQ_CON = 2

1.10 Trigger Processing

This section describes how the trigger circuit of the R64 works. The trigger is used to initiate a vertical operation (for example, capturing one frame). There are three possible external hardware inputs to the trigger circuit and a software input. Assertion of the trigger can be delayed by up to 8192 lines (granularity is 8 lines). This delay works only with the external hardware trigger. Figure 1-14 illustrates the trigger circuit.

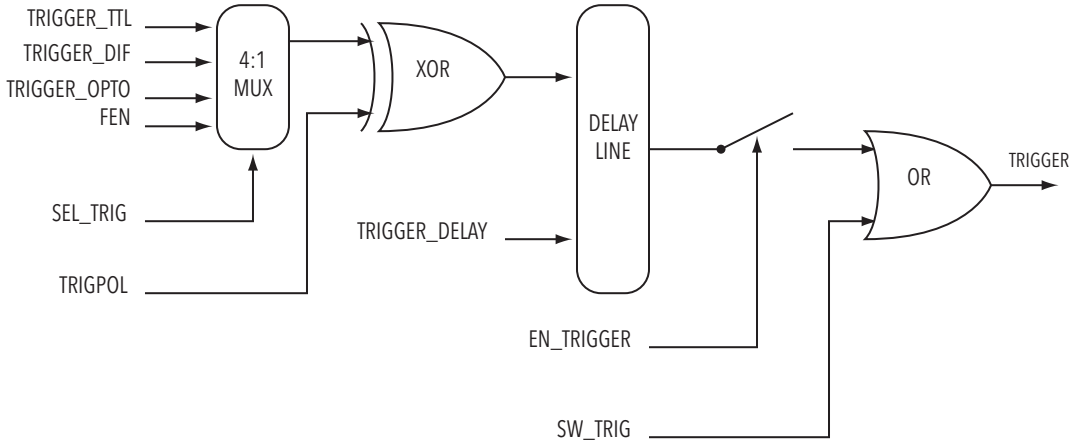


Figure 1-14 Trigger Circuit

1.11 Encoder Processing

This section describes how the encoder circuit of the R64 works. The encoder is used to initiate a horizontal operation (for example, capturing one line). There are three possible external hardware inputs to the encoder circuit and a software input. The selected external encoder can be divided by the value in the ENC_DIV register. Figure 1-15 illustrates the encoder circuit.

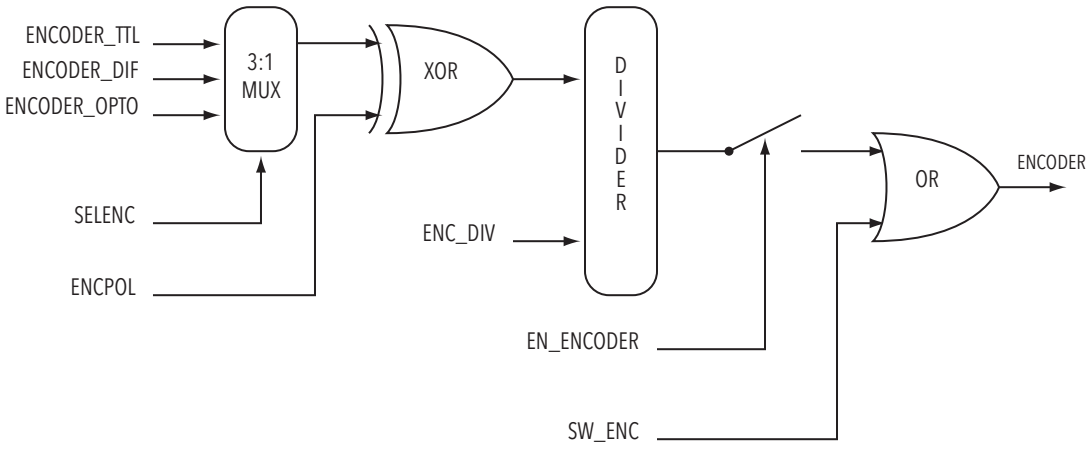


Figure 1-15 Encoder Circuit

1.12 The On-Board Signal Generator

On the R64 there is an on-board free running signal generator. This signal can be steered to the GPOUTs and/or to the camera CCs. This provides an additional tool for synchronization, triggering and camera control. The output of this generator is programmable. Figure 1-16 shows a block diagram of the generator.

The clock driving the generator is derived from the on-board clock. The frequency is controlled by CFREQ in CON0. The selected clock frequency can be optionally scaled down by 8192, depending on the SCALE_BY8K bit in CON18. The rate of the signal generator is set by FREE_RUN_RATE in CON17. The CLOCK_IN will be divided by the number programmed in FREE_RUN_RATE .

Register FREE_RUN_HI in CON17 defines the amount of CLOCK_INs that the signal will be high in a period. The purpose of this register is to be able to control the duty cycle (pulse width) of the signal generator independent of the frequency.

The output of the generator can be optionally inverted by the SIG_GEN_POL bit in CON18.

Let's look at an example. Assume we want to generate a signal 35 milliseconds wide at a rate of 2Hz. You would then program the signal generator as follows.

Set CFREQ = 5. This will program the clock generator to 30Mhz.

Set SCALE_BY8K = 1. This will divide the 30Mhz by 8K, yielding a CLOCK_IN of 3662.1Hz.

Set FREE_RUN_RATE = 1831 (3662/2). This will produce the 2Hz rate.

Set FREE_RUN_HI = 128 (3662.1x0.035 = 128.1). This will produce a pulse 0.035 seconds wide.

Set SIG_GEN_POL = 0. The output needed is active high.

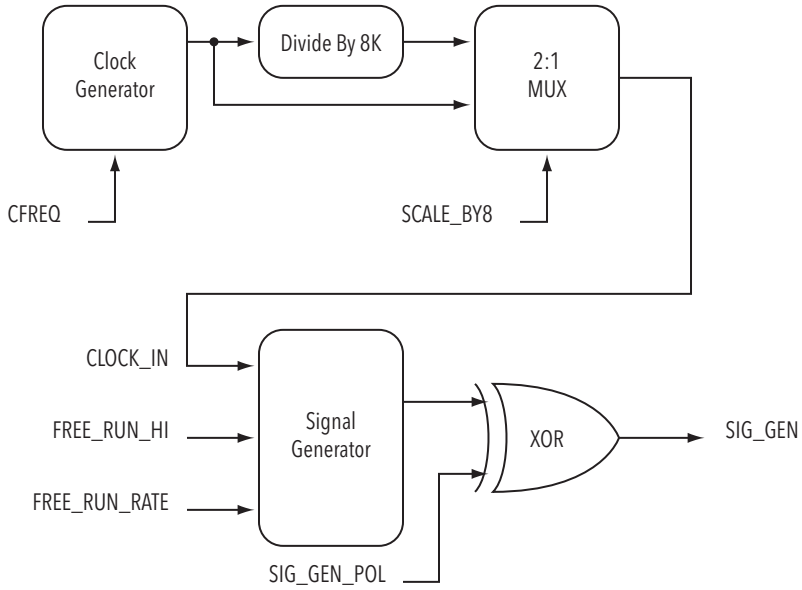


Figure 1-16 R64 Signal Generator

Register and Memory Mapping

Chapter 2

2.1 Introduction

This section explains how the registers and the various chunks of memory are mapped and accessed on the R64.

2.2 Memory Types

2.2.1 Registers

All registers are 64 bits wide and on 64-bit boundary. With the exception of the DPM, only data bits 31 to 0 are used, bits 63 to 32 are always “don't care”. The DPM uses all 64 bits. Out of the lower 32 LSBs, some registers use only a portion of the bits. Registers can also be accessed as 32 bit wide. Little endian addressing is used, i.e. MSB is bits 63-56.

For structure of the QL5064 register see QL documentation.

Note: There is no access to the QL5064 from the local bus

2.2.2 UART

The UART is 8 bit wide and its registers are on 64-bit boundary.

2.2.3 DPM

The DPM is 64 bit wide. The DPM can be accessed as 64-bit (on 64-bit boundary) or as 32-bit wide (on 32-bit boundary) memory. During acquisition (GRAB/SNAP), the slave read from DPM is inhibited. In this case, data read will be always zero.

2.2.4 TAG

At the start and the end of every frame there is an 8-byte long TAG quad. The source address of the TAG is irrelevant as there is no data read. The destination is a special trash can section of memory. The lower 4 bytes transferred are 13131313h. The upper four bytes are undefined.

2.2.5 CTABs

For host access, the CTABs are on 64-bit boundaries. Access is simultaneous to both the HCTAB and the VCTAB. The HCTAB is mapped on data bits 7 to 0; the VCTAB is mapped on data bits 15 to 8. The VCTAB address is 17 bits, AD, i.e. 128K locations. The HCTAB address is 15 bits, AD. The CTAB can be accessed only as 64 bit wide, i.e. there is no provision for accessing less than 64 bits.

2.3 Memory Map

The following table illustrates the physical location of the various sections of memory on the R64.

Memory	Bytes used	Address (hex)	Part	Comment
CON0	nnnnnnyy	00 80 00 00	3K	download, clock control
CON1	nnnnyyyy	00 00 00 00	DCC	
CON2	nnnnyyyy	00 02 00 00	DCC	
CON3	nnnnyyyy	00 04 00 00	DCC	
CON4	nnnnyyyy	00 06 00 00	DCC	
CON5	nnnnyyyy	00 08 00 00	DCC	
CON6	nnnnyyyy	00 0A 00 00	DCC	
CON7	nnnnyyyy	00 0C 00 00	DCC	
CON8	nnnnyyyy	00 0E 00 00	DCC	
CON9	nnnnyyyy	00 10 00 00	MUX	
CON10	nnnnyyyy	00 10 00 08	MUX	
CON11	nnnnyyyy	00 10 00 10	MUX	
CON12	nnnnyyyy	00 10 00 18	MUX	
CON13	nnnnyyyy	00 10 00 20	MUX	
CON14	nnnnyyyy	00 10 00 28	MUX	
CON15	nnnnyyyy	00 00 00 08	DCC	
CON16	nnnnyyyy	00 00 00 10	DCC	
CON17	nnnnyyyy	00 00 00 18	DCC	
CON18	nnnnyyyy	00 00 00 20	DCC	
CON19	nnnnyyyy	00 00 00 28	DCC	
CON20	nnnnyyyy	00 10 00 30	MUX	
CON21	nnnnyyyy	00 10 00 38	MUX	Board version dependent
CON22	nnnnyyyy	00 00 00 30	DCC	
CON23	nnnnyyyy	00 00 00 38	DCC	Board version dependent
CON24	nnnnyyyy	00 10 00 40	MUX	Board version dependent
CON25	nnnnyyyy	00 10 00 48	MUX	
CON26	nnnnyyyy	00 00 00 40	DCC	
CON27	nnnnyyyy	00 00 00 48	DCC	
CTABS	nnnnnnyy	00 20 00 00		ADD select 128K addresses
DPM	yyyyyyyy	00 50 00 00		ADD select 16K addresses for a 128K DPM
UART	nnnnnnny	00 70 00 00		8 internal 8-bit registers on 64 bit boundary
RO_ INFOHI	nnnnnnyy	00 80 00 08	3K	R/O info, model/rev, etc.
RO_ INFOLO	nnnnnnyy	00 80 00 10	3K	R/O info

The following pertains to the table above.

Bytes used in the 64 bit word: n - not used, y - used

All registers are treated as 64 bit wide. The R64 uses two BARs for PCI access:

BAR0, memory mapped, 1M size, is used for access to QL5064 internal registers.

BAR1, memory mapped, 16M size, is used for access to R64 registers, CTABs, DPM.

The R64 uses address lines 23 to 3. Pre-fetch and posting WRITEs are disabled for both BARs

2.4 Downloading Firmware

Firmware is downloaded using the tiny interface. The selection between the 'Tiny' interface (for download) and the full interface will be done on-the-fly according to the destination address.

The mechanics of the download (assertion of CLOCK, DATA, CONFIG etc..) is beyond the scope of this manual.

There are only two FPGAs to download: MUX and DCC. The MUX is downloaded first. Different types of firmware types can be downloaded for different applications. The board has been designed to handle different size gate arrays if needed.

2.5 PCI Configuration Space and Model/Revision Information

All R64 boards will have the same device ID. Information about different models and board capabilities will be stored in the INFO_HI and INFO_LO registers.

2.6 Scatter Gather DMA Instructions

The DMA engine is run by Scatter Gather DMA instructions. These called “quads” because they consist of four words. A list of instructions are called a Quad Table or QTAB. The entries in the quads are 64 bit wide, see QL manual. Each quad has four entries:

1. PCI address
2. User defined; that will be the DPM address
3. Transfer counter and control signals (direction, EOC, etc.)
4. Next descriptor address.

The following sections document the structure of the DMA QUADS.

2.7 PCI Address Quad

Bit	Name	Bit	Name
0	PCI Address LSB	32	PCI Address
1	PCI Address	33	PCI Address
2	PCI Address	34	PCI Address
3	PCI Address	35	PCI Address
4	PCI Address	36	PCI Address
5	PCI Address	37	PCI Address
6	PCI Address	38	PCI Address
7	PCI Address	39	PCI Address
8	PCI Address	40	PCI Address
9	PCI Address	41	PCI Address
10	PCI Address	42	PCI Address
11	PCI Address	43	PCI Address
12	PCI Address	44	PCI Address
13	PCI Address	45	PCI Address
14	PCI Address	46	PCI Address
15	PCI Address	47	PCI Address
16	PCI Address	48	PCI Address
17	PCI Address	49	PCI Address
18	PCI Address	50	PCI Address
19	PCI Address	51	PCI Address
20	PCI Address	52	PCI Address
21	PCI Address	53	PCI Address
22	PCI Address	54	PCI Address
23	PCI Address	55	PCI Address
24	PCI Address	56	PCI Address
25	PCI Address	57	PCI Address
26	PCI Address	58	PCI Address
27	PCI Address	59	PCI Address
28	PCI Address	60	PCI Address
29	PCI Address	61	PCI Address
30	PCI Address	62	PCI Address
31	PCI Address	63	PCI Address MSB

2.8 User Defined Quad

Bit	Name	Bit	Name
0	SOURCE_AD	32	User Defined
1	SOURCE_AD	33	User Defined
2	SOURCE_AD	34	User Defined
3	SOURCE_AD	35	User Defined
4	SOURCE_AD	36	User Defined
5	SOURCE_AD	37	User Defined
6	SOURCE_AD	38	User Defined
7	SOURCE_AD	39	User Defined
8	SOURCE_AD	40	User Defined
9	SOURCE_AD	41	User Defined
10	SOURCE_AD	42	User Defined
11	SOURCE_AD	43	User Defined
12	SOURCE_AD	44	User Defined
13	SOURCE_AD	45	User Defined
14	SOURCE_AD	46	User Defined
15	TAG	47	User Defined
16	QUAD_INFO	48	User Defined
17	QUAD_INFO	49	User Defined
18	QUAD_INFO	50	User Defined
19	QUAD_INFO	51	User Defined
20	QUAD_INFO	52	User Defined
21	QUAD_INFO	53	User Defined
22	QUAD_INFO	54	User Defined
23	QUAD_INFO	55	User Defined
24	QUAD_INFO	56	User Defined
25	QUAD_INFO	57	User Defined
26	QUAD_INFO	58	User Defined
27	QUAD_INFO	59	User Defined
28	QUAD_INFO	60	User Defined
29	QUAD_INFO	61	User Defined
30	QUAD_INFO	62	User Defined
31	QUAD_INFO	63	User Defined

2.9 Transfer Count and Control Quad

Bit	Name	Bit	Name
0	EOC	32	Transfer Count
1	DMA Direction	33	Transfer Count
2	Command	34	Transfer Count
3	64/32-Bit Master	35	Transfer Count
4	Reserved	36	Transfer Count
5	Reserved	37	Transfer Count
6	Reserved	38	Transfer Count
7	Reserved	39	Transfer Count
8	TXC	40	Transfer Count
9	TXC	41	Transfer Count
10	TXC	42	Transfer Count
11	TXC	43	Transfer Count
12	TXC	44	Transfer Count
13	TXC	45	Transfer Count
14	TXC	46	Transfer Count
15	TXC	47	Transfer Count
16	TXC	48	Transfer Count
17	TXC	49	Transfer Count
18	TXC	50	Transfer Count
19	TXC	51	Transfer Count
20	TXC	52	Transfer Count
21	QUAD_INT	53	Transfer Count
22	TAIL_TAG	54	Transfer Count
23	HEAD_TAG	55	Transfer Count
24	TXC_INFO	56	Transfer Count
25	TXC_INFO	57	Transfer Count
26	TXC_INFO	58	Transfer Count
27	TXC_INFO	59	Transfer Count
28	TXC_INFO	60	Transfer Count
29	TXC_INFO	61	Transfer Count
30	TXC_INFO	62	Transfer Count
31	TXC_INFO	63	Transfer Count

2.10 Next Quad Address

Bit	Name	Bit	Name
0	Next Quad Address LSB	32	Next Quad Address
1	Next Quad Address	33	Next Quad Address
2	Next Quad Address	34	Next Quad Address
3	Next Quad Address	35	Next Quad Address
4	Next Quad Address	36	Next Quad Address
5	Next Quad Address	37	Next Quad Address
6	Next Quad Address	38	Next Quad Address
7	Next Quad Address	39	Next Quad Address
8	Next Quad Address	40	Next Quad Address
9	Next Quad Address	41	Next Quad Address
10	Next Quad Address	42	Next Quad Address
11	Next Quad Address	43	Next Quad Address
12	Next Quad Address	44	Next Quad Address
13	Next Quad Address	45	Next Quad Address
14	Next Quad Address	46	Next Quad Address
15	Next Quad Address	47	Next Quad Address
16	Next Quad Address	48	Next Quad Address
17	Next Quad Address	49	Next Quad Address
18	Next Quad Address	50	Next Quad Address
19	Next Quad Address	51	Next Quad Address
20	Next Quad Address	52	Next Quad Address
21	Next Quad Address	53	Next Quad Address
22	Next Quad Address	54	Next Quad Address
23	Next Quad Address	55	Next Quad Address
24	Next Quad Address	56	Next Quad Address
25	Next Quad Address	57	Next Quad Address
26	Next Quad Address	58	Next Quad Address
27	Next Quad Address	59	Next Quad Address
28	Next Quad Address	60	Next Quad Address
29	Next Quad Address	61	Next Quad Address
30	Next Quad Address	62	Next Quad Address
31	Next Quad Address	63	Next Quad Address MSB

Electrical Interfacing

Chapter 3

3.1 Introduction

This chapter describes the electrical interface of the R64. This includes description of all of the connectors on the board, pin-outs for these connectors, and detailed information on the I/O signals. The mechanical layout of the R64-PCI-CL board is shown in Figure 3-1.

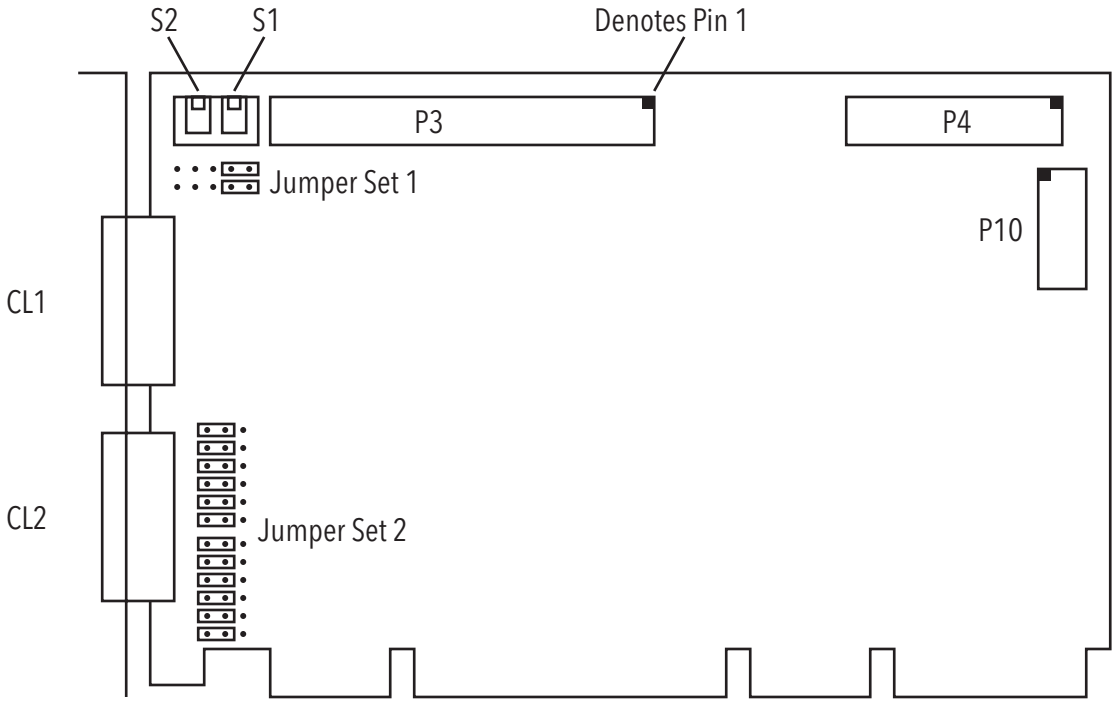


Figure 3-1 R64-PCI-CL Board Layout

The mechanical layout of the R64-PCE-CL is shown in Figure 3-2.

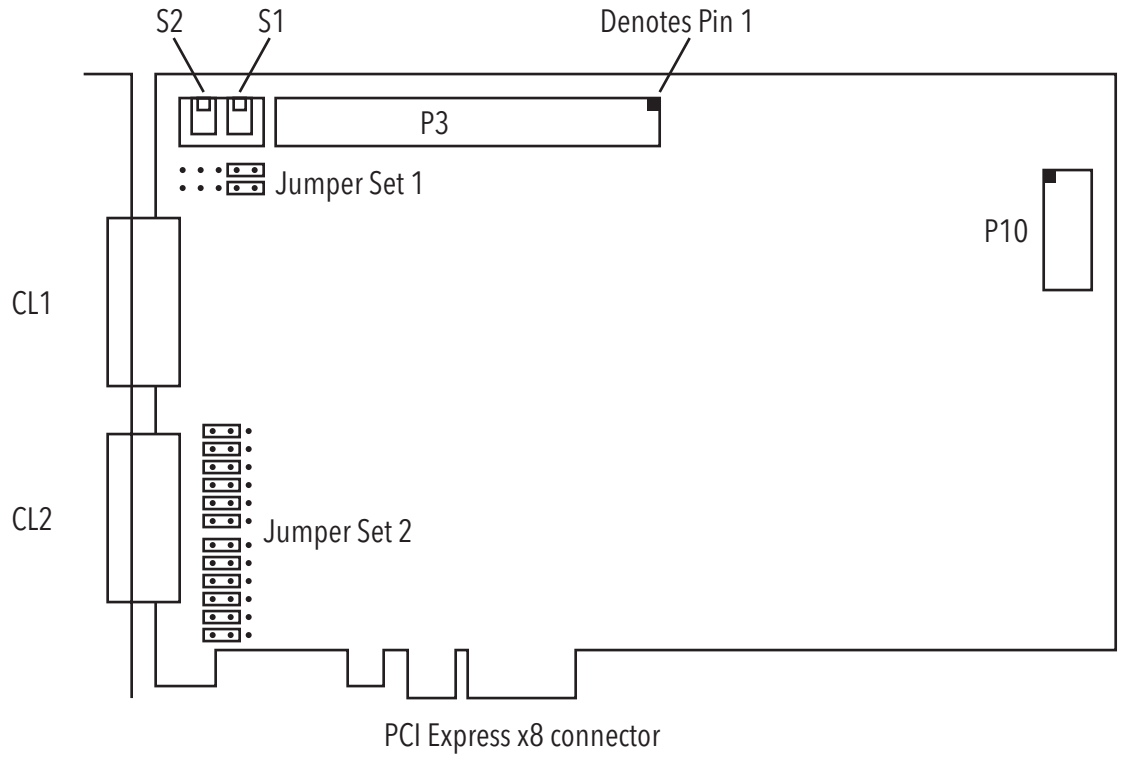


Figure 3-2 R64-PCE-CL Board Layout

3.2 The R64-CL Connectors

There are four connectors on the R64-CL:

CL1 - Camera Link Connector 1
CL2 - Camera Link Connector 2
P3 - I/O Connector
P4 - Test Connector (not mounted on production boards, not on the R64e)
P10 - Diagnostic Connector (not for customer use))

Table 3-1 illustrates how to connect the R64 to various types of Camera Link Cameras.

Table 3-1 CL Connector Configuration

Camera(s) type	CL1	CL2
Base Configuration	Camera's CL1	NC
Medium Configuration	Camera's CL1	Camera's CL2
Full Configuration	Camera's CL1	Camera's CL2
Dual Base	Camera 1	Camera 2

The I/O connector contains a number of general purpose inputs and outputs. The outputs can be used, for example, to control a strobe light or other devices. Some of the inputs have specific functions, for example the Trigger and Encoder, and some are general purpose, for example GPIN0, whose state can be read by software. These signals are described in detail in the following sections.

Figure 3-1 and Figure 3-2 show the locations of these connectors on the R64-CL.

3.3 The R64-CL Jumpers and Switches

On the R64-CL there are four jumper fields and two switches that are user configurable. Figure 3-1 and Figure 3-2 show the locations of these jumpers and switches.

3.3.1 Jumpers

Figure 3-3 shows the detailed structure of the jumpers.

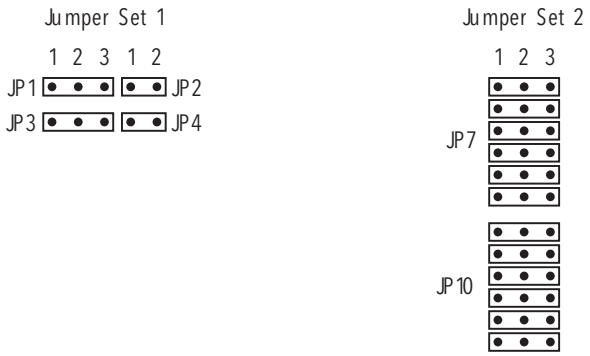


Figure 3-3 R64-CL Jumpers

Jumper fields JP1, JP2, JP3 and JP4 control the configuration of the open collector GPOUT5 and GPOUT6. See Section 3.7.4 on GPOUT5 and GPOUT6 configuration.

Jumper fields JP7 and JP10 are not user configurable. They are set at the factory in conjunction with FLASH programmable logic, when the board is configured as a FULL or DUAL model. The user should not change the factory configuration of JP7 and JP10 as it will result in malfunction of the board. The jumpers setting will disagree with the on-board FLASH logic.

Table 3-2 illustrates the configurations of JP1, JP2, JP3 and JP4. See also Section 3.7.4 on configuration of GPOUT5 and GPOUT6.

Table 3-2 Jumper Set 1

Jumper	Position 1-2	Position 2-3	No Jumper
JP1	5 Volt connected to GPOUT5_VCC through a 220 Ohm resistor	12 Volt connected to GPOUT5_VCC through a 680 Ohm resistor	Power disconnected from GPOUT5_VCC (factory default)
JP2	1K pull-up resistor installed between GPOUT5_OC and GPOUT5_VCC (factory default)	N. A.	No pull-up on GPOUT5
JP3	5 Volt connected to GPOUT6_VCC through a 220 Ohm resistor	12 Volt connected to GPOUT6_VCC through a 680 Ohm resistor	Power disconnected from GPOUT6_VCC (factory default)
JP4	1K pull-up resistor installed between GPOUT6_OC and GPOUT6_VCC (factory default)	N.A.	No pull-up on GPOUT6

Table 3-3 illustrates the factory setting for JP7 and JP10.

Table 3-3 Jumper Set 2

Jumper Field	Position 1-2	Position 2-3
JP7	Full Configuration Cameras	Dual Base and Medium Configuration Cameras
JP10	Full Configuration Cameras	Dual Base and Medium Configuration Cameras

Note: Users should not change the factory setting of JP7 and JP10.

3.3.2 Switches

There is one piano-type switch block on the R64-CL with two switches. These are used to identify individual boards when there is more than one board in a system. The idea is to set the switches differently on each board in the system. The switch settings can

be read for each board from software (by reading the SW bitfield). SysReg also shows the switch setting for each board. See Table 3-4 below shows the switch settings and the corresponding value in the SW bitfield.

Table 3-4 Switch Setting

S1	S2	SW register
down	down	0
down	up	1
up	down	2
up	up	3

3.4 The Camera Link Connector Pinouts (CL1 & CL2)

The pinouts for connectors CL1 and CL2 conform to the Camera Link specification for frame grabbers. This specification is maintained by the Automated Imaging Association. Please contact this organization for a copy of the specification. At the time of this printing, it is available on the web at www.machinevisiononline.org. It is important to understand that some of these signals are the output of a high speed serial converter chip, and cannot be observed by normal instrumentation.

3.5 The I/O Connector Pinout (P3)

The pin-out for the I/O Connector (P3) is illustrated in the following table.

PIN	I/O	Signal	Comment
1	In	TRIGGER+	Differential
2	In	TRIGGER-	Differential
3	In	TRIGGER_TTL	TTL
4	In	TRIGGER_OPTO_K	Cathode of optocoupling sensor
5	In	TRIGGER_OPTO_A	Anode of optocoupling sensor
6		GND	
7	In	ENCODER+	Differential
8	In	ENCODER-	Differential
9	In	ENCODER_TTL	TTL
10	In	ENCODER_OPTO_K	Cathode of optocoupling sensor
11	In	ENCODER_OPTO_A	Anode of optocoupling sensor
12		GND	
13	In	GPIN0_TTL	TTL
14	In	GPIN1_TTL	TTL
15	In	GPIN2+	Differential
16	In	GPIN2-	Differential
17	In	GPIN3+	Differential
18	In	GPIN3-	Differential
19	In	GPIN4+	Differential
20	In	GPIN4-	Differential
21		GND	
22	Out	GPOUT0+	Differential
23	Out	GPOUT0-	Differential
24	Out	GPOUT1+	Differential
25	Out	GPOUT1-	Differential
26	Out	GPOUT2+	Differential
27	Out	GPOUT2-	Differential
28	Out	GPOUT3_TTL	TTL
29	Out	GND	
30	Out	GPOUT4_TTL	TTL
31	Out	GPOUT5_OC	Open Collector driver
32	Out	GPOUT5_VCC	Pull-up or power for the Open Collector driver
33	Out	GPOUT6_OC	Open Collector driver
34	Out	GPOUT6_VCC	Pull-up or power for the Open Collector driver
35		GND	
36		GND	
37		SOUT_RS232	Camera RS232 out
38		GND	
39		SIN_RS232	Camera RS232 in
40		GND	

3.6 The Test Connector Pinout (P4)

All the signals on the test connector are outputs. All signals are buffered by a TTL driver so that they can be viewed on an oscilloscope without the risk of affecting the operation of the board. The main use of this connector if for system debug and diagnostics. The test connector is not normally mounted. However, if required by the customer, the R64 can be delivered with this connector installed. The pinout for this connector is in the following table. The test connector is not available on the R64e.

Pin	Signal	Comment
1	GND	
2	CLK-CL	CLOCK from CL chip X
3	GND	
4	LEN	LEN from CL chip X
5	FEN	FEN from CL chip X
6	VALID	VALID from CL chip X
7	DATA0	DATA0 from CL chip X
8	SPARE	SPARE from CL chip X
9	GND	
10	CC1	CC1 to CL chip X
11	CC2	CC2 to CL chip X
12	CC3	CC3 to CL chip X
13	CC4	CC4 to CL chip X
14	GND	
15	TRIGGER_SELECTED	Replica of the trigger selected by SELTRIG, see CON5
16	H_WIN	Horizontal Acquisition Window
17	GND	
18	ENCODER_ SELECTED	Replica of the encoder selected by SELENC, see CON5
19	V_WIN	Vertical Acquisition Window
20	GND	
21	NOER	READ from FIFO
22	NWRL_A	WRITE to FIFO
23	TEST_PIN_1	Programmable signal from DCC FPGA
24	TEST_PIN_2	Programmable signal from MUX FPGA
25	GND	
26	GND	

3.7 Input and Output Signals

This chapter describes the function and use of the I/O signals on the R64-CL's P3 connector.

3.7.1 Trigger

Trigger Input Types

There are four trigger inputs.

TRIGGER_TTL - Single ended TTL level trigger
TRIGGER_DIFF - Differential (LVDS) trigger
TRIGGER_OPTO - Optocoupled trigger
FEN - The FEN signal on the CL1 connector.

The hardware trigger is enabled/disabled by the bit EN_TRIGGER. Only one input at a time is active (the software trigger bit, SW_TRIG, is always active). The active trigger is selected by the bitfield SEL_TRIG. The current level of these inputs can be read from software by reading the bits RD_TRIG_DIFF, RD_TRIG_TTL, RD_TRIG_OPTO and RD_FEN. The unselected triggers will have no effect on the board. However, they can be used as general purpose inputs.

The Optocoupled Trigger

The opto-coupled trigger allows the R64 to accept a trigger signal without having a galvanic connection to the trigger source. This is mandatory in some medical and industrial application. The trigger information is passed as a light pulse from an on-board LED that is coupled to a receiving phototransistor. The LED and the phototransistor are in the same package, a Sharp PC3H711. Figure 3-4 shows the electrical diagram of the optocoupled trigger circuit and a suggested circuit for the driver. The LED is driven by an open collector driver. The user must supply his +5V power to the LED. Note that there is no galvanic connection between the user's circuit and the R64.

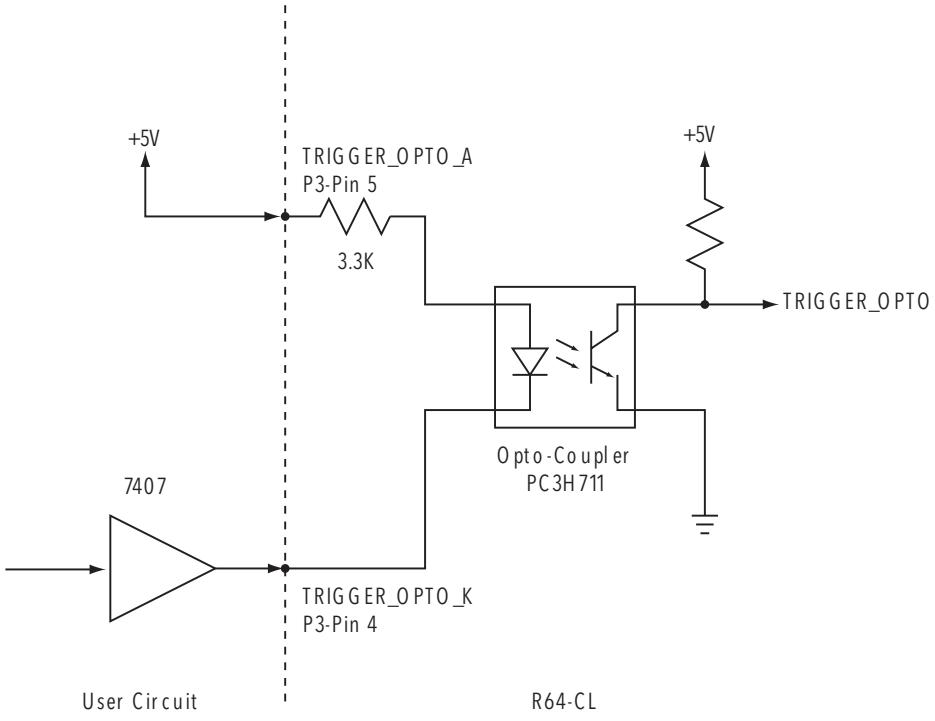


Figure 3-4 Driver Circuit for Opto-Coupled Trigger

3.7.2 Encoder

Encoder Input Types

There are three encoder inputs.

ENCODER_TTL - Single ended TTL level encoder
ENCODER_DIFF - Differential (LVDS) encoder
ENCODER_OPTO - Optocoupled encoder

The hardware encoder is enabled/disabled by the bit EN_ENCODER. Only one input at a time is active (the software encoder bit, SW_ENC, is always active). The active encoder is selected by the bitfield SEL_ENC. The current level of these inputs can be read from software by reading the bits RD_ENC_DIFF, RD_ENC_TTL and RD_ENCO-PTO. The unselected inputs will have no effect on the board. However, they can be used as general purpose inputs.

The Optocoupled Encoder

The opto-coupled encoder allows the R64 to accept an encoder signal without having a galvanic connection to the encoder source. This is mandatory in some medical and industrial application. The encoder information is passed as a light pulse from an on-board LED that is coupled to a receiving phototransistor. The LED and the phototransistor are in the same package, a Sharp PC3H711. Figure 3-5 shows the electrical diagram of the optocoupled encoder circuit and a suggested circuit for the driver. The LED is driven by an open collector driver. The user must supply his +5V power to the LED. Note that there is no galvanic connection between the user's circuit and the R64.

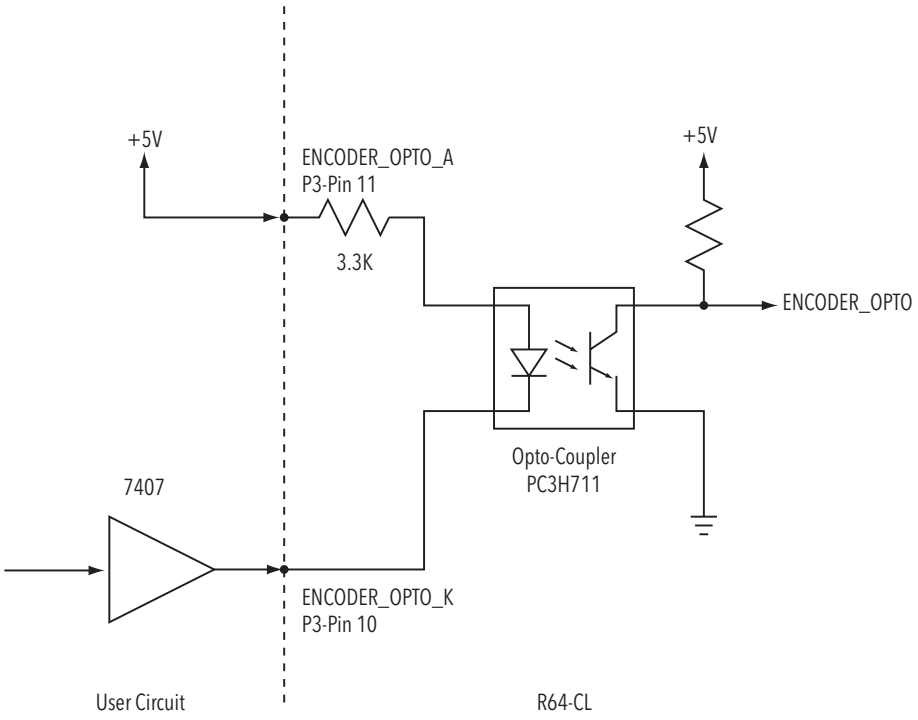


Figure 3-5 Driver Circuit for Opto-Coupled Encoder

3.7.3 General Purpose Inputs (GPIN)

There are five general purpose inputs. The signal level on each input can be read on the corresponding GPIN bit. The electrical characteristic of these inputs is shown in the following list.

GPIN0, GPIN1 - Single ended TTL level inputs
GPIN2, GPIN3, GPIN4 - Differential (LVDS) inputs

3.7.4 General Purpose Outputs (GPOUT)

There are seven general purpose outputs. The signal level on each output is controlled by one of several sources (see below). The electrical characteristic of these outputs is shown in the following list.

GPOUT0, GPOUT1, GPOUT2 - Differential (LVDS) outputs
GPOUT3, GPOUT4 - Single ended TTL level outputs
GPOUT5 - Open collector
GPOUT6 - Open collector

The source for each GPOUT bit is controlled by the corresponding GPOUTx_CON bitfield. These are located in CON8. The source for each GPOUT can be programmed independently of the others. Table 3-5 shows the sources for each GPOUT.

Table 3-5 GPOUTx_CON

GPOUTx_CON	GPOUTx Source
0 (000b)	GPOUTx bit
1 (001b)	CT3 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	CT1 from CTAB
4 (100b)	CT0 from CTAB
5 (101b)	Internally generated clock. Frequency set by CFREQ.
6 (110b)	Free running on board signal generator. Controlled by FREE_RUN_RATE and FREE_RUN_HIGH
7 (111b)	Reserved

The Open Collector Drivers for GPOUT5 and GPOUT6

GPOUT5 and GPOUT6 are open collector drivers. Figure 3-6 shows the GPOUT5 and GPOUT6 driver circuits and their associated jumpers for various configurations. The R64 is shipped in with JP2 in position 1-2, JP4 in position 1-2, no jumpers in JP1 and JP3.

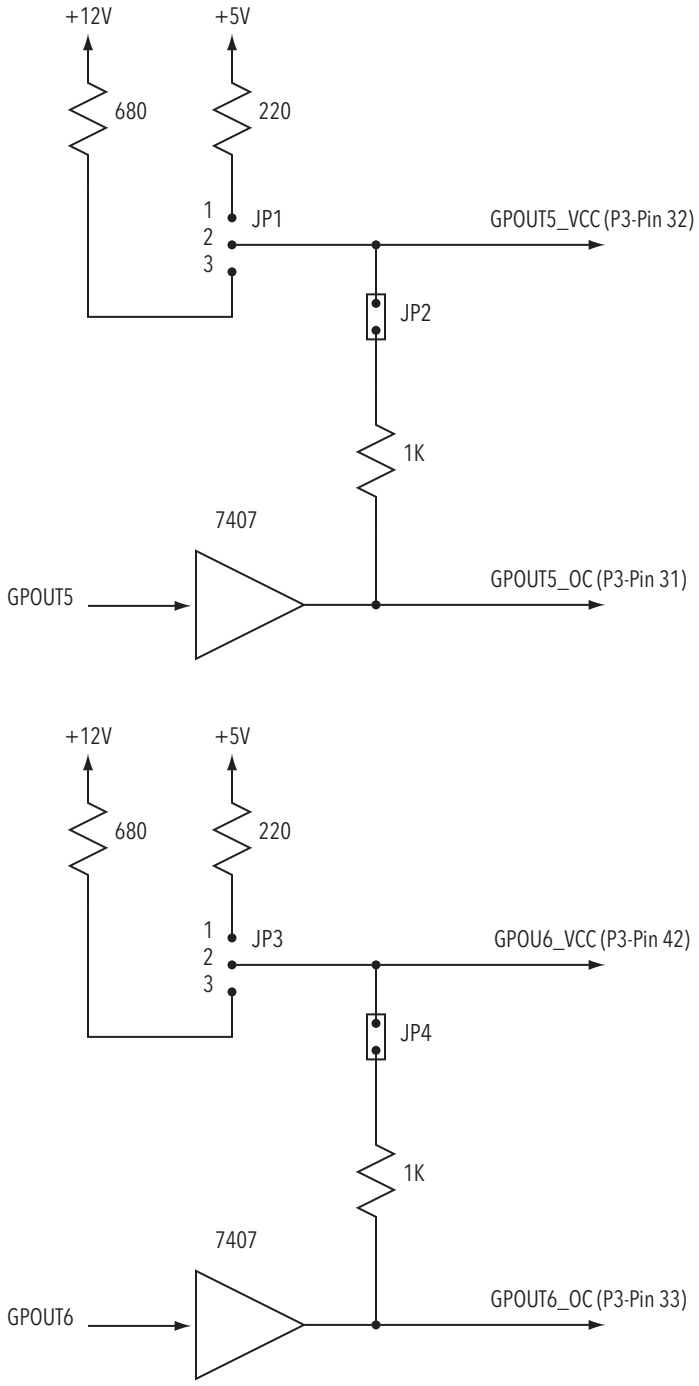


Figure 3-6 Driver Circuits for GPOUT5 and GPOUT6 (R64-CL in Default Configuration)

Figure 3-7 shows how the open collector GPOUT5 in the factory configuration can drive an opto-coupling device. The user must supply the +5V to his LED and the two systems must have their grounds connected. In this configuration the R64 and the user's system must have a common electrical ground.

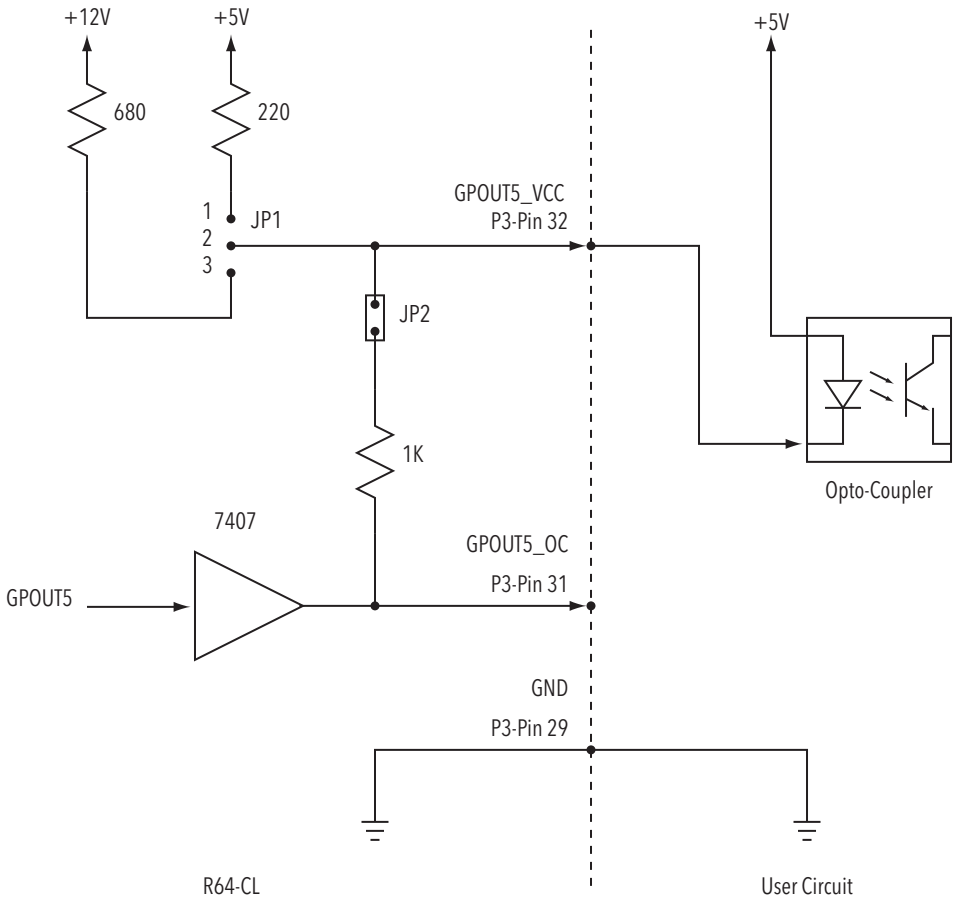


Figure 3-7 GPOUT5 Driving Opto-Coupled Circuit (R64-CL in Default Configuration)

Figure 3-8 shows how the R64's open collector GPOUT5 can drive an user's opto-coupled device configured for galvanic isolation between the R64 and the user. The power to the user's LED is supplied by the R64's 5V through a 220 Ohm resistor. This is achieved by inserting the short in position 1-2 at JP1. The jumper at JP2 is removed. The open collector driver will sink the current from the LED. There is no galvanic connection between the R64 and the user's circuit. Information is passed from the R64 to the user as light, transmitted by the LED and received by the photo-transistor.

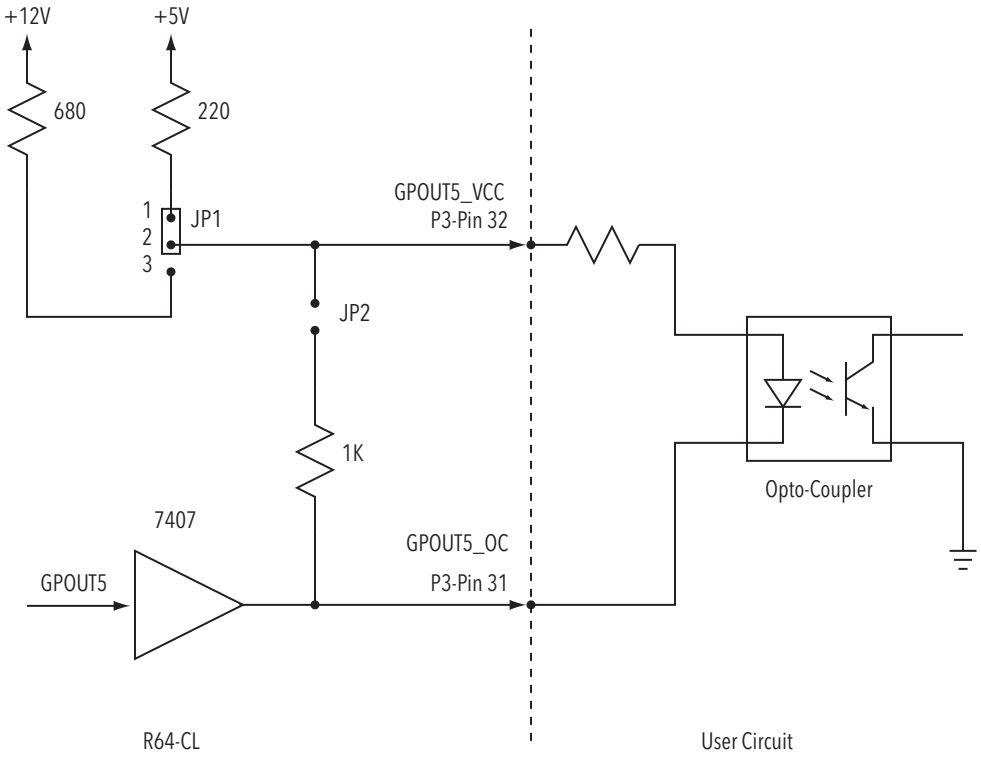


Figure 3-8 GPOUT5 Driving Opto-Coupled Circuit using Galvanic Isolation

3.7.5 Camera Link Controls (CCs)

The Camera Link cable caries four general purpose Camera Control (CC) signals that can be use to control the camera. These are labeled CC1, CC2, CC3, CC4. The source for each CC is controlled by the corresponding CCx_CON bitfield. Table 3-6 illustrates the source for each CCx as a function of its associated CCx_CON bitfield.

Table 3-6 CCx_CON

CCx_CON	CCx Source
0 (000b)	CT0 from CTAB
1 (001b)	CT1 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	Free running on board signal generator. Controlled by FREE_RUN_RATE and FREE_RUN_HIGH

Table 3-6 CCx_CON

CCx_CON	CCx Source
4 (100b)	Internally generated clock. Frequency set by CFREQ.
5 (101b)	GPIN0's signal level
6 (110b)	Forced low
7 (111b)	Forced high

3.7.6 Serial Port (RS232)

The I/O connector also contains the RS232 signals from the camera's serial port. This is the serial port that is contained within the camera link cable. The reason that these signals are made available is so that the R64's UART can be bypassed completely. This is done by connecting these signals to the host PC's serial port via a short RS232 cable. Connecting these signals this way allows camera control software, that does not support the Camera Link serial API, to work with an operating system COM port. These pins are activated by programming the UART_CON bitfield. When the R64 is used in dual base mode (i.e. two base configuration cameras) both camera's serial ports can be made available on these pins. Again, UART_CON is programmed to select the appropriate camera.

System Status

Chapter 4

4.1 Introduction

This chapter describes the system status report that the R64 supplies through its registers. The system status will help the users in setting up their system: the camera, the frame grabber, the cabling, the I/O and the software. The list of the status bits is given in the Table 4-1. If more information is available for a given specification there will be an entry in the column marked "Details". In addition, all of these registers are also described in Register Map chapter of this manual.

Table 4-1 Status Bits

Status Bits	Function and Relationship	Register	Details
AQSTAT	Acquistion status	CON3	Section 1.9
FACTIVE	Acquistion status, vertical active	CON3	Section 4.2
FCOUNT	Acquistion status, 3-bit frames counter	CON3	Section 4.2
LCOUNT	Camera status, LEN is toggling	CON4	Section 4.3
PCOUNT	Camera status, PCLK is toggling	CON4	Section 4.3
FENCOUNT	Camera status, FEN is toggling	CON4	Section 4.3
RD_TRIG_DIFF/TTL/OPTO	Trigger status	CON5	Section 4.4
RD_ENC_DIFF/TTL/OPTO	Encoder status	CON5	Section 4.4
VCOUNT	Acquistion status, VCTAB cycling	CON6	Section 4.5
HCOUNT	Acquistion status, HCTAB cycling	CON6	Section 4.5
LINES_TOGO	Acquistion status, current line in frame	CON19	Section 4.5
FIFO_EQ	Camera status, video value	CON20	Section 4.6
DEST_ADD	DMA running	CON22	Section 4.7

4.2 FACTIVE, FCOUNT

FACTIVE is 1 during the active vertical. It works for both area scan and line scan cameras. For both line scan and area scan cameras there is always a vertical size defined by ALPF.

FCOUNT is a 3-bit frame counter that is incremented by the rising edge of FACTIVE. It can be used to track acquisition, especially in triggered modes. FCOUNT works for both area scan and line scan cameras.

4.3 PCOUNT, LCOUNT, FENCOUNT

Thase three registers give an indication of the status the camera connected to the main connector:

PCOUNT is a 2-bit counter clocked by the camera's PCLK. Reading a constant value from this register indicates that the camera's clock does not reach the R64.

LCOUNT is a 2-bit counter clocked by the camera's LEN. Reading a constant value from this register indicates that the camera's LEN does not reach the R64.

FENCOUNT is a 2-bit counter clocked by the camera's FEN. Reading a constant value from this register indicates that the camera's FEN does not reach the R64.

4.4 RD_TRIG_DIFF/TTL/OPTO, RD_ENC_DIFF/TTL/OPTO

The level of all three trigger and all three encoder inputs can be read. This helps establish connection with external industrial equipment.

4.5 VCOUNT, HCOUNT, LINES_TOGO

These three registers give feedback about the operation of the horizontal and vertical CTABs. VCOUNT is the address counter of the VCTAB. This register indicates the current VCTAB address.

HCOUNT is the 2 LSB of the HCTAB address counter. This register indicates only if the HCTAB is cycling. Reading a constant value on HCOUNT indicates that the HCTAB address is stuck.

LINES_TOGO specifies how more many lines there are till the end of the frame.

4.6 FIFO_EQ

This register gives the 8-bit value of the video from the first eight bits of the main connector. It is helpful to determine if the camera is reacting to light. Convering the camera's lense will yield a low value in this register. Pointing the camera to a light source will yield a high value in this register.

4.7 DEST_ADD

This register gives the DMA destination address. During acquisition, this register should change. Reading a constant value from this register suggests that the DMA operation is not progressing.

Register Map

Chapter 5

5.1 Introduction

This section enumerates all of the bitfields in all of the registers on the R64. All of the registers are 32 bits wide. These wide registers are named CON0, CON1, etc. Each registers is broken into one or more bitfields. Bitfields can be from one to 32 bits wide. Each bitfield controls a specific function on the board.

5.1.1 Bitfield definitions

What follows is an explanation of bitfield definition sections.

BITFIELD R/W, CON0[7..0]

Bitfield explanation.

The definitions is broken into three sections (see Table 5-1).

Table 5-1 Bitfield Sections.

Section	Meaning
Bitfield name	This is the name of the bitfield. This name is use to program this bitfield from software or from within and camera configuration file. When programming bitfields from software using a Peek or Poke function, the bitfield is preceded with "REG_". For example the bitfield CFREQ is referred to in software as REG_CFREQ.
Bitfield details	This section describes how the bitfield is accessed. The first part describes the how the bits can be accessed. For example R/W means the register can be both read and writen. See theTable 5-2 for details.The second part is the wide register that the bitfield is located in. In the example above this bitfield is in CON0. Following the wide register name is a bitfield location description, in hardware engineering format. For example, [7..0], means the bitfield has 8 bits, location in positions 0 to 7.
Bitfield explanation	This section explains the purposed of the bitfield in detail. Usually meaning of every possible value of the bitfield is listed.

Table 5-2 Access Definitions

Access	Meaning
R/W	Bitfield can be read and written.
RO	Bitfield can only be read. Writing to this bit has no effect.
WO	Bitfield can only be written. Reading from this bit will return meaningless values.

5.2 CON0 Register

Bit	Name
0	CFGDATA
1	CFGSTATUS
2	CFGEN
3	CFGDONE
4	CFGCLOCK
5	FW_7MHZ
6	Reserved
7	Reserved
8	CFREQ
9	CFREQ
10	CFREQ
11	Reserved
12	L_CLKCON
13	L_CLKCON
14	SEL_UCLKC_7MHZ
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

CFGDATA R/W, CON0[0]

Used for downloading firmware.

CFGSTATUS R/W, CON0[1]

Used for downloading firmware.

CFGEN R/W, CON0[2]

Used for downloading firmware.

CFGDONE R/W, CON0[3]

Used for downloading firmware.

CFGCLOCK R/W, CON0[4]

Used for downloading firmware.

FW_7MHZ RO, CON0[5]

If this bit is set, then the board has the update Firmware which can program the frequency of the UART clock to 7.3 MHz. If this bit is zero, then the board has the origonal firmware and the UART can only be driver by an 8 MHz clock. See also the bit: SEL_UCLK_7MHz.

CFREQ R/W, CON0[10..8]

These bits control the frequency of the CLOCK generated on-board..

CFREQ	Frequency
0 (000b)	DC
1 (001b)	3.75 MHz
2 (010b)	7.5 MHz
3 (011b)	15 MHz
4 (100b)	24 MHz
5 (101b)	30 MHz
6 (110b)	48 MHz
7 (111b)	60 MHz

L_CLKCON0 R/W, CON0[13..12]

These bits control the local bus clock frequency. For normal operation, this register should always be set for 00. The other codes are for test/diagnostics.

L_CLKCON	Frequency
0 (000b)	60 MHz
1 (001b)	48 MHz
2 (010b)	24 MHz
3 (011b)	Reserved

SEL_UCLK_ 7MHZ R/W, CON0[14]

This bit selects the frequency that is used to driver the UART for serial communications. This functionality is only available on boards with update firmware. The bit FW_ 7MHZ can be used to check the version of the firmware.

SEL_UCLK_ 7MHZ	Frequency
0	8 MHz
1	7.3 MHz

5.3 CON1 Register

Bit	Name
0	VCNT_RLS_ZERO
1	VCNT_RLS_ZERO
2	VCNT_RLS_ZERO
3	VCNT_RST
4	VCNT_RST
5	VCNT_RST
6	VCNT_LD
7	VCNT_LD
8	VCNT_LD
9	VCNT_RLS_STK
10	VCNT_RLS_STK
11	VCNT_RLS_STK
12	ABORT_CON
13	ABORT_CON
14	ABORT_CON
15	NO_VB_WAIT
16	ACQ_CON
17	ACQ_CON
18	ACQ_CON
19	FREEZE_CON
20	FREEZE_CON
21	FREEZE_CON
22	ACQ_SAFETY
23	NO_RULE
24	INT_CTAB
25	INT_OVSTEP
26	INT_HW
27	INT_TRIG
28	INT_SER
29	INT_QUAD
30	INT_TRIGCON
31	INT_TRIGCON

VCNT_RLS_ZERO R/W, CON1[2..0]

This register controls how the Vertical CTAB counter (VCOUNT) is released from zero.

VCNT_RLS_ZERO	Meaning
0 (000b)	Normal operation. VCOUNT does not stick at zero.
1 (001b)	Edge Mode - VCOUNT sticks at zero. VCOUNT is released from zero by the leading edge of the trigger.
2 (010b)	Level Mode - VCOUNT sticks at zero only if the trigger is de-asserted. If trigger is asserted, then VCOUNT does not stick at zero. VCOUNT is released from zero by the leading edge of trigger.
3 (011b)	Reserved.

VCNT_RST R/W, CON1[5..3]

This register controls how the Vertical CTAB counter (VCOUNT) is reset to zero. In all modes the VCOUNT will also be reset by any of the following four signals/events:

The SW_RESET
The ABORT command
The RST_HVCOUNT bit in CON4
VCOUNT reaching a 1 in the VRESET CTAB

VCNT_RST	Meaning
0 (000b)	VCOUNT is reset by the End of Vertical Acquisition Window or by the VRESET column in the VCTAB.
1 (001b)	VCOUNT is reset by the de-assertion of the trigger (triggered termination) or the end of VAW or by the VRESET column in the VCTAB.
2 (010b)	VCOUNT is reset by the VRESET column in the VCTAB.
3 (011b)	VCOUNT is reset by the assertion of FEN or by the VRESET column in the VCTAB.
4 (100b)	VCOUNT is reset by the de-assertion of the trigger, or by the VRESET column in the VCTAB.

VCNT_LD R/W, CON1[8..6]

This registers controls how the Vertical CTAB counter (VCOUNT) is loaded with the 8000h value.

VCNT_LD	Meaning
0 (000b)	No load operation performed.
1 (001b)	VCOUNT is loaded at the assertion of FEN qualified with the ENVLOAD column in the VCTAB.
2 (010b)	VCOUNT is loaded at the assertion of FEN.
3 (011b)	VCOUNT is loaded at the assertion of trigger.

VCNT_RLS_STK R/W, CON1[11..9]

This register controls the stick/release of the VCOUNT to/from address 7ff0h.

VCNT_RLS_STK	Meaning
0	VCOUNT does not stick at 7FF0h.
1	VCOUNT sticks at 7FF0h. It will be released from that address by a LOAD or RESET operation.

ABORT_CON R/W, CON1[14..12]

This register controls the ABORT operation of the Acquisition State Machine.

ABORT_CON	Meaning
0	Acquisition will be aborted by a host command.
1	Acquisition will be aborted by de-assertion of trigger of by a host ABORT command.

NO_VB_WAIT R/W, CON1[15]

This bit has the following properties.

NO_VB_WAIT	Meaning
0	Wait for the Vertical Active Window before executing the Head Tag Quad.
1	Do not wait for the Vertical Active Window for executing the Head Tag Quad.

ACQ_CON R/W, CON1[18..16]

This register controls the execution of the acquisition command.

ACQ_CON	Meaning
0 (000b)	Acquisition is initiated by host writing the command.
1 (001b)	The acquisition command written by host will start executing at assertion of trigger (triggered acquisition).
2 (010b)	While the GRAB command is on, a frame will be acquired at the assertion of trigger.
3 (011b)	Continuous acquisition mode. Host commands are ignored. Data will be acquired continuously as long as the TRIGGER is asserted.

FREEZE_CON R/W, CON1[21..19]

This register controls the FREEZE operation.

FREEZE_CON	Meaning
0 (000b)	FREEZE initiated by host command.
1 (001b)	FREEZE initiated by the Acquisition Counter or by the host command.
2 (010b)	FREEZE initiated by the de-assertion of trigger or by the host command.

ACQ_SAFETY R/W, CON1[22]

Future use

NO_RULE R/W, CON1[23]

Test/diagnostic bit. For normal operation this bit should always be set to 0. When set to 1, the DMA engine will DMA data at maximum speed, regardless of wether the data is valid.

INT_CTAB R/W, CON1[24]

This interrupt will be set by the interrupt bit in the VCTAB or by the host writing to this bit. The interrupt will be enabled if its corresponding mask, ENINT_CTAB, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 1.

INT_CTAB	Meaning
0	No interrupt from CTAB
1	Interrupt from CTAB asserted.

INT_OVSTEP R/W, CON1[25]

This interrupt will be set if an overflow occurred in the FIFO or by the host writing to this bit. The interrupt will be enabled if its corresponding mask, ENINT_OVSTP, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 2.

INT_OVSTP	Meaning
0	No interrupt from overflow
1	Interrupt from overflow asserted.

INT_HW R/W, CON1[26]

This interrupt will be set by a hardware exception, a loss of sync or by the host writing to this bit. The interrupt will be enabled if its corresponding mask, ENINT_HW, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 3.

INT_HW	Meaning
0	No interrupt from HW
1	Interrupt from HW asserted.

INT_TRIG R/W, CON1[27]

This interrupt will be set by a trigger edge or by the host writing to this bit (see register INT_TRIGCON below). The interrupt will be enabled if its corresponding mask, ENINT_TRIG, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 4.

INT_TRIG	Meaning
0	No interrupt from trigger
1	Interrupt from trigger asserted.

INT_SER RO, CON1[18]

This interrupt will be set by the on board UART that implements the serial communication protocol. The interrupt will be enabled if its corresponding mask, ENINT_SER, has been set to 1. This interrupt can be cleared by the host writing to the UART.

INT_SER	Meaning
0	No interrupt from UART
1	Interrupt from UART asserted.

INT_QUAD R/W, CON1[29]

This interrupt will be set by a DMA QUAD or by the host writing to this bit. The interrupt will be enabled if its corresponding mask, ENINT_QUAD, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 5.

INT_QUAD	Meaning
0	No interrupt from QUAD
1	Interrupt from QUAD asserted.

INT_TRIGCON R/W, CON1[31..20]

This register controls the trigger edge that will cause an interrupt:

INT_TRIGCON	Meaning
0 (00b)	reserved
1 (01b)	Assert interrupt on rising edge of trigger.
2 (10b)	Assert interrupt on falling edge of trigger.
3 (11b)	Assert interrupt on both the rising and the falling edge of the trigger.

5.4 CON2 Register

Bit	Name
0	HCNT_RLS_ZERO
1	HCNT_RLS_ZERO
2	HCNT_RLS_ZERO
3	HCNT_RST
4	HCNT_RST
5	HCNT_RST
6	HCNT_LD
7	HCNT_LD
8	HCNT_LD
9	HCNT_RLS_STK
10	HCNT_RLS_STK
11	HCNT_RLS_STK
12	RST_HVCOUNT
13	RST_DPM_ADDR
14	CTABHOLD
15	Reserved
16	CC1_CON
17	CC1_CON
18	CC1_CON
19	CC2_CON
20	CC2_CON
21	CC2_CON
22	CC3_CON
23	CC3_CON
24	CC3_CON
25	CC4_CON
26	CC4_CON
27	CC4_CON
28	CMDWRITE
29	CMDWRITE
30	CMDWRITE
31	QTBSRC

HCNT_RLS_ZERO R/W, CON2[2..0]

This register controls the release of the HCOUNT from zero.

HCNT_RLS_ZERO	Meaning
0	HCOUNT does not stop at 000h.
1	HCOUNT stops at 000h. It will be released by the assertion of the encoder.

HCNT_RST R/W, CON2[5..3]

This register controls the reset of the HCOUNT. In all cases, the HCOUNT will also be reset by any of the following functions:

SW_RESET
RST_HVCOUNT
ABORT command.

HCNT_RST	Meaning
0 (000b)	HCOUNT will be reset by the end of the Horizontal Active Window.
1 (001b)	HCOUNT will be reset by the assertion of FEN or the HRESET from the HCTAB.
2 (010b)	HCOUNT will be reset by the HRESET in the HCTAB.

HCNT_LD R/W, CON2[8..6]

This register controls the loading of the HCOUNT with 2000h.

HCNT_LD	Meaning
0 (000b)	HCOUNT will not be loaded.
1 (001b)	HCOUNT will be loaded by assertion of LEN if the ENHLOAD function in the HCTAB is set to 1.
2 (010b)	HCOUNT will be loaded by assertion of encoder if the ENHLOAD function in the HCTAB is set to 1.

HCNT_RLS_STK R/W, CON2[11..9]

This register controls the HCOUNT sticking at 1FF0h.

HCNT_RLS_STK	Meaning
0	HCOUNT will not stick at 1FF0h.
1	HCOUNT will stick at 1FF0h. It will be released by a load or reset command.

RST_HVCOUNT WO, CON2[12]

This bit has the following properties.

RST_HVCOUNT	Meaning
0	Normal operation for HCOUNT, VCOUNT
1	Reset HCOUNT, VCOUNT..

RST_DPM_ADDR WO, CON2[13]

This bit has the following properties.

RST_DPM_ADDR	Meaning
0	Normal operation for DPM_ADDR
1	Reset DPM_ADDR..

CTABHOLD R/W, CON2[14]

This bit has the following properties.

CTABHOLD	Meaing
0	Normal operation for CTABs
1	Freeze outputs and operation of CTABs..

CCI_CON R/W, CON2[18..16]

This register selects the signal steered to the CC1.

CC1_CON	Signal steered to CC1
0 (000b)	CT0 from CTAB
1 (001b)	CT1 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	Free running signal generated on-board
4 (100b)	On-board generated CLOCK
5 (101b)	GPIN0
6 (110b)	0
7 (111b)	1

CC2_CON R/W, CON2[21..19]

This register selects the signal steered to the CC2.

CC2_CON	Signal steered to CC2
0 (000b)	CT0 from CTAB
1 (001b)	CT1 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	Free running signal generated on-board
4 (100b)	On-board generated CLOCK
5 (101b)	GPIN0
6 (110b)	0
7 (111b)	1

CC3_CON R/W, CON2[24..22]

This register selects the signal steered to the CC3.

CC3_CON	Signal steered to CC3
0 (000b)	CT0 from CTAB
1 (001b)	CT1 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	Free running signal generated on-board
4 (100b)	On-board generated CLOCK
5 (101b)	GPIN0
6 (110b)	0
7 (111b)	1

CC4_CON R/W, CON2[27..25]

This register selects the signal steered to the CC4. Note that this CC control is slightly different than the previous three. CC4 can be controlled by CT3. This changes allows all four CTs to be tied to a CC.

CC4_CON	Signal steered to CC4
0 (000b)	CT0 from CTAB
1 (001b)	CT1 from CTAB
2 (010b)	CT2 from CTAB
3 (011b)	Free running signal generated on-board
4 (100b)	CT3 from CTAB
5 (101b)	GPIN0
6 (110b)	0
7 (111b)	1

CMDWRITE R/W, CON2[30..28]

This registers selects the interrupt bit to be modified by the host. While an interrupt's code is set, that interrupt can not be asserted by its source. It can be modified only by the host. This mechanism allows to perform reliable read-modify-write cycles.

CMDWRITE	Interrupt allowed for host access
0 (000b)	No interrupt can be accessed by host
1 (001b)	INT_CTAB
2 (010b)	INT_OVSTP
3 (011b)	INT_HW
4 (100b)	INT_TRIG
5 (101b)	INT_QTAB
6 (110b)	INT_EOF
7 (111b)	reserved

QTBSRC RO, CON2[31]

Always read back 1.

5.5 CON3 Register

Bit	Name
0	AQCMD
1	AQCMD
2	AQSTAT
3	AQSTAT
4	FACTIVE
5	FCOUNT
6	FCOUNT
7	FCOUNT
8	REV_DCC
9	REV_DCC
10	REV_DCC
11	REV_DCC
12	REV_DCC
13	REV_DCC
14	REV_DCC
15	REV_DCC
16	REV_DCC
17	REV_DCC
18	REV_DCC
19	REV_DCC
20	REV_DCC
21	REV_DCC
22	REV_DCC
23	REV_DCC
24	Reserved
25	GPIN0
26	GPIN1
27	GPIN2
28	GPIN3
29	GPIN4
30	SW
31	SW

AQCMD R/W, CON3[1..0]

This register is the acquisition command to be executed in the next frame.

AQCMD	Meaning
0 (00b)	FREEZE
1 (01b)	ABORT
2 (10b)	SNAP
3 (11b)	GRAB

AQSTAT RO, CON3[3..2]

The AQSTAT register describes the acquisition command currently being executed.

AQSTAT	Meaning
0 (00b)	FREEZE
1 (01b)	ABORT
2 (10b)	SNAP
3 (11b)	GRAB

FACTIVE RO, CON3[4]

FACTIVE	Meaning
0	Camera outside the Vertical Acquisition Window
1	Camera within the Vertical Acquisition Window

FCOUNT RO, CON3[7..5]

This is a 3-bit modulo-8 counter. The counter is incremented by the start of the Vertical Acquisition Window. It is used as a debug/diagnostic tool.

REV_DCC WO, CON3[23..8]

FW revision.

GPIN0 RO, CON3[25]

TTL general purpose input, from pin 13 of the IO connector. The logical value applied to this pin will be reflected in this register.

GPIN1 RO, CON3[26]

TTL general purpose input, from pin 14 of the IO connector. The logical value applied to this pin will be reflected in this register

GPIN2 RO, CON3[27]

LVDS general purpose input, from pins 15,16 of the IO connector. The logical value applied to those pins will be reflected in this register

GPIN3 RO, CON3[28]

LVDS general purpose input, from pins 17, 18 of the IO connector. The logical value applied to those pins will be reflected in this register

GPIN4 RO, CON3[29]

LVDS general purpose input, from pins 19, 20 of the IO connector. The logical value applied to those pins will be reflected in this register

SW RO, CON3[31..30]

This register reads back the setting of the two mechanical switches installed on the edge of the board. Helps physical identification of up to four boards installed in one PC.

5.6 CON4 Register

Bit	Name
0	ENINT_CTAB
1	ENINT_OVSTEP
2	ENINT_HW
3	ENINT_TRIG
4	ENINT_SER
5	ENINT_QUAD
6	EOF_IN_AQ
7	Reserved
8	Reserved
9	Reserved
10	GPOUT0
11	GPOUT1
12	GPOUT2
13	GPOUT3
14	GPOUT4
15	GPOUT5
16	GPOUT6
17	RST_SER
18	OVS
19	RST_OVS
20	CL_DISABLE
21	LCOUNT
22	LCOUNT
23	PCOUNT
24	PCOUNT
25	FENCOUNT
26	FENCOUNT
27	POP_TOSS
28	PUMP_OFF
29	DMA_BUSY
30	HAW_START
31	VAW_START

ENINT_CTAB R/W, CON4[0]

This bit has the following properties.

ENINT_CTAB	Meaning
0	CTAB interrupt disabled
1	CATB interrupt enabled

ENINT_OVSTEP R/W, CON4[1]

This bit has the following properties.

ENINT_OVSTEP	Meaning
0	OVERSTEP interrupt disabled
1	OVERSTEP interrupt enabled

ENINT_HW R/W, CON4[2]

This bit has the following properties.

ENINT_HW	Meaning
0	HW interrupt disabled
1	HW interrupt enabled

ENINT_TRIG R/W, CON4[3]

This bit has the following properties.

ENINT_TRIG	Meaning
0	Trigger interrupt disabled
1	Trigger interrupt enabled

ENINT_SER R/W, CON4[4]

This bit has the following properties.

ENINT_SER	Meaning
0	UART interrupt disabled
1	UART interrupt enabled

ENINT_QUAD R/W, CON4[5]

This bit has the following properties.

ENINT_QUAD	Meaning
0	QUAD interrupt disabled
1	QUAD interrupt enabled

EOF_IN_AQ R/W, CON4[6]

This bit enables gating the INT_EOF interrupt with acquisition. This functionality makes it easier to write software that relies on the INT_EOF interrupt. Without this functionality, the INT_EOF interrupt would occur continuously based on the camera or trigger's timing, even if the board is not currently acquiring. In this case, the software will have to flush these interrupts out of the queue before starting acquisition. With this functionality enable, interrupts only occur during acquisition..

EOF_IN_AQ	Meaning
0	INT_EOF interrupt will be asserted unconditionally at the end of the frame.
1	INT_EOF interrupt will be asserted at the end of the frame only if the board is acquiring, i.e. only during SNAP/GRAB states.

GPOUT0 R/W, CON4[10]

The value written in this register will be reflected on the differential outputs 22, 23 on the IO connector. See also CON8 for signals steered to the GPOUTs.

GPOUT1 R/W, CON4[11]

The value written in this register will be reflected on the differential outputs 24, 25 on the IO connector. See also CON8 for signals steered to the GPOUTs.

GPOUT2 R/W, CON4[12]

The value written in this register will be reflected on the differential outputs 26, 27 on the IO connector. See also CON8 for signals steered to the GPOUTs.

GPOUT3 R/W, CON4[13]

The value written in this register will be reflected on the TTL output 28 on the IO connector. See also CON8 for signals steered to the GPOUTs.

GPOUT4 R/W, CON4[14]

The value written in this register will be reflected on the TTL output 29 on the IO connector. See also CON8 for signals steered to the GPOUTs

GPOUT5 R/W, CON4[15]

The value written in this register will be reflected on the open collector output 31 on the IO connector. See also CON8 for signals steered to the GPOUTs

GPOUT6 R/W, CON4[16]

The value written in this register will be reflected on the open collector output 33 on the IO connector. See also CON8 for signals steered to the GPOUTs

RST_SER R/W, CON4[17]

This bit has the following properties.

RST_SER	Meaning
0	UART normal operation
1	UART's reset line asserted

OVS RO, CON4[18]

This is a latched overstep bit.

OVS	Meaning
0	No overstep occurred since this bit was cleared
1	At least one overstep occurred since this bit was cleared

RST_OVS R/W, CON4[19]

This bit has the following properties.

RST_OVS	Meaning
0	OVS bit in normal operation
1	OVS bit is reset

CL_DISABLE R/W, CON4[20]

This bit enables/disables the CL chips; used for diagnostics. For normal operation this bit should always be set to 0.

CL_DISABLE	Meaning
0	All CL receivers are enabled.
1	All CL receivers are disabled.

LCOUNT RO, CON4[22..21]

This is a 2-bit counter clocked by the LEN supplied by the Camera Link main connector. Reading this counter and observing changes between reads indicates an active LEN.

PCOUNT RO, CON4[24..23]

This is a 2-bit counter clocked by the PCLK supplied by the Camera Link main connector. Reading this counter and observing changes between reads indicates an active PCLK.

FENCOUNT RO, CON4[26..25]

This is a 2-bit counter clocked by the FEN supplied by the Camera Link main connector. Reading this counter and observing changes between reads indicates an active FEN.

POP_TOSS R/W, CON4[27]

For normal operation this bit should be set to 0. It is used for high-level clean-up.

POP_TOSS	Meaning
0	DMA engine's normal operation.
1	DMA engine flushes the receive FIFO without executing any QUADs.

PUMP_OFF R/W, CON4[28]

For normal operation this bit should be set to 0. It is used for high-level clean-up.

PUMP_OFF	Meaning
0	DMA engine's normal operation.
1	Inhibit DMA operation.

DMA_BUSY RO, CON4[29]

This bit indicates the state of the DMA engine.

DMA_BUYS	Meaning
0	DMA engine is idle.
1	DMA engine is currently DMAing data.

HAW_START R/W, CON4[30]

This bit has the following properties.

HAW_START	Meaning
0	The start of the Horizontal Active Window (HAW) is controlled by the start of the LEN.
1	The start of the Horizontal Active Window is controlled by the HSTART column in the HCTAB.

VAW_START R/W, CON4[31]

This bit has the following properties.

VAW_START	Meaning
0	The start of the Vertical Active Window (VAW) is controlled by the start of the FEN.
1	The start of the Vertical Active Window is controlled by the VSTART column in the VCTAB.

5.7 CON5 Register

Bit	Name
0	SEL_TRIG
1	SEL_TRIG
2	TRIGPOL
3	SW_TRIG
4	SELENC
5	SELENC
6	ENCPOL
7	SW_ENC
8	RD_TRIG_DIFF
9	RD_TRIG_TTL
10	RD_TRIG_OPTO
11	RD_ENC_DIFF
12	RD_ENC_TTL
13	RD_ENC_OPTO
14	TRIGGER_DELAY
15	TRIGGER_DELAY
16	TRIGGER_DELAY
17	TRIGGER_DELAY
18	TRIGGER_DELAY
19	TRIGGER_DELAY
20	TRIGGER_DELAY
21	TRIGGER_DELAY
22	TRIGGER_DELAY
23	TRIGGER_DELAY
24	ENINT_EOF
25	INT_EOF
26	RD_FEN
27	CCSYNC
28	CCSYNC
29	CCSYNC
30	EN_TRIGGER
31	EN_ENCODER

SEL_TRIG R/W, CON5[1..0]

Controls the source of the internal trigger signal.

SEL_TRIG	Meaning
0 (00b)	The trigger used by the board is the differential trigger on the IO connector.
1 (01b)	The trigger used by the board is the TTL trigger on the IO connector.
2 (10b)	The trigger used by the board is the opto-coupled trigger on the IO connector.
3 (11b)	The FEN signal on the CL1 connector will be used as trigger. When this mode is used, the register FENPOL is used to control the polarity of the trigger signal.

TRIGPOL R/W, CON5[2]

This bit has the following properties.

TRIGPOL	Meaning
0	Trigger is asserted on the rising edge.
1	Trigger is asserted on the falling edge.

SW_TRIG R/W, CON5[3]

The SW trigger is OR-ed with the external trigger. The polarity of the SW trigger is always active-HI. TRIGPOL has no effect on the SW trigger.

SW_TRIG	Meaning
0	SW trigger de-asserted.
1	SW trigger asserted.

SELENC R/W, CON5[5..4]

This bitfield has the following properties.

SELENC	Meaning
0 (00b)	The encoder used by the board is the differential encoder on the IO connector.
1 (01b)	The encoder used by the board is the TTL encoder on the IO connector.
2 (10b)	The encoder used by the board is the opto-coupled encoder on the IO connector.
3 (11b)	Reserved

ENCPOL R/W, CON5[6]

This bitfield has the following properties.

ENCPOL	Meaning
0	Encoder is asserted on rising edge.
1	Encoder is asserted on falling edge.

SW_ENC R/W, CON5[7]

The SW encoder is OR-ed with the external encoder. The polarity of the SW encoder is always active-HI. ENCPOL has no effect on the SW encoder

SW_ENC	Meaning
0	SW encoder de-asserted.
1	SW encoder asserted.

RD_TRIG_DIFF RO, CON5[8]

This register reflects the status of the differential trigger input on the IO connector, pins 1,2.

RD_TRIG_TTL RO, CON5[9]

This register reflects the status of the TTL trigger input on the IO connector, pin 3.

RD_TRIG_OPTO RO, CON5[10]

This register reflects the status of the opto-coupled trigger input on the IO connector, pins 4,5.

RD_ENC_DIFF RO, CON5[11]

This register reflects the status of the differential encoder input on the IO connector, pins 7,8.

RD_ENC_TTL RO, CON5[12]

This register reflects the status of the TTL encoder input on the IO connector, pin 9

RD_ENC_OPTO RO, CON5[13]

This register reflects the status of the opto-coupled encoder input on the IO connector, pins 10, 11.

TRIGGER_DELAY R/W, CON5[23..14]

The number N written in this register will delay the trigger by 8N lines.

ENINT_EOF R/W, CON4[24]

This bitfield has the following properties.

ENINT_EOF	Meaning
0	End of frame interrupt disabled.
1	End of frame interrupt enabled.

INT_EOF R/W, CON4[25]

This interrupt will be set by the acquisition state machine at the end of the frame (end of VAW). This ordinarily corresponds to the camera's end of frame. However, if the board is in start-stop triggered mode, this interrupt with also occur when the trigger de-asserts. The host writing a 1 to this bit will also cause and interrupt. The interrupt

will be enabled if its corresponding mask, ENINT_EOF, has been set to 1. This interrupt can be cleared by the host writing a 0 to this location. For the host to be able to write to this location, the CMDWRITE code must be set to 6.

INT_TRIG	Meaning
0	No interrupt from end of frame.
1	Interrupt from end of frame.

RD_FEN RO, CON5[26]

This register reflects the status of the FEN signal on the CL1 connector.

CC_SYNC R/W, CON5[29..26]

This register controls how the CC outputs are synchronized.

CCSYNC	Meaning
0 (000b)	CCs are not synchronized
1 (001b)	CCs are synchronized to the pixel clock of the primary camera
2 (010b)	CCs are synchronized to the pixel clock of the secondary camera
3 (011b)	Each set of CCs are synchronized to the pixel clock of their corresponding camera. In other words, the CCs on the primary connector are synchronized to the primary camera's pixel clock, and the CCs on the secondary camera are synchronized to secondary camera's pixel clock.
4 (100b)	Reserved
5 (101b)	Reserved
6 (110b)	Reserved
7 (111b)	Reserved

EN_TRIGGER R/W, CON5[30]

This bitfield has the following properties.

EN_TRIGGER	Meaning
0	External (HW) selected trigger is disabled.
1	External (HW) selected trigger is enabled.

EN_ENCODER R/W, CON5[31]

This bitfield has the following properties.

EN_ENCODER	Meaning
0	External (HW) selected encoder is disabled.
1	External (HW) selected encoder is enabled.

5.8 CON6 Register

Bit	Name
0	VCOUNT
1	VCOUNT
2	VCOUNT
3	VCOUNT
4	VCOUNT
5	VCOUNT
6	VCOUNT
7	VCOUNT
8	VCOUNT
9	VCOUNT
10	VCOUNT
11	VCOUNT
12	VCOUNT
13	VCOUNT
14	VCOUNT
15	VCOUNT
16	VCOUNT
17	LAL
18	ENC_DIV
19	ENC_DIV
20	ENC_DIV
21	ENC_DIV
22	ENC_DIV
23	ENC_DIV
24	ENC_DIV
25	ENC_DIV
26	ENC_DIV
27	ENC_DIV
28	HCOUNT
29	HCOUNT
30	Reserved
31	Reserved

VCOUNT RO, CON6[16..0]

This is the value of the VCOUNT, the VCTAB's address counter.

LAL R/W, CON6[17]

LAL stands for Last Active Line. It controls the mode the VCOUNT is read.

LAL	Meaning
0	VCOUNT register reflects the current value of the VCOUNT.
1	VCOUNT register holds the last active line of the previous frame.

ENC_DIV R/W, CON6[27..18]

The encoder pulses will be divided down by the number written in this register. If, for example, ENC_DIV[] = 5, for every five pulses on the selected encoder, the divider will supply one pulse to the board. Programming this register to 0 or 1 will both divide by 1.

HCOUNT R/W, CON6[29..28]

This register reflects the current value of the two LSBs of the HCOUNT. Reading this register and observing changes in its value means that the HCOUNT is cycling.

5.9 CON7 Register

Bit	Name
0	AQ_COUNT
1	AQ_COUNT
2	AQ_COUNT
3	AQ_COUNT
4	AQ_COUNT
5	AQ_COUNT
6	AQ_COUNT
7	AQ_COUNT
8	AQ_COUNT
9	AQ_COUNT
10	AQ_COUNT
11	AQ_COUNT
12	AQ_COUNT
13	AQ_COUNT
14	AQ_COUNT
15	AQ_COUNT
16	AQ_COUNT
17	AQ_COUNT
18	AQ_COUNT
19	AQ_COUNT
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	TAG_BANK
25	TAG_BANK
26	TAG_BANK
27	TAG_BANK
28	TAG_BANK
29	TAG_BANK
30	Reserved
31	Reserved

AQ_COUNT R/W, CON7[19..0]

The number N written in this register is used to tell the acquisition logic to FREEZE acquisition after N frames have been acquired. The register FREEZE_CON code must be set to 1.

TAG_BANK RO, CON7[29..24]

This is the calculated bank from the address generator latched by the TAG QUAD; diagnostics/test register.

5.10 CON8 Register

Bit	Name
0	GPOUT0_CON
1	GPOUT0_CON
2	GPOUT0_CON
3	GPOUT1_CON
4	GPOUT1_CON
5	GPOUT1_CON
6	GPOUT2_CON
7	GPOUT2_CON
8	GPOUT2_CON
9	GPOUT3_CON
10	GPOUT3_CON
11	GPOUT3_CON
12	GPOUT4_CON
13	GPOUT4_CON
14	GPOUT4_CON
15	GPOUT5_CON
16	GPOUT5_CON
17	GPOUT5_CON
18	GPOUT6_CON
19	GPOUT6_CON
20	GPOUT6_CON
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

GPOUT0_CON R/W, CON8[2..0]

This register selects the signal steered to GPOUT0 on the IO connector

GPOUT0_CON	Selected signal steered to GPOUT0
0 (000b)	GPOUT0 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT1_CON R/W, CON8[5..3]

This register selects the signal steered to GPOUT1 on the IO connector

GPOUT1_CON	Selected signal steered to GPOUT1
0 (000b)	GPOUT1 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT2_CON R/W, CON8[8..6]

This register selects the signal steered to GPOUT2 on the IO connector

GPOUT2_CON	Selected signal steered to GPOUT2
0 (000b)	GPOUT2 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT3_CON R/W, CON8[11..9]

This register selects the signal steered to GPOUT3 on the IO connector

GPOUT3_CON	Selected signal steered to GPOUT3
0 (000b)	GPOUT3 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT4_CON R/W, CON8[14..12]

This register selects the signal steered to GPOUT4 on the IO connector

GPOUT4_CON	Selected signal steered to GPOUT4
0 (000b)	GPOUT4 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT5_CON R/W, CON8[17..15]

This register selects the signal steered to GPOUT5 on the IO connector

GPOUT5_CON	Selected signal steered to GPOUT5
0 (000b)	GPOUT5 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

GPOUT6_CON R/W, CON8[20..18]

This register selects the signal steered to GPOUT6 on the IO connector

GPOUT6_CON	Selected signal steered to GPOUT6
0 (000b)	GPOUT6 bit written by host in CON4
1 (001b)	CT0 from CTAB.
2 (010b)	CT1 from CTAB.
3 (011b)	CT2 from CTAB.
4 (100b)	CT3 from CTAB.
5 (101b)	Internally generated CLOCK (frequency controlled by CFREQ in CON1).
6 (110b)	Internally generated signal (frequency and duty-cycle controlled by CON17).
7 (111b)	reserved.

5.11 CON9 Register

Bit	Name
0	MUX_REV
1	MUX_REV
2	MUX_REV
3	MUX_REV
4	MUX_REV
5	MUX_REV
6	MUX_REV
7	MUX_REV
8	MUX_REV
9	MUX_REV
10	MUX_REV
11	MUX_REV
12	TRIM
13	TRIM
14	TRIM
15	TRIM
16	FW_TYPE
17	FW_TYPE
18	FW_TYPE
19	FW_TYPE
20	DISPLAY
21	CLIP
22	SHORT_FRAME
23	RST_CALC_BANK
24	CALC_BANK
25	CALC_BANK
26	CALC_BANK
27	CALC_BANK
28	CALC_BANK
29	CALC_BANK
30	ACPL_MUL
31	ACPL_MUL

MUX_REV RO, CON9[11..0]

Firmware revision.

TRIM R/W, CON9[15..12]

This bit field will delay the LEN relative to the video. The delay, in units of pixels, equals the number programmed in the TRIM[] field.

The net effect for a simple, one tap camera will be a shifting to the left of the displayed image. For multi-tap cameras the visual effect is more complex and depends on the CCD architecture.

The purpose of this bit field is to align the image presented by the different taps. This bit field has the opposite effect of the DELAY field in CON14.

TRIM	Meaning
0 (000b)	LEN is not delayed
1 (001b)	LEN is delayed by 1 clocks
2 (010b)	LEN is delayed by 2 clocks
3 (011b)	LEN is delayed by 3 clocks
4 (100b)	LEN is delayed by 4 clocks
5 (101b)	LEN is delayed by 5 clocks
6 (11ob)	LEN is delayed by 6 clocks
7 (111b)	LEN is delayed by 7 clocks

FW_TYPE RO, CON9[19..16]

Firmware type.

DISPLAY R/W, CON9[20]

This bit controls the acquisition of data that is more than 8 bits/pixel. When this bit is set, only the 8 LSB of the data will be acquired in each lane. To be able to display the 8 MSB (or any other consecutive group of 8 bits), the data must be shifted accordingly with the barrel shifter. For 9 to 16-bit cameras, setting this bit will result in an 8-bit dis-

playable pixel. For high bit depth color cameras, setting this bit will result in a 24-bit color displayable pixel. In both cases. the barrel shifter must be set correctly to get the displayable bits out of the incoming pixels.

DISPLAY	Meaning
0	Acquire full bit depth.
1	Acquire 8 LSBs of each data lane.

CLIP R/W, CON9[21]

This bit will clip the upper and lower 15 gray levels. This is useful for displaying gray level images on VGA monitors set in 256 colors mode. The upper and lower 15 gray levels are dedicated to Windows graphics.

CLIP	Meaning
0	Acquire data as is.
1	Clip upper and lower 15 gray levels to 240 and 15 respectively.

SHORT_FRAME R/W, CON9[22]

Future use.

RST_CALC_ BANK R/W, CON9[23]

For normal operation this bit should be 0.

RST_CALC_BANK	Meaning
0	Normal operation
1	Reset the calculated starting bank.

CALC_BANK RO, CON9[29..24]

Value of the current calculated starting bank.

ACPL_MUL R/W, CON9[31..30]

This register is used to increase the maximum line size the R64 can acquire. The settings act as muliplier for the ACPL (Active Clocks Per Line) register.

ACPL_MUL	Meaning
0 (00b)	Normal operation. ACPL is used as is
1 (01b)	ACPL is multiplied by 2
2 (10b)	Reserved
3 (11b)	Reserved

5.12 CON10 Register

Bit	Name
0	ACPL
1	ACPL
2	ACPL
3	ACPL
4	ACPL
5	ACPL
6	ACPL
7	ACPL
8	ACPL
9	ACPL
10	ACPL
11	ACPL
12	ACPL
13	ACPL
14	ACPL
15	ACPL
16	ACPL
17	FORMAT
18	FORMAT
19	FORMAT
20	FORMAT
21	FORMAT
22	VID_SOURCE
23	VID_SOURCE
24	VID_SOURCE
25	VID_SOURCE
26	PIX_DEPTH
27	PIX_DEPTH
28	PIX_DEPTH
29	PIX_DEPTH
30	PIX_DEPTH
31	FORCE_8BIT

ACPL R/W, CON10[16..0]

This register defines the Active Clocks Per Line of the horizontal acquisition window. Let's assume for example a single tap camera with 2K pixels per line. If we want to acquire 400 pixels per line, the ACLP will be programmed to 400. For a 2-tap odd-even pixels camera, with 2K pixels per line, to acquire 400 pixels the ACLP will be programmed with the value 200, as for every clock the camera supplies two pixels.

FORMAT RO, CON10[21..17]

This register defines the camera(s) format in terms of taps and scanning architecture. For every FORMAT there is an associated firmware that is downloaded in the FPGAs. The firmware is identified in the camera file by the FORMAT.

FORMAT	Firmware Name	Format Description
0 (00000b)	MUX	1 tap cameras
1 (00001b)	MUX_2TOEP	2 taps, odd-even pixels
2 (00010b)	MUX_2TOEL	2 taps, odd-even lines
3 (00011b)	MUX_2TS	2 taps, segmented
4 (00100b)	MUX_2TS1RI	2 taps, segmented, right inverted
5 (00101b)	MUX_4TS	4 taps, segmented
6 (00110b)	MUX_4T2S2RIOEP	4 taps, odd-even pixels, right taps inverted
7 (00111b)	MUX_4TQ2RI2BU	4 quads, right quads inverted, bottom quads upside down
8 (01000b)	MUX_2CAM	2 cameras: 1 tap each
9 (01001b)	MUX_2CAM_2TOEP	2 cameras: 2 taps, odd-even pixels
10 (01010b)	MUX_2CAM_2TS1RI	2 cameras: 2 taps, segmented, right-inverted
11 (01011b)	MUX_2CAM_2TS	2 cameras: 2 taps, segmented
12 (01100b)	MUX_2CAM_2TOEL	2 cameras: 2 taps, odd-even lines
13 (01101b)	MUX_8TS	8 taps, segmented
14 (01110b)	MUX_BAY	Bayer decoder, 1 tap 8 bit
15 (01111b)	MUX_BAY_OE	Bayer decoder, 2 taps, odd-even pixels
16 (10000b)	MUX_BAY_2TS	Bayer decoder, 2 taps, segmented
17 (10001b)	MUX_4WI	4 taps, 4-way interleaved

FORMAT	Firmware Name	Format Description
18 (10010b)	MUX_2TOEPI	2 taps, odd-even pixels, both inverted
19 (10011b)	MUX_1TI	1 tap, inverted
20 (10100b)	MUX_8WI	8 taps, 8-way interleaved
21 (10101b)	MUX_BAY_2TS_RI	Bayer decoder, 2 taps, segmented, right inverted

VID_SOURCE R/W, CON10[25..22]

This register defines the video source and the pattern for the synthetic video. The synthetic patterns appear on all 8 taps, except for code 9.

VID_SOURCE	Video source
0 (0000b)	Camera
1 (0001b)	Camera, special mode for cameras that do not assert the VALID signal.
2 (0010b)	reserved
3 (0011b)	Synthetic horizontal static wedge
4 (0100b)	Synthetic dynamic wedge
5 (0101b)	Synthetic 00h
6 (0110b)	Synthetic FFh
7 (0111b)	Synthetic AAh
8 (1000b)	Synthetic 55h
9 (1001b)	Synthetic ABCDEF0123456789h
10 (1010b)	Synthetic vertical static wedge

PIX_DEPTH R/W, CON10[30..26]

This register defines the pixel depth as well as the color order and packing mode for RGB cameras.

PIX_DEPTH	Bit/pixel, color order and packing
0 (0000b)	8 bits
1 (0001b)	10 bits
2 (0010b)	12 bits
3 (0011b)	14 bits

PIX_DEPTH	Bit/pixel, color order and packing
4 (0100b)	16 bits
5 (0101b)	3x8 bits BGR, DMAed as 32 bits, upper MSB set to 00h
6 (0110b)	3x8 bits BGR, DMAed as 24 bits (packed)
7 (0111b)	3x10 bits RGB, DMAed as 32 bits, display mode is 24 bits
8 (1000b)	3x12 bits RGB, DMAed as 48 bits (packed), display mode is 24 bits
9 (1001b)	32 bits
10 (1010b)	64 bits
11 (1011b)	3x8 bits RGB, DMAed as 32 bits, upper MSB set to 00h
12 (1100b)	3x8 bits RGB, DMAed as 24 bits (packed)
13 (1101b)	3x10 BGR, DMAed as 32 bits, display mode is 24 bits
14 (1110b)	3x12 BGR, DMAed as 48 bits (packed), display mode is 24 bits

FORCE_8BIT R/W, CON10[31]

This bitfield has the following properties.

FORCE_8BIT	Meaning
0 (000b)	Normal operation
1 (001b)	Only 8 LSB of pixel will be acquired

5.13 CON11 Register

Bit	Name
0	ALAST_ADD
1	ALAST_ADD
2	ALAST_ADD
3	ALAST_ADD
4	ALAST_ADD
5	ALAST_ADD
6	ALAST_ADD
7	ALAST_ADD
8	ALAST_ADD
9	ALAST_ADD
10	ALAST_ADD
11	ALAST_ADD
12	ALAST_ADD
13	ALAST_ADD
14	ALAST_ADD
15	Reserved
16	BLAST_ADD
17	BLAST_ADD
18	BLAST_ADD
19	BLAST_ADD
20	BLAST_ADD
21	BLAST_ADD
22	BLAST_ADD
23	BLAST_ADD
24	BLAST_ADD
25	BLAST_ADD
26	BLAST_ADD
27	BLAST_ADD
28	BLAST_ADD
29	BLAST_ADD
30	BLAST_ADD
31	Reserved

ALAST_ADD RO, CON11[14..0]

Last address for lane A (used for diagnostics).

BLAST_ADD RO, CON11[30..16]

Last address for lane B (used for diagnostics).

5.14 CON12 Register

Bit	Name
0	CLAST_ADD
1	CLAST_ADD
2	CLAST_ADD
3	CLAST_ADD
4	CLAST_ADD
5	CLAST_ADD
6	CLAST_ADD
7	CLAST_ADD
8	CLAST_ADD
9	CLAST_ADD
10	CLAST_ADD
11	CLAST_ADD
12	CLAST_ADD
13	CLAST_ADD
14	CLAST_ADD
15	Reserved
16	DLAST_ADD
17	DLAST_ADD
18	DLAST_ADD
19	DLAST_ADD
20	DLAST_ADD
21	DLAST_ADD
22	DLAST_ADD
23	DLAST_ADD
24	DLAST_ADD
25	DLAST_ADD
26	DLAST_ADD
27	DLAST_ADD
28	DLAST_ADD
29	DLAST_ADD
30	DLAST_ADD
31	Reserved

CLAST_ADD RO, CON11[14..0]

Last address for lane C (used for diagnostics).

DLAST_ADD R/W, CON11[30..16]

Last address for lane D (used for diagnostics).

5.15 CON13 Register

Bit	Name
0	VIDEO_MASK
1	VIDEO_MASK
2	VIDEO_MASK
3	VIDEO_MASK
4	VIDEO_MASK
5	VIDEO_MASK
6	VIDEO_MASK
7	VIDEO_MASK
8	VIDEO_MASK
9	VIDEO_MASK
10	VIDEO_MASK
11	VIDEO_MASK
12	VIDEO_MASK
13	VIDEO_MASK
14	VIDEO_MASK
15	VIDEO_MASK
16	VIDEO_MASK
17	VIDEO_MASK
18	VIDEO_MASK
19	VIDEO_MASK
20	VIDEO_MASK
21	VIDEO_MASK
22	VIDEO_MASK
23	VIDEO_MASK
24	VIDEO_MASK
25	VIDEO_MASK
26	VIDEO_MASK
27	VIDEO_MASK
28	VIDEO_MASK
29	VIDEO_MASK
30	VIDEO_MASK
31	VIDEO_MASK

VIDEO_MASK R/W, CON13[31..0]

With the aid of this mask, individual bits in the video data stream can be set to 0. The 32 bit mask is duplicated for the 32 MSB of a 64 bit word.

Bit N in VIDEO_MASK	Meaning
0	Set bit N to 0
1	Pass bit N as is

5.16 CON14 Register

Bit	Name
0	SWRESET
1	FENPOL
2	LENPOL
3	BUTTONS
4	BUTTONS
5	BUTTONS
6	BUTTONS
7	BUTTONS
8	BUTTONS
9	BUTTONS
10	BUTTONS
11	BUTTONS
12	BUTTONS
13	BUTTONS
14	BUTTONS
15	BUTTONS
16	SHIFT_RAW
17	SHIFT_RAW
18	SHIFT_RAW
19	SHIFT_RAW
20	SHIFT_RAW_LEFT
21	DELAY
22	DELAY
23	DELAY
24	SWAP
25	UART_CON
26	UART_CON
27	Reserved
28	DPM_SPLIT
29	DPM_SPLIT
30	DPM_SPLIT
31	DPM_SPLIT

SW_RESET WO, CON14[0]

This bit will always read back 0.

SW_RESET	Meaning
0	Reset de-asserted
1	General reset to R64.

FENPOL R/W, CON14[1]

This bitfield has the following properties.

FENPOL	Meaning
0	FEN is asserted on rising edge.
1	FEN is asserted on falling edge.

LENPOL R/W, CON14[2]

This bitfield has the following properties.

LENPOL	Meaning
0	LEN is asserted on rising edge.
1	LEN is asserted on falling edge.

BUTTONS R/W, CON14[15..3]

R/W register for test/diagnostics.

SHIFT_RAW R/W, CON14[19..16]

This register defines for the barrel shifter the amount of shift for the data to be acquired

SHIFT_RAW_LEFT R/W, CON14[20]

This register defines for the barrel shifter the shift direction for the data to be acquired.

SHIFT_RAW_LEFT	Meaning
0	Shift right
1	Shift left

DELAY R/W, CON14[23..21]

This register is used for aligning the Horizontal Active Window (HAW) relative the Line ENable signal (LEN). If the first active pixel occurs simultaneously with the assertion of LEN, then no delay is needed. If the first active pixel occurs between 1 and 7 clocks later than LEN, the DELAY register must be programmed accordingly. The CTABs can be used to compensate for delays over 7 clocks. However, the granularity of the CTABs is 8 clocks, so both DELAY and the CTABS may have to be used in together to accommodate for some delays.

The net effect for a simple, one tap camera will be a shifting to the right of the displayed image. For multi-tap cameras the visual effect is more complex and depends on the taps architecture. All taps are delayed by the same amount.

The purpose of this bit field is to align the image presented by the different taps. This bit field has the opposite effect of the TRIM field in CON9.

DELAY	Meaning
0 (000b)	HAW is not delayed
1 (001b)	HAW is delayed by 1 clocks
2 (010b)	HAW is delayed by 2 clocks
3 (011b)	HAW is delayed by 3 clocks
4 (100b)	HAW is delayed by 4 clocks
5 (101b)	HAW is delayed by 5 clocks
6 (11ob)	HAW is delayed by 6 clocks
7 (111b)	HAW is delayed by 7 clocks

SWAP R/W, CON14[24]

Future use.

UART_CON R/W, CON14[26..25]

This register will control the connection of the serial ports of the two camera Link connectors.

UART_CON	Connection
0 (00b)	On-board UART connected to CL serial port of main connector
1 (01b)	On-board UART connected to CL serial port of auxiliary connector
2 (10b)	Serial port of main connector CL connected to external serial port, through the IO connector.
3 (11b)	Serial port of auxiliary connector CL connected to external serial port, through the IO connector

DPM_SPLIT R/W, CON14[31..28]

This register controls how incoming data is written to the DPM.

DPM_SPLIT	Mode
0 (0000b)	Normal mode
1 (0001b)	Each tap's output is split in half.
2 (0010b) to 14 (1110b)	Reserved
15 (1111b)	Each tap's output is written in 4K chunks

5.17 CON15 Register

Bit	Name
0	SOURCE_ADD
1	SOURCE_ADD
2	SOURCE_ADD
3	SOURCE_ADD
4	SOURCE_ADD
5	SOURCE_ADD
6	SOURCE_ADD
7	SOURCE_ADD
8	SOURCE_ADD
9	SOURCE_ADD
10	SOURCE_ADD
11	SOURCE_ADD
12	SOURCE_ADD
13	SOURCE_ADD
14	SOURCE_ADD
15	TAG_QUAD
16	QUAD_INFO
17	QUAD_INFO
18	QUAD_INFO
19	QUAD_INFO
20	QUAD_INFO
21	QUAD_INFO
22	QUAD_INFO
23	QUAD_INFO
24	QUAD_INFO
25	QUAD_INFO
26	QUAD_INFO
27	QUAD_INFO
28	QUAD_INFO
29	QUAD_INFO
30	QUAD_INFO
31	QUAD_INFO

ADD_SOURCE RO, CON15[14..0]

DMA source address pointing to a 64-bit long word in the DPM.

TAG_QUAD RO, CON15[15]

TAG marker.

QUAD_INFO RO, CON15[31..16]

16 bits of QUAD information.

5.18 CON16 Register

Bit	Name
0	TXC
1	TXC
2	TXC
3	TXC
4	TXC
5	TXC
6	TXC
7	TXC
8	TXC
9	TXC
10	TXC
11	TXC
12	TXC
13	QUAD_INT
14	TAIL_TAG
15	HEAD_TAG
16	TXC_INFO
17	TXC_INFO
18	TXC_INFO
19	TXC_INFO
20	TXC_INFO
21	TXC_INFO
22	TXC_INFO
23	TXC_INFO
24	EOC
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

TXC RO, CON16[12..0]

DMA transfer count in units of bytes.

QUAD_INT RO, CON16[13]

This bitfield has the following properties.

QUAD_INT	Meaning
0	No interrupt at end of this QUAD
1	An interrupt will be asserted at after this QUAD has been executed.

TAIL_TAG RO, CON16[14]

This bitfield has the following properties.

TAIL_TAG	Meaning
0	Current QUAD is not a tail TAG
1	Current QUAD is a tail TAG.

HEAD_TAG RO, CON16[15]

This bitfield has the following properties.

TAIL_TAG	Meaning
0	Current QUAD is not a head TAG
1	Current QUAD is a head TAG.

TXC_INFO RO, CON16[23..16]

Transmit information from current QUAD.

EOC RO, CON16[24]

This bitfield has the following properties.

EOC	Meaning
0	Current QUAD is not an end of chain
1	Current QUAD is an end of chain.

5.19 CON17 Register

Bit	Name
0	FREE_RUN_RATE
1	FREE_RUN_RATE
2	FREE_RUN_RATE
3	FREE_RUN_RATE
4	FREE_RUN_RATE
5	FREE_RUN_RATE
6	FREE_RUN_RATE
7	FREE_RUN_RATE
8	FREE_RUN_RATE
9	FREE_RUN_RATE
10	FREE_RUN_RATE
11	FREE_RUN_RATE
12	FREE_RUN_RATE
13	FREE_RUN_RATE
14	FREE_RUN_RATE
15	FREE_RUN_RATE
16	FREE_RUN_HI
17	FREE_RUN_HI
18	FREE_RUN_HI
19	FREE_RUN_HI
20	FREE_RUN_HI
21	FREE_RUN_HI
22	FREE_RUN_HI
23	FREE_RUN_HI
24	FREE_RUN_HI
25	FREE_RUN_HI
26	FREE_RUN_HI
27	FREE_RUN_HI
28	FREE_RUN_HI
29	FREE_RUN_HI
30	FREE_RUN_HI
31	FREE_RUN_HI

FREE_RUN_RATE R/W, CON17[15..0]

This register defines the period of the on-board free running generator. The clock driving the generator is the on-board generated clock, whose frequency is programmed in CON0. Programming the FREE_RUN_RATE to 200 for example, will yield a signals whose period is 200 clocks.

FREE_RUN_HI R/W, CON17[31..16]

This register defines the amount of time the free running generator is 1 during a period. Setting this register to 100, for example, will yield a signal that is 1 for 100 clocks, regardless of the period. Obviously, the number programmed in FREE_RUN_RATE must be larger than the number programmed in FREE_RUN_HI.

5.20 CON18 Register

Bit	Name
0	ALPF
1	ALPF
2	ALPF
3	ALPF
4	ALPF
5	ALPF
6	ALPF
7	ALPF
8	ALPF
9	ALPF
10	ALPF
11	ALPF
12	ALPF
13	ALPF
14	ALPF
15	ALPF
16	ALPF
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	SIG_GEN_POL
31	SCALE_BY8K

ALPF R/W, CON18[16..0]

This register defines the Active Lines Per Frame of the vertical acquisition window. Let's assume for example a single tap camera with 2K lines per frame. If we want to acquire 400 lines per frame, the ALPF will be programmed to 400. For a 2-tap odd-even lines camera, with 2K lines per frame, to acquire 400 pixels the ALPF will be programmed with the value 200, as for every LEN the camera supplies two lines.

SIG_GEN_POL R/W, CON18[30]

This bit allows for the inversion of the free running generator's output.

SIG_GEN_POL	Meaning
0	Free running generator supplies signal as is
1	Invert output of the free running signal generator.

SCALE_BY8K R/W, CON18[31]

Scaling down the clock to the free running generator can yield waveforms on the order of single Hz.

SCALE_BY8K	Meaning
0	Use on board CLOCK as is for the free running signal generator
1	Divide by 8K the on-board CLOCK to be used by the free running generator..

5.21 CON19 Register

Bit	Name
0	LINES_TOGO
1	LINES_TOGO
2	LINES_TOGO
3	LINES_TOGO
4	LINES_TOGO
5	LINES_TOGO
6	LINES_TOGO
7	LINES_TOGO
8	LINES_TOGO
9	LINES_TOGO
10	LINES_TOGO
11	LINES_TOGO
12	LINES_TOGO
13	LINES_TOGO
14	LINES_TOGO
15	LINES_TOGO
16	LINES_TOGO
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

LINES_TOGO R/W, CON19[16..0]

This register will reflect the number of remaining lines left to be acquired till the end of the frame.

5.22 CON20 Register

Bit	Name
0	FIFO_EQ
1	FIFO_EQ
2	FIFO_EQ
3	FIFO_EQ
4	FIFO_EQ
5	FIFO_EQ
6	FIFO_EQ
7	FIFO_EQ
8	VID_BRL
9	VID_BRL
10	VID_BRL
11	VID_BRL
12	VID_BRL
13	VID_BRL
14	VID_BRL
15	VID_BRL
16	VIDEO_2DPM
17	VIDEO_2DPM
18	VIDEO_2DPM
19	VIDEO_2DPM
20	VIDEO_2DPM
21	VIDEO_2DPM
22	VIDEO_2DPM
23	VIDEO_2DPM
24	COLOR_MASK
25	COLOR_MASK
26	SHIFT_DSP_SELECT
27	SHIFT_DSP
28	SHIFT_DSP
29	SHIFT_DSP
30	SHIFT_DSP
31	SHIFT_DSP_LEFT

FIFO_EQS RO, CON20[7..0]

This register reflects the instantaneous value of the 8 LSB of the first tap of the main CL connector. Used for diagnostics/test.

VID_BRL RO, CON20[15..8]

This register reflects the instantaneous value of the 8 LSB of the barrel shifter of lane A. Used for diagnostics/test.

VIDEO_2DPM RO, CON20[23..16]

This register reflects the instantaneous value of the 8 LSB of the video written in the DPM's lane A. Used for diagnostics/test.

COLOR_MASK R/W, CON20[25..24]

This bitfield can be used to mask out color channels when acquiring color pixels formats (e.g 24-bit color, 36-bit color, etc.).

COLOR_MASK	Meaning
0 (00b)	Pass all colors
1 (01b)	Pass only the red channel, set the blue and green channels to 0
2 (10b)	Pass only the green channel, set the blue and red channels to 0
3 (11b)	Pass only the blue channel, set the red and green channels to 0

SHIFT_DSP_SELECT R/W, CON20[26]

This bitfield has the following properties.

SHIFT_DSP_SELECT	Meaning
0	Supply barrel shifter with the acquisition shift code
1	Supply barrel shifter with the display shift code.

SHIFT_DISP R/W, CON20[30..27]

This register holds the shift amount for data to be displayed.

SHIFT_DSP_LEFT R/W, CON20[31]

This bitfield has the following properties.

SHIFT_DSP_LEFT	Meaning
0	Shift display data right
1	Shift display data left.

5.23 CON21 Register (Bayer Version)

Bit	Name
0	RED_GAIN
1	RED_GAIN
2	RED_GAIN
3	RED_GAIN
4	RED_GAIN
5	RED_GAIN
6	RED_GAIN
7	RED_GAIN
8	GREEN_GAIN
9	GREEN_GAIN
10	GREEN_GAIN
11	GREEN_GAIN
12	GREEN_GAIN
13	GREEN_GAIN
14	GREEN_GAIN
15	GREEN_GAIN
16	BLUE_GAIN
17	BLUE_GAIN
18	BLUE_GAIN
19	BLUE_GAIN
20	BLUE_GAIN
21	BLUE_GAIN
22	BLUE_GAIN
23	BLUE_GAIN
24	DECODER_OUT
25	DECODER_OUT
26	DECODER_OUT
27	Reserved
28	BAYER_BIT_DEPTH
29	BAYER_BIT_DEPTH
30	DECODER_PHASE
31	DECODER_PHASE

CON21 is a “soft” register. Soft registers change definitions depending on the version board and the firmware that is downloaded to the board.

REG_GAIN R/W, CON21[7..0]

This register controls the gain of the red channel. The video value is multiplied by the value in RED_GAIN and after that scaled down by 64. Numbers above 255 are clipped to 255 (saturation effect).

GREEN_GAIN R/W, CON21[15..8]

This register controls the gain of the green channel. The video value is multiplied by the value in GREEN_GAIN and after that scaled down by 64. Numbers above 255 are clipped to 255 (saturation effect).

BLUE_GAIN R/W, CON21[23..16]

This register controls the gain of the blue channel. The video value is multiplied by the value in BLUE_GAIN and after that scaled down by 64. Numbers above 255 are clipped to 255 (saturation effect).

DECODER_OUT R/W, CON21[26..24]

These bits controls the output of the Bayer decoder.

DECODER_OUT	Meaning
0 (000b)	Decode RGB on all three channels
1 (001b)	Raw data on all three channels
2 (010b)	Decode intensity on all three channels
3 (011b)	Decode red on all three channels
4 (100b)	Decode green on all three channels
5 (101b)	Decode blue on all three channels
6 (110b)	Reserved
7 (111b)	Reserved

BAYER_BIT_DEPTH R/W, CON21[29..28]

This bit is set if the pixel depth from the camera is 10 bits.

BAYER_10_BIT	Meaning
0 (00b)	8-bit pixels
1 (01b)	12-bit pixels
2 (10b)	10-bit pixels
3 (11b)	Reserved

DECODER_PHASE R/W, CON21[31..30]

These bits control the starting phase of the Bayer decoder. This register is set based on the arragement of the color matrix in the camera's CCD.

DECODER_PHASE	Meaning
0 (00b)	First two pixels: Blue, Green
1 (01b)	First two pixels: Green, Blue
2 (10b)	First two pixels: Red, Green
3 (11b)	First two pixels: Green, Red

5.24 CON22 Register

Bit	Name
0	DEST_ADD
1	DEST_ADD
2	DEST_ADD
3	DEST_ADD
4	DEST_ADD
5	DEST_ADD
6	DEST_ADD
7	DEST_ADD
8	DEST_ADD
9	DEST_ADD
10	DEST_ADD
11	DEST_ADD
12	DEST_ADD
13	DEST_ADD
14	DEST_ADD
15	DEST_ADD
16	DEST_ADD
17	DEST_ADD
18	DEST_ADD
19	DEST_ADD
20	DEST_ADD
21	DEST_ADD
22	DEST_ADD
23	DEST_ADD
24	DEST_ADD
25	DEST_ADD
26	DEST_ADD
27	DEST_ADD
28	DEST_ADD
29	DEST_ADD
30	DEST_ADD
31	DEST_ADD

DEST_ADD RO, CON22[31..0]

Current QUAD's destination address. Used for test/diagnostics.

5.25 CON23 Register

Bit	Name
0	Reserved
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

5.26 CON24 Register

Bit	Name
0	LUT_HOST_DATA
1	LUT_HOST_DATA
2	LUT_HOST_DATA
3	LUT_HOST_DATA
4	LUT_HOST_DATA
5	LUT_HOST_DATA
6	LUT_HOST_DATA
7	LUT_HOST_DATA
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	LUT_ON
16	LUT_HOST_ADDR
17	LUT_HOST_ADDR
18	LUT_HOST_ADDR
19	LUT_HOST_ADDR
20	LUT_HOST_ADDR
21	LUT_HOST_ADDR
22	LUT_HOST_ADDR
23	LUT_HOST_ADDR
24	LUT_BANK
25	LUT_BANK
26	Reserved
27	LUT_DATA_WRITE_ SEL
28	LUT_HOST_LANE
29	LUT_HOST_LANE
30	LUT_WEN
31	LUT_HOST_ACCESS

CON24 is a “soft” register. Soft registers change definitions depending on the version board and the firmware that is downloaded to the board.

LUT_HOST_DATA R/W, CON24[7..0]

This register is used to read and write data from the LUT. The LUT is programmed indrectly using this and the other registers in CON24.

The procedure to write data to the LUT is as follows:

Set LUT_HOST_ACCESS to 1.
Set LUT_DATA_WRITE_SEL to 1.
Set LUT_BANK to the desired bank to program.
Set LUT_HOST_LANE to the desired LUT lane to program.
Set LUT_HOST_ADDR to the desired LUT location to program (LUT input).
Set LUT_HOST_DATA to the value desired (LUT output).
Write LUT_WEN to 1, this copies the value from the LUT_HOST_DATA register to the LUT's memory location as specified by LUT_HOST_ADDR.

The procedure to read data from the LUT is as follows:

Set LUT_HOST_ACCESS to 1.
Set LUT_DATA_WRITE_SEL to 0.
Set LUT_BANK to the desired bank to read.
Set LUT_HOST_LANE to the desired LUT lane to read.
Set LUT_HOST_ADDR to the desired LUT location to read.
Read LUT_HOST_DATA, the value returned in this register is the value in the LUT's memory.

LUT_ON R/W, CON24[15]

This register is used to insert or bypass the LUT from the path of incoming camera data.

LUT_ON	Meaning
0	LUT is not in the data path (bypassed)
1	LUT is in the data path

LUT_HOST_ADDR R/W CON24[23..16]

This register is used to set the address for a read operation from the LUT memory or a write operation to the LUT memory. See the description of LUT_HOST_DATA for more details.

LUT_BANK R/W, CON24[25..24]

These bits control which bank of the LUT is being programmed, and which bank is being used to pass image data.

LUT_BANK	Meaning
0 (000b)	Host access to bank 0, data passes through bank 0
1 (001b)	Host access to bank 1, data passes through bank 1
2 (010b)	Host access to bank 2, data passes through bank 2
3 (011b)	Host access to bank 3, data passes through bank 3

LUT_DATA_WRITE_SEL R/W, CON24[27]

This bit is used to control how the LUT data is being accessed.

LUT_DATA_WRITE_SEL	Meaning
0	When reading LUT_HOST_DATA, the register returns the value currently in the LUT. In this mode LUT_HOST_DATA is read only.
1	LUT_HOST_DATA acts like a normal register. It can be written and read normally. The value in the LUT_HOST_DATA register is not transfered to the LUT memory until a 1 is written to LUT_WEN.

LUT_HOST_LANE R/W, CON24[29..28]

These bits control which LUT lane can be access by the host.

LUT_HOST_LANE	Meaning
0 (000b)	Host access to lane 0
1 (001b)	Host access to lane 1
2 (010b)	Host access to lane 2
3 (011b)	Host access to lane 3

LUT_WEN WO, CON24[30]

When LUT_DATA_WRITE_SEL is set to 1, Writing a 1 to this bit casues the value in LUT_HOST_DATA to be transfered to the LUT memory. When LUT_DATA_WRITE_SEL is set to 0, writing to this bit has no effect. See LUT_HOST_DATA for more information.

LUT_HOST_ACCESS R/W, CON24[31]

These bits turns on and off host access to the LUT..

DECODER_OUT	Meaning
0	The LUT cannot be accessed by the host
1	The LUT can be accessed by the host

5.27 CON25 Register

Bit	Name
0	DELAY_TAP1
1	DELAY_TAP1
2	DELAY_TAP1
3	DELAY_TAP1_SEL
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

DELAY_TAP1 R/W, CON25[2..0]

These bits control the delay for tap 1 only when DELAY_TAP1_SEL = 1. In this mode, tap 0 and tap 1 can be delayed independently. These bits have no effect if DELAY_TAP1_SEL = 0. This register works in a similar manner to the DELAY register.

DELAY_TAP1	Meaning
0 (000b)	HAW is not delayed
1 (001b)	HAW is delayed by 1 clocks
2 (010b)	HAW is delayed by 2 clocks
3 (011b)	HAW is delayed by 3 clocks
4 (100b)	HAW is delayed by 4 clocks
5 (101b)	HAW is delayed by 5 clocks
6 (11ob)	HAW is delayed by 6 clocks
7 (111b)	HAW is delayed by 7 clocks

DELAY_TAP1_SEL R/W, CON25[3]

This bit selects the register that controls the delay for tap 1. Tap 0 is always controlled by the register DELAY.

DELAY_TAP1_SEL	Meaning
0	Tap 1 is controlled by DELAY
1	Tap 1 is controlled by DELAY_TAP1

5.28 CON26 Register

Bit	Name
0	Reserved
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

5.29 CON27 Register

Bit	Name
0	Reserved
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

Specifications

Chapter 6

6.1 Introduction

This chapter describes the general specifications of the R64. The numerical values for he specifications are listed in Table 6-1. If more information is available for a given specification there will be an entry in the column marked "Details".

Table 6-1 R64 Specifications

Specifications	Value	Units	Details
PCI Bus frequencies (PCI Version)	33 and 66	MHz	Section 6.6
PCI Bus data widths (PCI Version)	32 and 64	Bits	
PCIe Compatibility (PCI Express Version)	x8 and x16	Slot size	
PCI Bus compatible voltages	3.3 and 5	Volts	
Maximum Input Pixel Clock Frequency	80	MHz	
Minimum Input Pixel Clock Frequency	20	MHz	
Pixel clock frequency match between two cameras in Dual Mode			Section 6.2
Maximum Pixels Per Line (1 tap)	262,144 (256K)	Pixels	Section 6.3
Maximum Lines Per Frame	131,072 (128K)	Lines	Section 6.4
Minimum clocks between lines	4	Clocks	
Minimum lines between frames	0	Lines	
Minimum pixel clocks between frames	4	Clocks	
Minimum trigger pulse	600	Nanoseconds	
Minimum encoder pulse	600	Nanoseconds	
Current consumption (+5V)	0.5	Amps	Section 6.5
Temperature range	0 to 50	Degrees Celsius	
Humidity	25% to 80%		
Mechanical dimensions	6.8 x 4.2	Inches	
Mechanical dimensions	17.27 x 10.67	Centimeters	
Minimum UART baud rate	110	Bits/Second	
Maximum UART baud rate	256K	Bits/Second	

6.2 Frequency Match Between Two Cameras In Dual Mode

When the R64 is used in Dual mode (i.e. acquiring from two cameras simultaneously), the pixels clocks of both cameras must be the same frequency. The accuracy of the frequency match is approximated by the following formula:

PPM x ACPL = 2,000,000

PPM - accuracy of the frequency in Parts Per Million

ACPL - Active Clocks Per Line

Example: If the accuracy of the clocks is 100 PPM, the maximum clocks per line would be 20,000.

For a single tap camera,that translates into 20,000 pixels per line. For a dual tap camera that supplies odd/even pixels for example, that translates into 40,000 pixels per line.

6.3 Maximum Pixels Per Line

The maximum number of pixels per line is given by the following formula:

Max_pix_per_line = 256K x Taps

Taps is the number of taps. A tap supplies a whole pixel.

Examples:

A two tap camera that supplies odd/even pixels, Max_pix_per_line = 512K.
An RGB camera that supplies RGB over 24 bits, Max_pix_per_line = 256K, as every clock the camera supplies one single pixel.
A four tap, two segments, each left right, Max_pix_per_line = 1M

6.4 Maximum Lines Per Frame

For area scan cameras, the maximum number of lines per frame is given by the following formula:

Max_lines_per_frame = 128K x Line_taps

Line_taps is the number of taps that supply a whole line.

Examples:

A one tap camera, Max_lines_per_frame = 128K.
A two tap camera that supplies odd/even lines, Max_lines_per_frame = 256K.
A two tap camera that supplies odd/even pixels, Max_lines_per_frame = 128K.

6.5 Power Consumption

The R64 needs a maximum current of 0.5 Amperes from the +5 Volt rail on the PCI bus. The +3.3, +12 and -12 Volt rails are not used.

6.6 Running the R64 in a PCI-X Slot

PCI-X slots are fully compatible with standard PCI boards. Thus, the R64 (PCI version) will function correctly in any PCI-X slot. PCI-X runs a various bus clock fequencies, however, the bus that the R64 is in will run at 66 MHz.

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