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Road Runner and R3 Differential Models

Hardware Reference Manual

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Preface

Chapter P

P.1 Purpose

This Hardware Reference Manual is intended for anyone installing or using the Road Runner or R3 camera interface. This manual only covers the differential input versions of these boards. There is a separate manual for the Camera Link versions. The purpose of this manual is two-fold. First, this manual completely describes how the board works. Second, it is a reference manual describing in detail what all of the board's registers do.

P.1.1 Support Services

BitFlow, Inc. provides both sales and technical support for the Road Runner/R3 product.

P.1.2 Technical Support

Our web site is www.bitflow.com.

Technical support is available at 781-932-2900 from 9:00 AM to 6:00 PM Eastern Standard Time, Monday through Friday.

For technical support by email (support@bitflow.com) or by FAX (781-933-9965), please include the following:

Product name
Camera type and mode being used
Software revision number
Computer CPU type, PCI chipset, bus speed
Operating system
Example code (if applicable)

P.1.3 Sales Support

Contact your local BitFlow Sales Representative, Dealer, or Distributor for information about how BitFlow can help you solve your most demanding camera interfacing problems. Refer to the BitFlow, Inc. website (www.bitflow.com) for a list of North American and International sales representatives.

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Introduction

Chapter 1

1.1 Overview

The Road Runner and the R3 are high-performance, PCI-based frame grabbers. They are targeted at digital cameras and general purpose digital data acquisition. The DMA engine transfers data directly into system memory. The digital port can accept up to 32 bits of data. This data can correspond to any arrangement of camera output taps (e.g. four 8-bit taps, or two 12-bit taps). On board circuitry will reformat the data on-the-fly. Figure 1-1 shows a general block diagram of the Road Runner/R3. The main blocks include:

The differential receivers
The Stack
Input multiplexers
Video FIFOs
LUTs
Descriptors Table
CTABs and camera control block
PLX PCI bus interface and DMA engine
Local bus controller

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1.2 Description

Basically, the input MUXs with the Video FIFOs and Video STACK will reformat the data from multi-tap cameras, up to four taps. The LUT is 8in-8out or 12in-16out (optionally 16in-16out). The CTABs (Control Tables) will control the attached cameras. The PCI bus interface is implemented with a PLX PCI90x0 device. This chip has all the circuitry for performing DMA. The Descriptors Table is part of a DMA address generator. The local bus controller will manage all the activity on the local bus.

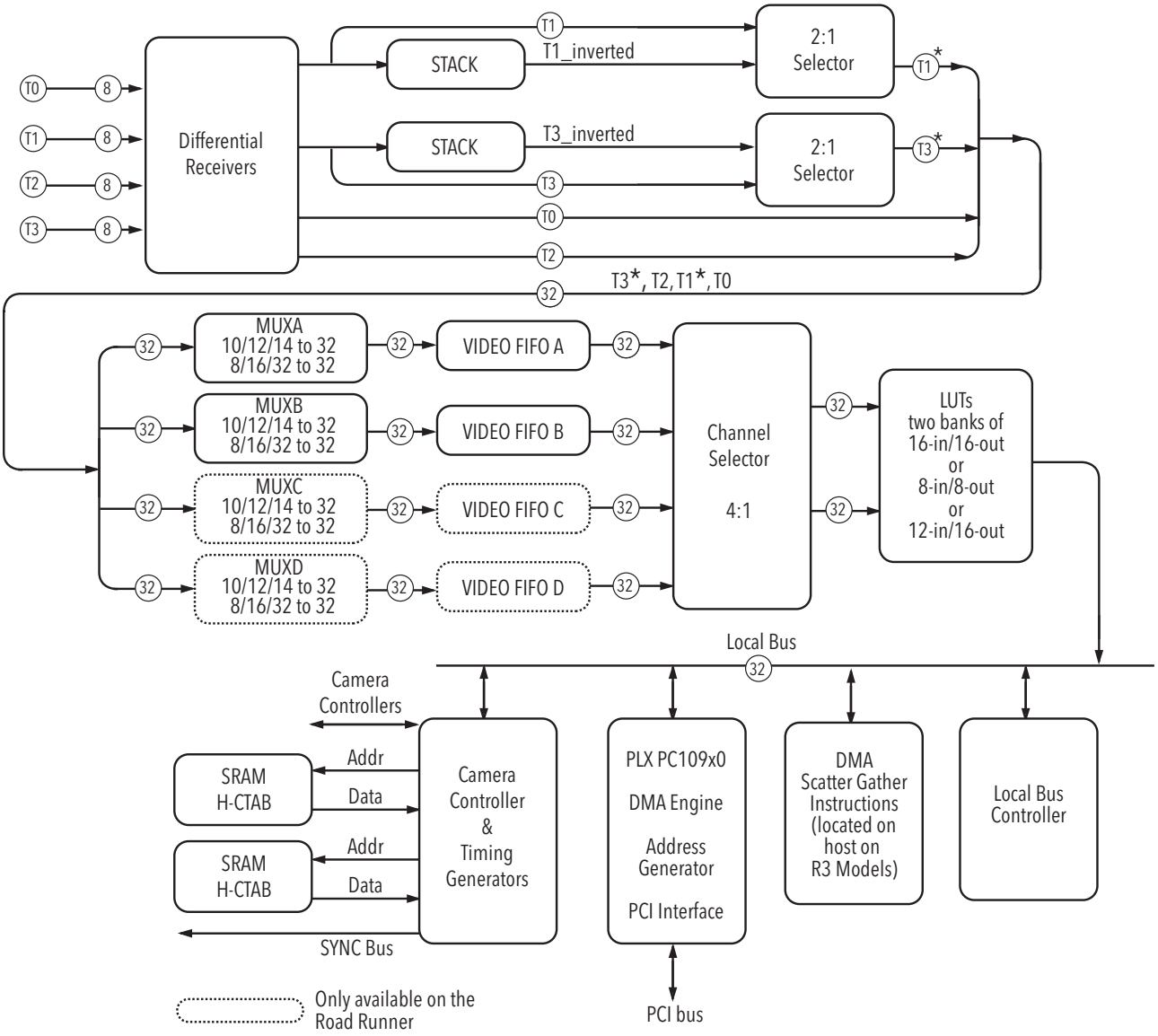


Figure 1-1 Road Runner/R3 Block Diagram

The layout of the Road Runner is provided in Figure 1-2.

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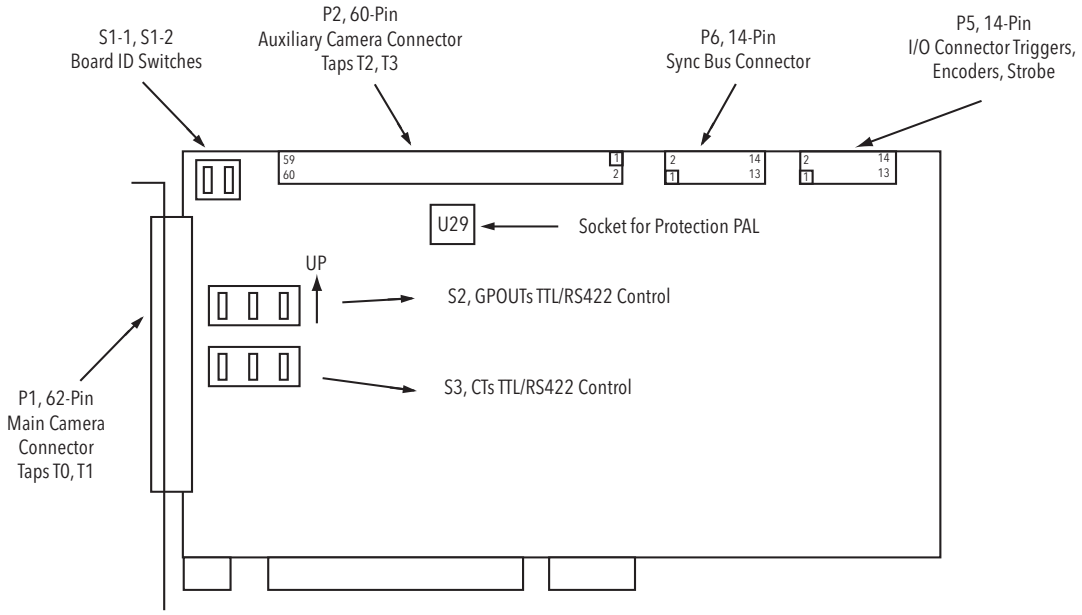


Figure 1-2 Road Runner Layout

The layout of the R3 is provided in Figure 1-3.

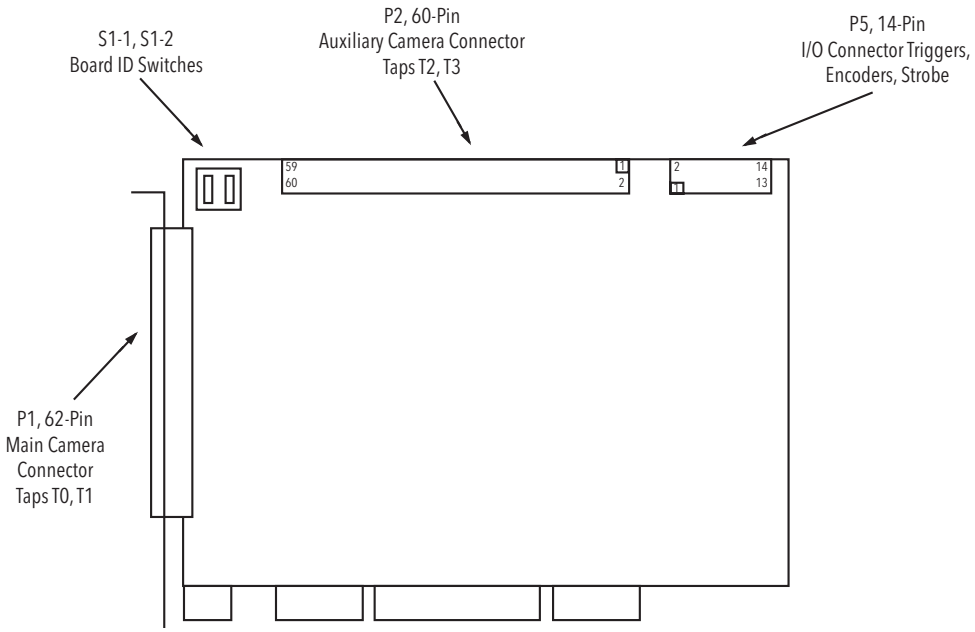


Figure 1-3 R3 Layout

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Connector P1 is the main camera connector. It has all the control signals to interface to a camera up to 16-bits wide. Those 16 bits are connected to taps T0 and T1. Connector P1 comes out of the PC through a bracket.

Connector P2 is the auxiliary camera connector. It brings into the board 16 bits of digital data on taps T2 and T3. Those taps, in conjunction with taps T0 and T1, can be used for cameras with outputs greater than 16 bits.

Connector P2 has all the control signals to connect to a camera up to 16 bits wide. It can be used for connecting to a second camera, independent of the camera connected to connector P1.

Connector P2 is brought out of the PC through an optional cable (CAB-RUN-TAP34 or CAB-RUN-CAM2D) that connects to a bracket. This bracket is mounted on the PC bracket holder.

P6 is a connector that connects the Sync bus between two or more Road Runner boards (Model 44 only).

P5 is a connector that connects the I/O signals to a bracket that mounts on the PC bracket holder with an optional cable (CAB-RUN-CONNIO). These I/O signals are related to industrial controls: triggers, encoders, and strobes.

S1-1, S1-2 are two mechanical switches that allow board identification in a system that has more than one Road Runner. The setting of these switches can be read by the software, so that the software knows which board is in each slot.

Note: The following paragraphs pertain to Road Runners only.

S2 are three switches that select between TTL and RS422 output for the GPOUT signals. S2-1 controls GPOUT0, S2-2 controls GPOUT1, and S2-3 controls GPOUT2. When the switch is in the UP position, as shown by the arrow, the respective output is RS422. In the down position, the output is TTL.

S3 are three switches that select between TTL and RS422 output for the camera controls and CT signals. S3-1 controls CT0, S3-2 controls CT1, and S3-3 controls CT2. When the switch is in the UP position, as shown by the arrow, the respective output is RS422. In the down position, the output is TTL.

At U29 there is a socket for a 20-pin protection PAL.

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Technical Description

Chapter 2

2.1 Road Runner Models

2.1.1 Description

The Road Runner is available in five models; RUN-PCI-11, RUN-PCI-12, RUN-PCI-14, RUN-PCI-24 and RUN-PCI-44. Each are described as follows.

RUN-PCI-44

This is the fully populated model. It has four taps input and four video FIFOs. The T1 and T3 taps have Stacks, so that they can scan reverse the input. The Sync bus and its associated logic is implemented.

RUN-PCI-24

This model has four taps input, but only two video FIFOs. The T1 and T3 taps have Stacks, so that they can scan reverse their inputs. The Sync bus is not implemented.

RUN-PCI-14

This model has four taps input, but only one single video FIFO. There is no Stack. The Sync bus is not implemented.

RUN-PCI-12

This model has only two taps input and one video FIFO. There is no Stack and the Sync bus is not implemented. Note that this model can acquire from a camera with 16 bits maximum.

RUN-PCI-11

This model can only handle 8-bits of data. There are not LUTs mounted on this model.

2.1.2 Options

Each model can be ordered with the following options.

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OPT-RUN-40 or -M

This option will have 40 MHz RS644 (LVDS) transceivers. It is recommended for cameras that have LVDS outputs. This option is identified by the letter "M" at the end of the board's serial number, see illustration.

OPT-RUN-16

This option will install LUTs 16in-16out. It is recommended for a pixel depth of more than 12 bits. This option is identified by the letter "L" at the end of the board's serial number, see illustration.

2.1.3 Identification

The model and the installed options can be identified by the board's serial number. The serial number is written on the back of the board. The format is as follows:

MMM-R.R-SSSS-O

Where:

MMM - Model
R.R - Revision
SSSS - Serial number
O - Options

The serial number for a model R12 without any options would be:

R12-2.4-4567

If both the OPT-RUN-40 and the OPT-RUN-LUT16 were installed on the board above, its serial number would be:

R12-2.4-4567-LM

2.1.4 R3 Models

There is only one model of the R3. There is also a Camera Link version of the R3, that is covered by a separate reference manual. The part number is as follows

R3-PCI-DIF

2.1.5 Options

The R3 has ben designed to work with almost all modern cameras. There are not, therefore, separate models to support LVDS and RS422 cameras. The only option for the R3 is a 16-in/16-out Look Up Table (LUT). This option is indicated by a -L at the end of the part number:

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R3-PCI-DIF-L

2.1.6 Identification

The model and the installed options can be identified by the board's serial number. The serial number is written on the back of the board. The format is as follows:

MMM-R.R-SSSS-O

Where:

MMM - Model
R.R - Revision
SSSS - Serial number
O - Options

The serial number for a model R3 differential without any options would be:

R3D-3.0-1010

The serial number for a model R3 differential with a LUT would be:

R3D-3.0-1012-L

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2.2 Camera Taps

The digital data on the four 8-bit taps is marked as T3, T2, T1, T0. A camera with an 8-bit output will be connected to tap T0. A camera with 9 to 16 bits will connect on T1, T0. The MSB is on T1. A 32-bit camera will connect to T3,T2, T1, T0. The MSB is on T3.

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2.3 Stack

On the Road Runner/R3, Taps T1 and T3 can be optionally scan-reversed. This operation is performed by the Stack. This temporary buffer acts like a stack or LIFO (Last In First Out). It will reverse the scan direction of a single video line. It will acquire a line, and then read it out backwards. It has a width of 16 bits and a depth of 4K words. T1,T3 are both treated as a single 16-bit stream. In Figure 1-1, the output of the selector T3*, T1* will be T3,T1 straight from the camera, or both of them scan reversed. The control bit STRAIGHT will select between inverted or the non-inverted T1,T3.

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2.4 Video FIFOs and MUXs

There are four internal channels on the Road Runner, and two internal channels on the R3. Each one is made up of a MUX and a FIFO. The channels are marked as A, B, C, D. Each channel accepts an 8/16/32-bit input from the four taps and packs it into 32 bits. The FIFO is a temporary storage device, for decoupling the camera input from the PCI bus. To get maximum efficiency, data over the PCI bus is always transferred as 32 bits.

The four channels are identical. Each MUX will select one or more taps from the T3*,T2,T1*,T0 set and format it in a 32-bit word. The type of formatting will be done according to a 3-bit code associated with each channel, and according to the firmware downloaded into each MUX.

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2.5 LUTs

On the Road Runner models, the LUTs are two banks of four lanes of 8-in/8-out or two lanes of 12-in/16-out. The mode, 8-in or 12-in, is determined by the BY8 bit in the ATTRIBUTE field and the HBY8 in the CON4 register. The bank selected is set by the BANK bit. There are multiple lanes because the data passes through the LUTs as a 32-bit word. Thus multiple LUTs must be used in parallel to cover all 32 bits (i.e. four lanes of 8-bit LUTs or two lanes of 12-bit LUTs).

The Road Runner can be ordered with an optional 16-in/16-out LUT. This LUT is organized as two banks of 16-in/16-out. For this model, the BY8 bit should always be set to 0.

The R3 can be ordered with no LUTs or with a 16-in/16-out LUT.

The access to the LUTs from the host is through a data port. The addressing is done through a 32-bit pointer, LUTADDR. Data is accessed through the 32-bit LUTDATA port.

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2.6 CTABs and Camera Controls

The circuitry for non-standard cameras has a programmable block that can generate a flexible set of horizontal and vertical signals.

The controls for non-standard cameras are implemented with two general purpose SRAMs: one for the horizontal axis called the Horizontal Control Table (HCTAB), the other for the vertical axis called the Vertical Control Table (VCTAB). The size of the HCTAB is 8Kx8. The size of the VCTAB is 32Kx8. In those tables are programmed the position and size of the various control signals. The HCTAB is addressed by a counter clocked by ¼ of the horizontal pixel clock. The horizontal control signals' resolution is on a four pixel boundary. Both the HCTAB and the VCTAB are programmed from the host.

2.6.1 Horizontal Control Table

Figure 2-1 depicts the structure of the HCTAB. For clarity, the address and data path that allow the host to program the HCTAB are not shown

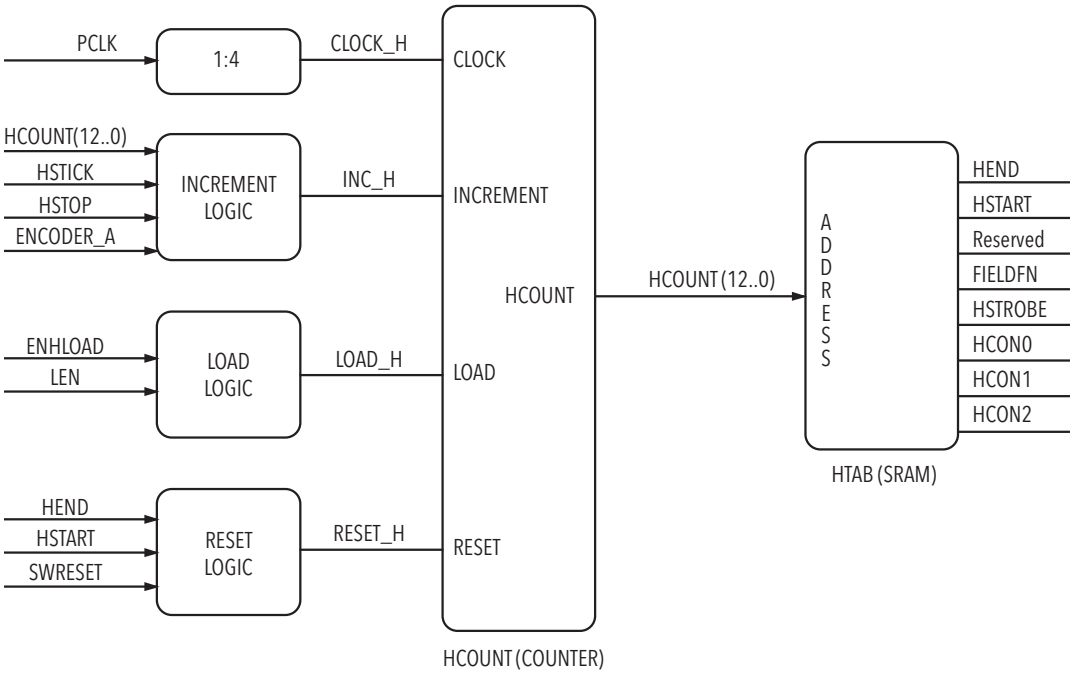


Figure 2-1 Horizontal Control

The Horizontal Control Table is made up of the following blocks:

HCOUNT - a synchronous counter that can be incremented, loaded and reset. The clock that drives HCOUNT is a free running clock, PCLK/4, i.e., the pixel clock divided by four. HCOUNT is 13 bits wide and is connected to the address input of the HCTAB.

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Logic for generating INC_H - the increment control signal to the HCOUNT.

Logic for generating LOAD_H - the load control signal to the HCOUNT. When LOAD_H is asserted, HCOUNT is loaded with the value of 2048.

Logic for generating RESET_H - the reset control signal to the HCOUNT. When RESET_H is asserted, HCOUNT is reset to 0.

HCTAB - a static memory (SRAM) that outputs eight HCTAB control signals. The address of this SRAM is driven by HCOUNT.

Logic for generating CLOCK_H - the clock to the HCOUNT. This is a frequency divider. CLOCK_H is PCLK, the pixel clock divided by four.

Note: If RESET_H and LOAD_H are asserted simultaneously, RESET_H overrides.

As the HCOUNT counts, it scans the address of the HCTAB in ascending order. The output of the HCTAB depends on the data that has been written in the HCTAB by the host. If the HCOUNT is free running, it will cyclically scan all the HCTAB's addresses. Any arbitrary cyclic waveform can be implemented by programming the HCTAB with the adequate data.

The LOAD_H and RESET_H will enable the synchronization between external events and the waveforms generated by the HCTAB. LOAD_H and RESET_H will force the HCOUNT to fixed values, 2048 and 0 respectively.

The INC_H signal will allow for stopping the counter from incrementing. In that case, the output of the HCTAB will be constant. While the HCOUNT is not incrementing, it can still be loaded or reset, see the logic below.

2.6.2 The HCTAB Functions

The functions assigned to the columns in the HCTAB are shown in Table 2-1.

Table 2-1 HCTAB Functions

Bit Column	Function
D0	HEND
D1	HSTART
D2	Reserved
D3	Reserved
D4	HSTROBE
D5	HCON0
D6	HCON1
D7	HCON2

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The HSTART and HEND define the horizontal acquisition window. The logic is shown in Table 2-2.

Table 2-2 HSTART and HEND

HSTART	HEND	Function
1	0	Start HWINDOW, the horizontal acquisition window.
0	1	End HWINDOW, the horizontal acquisition window.
1	1	End line; reset horizontal counter and increment vertical counter. Also ends the HWINDOW, if still active.

Basically, HSTART and HEND tell us where the horizontal acquisition window starts and where it ends. Video will be acquired only while the HWINDOW is active. For a continuous acquisition window, we have to program only two entries in the HCTAB, regardless of the window's size.

HWINDOW, the horizontal acquisition window, does not have to be continuous. We can selectively acquire sections of a line by properly manipulating HSTART and HEND.

HSTROBE is ANDed with vertical strobe function to fire a strobe at a precise point in time. HCON0, HCON1 and HCON2 are general purpose horizontal functions. Some of them are combined with the vertical functions to generate CT, the camera control functions.

INC_H

INC_H, the logic for incrementing HCOUNT.

There are only two instances when we want to inhibit the incrementing of HCTAB. The first instance is when HCOUNT reaches 0, "Stop at 0" case. The other instance is when HCOUNT reaches 2040, the "Stop at 2040" case.

Stop at 0

Usually, HCOUNT will reach 0 because of a RESET_H signal. After HCOUNT is reset, there are two programmable options:

HCOUNT keeps on counting.

HCOUNT stays at 0 until ENCODER_A is asserted.

The selection between option 1 and 2 is done by the HSTOP bit in CON5 as shown in Table 2-3.

Table 2-3 HSTOP Functionality

HSTOP	Function
0	After reaching 0, keep counting.
1	After reaching 0, stop counting until ENCODER_A is asserted.

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This operating mode is especially useful for synchronizing line scan cameras to external events. ENCODER_A is usually the output of an encoder or a tachometer signal. Until this signal is asserted, the HCOUNT waits at address 0. After the ENCODER_A is asserted, HCOUNT starts counting, i.e., scanning the HCTAB in ascending order. At some address, usually in HCON1, we will program a sync signal to be asserted to the line scan camera. In response to this sync signal, the camera will give back a line, and it will assert LEN. The LEN will load address 2048 into HCOUNT. In the HCTAB, we will program the horizontal acquisition window after address 2048. At the end of the horizontal acquisition window the RESET_H will be asserted, which in turn will reset the HCOUNT. HCOUNT will wait at address 0 until ENCODER_A is asserted.

Stop at 2040

Using the previous example, assume that after we asserted the sync signal to the camera, we expect the camera to give us a line, i.e., assert LEN. While we expect the camera to assert LEN, HCOUNT is still being incremented. If it takes too long for the camera to respond, HCOUNT will eventually reach and pass beyond 2048. A horizontal acquisition window will be asserted even though the camera did not assert LEN. To avoid such a situation, just before address 2048, when HCOUNT reaches 2040, it will stop. It will stay at 2040 until LEN is asserted. Then, HCOUNT will be loaded with 2048.

The stop at 2040 will occur only if the HSTICK bit is asserted, see CON6. If HSTICK is not asserted, HCOUNT will be free running and it will not stop at 2040.

LOAD_H

LOAD_H, the logic of loading HCOUNT.

HCOUNT will be loaded with the value 2048 by the rising/falling edge of LEN, if ENHLOAD is asserted. LEN usually marks the start of valid data in a line. The horizontal acquisition window can be placed starting at address 2048.

ENHLOAD is a bit in CON5 that enables the LEN. There are cameras that do not assert LEN. In that case, the LEN differential receiver must be disabled, otherwise its behavior is unpredictable.

Operation on the rising/falling edge of LEN is selected by LENPOL, see CON3.

RESET_H

RESET_H, the logic of reset HCOUNT.

HCOUNT can be reset from two sources:

From within the HCTAB.
From SWRESET.

In the first case, HCOUNT will be reset when HSTART AND HEND = 1. This will always happen at the end of the line.

In the second case, HCOUNT will be reset by SWRESET, a software reset that initializes the hardware. SWRESET is a bit in CON4.

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Example:

Lets look at a simple example to clarify the concept of the HCTAB. Assume we want to program a free running horizontal window of 16 pixels active area. Just before the active area we want to fire a strobe with the function in HSTROBE. D0 (HEND) and D1 (HSTART) define the active horizontal acquisition window. They also define the RESET_H function. D4 is the strobe pulse.

Taking into account that the address counter is clocked by ¼ the pixel clock, the HCTAB memory map will be as shown in Table 2-4.

Table 2-4 HCTAB Example

HCTAB Address	HEND D0	HSTART D1	HSTROBE D4	Comments
0	0	0	0	You got here from address 8
1	0	0	0	
2	0	0	0	
3	0	0	1	Fire the strobe
4	0	1	0	Start Horizontal Acquisition Window
5	0	0	0	Acquire
6	0	0	0	Acquire
7	0	0	0	Acquire
8	1	1	0	Stop acquisition, assert RESET_H
9	0	0	0	

Now lets assume a line scan camera that does not supply any type of signal, but it has to be driven. We must supply a LEN type signal to the camera. In that case, the RESET_H signal will take care of generating a cyclical signal. The position of RESET_H relative to address 0 will determine the period of the horizontal scanning. If RESET_H is set at address X1, then the horizontal active window should be programmed between 0 and X1.

Some line scan cameras require a line start command after the previous line has been read out. We can program the HCTAB to stop incrementing after the line has been read. The ENCODER_A will restart the count (from address 000H). Program the line start command to the camera in the 0-2048 area. In response to the line start command, the camera will give back a LEN. Set LENPOL = 1 so that the loading occurs on the rising edge of LEN. After address 2048, program the position and size of the horizontal acquisition window by setting HSTART end HEND.

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Table 2-5 shows the effect of LEN on HCOUNT for different settings of ENHLOAD and LENPOL.

Table 2-5 The effect of LEN on HCOUN

LENPOL	ENHLOAD	Signal	HCOUNT @ Current CLOCK_H	HCOUNT @ Next CLOCK_H
0	0	Leading edge of LEN	HCOUNT	HCOUNT+1
0	1	Leading edge of LEN	HCOUNT	2048
1	0	Trailing edge of LEN	HCOUNT	HCOUNT+1
1	1	Trailing edge of LEN	HCOUNT	2048

Table 2-6 shows the effect of ENCODER_A and RESET_H on HCOUNT for different settings of HSTOP. The assumption is that the encoder polarity is positive, ENCPOL = 0. For ENCPOL = 1, substitute “rising edge” with “falling edge.”

Table 2-6 The effect of ENCODER_A and RESET_H on HCOUNT

HSTOP	Signal	HCOUNT @ Current CLOCK_H	HCOUNT @ Next CLOCK_H
0	None	HCOUNT	HCOUNT+1
1	None	0	0
1	Rising edge of ENCODER_A	0	1
1	Rising edge of ENCODER_A	HCOUNT > 0	HCOUNT+1
0	RESET_H	HCOUNT	0
1	RESET_H	HCOUNT	0

2.6.3 Vertical Control Table

Figure 2-2 depicts the structure of the Vertical Control Table (VCTAB). For clarity, the address and data path that allow the host to program the VCTAB are not shown.

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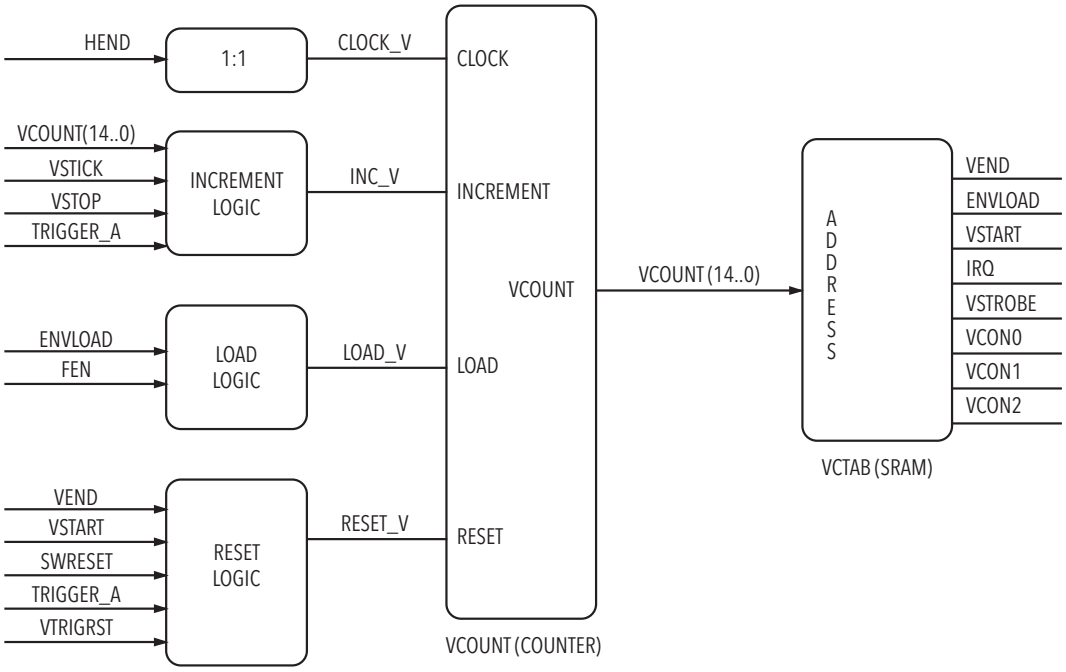


Figure 2-2 Vertical Control

The Vertical Control Table is made up of the following blocks:

VCOUNT - a synchronous counter that can be incremented, loaded and reset. The clock that drives VCOUNT is derived from the HCTAB, see below. VCOUNT is 15-bit wide and is connected to the address input of the VCTAB.

Logic for generating INC_V - the increment control signal to the VCOUNT.

Logic for generating LOAD_V - the load control signal to the VCOUNT. When LOAD_V is asserted, VCOUNT is loaded with the value of 4096.

Logic for generating RESET_V - the reset control signal to the VCOUNT. When RESET_V is asserted, VCOUNT is reset to 0.

Logic for generating CLOCK_V - the clock to the VCOUNT.

VCTAB - a static memory (SRAM) that outputs eight VCTAB control signals. The address of this SRAM is driven by VCOUNT.

If RESET_V and LOAD_V are asserted simultaneous, RESET_V overrides.

As the VCOUNT counts, it scans the address of the VCTAB in ascending order. The output of the VCTAB depends on the data that has been written in the VCTAB by the host. If the VCOUNT is free running, it will cyclically scan all the VCTAB's addresses. Any arbitrary cyclic waveform can be implemented by programming the VCTAB with the adequate data.

The LOAD_V and RESET_V will enable the synchronization between external events and the waveforms generated by the VCTAB. LOAD_V and RESET_V will force the VCOUNT to known values, 4096 and 0 respectively.

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The INC_V signal will allow for stopping the counter from incrementing. In that case, the output of the VCTAB will be constant. While the VCOUNT is not incrementing, it can still be loaded or reset, see the logic below.

The VCTAB Functions

The functions assigned to the columns in the VCTAB are shown in Table 2-7.

Table 2-7 CVTAB Functions

Bit Column	Function
D0	VEND
D1	ENVLOAD
D2	VSTART
D3	IRQ
D4	VSTROBE
D5	VCON0
D6	VCON1
D7	VCON2

VSTART and VEND define the vertical acquisition window. The logic is shown in Table 2-8.

Table 2-8 VSTART and VEND

VSTART	VEND	Function
1	0	Start VWINDOW, the vertical acquisition window.
0	1	End VWINDOW, the vertical acquisition window.
1	1	End frame and reset VCOUNT. Also ends the VWINDOW, if still active.

Basically, VSTART and VEND tell us where the vertical acquisition window starts and where it ends. Video will be acquired only while the VWINDOW is active. For a continuous acquisition window, we have to program only two entries in the VCTAB, regardless of the window's size.

VWINDOW, the vertical acquisition window, does not have to be continuous. We can selectively acquire sections of a frame by properly manipulating VSTART and VEND. VWINDOW is used in conjunction with HWINDOW to control when video data is written to memory.

ENVLOAD enables the FEN to load the VCOUNT. The rationale behind the ENVLOAD column from the VCTAB is that some cameras might not give a FEN, but only two pulses: the start and end of FEN. With the ENVLOAD, we can mask out the unwanted one.

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IRQ provides an interrupt to the bus, allowing an interrupt to occur at any point on the vertical axis.

VSTROBE, used in conjunction with HSTROBE, fires a strobe at a precise point in time.

VCON0, VCON1 and VCON2 are general purpose vertical functions, see usage below.

Note: If a VRESET pulse happens coincident with a LOAD, the LOAD is overriding.

CLOCK_V

CLOCK_V, the clocking of the VCOUNT.

CLOCK_V is generated by the HCTAB. Whenever HSTART 'AND' HEND = 1, the VCOUNT will be incremented. This will always happen at the end of the line.

INC_V, the logic for incrementing VCOUNT.

There are only two instances when we want to inhibit the incrementing of VCTAB. The first instance is when VCOUNT reaches 0, the "Stop at 0" case. The other instance is when HCOUNT reaches 4088, the "Stop at 4088" case.

Stop at 0

Usually, VCOUNT will reach 0 because of a RESET_V signal. After VCOUNT is reset, there are two programmable options:

VCOUNT keeps on counting.
VCOUNT stays at 0 until TRIGGER_A is asserted.

The selection between option 1 and 2 is done by the VSTOP bit in CON5 as shown in Table 2-9.

Table 2-9 VSTOP

VSTOP	Function
0	After reaching 0, keep counting.
1	After reaching 0, stop counting until TRIGGER_A is asserted.

This operating mode is especially useful for synchronizing cameras to external events. TRIGGER_A is usually the output of a part-in-place signal. Until this signal is asserted, the VCOUNT waits at address 0. After the TRIGGER_A is asserted, VCOUNT starts counting, i.e., scanning the VCTAB in ascending order. At some address, usually in VCON0, we will program a sync signal to be asserted to the camera. In response to this sync signal, the camera will give back a frame, and it will assert FEN. The FEN will load address 4096 into VCOUNT. In the VCTAB, we will program the vertical acquisition window after address 4096. At the end of the vertical acquisition window the RESET_V will be asserted, which in turn will reset the VCOUNT. VCOUNT will wait at address 0 until TRIGGER_A is asserted.

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Stop at 4088

Using the previous example, assume that after we asserted the sync signal to the camera, we expect the camera to give us a frame, i.e., assert FEN. While we expect the camera to assert FEN, VCOUNT is still being incremented. If it takes too long for the camera to respond, VCOUNT will eventually reach and pass beyond 4096. A vertical acquisition window will be asserted, even though the camera did not assert FEN. To avoid such a situation, just before address 4096, when VCOUNT reaches 4088, it will stop. It will stay at 4088 until FEN is asserted. Then, VCOUNT will be loaded with 4096.

The stop at 4088 will occur only if the VSTICK = 1, see CON8. If VSTICK is not asserted, VCOUNT will be free running and it will not stop at 4088.

LOAD_V

LOAD_V, the logic of loading VCOUNT.

VCOUNT will be loaded with the value 4096 by the rising/falling edge of FEN, if ENVLOAD is asserted. FEN usually marks the start of a valid frame. The vertical acquisition window can be placed starting at address 4096.

ENVLOAD is a column in the VCTAB. There are cameras that do not assert FEN. In this case, the FEN differential receiver must be disabled, otherwise its behavior is unpredictable. Some other type of cameras assert only the start and stop of a frame. In this case, ENVLOAD can mask out the unwanted signals.

Operation on the rising/falling edge of FEN is selected by FENPOL, see CON3

RESET_V

RESET_V, the logic of reset VCOUNT.

VCOUNT can be reset from four sources:

From within the VCTAB.
From TRIGGER_A.
From SWRESET.
If the board is in triggered termination mode (start-stop mode) and the end of document trigger is asserted.

In the first case, VCOUNT will be reset when VSTART AND VEND = 1. This will always happen at the end of the frame.

In the second case, VCOUNT can be reset by TRIGGER_A if VTRIGRST is asserted. VTRIGRST is a bit in CON5. It will enable the TRIGGER_A to reset the VCOUNT.

In the third case, VCOUNT will be reset by SWRESET, a software reset that initializes the hardware. SWRESET is a bit in CON4.

In the fourth case, when the board is in start-stop mode, VCOUNT will be reset when one of the following conditions occur: 1. The trailing edge of TRIGGERA (if the bit TRIGSTOPA = 1). 2. TRIGGERB is asserted (if bit TRIGSTOPA = 0).

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Note: Unpredictable behavior occurs for TRIGGERA feature if both VSTOP and VTRIGRST are each set.

Table 2-10 shows the effect of FEN on VCOUNT for different settings of ENVLOAD and FENPOL.

Table 2-10 The effect of FEN on VCOUNT

FENPOL	ENVLOAD	FEN	VCOUNT @ Current CLOCK_V	VCOUNT @ Next CLOCK_V
0	0	Leading edge of FEN	VCOUNT	VCOUNT + 1
0	1	Leading edge of FEN	VCOUNT	4096
1	0	Trailing edge of FEN	VCOUNT	VCOUNT + 1
1	1	Trailing edge of FEN	VCOUNT	4096

Table 2-11 shows the effect of TRIGGER_A and RESET_V on VCOUNT, for different settings of VSTOP. The table assumes TRIGPOL = 0. If TRIGPOL = 1, substitute “falling edge” instead of “rising edge” for TRIGGER_A.

Table 2-11 The effect of TRIGGER_A and RESET_V vs. VSTOP

VSTOP	Signal Asserted	VCOUNT @ Current CLOCK_V	VCOUNT @ Next CLOCK_Vn
0	None	VCOUNT	VCOUNT+1
0	Rising edge of TRIGGER_A	VCOUNT	VCOUNT+1
1	None	0	0
1	Rising edge of TRIGGER_A	0	1
1	Rising edge of TRIGGER_A	VCOUNT > 0	VCOUNT+1
1	RESET_V	VCOUNT	0
0	RESET_V	VCOUNT	0

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Table 2-11 shows the effect of TRIGGER_A and RESET_V on VCOUNT, for different settings of VTRIGRST. The table assumes TRIGPOL = 0. If TRIGPOL = 1, substitute “falling edge” instead of “rising edge” for TRIGGER_A.

Table 2-12 The effect of TRIGGER_A and RESET_V vs. VTRIGRST

VTRIGRST	Signal Asserted	VCOUNT @ Current CLOCK_V	VCOUNT @ Next CLOCK_V
0	Rising edge of TRIGGER_A	VCOUNT	VCOUNT+1
0	RESET_V	VCOUNT	0
1	Rising edge of TRIGGER_A	VCOUNT	0
1	RESET_V	VCOUNT	0

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2.7 Camera Control Signals

2.7.1 Definition

The camera controls CT and STROBE have two modes of operation:

Dynamic, driven by the HCTAB, VCTAB.
Static, driven by control bits.

For the dynamic mode, the functions for the camera controls are defined in Table 2-13.

Table 2-13 CT's to CTAB mapping

Signal	Comments
CT0 = VCON0 + (VCON1 * HCON0)	Suggested for camera shutter control.
CT1 = VCON2 * HCON1	Suggested for vertical sync control.
CT2 = HCON2	Suggested for horizontal sync control.
STROBE = VSTROBE * HSTROBE	Light strobe.

Note: In the table above, "" means a logical AND, "+" means a logical OR*

The CT and STROBE can be forced to static states, i.e., like registers written from the host. This is useful for cameras that demand a static value on some lines, or for very slow changing signals that can be controlled directly from software.

With each one of the camera controls CT, there are two associated control bits; CT0CON, CT1CON, CT2CON. These control bits are static. They define the behavior of CT as shown in Table 2-14, Table 2-15, Table 2-16 and Table 2-17.

Table 2-14 CT0CON

CT0CON	CT0
0 00b	Dynamic, defined by CTABs
1 01b	TBD
2 10b	0
3 11b	1

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Table 2-15 CT1CON

CT1CON	CT1
0 00b	Dynamic, defined by CTABs
1 01b	TBD
2 10b	0
3 11b	1

Table 2-16 CT2CON

CT2CON	CT2
0 00b	Dynamic, defined by CTABs
1 01b	TBD
2 10b	0
3 11b	1

Table 2-17 STCON

STCON	STROBE
0 00b	Dynamic, defined by CTABs
1 01b	TBD
2 10b	0
3 11b	1

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2.8 Host Access to VCTAB and HCTAB

When looking from the host side, the two tables are organized as one memory 32Kx32 bits, where bits 7..0 are the HCTAB and bits 15..8 are the VCTAB. The host access looks like 32-bit wide memory on the local bus. The HCTAB, VCTAB are mapped in the lower half. Access should be as a 32-bit word, where the upper 16 bits are unused. In order to modify only one table, a read-modify-write cycle must be performed. The host can access the tables anytime, as they are memory mapped on the local bus. Whenever the circuit detects host access, it will automatically connect the tables to the local bus. For this reason, it is good practice to stop the tables from incrementing while programming. This can be done with the CTABHOLD bit. This bit disables clocking of both tables, but leaves the state unchanged. If the tables are programmed when they are running, unpredictable controls might be given to the camera.

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2.9 The DMA Engine

Figure 2-3 shows the structure of the DMA engine. The DMA engine is designed around the PLX PCI90x0 controller. The DMA will be done in Chaining Mode (see the PCI90x0 manual).

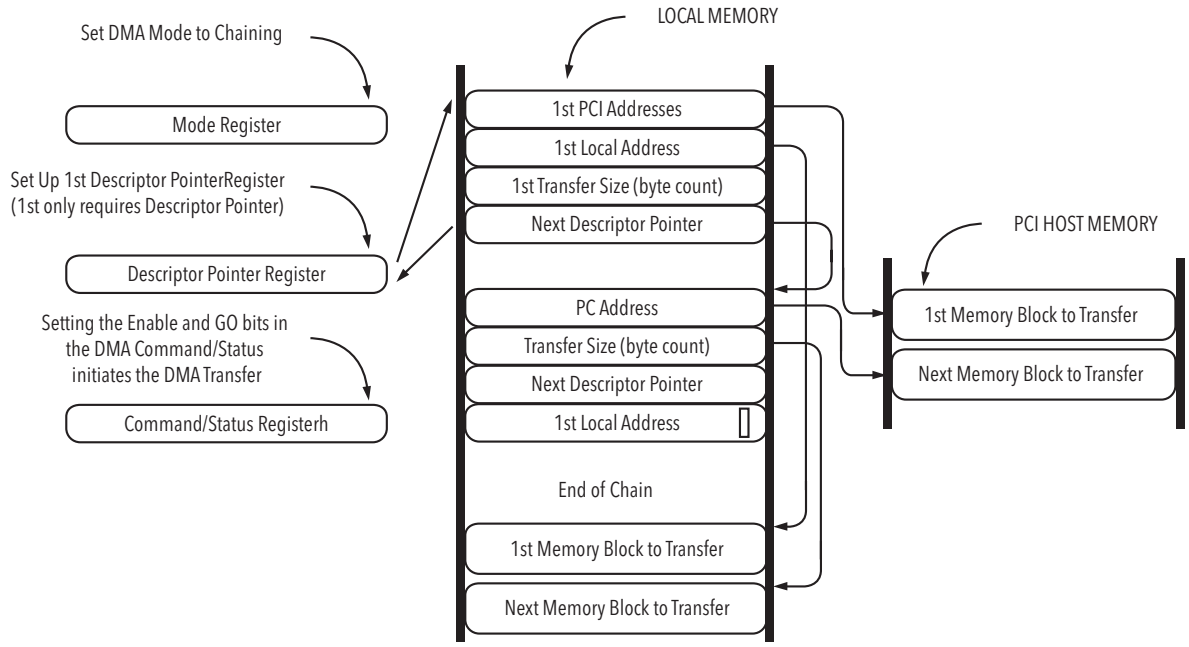


Figure 2-3 The DMA Engine

The host sets up descriptor blocks in the Descriptor Table. This table is a SRAM on the local bus, 32Kx32. When accessed from the host, the Descriptor Table looks like a continuous 32Kx32 block. When in DMA mode, the Descriptor Table is divided into two banks, bank 0 and bank 1, each one 16Kx32. In DMA mode, the active bank is selected by the DBANK (Descriptor BANK) bit. This bit will actually set address bit 15 of the Descriptor Table. DBANK is written by the host anytime. It is latched by any one of the following two conditions:

The DMA GO bit is written by the host (DMA_COM_CHx_GO register bit 1) at the beginning of a new sequence (for more information, see the Acquisition section).

The idea behind the two banks is to have the capability to change sequences in real time.

Each descriptor block has four entries, each one 32 bits wide and consists of the following:

- PCI address
- Local address
- Transfer count and attributes
- Address of next descriptor block

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To start a DMA transfer, the following conditions must be met:

The Bus Master enable bit in the PCI90x0 PCI configuration space is set.
The Descriptor Table has been loaded with descriptors.
The DMA channel enable bit has been set in the PCI90x0 DMA command/status register.
The address of the first descriptor has been written in the PCI90x0 descriptor pointer register.
The GO bit in the PCI90x0's DMA command/status register has been set.

The PCI90x0 loads the first descriptor block from the table into four internal registers and initiates the data transfer. The PCI90x0 continues to load descriptor blocks and transfer data until it detects the End Of Chain bit set in the next descriptor pointer register.

The DMA process can be paused by deasserting the DMA channel enable bit in the PCI90x0 DMA command/status register.

The DMA process can be aborted by setting the abort in the PCI90x0 DMA command/status register.

The PCI90x0 can be programmed to assert a DMA interrupt in two cases:

Completion of a block transfer.
All blocks have been transferred.

The interrupt is asserted on the local bus. Control logic will pick it up and assert the interrupt on the PCI (see the Interrupts Section).

The following sections discuss the four entries that make up one descriptor block. For more information, refer to the PLX PCI90x0 data book.

2.9.1 PCI (Destination) Address

This is a 32-bit address. It should be on a long word boundary as we always transfer 32-bit words. The address is loaded in the PCI90x0 PCI address register. This register is read/write-able from the PCI.

2.9.2 Local Bus (Source) Address

This is the address of the data on the local bus. For transfer of video data, it will be the address of the Video FIFO. In that case, a control bit can be set that will disable the incrementing of the local address during DMA transfers, i.e. all accesses on the local bus will be done to the same address. It is also possible to DMA other type of data between the Road Runner board and the PCI, like the CTABs and the Descriptor Tables.

The 12 MSBs of the local address entry are not used by the PCI90x0. Those bits will be used by external control logic (logic located outside the PCI90x0 chip) as attributes. Those attributes will control specific hardware functions related to current transfer.

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Control logic will snoop the local bus and whenever the PCI90x0 will read the local address from the Descriptor Table, it will latch the nine MS bits in the Attribute Register.

Note: To be able to snoop the reading of the attributes, it is imperative that the descriptors are loaded in the Descriptor Table on boundaries of four long words.

The following sections provide a description of the seven attribute bits.

EOX, End of Sequence

This bit denotes the end of sequence. If set, it tells the controller that the current descriptor is the last one in a transfer sequence. This bit is needed for controlling the latching of the DBANK bit. Used mainly for circular sequences, where the EOC bit is not set, see the next section.

BANK, BYPASS, BY8, LUT Controls

These three bits will control the LUTs during a DMA transfer. They can select Bank 1, Bank 0, or bypass mode. BY8 will set the LUTs in 8/12 bit mode. When the board is in slave mode, these functions are controlled by the HBANK, HBYPASS and HBY8 bits ("H" stands for host access), see the registers description.

MCHSEL

Channel MUX control in master mode. These two bits control the channel MUX for a specific transfer, while the board is in master mode.

FLUSH

FLUSH, Control bit for the local bus READY signal.

This signal will control the assertion of the local READY signal while the PCI90x0 is reading data from the video FIFO, see the section on local bus activity.

The other two attribute bits are TBD.

2.9.3 Transfer Size

This entry holds the size of the transfer in the 23 LSBs. Maximum transfer size per descriptor is 8 megabytes. PLX claims that zero size is legal. No transfer will take place, but the descriptor will be read in. Can be handy in controlling the events.

2.9.4 Descriptor Pointer

The 28 MSBs of this entry point to the address of the next descriptor block on the local bus. The four LSBs are control bits:

Bit 0 Reserved

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Bit 1 End Of Chain (EOC)

Bit 2 Interrupt after terminal count for this descriptor

Bit 3 Direction of transfer

If the EOC bit is set, the PCI90x0 will stop the DMA after transferring the current block. We can achieve a circular sequence, if the last descriptor points to the first one, and the EOC bit is not set. This is comes in handy if you want to have a continuous display, for example.

Bit 2 will enable us to assert an interrupt at the completion of the current descriptor.

Bit 3 will determine the direction of the DMA, 1 for local to PCI (i.e. the board is writing to the host memory).

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2.10 Sync Bus

2.10.1 Definition

The Sync Bus is used for synchronizing two or more Road Runner boards. This option is not available on the R3. A board can be a master or a slave on the Sync bus. Master/slave in this context relates to driving/receiving the camera-related control signals listed below. That will be determined by a software controlled bit, SYNCMASTER, see below. A master will drive all signals on the bus. A slave will receive all the signals. The bus is implemented with a daisy chain ribbon cable. All signals are TTL.

Figure 2-4 shows the structure of the Sync bus.

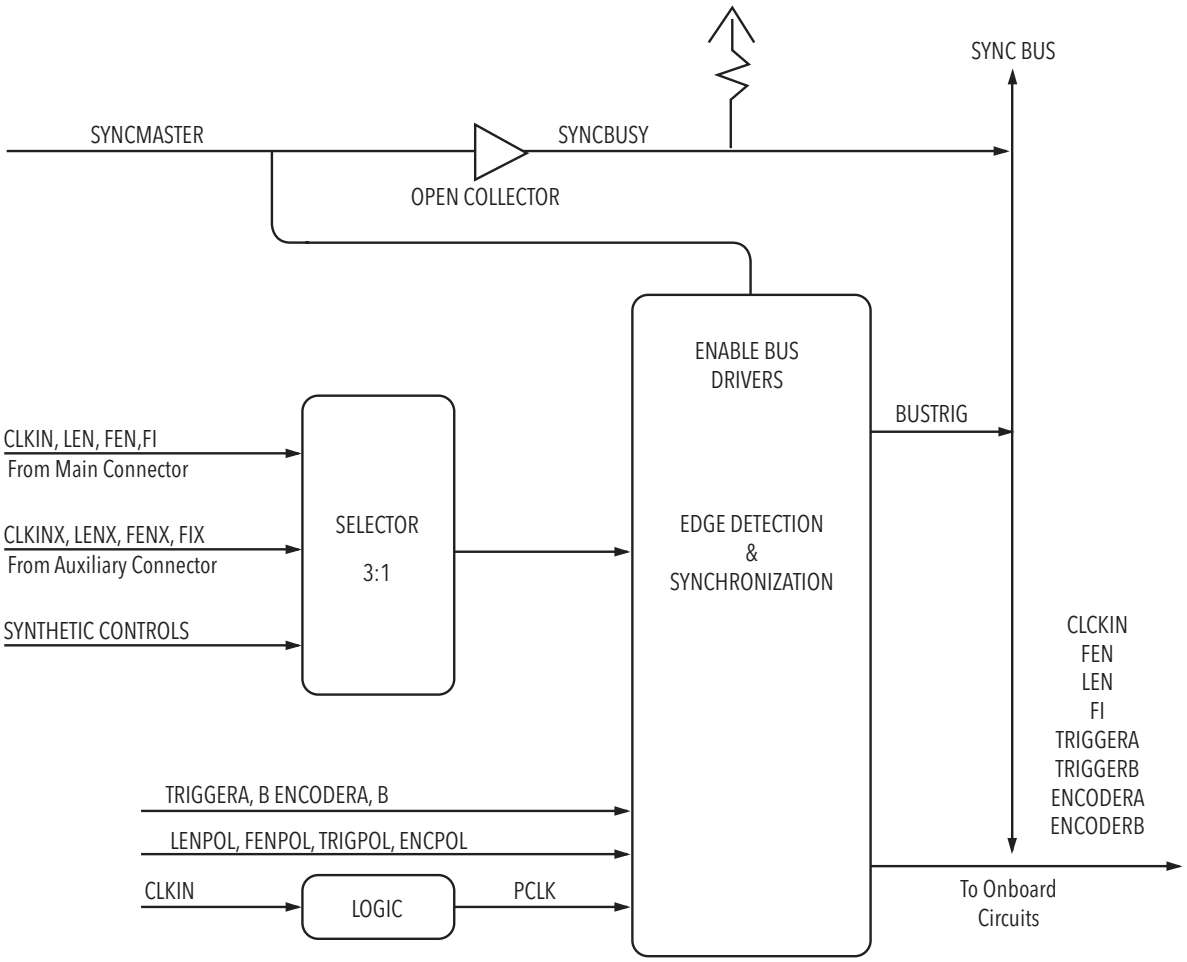


Figure 2-4 Sync Bus

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The idea behind the Sync bus is to be able to have one board supply the clock and the sync signals to other boards. These signals are TTL, which means that the RS422 receivers that accept these signals will be on the master board. Slave boards will pick up the signals from the Sync bus, instead of their own RS422 receivers. Camera cabling must be such that control signals mentioned above go only to the master.

The signals on the Sync bus include:

CLKIN
LEN
FEN
FI
TRIGGER_A
TRIGGER_B
ENCODER_A
ENCODER_B
SYNCBUSY
BUSTRIG
MXSYNC

The CLKIN and the FI are transmitted as-is over the Sync bus.

Most signals above are self-explanatory. The less obvious are described as follows.

Note: On the master board, CLKIN, LEN, FEN, and FI can be selected from the 62-pin connector, the main camera, or from the 60-pin connector, the auxiliary camera.

MXSYNC is a signal needed to synchronize some state machines on all boards.

SYNCBUSY is an open collector signal that the Sync bus master will assert when its SYNCMASTER bit is set to 1. Once a board asserts SYNCBUSY, a host cannot set SYNCMASTER on another board. SYNCBUSY will inhibit the assertion of SYNCMASTER. SYNCBUSY acts as a safety. The host can read the SYNCBUSY from any board.

BUSTRIG is a trigger signal derived from the ORing of SWTRIGA and TRIGGERA on the Sync bus master board. If a board is a slave on the Sync bus, its SWTRIGA will be substituted with the BUSTRIG. The idea is to be able to give a synchronous, safe acquisition command to boards synchronized through the Sync bus. The boards will all be set in triggered acquisition mode. A SWTRIGA/TRIGGERA will be asserted on the Sync bus master. This signal, synchronized to the PCLK, will be broadcast as BUSTRIG to all boards on the Sync bus.

The LEN, FEN, TRIGGER_A,B and the ENCODER_A,B signals on the bus will be first edge detected, stretched, and synchronized to the PCLK, on the master board. PCLK is the Pixel Clock derived from CLKIN. The slave boards will have to generate an identical copy of PCLK from CLKIN, by programming the CLKCON bits the same as on the master board. This will guarantee that all the interconnected boards will be reliably synchronized to camera, trigger, and encoder signals. It will also enable us to interface to control signals that are of very short duration, i.e., down to ~20nS.

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2.11 Interrupts

Interrupts to the PCI can come from two groups:

Interrupts generated in the PCI90x0 related to the operation of the PCI.
Interrupts related to the acquisition process.

The interrupts related to the acquisition process are listed as follows:

INT_FIFO Video FIFO overflow
INT_HW HW exception (local bus time-out, video FIFO imbalance, etc.)
INTD_DMA DMA circuit
INT_CTAB is the interrupt programmed in the CTABs.

INT_FIFO will be asserted if there is a Video FIFO overflow, i.e., the transfers over the PCI cannot keep up with the data rate from the camera.

INT_HW will be set when there is a local bus time-out or some other HW exception. On the local bus there is a timer, and if the bus hangs, it will reset the bus and assert an interrupt. This interrupt is also asserted if there is a FIFO imbalance. This condition is usually caused when the acquisition circuitry and the DMA engine are out of synchronization. In other words, when last pixel of the acquired frame is not the last pixel to be DMAed.

The DMA engine in the PCI90x0 can also assert an interrupt. It can be from the end of a sequence or from the completion of a descriptor (see Interrupt Control/Status register of the PCI90x0). It is important to note that in order to enable the DMA interrupts, the respective control bits must be set in the PCI90x0 control registers. The DMA circuit in the PCI90x0 cannot assert an interrupt on the PCI bus. It will assert the LINTO* (Local Interrupt Out) pin on the local bus. This signal will be routed to the local bus controller and ORed with interrupt signals. The output of this ORing will be connected to the LINTI* input of the PCI90x0 chip. This pin will generate an interrupt on the PCI bus, if the PCI90x0 PCI interrupt enable and the local interrupt enable bits are set (see the PCI90x0 Interrupt Control/Status register).

Each interrupt source has its own interrupt enable bit. The host can read/write each one of the interrupt bits. It is important to remember that all the interrupts share one single line on the PCI bus. The SW will have to find out who asserted the interrupt and act accordingly.

With each interrupt there is an associated CMDWRITE code. This code will enable host access to the specific interrupt (see the CON4 description). This is needed to be able to reliably perform a read-modify-write operation.

2.11.1 Example:

The following is a list of the bits that must be set to enable a DMA interrupt at the end of a DMA chain, i.e., after the last descriptor has been processed.

Set PCI interrupt enable, bit 8, in PCI90x0 Interrupt Control/Status register.

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Set PCI local interrupt enable (LINTI*), bit 11, in PCI90x0 Interrupt Control/Status register.
Set DMA Channel 1 interrupt enable, bit 19, in PCI90x0 Interrupt Control/Status register.
Set local interrupt input enable (LINTO*), bit 16, in PCI90x0 Interrupt Control/Status register.
Set bit 12, Channel 1 Done, in PCI90x0 DMA Command/Status register.

To clear this specific interrupt, a 1 must be written to bit 11 in the PCI90x0 DMA Command/Status register.

Now lets assume we want to enable an interrupt from the CTABs:

Program CTABs for desired interrupt.
Set ENINT0_CTAB in CON4.
Set PCI interrupt enable, bit 8, in PCI90x0 Interrupt Control/Status register.
Set PCI local interrupt enable (LINTI*), bit 11, in PCI90x0 Interrupt Control/Status register.

To clear the CTAB interrupt, set CMDWRITE to 1, write a 0 to INT0 in CON1, and set CMDWRITE back to 0.

For interrupts related to the operation of the PCI interface, see Interrupt Control/Status register in the PCI90x0 manual.

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2.12 The Acquisition Process

The Acquisition modes are controlled by the TRIGCON register as shown in Table 2-18.

Table 2-18 TRIGCON

TRIGCON	Function
0 00b	TRIGGERA active, B disabled
1 01b	Start on A, stop on B
2 10b	Continuous acquisition
3 11b	Triggered Termination

The process of acquiring data (writing) into the video FIFOs is independent of the process of reading data out of the video FIFOs. The readout is controlled by the DMA engine. The writing into the FIFOs is controlled by the acquisition command bits AQ.

Let's first analyze the writing into the video FIFOs. The description below is for acquisition modes. For those modes, the trigger mode control bits will be TRIGCON = 0. For new modes, see the next section.

The definition of the acquisition command is shown in Table 2-19:

Table 2-19 AQ Command

AQ	Function
0 00b	FREEZE
1 01b	ABORT
2 10b	SNAP
3 11b	GRAB

In non-triggered acquisition (TRIGAQCMD = 0), the acquisition command will be latched at the start of the next active frame. In triggered acquisition, TRIGAQCMD =1, the acquisition command will be latched at the beginning of the first frame after the trigger is asserted.

AQSTAT will mirror the type of acquisition in process. AQSTAT are actually the AQ bits latched at the start of the active video, after an acquisition command has been issued. They reflect the type of acquisition in progress. The following sections describe the four states.

2.12.1 FREEZE

When a FREEZE is asserted, acquisition will stop at the end of the current frame. This is usually used to stop the grab in an orderly manner and to return the acquisition to state 00, that is, the idle state.

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2.12.2 ABORT

The ABORT command will stop acquisition immediately, unconditionally. Writing a 01 in the acquisition command will stop all acquisition activity. The acquisition command AQ and the AQSTAT bits will read back 00, as the acquisition is in the idle state.

2.12.3 SNAP

This command will acquire a single frame (or frame/field in interlaced). After the frame has been acquired, the status will read back 00, the idle state.

After the AQCMD bits have been latched in the AQSTAT bits, at the start of the frame, they will be cleared. This way, the SW will know if a new SNAP/GRAB command has been issued while a SNAP is in progress.

A SNAP command can be issued while the Road Runner is acquiring in SNAP mode. This will make the Road Runner SNAP another frame. Issuing more than one SNAP command while acquiring in SNAP mode will have no effect.

A GRAB command can be issued while the Road Runner is acquiring in SNAP mode. After the SNAP is done, it will start a GRAB.

A FREEZE command while acquiring in SNAP mode will have no effect.

An ABORT command while snapping will immediately stop the acquisition.

2.12.4 GRAB

This command will cause the board to acquire continuously, beginning with the next active frame

A SNAP command can be issued while the Road Runner is grabbing. The next frame will be a SNAP operation.

A GRAB command can be issued while in GRAB mode. You do that if you want to change the active channels, see below.

A FREEZE command will stop the acquisition after the current frame.

ABORT will stop acquisition unconditionally.

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After the acquisition command is written, the bits shown in Table 2-20 are latched at the beginning of the next frame:

Table 2-20 Latched Bits

Control Bits	Description
AACTIVE, BACTIVE, CACTIVE, DACTIVE	The active channels bits.
TG1AQW, TG2AQW	The acquisition width/zoom.
WDX,WDY, WSX, WSY	The auxiliary acquisition window parameters.

To change a zoom factor, to start/stop acquiring into a different set of channels, or to change the display window, a new acquisition command must be issued.

Figure 2-5 shows the behavior of the AQCMD and AQSTAT bits. Only the SNAP while displaying and acquire on trigger while displaying need more discussion.

Assume we have a live display and we want to SNAP a frame into system memory.

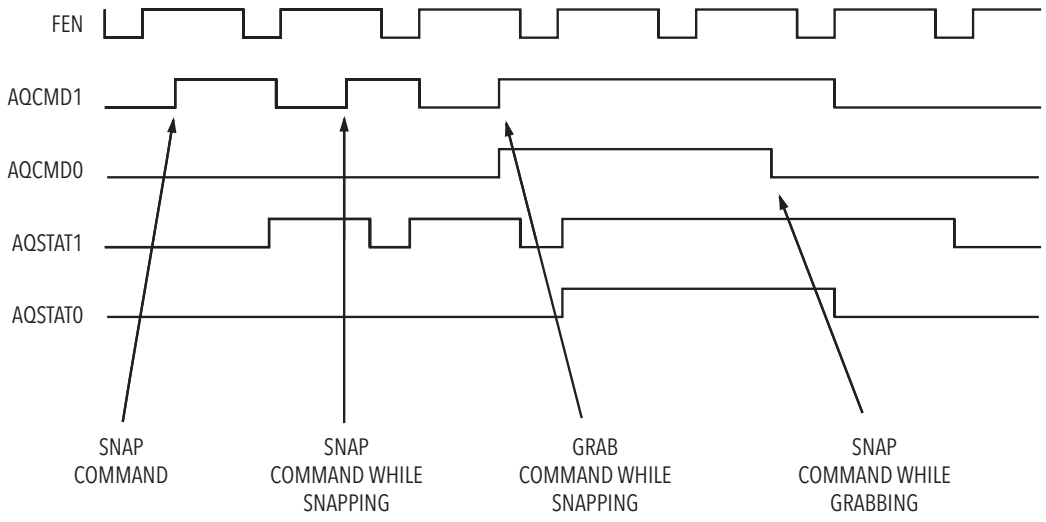


Figure 2-5 AQCMD and AQSTAT Bits Behavior

2.12.5 Comments on the DBANK Bit

There is a synchronization problem as to when the video FIFO's outputs are ready for the DMA engine. Looking at the A,B,C,DACTIVE bits is not reliable enough. The reason is that these bits are related to the camera VB. These signals control the writing

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into the FIFO. But on the time scale, the output of the video FIFOs is uncorrelated from its input (that is the purpose of a FIFO). Here is the place that the EOX bit can help.

Assume the Descriptor Table bank 0 has a circular sequence for host acquisition only, and bank 1 has a circular sequence for display and host acquisition. If during continuous grab we want to turn the display ON/OFF, we have to issue a new GRAB command and set the corresponding Descriptor bank.

The new grab command with the A,B,C,DACTIVE bits is latched at the beginning of the vertical active. We cannot safely change the DBANK bit at this point in time, as there might be data in the video FIFOs. We can change the Descriptor bank only after we know that a sequence has been processed. The last descriptor in a sequence will have an EOX bit. The control circuitry will check this bit and will latch the DBANK bit just before the 90x0 reads the next descriptor, which should be the first descriptor in a sequence. Note that the EOX bit is different from the EOC (End Of Chain) bit, used in the 90x0. The EOC bit is used for marking the end of the DMA. In a circular sequence, EOC will not be set. The last descriptor will point to the first descriptor, so that we get a loop. The EOX bit, in the last descriptor, will mark the end of the frame, and the point in time where we can safely change the Descriptors bank.

Before the DMA is started, the DBANK bit will get latched when the GO bit is written in the PCI90x0 DMA Command/Status register.

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2.13 Advanced Acquisition Modes

Two new acquisition modes are available. These modes are set by the trigger control bits TRIGCON

2.13.1 Triggered Grab Command

In this mode, the start of the acquisition will be initiated by TRIGGER_A. The end of the acquisition will be initiated by TRIGGER_B. In this mode, asserting TRIGGGER_B is identical to a FREEZE command. Set CTABs, AQCMD, TRIGAQCMD, and descriptors for triggered GRAB.

Note: The triggered Grab Command mode can be done from external hardware, software, or a combination of both. SWTRIG_A,B have the same effect as TRIGGER_ A,B.

2.13.2 Continuous Acquisition

In this mode, the Road Runner will acquire continuous acquisition. The CTABs, AQCMD, and TRIGAQCMD bits will not be involved in this type of acquisition. The acquisition will be controlled by TRIGGER_A only. Whenever TRIGGER_A is asserted HI, data will be acquired. The same effect can be achieved by using SWTRIG_A. In both cases the command will also be broadcast on the Sync bus by BUSTRIG. To initiate a continuous acquisition, the sequence of events would be:

Load Descriptor Table
Enable DMA channel DMA GO bit
Set TRIGCON = 2
Assert SWTRIG_A (or wait for TRIGGER_A)
When done, assert GRNTCTL bit to flush the Video FIFO
Check Video FIFO empty
Abort DMA operation

To be on the safe side, the descriptors will have to “cover” more memory than expected data. When done, the GRNTCTL will make sure that the last eight entries in the FIFOs have been read. After the video FIFOs are empty, a DMA abort is issued since there is no more data but there are more descriptors.

An interrupt can be asserted at the start or the end of the acquisition, depending on bit CONTINTPOL in CON4.

2.13.3 Triggered Termination (Start-Stop)

This mode is used to terminate the acquisition immediately, without waiting for the end of the frame. It is slightly different than the assertion of the ABORT command. It will end the acquisition process and the DMA process in a graceful way. Acquisition

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can be started normally with a GRAB command, or triggered by TRIGGERA. The acquisition can be terminated by TRIGGERA or TRIGGERB, depending on the setting of bit TRIGASTOP in CON10.

TRIGASTOP	Meaning
0	Terminate acquisition assertion of TRIGGERB
1	Terminate acquisition with de-assertion of TRIGGERA

In the second mode, termination by de-assertion of TRIGGERA, TRIGGERA can still be used to start the acquisition by its assertion. The assertion polarity is controlled by TRIGPOL.

2.13.4 Two Timing Generators

On the Road Runner there are two timing generators: TG1 and TG2. The second timing generator is handy for generating a display window that is different from the acquisition window. For example, you acquire a 2Kx2K image but want to display only a window 512x512. The whole 2Kx2K image will be DMAed into system memory according to TG1, the first timing generator. The 512x512 section will be DMAed into the VGA memory according to the TG2 timing generator.

Each timing generator needs two types of information to be able to generate the controls for writing an image into a FIFO:

Horizontal and vertical size of the image to be acquired.

The width of the data to be acquired (8/16/32 bit/pixel, 8bit/pixel zoomed 1/2).

Figure 2-6 shows the structure of the two timing generators. TG1 is driven by the main acquisition window, size HWxVW and by TG1AQW0..1. HW, VW is generated by the CTABs. The TG1AQW0..1 (Timing Generator #1 AcQuisition Width) bits are set by the host. For each channel we can select the TG1 or TG2 timing controls, see TGA,B,C,D in control register 6.

Note: The second timing generator is only avaliable with special firmware. Contact BitFlow for more information.

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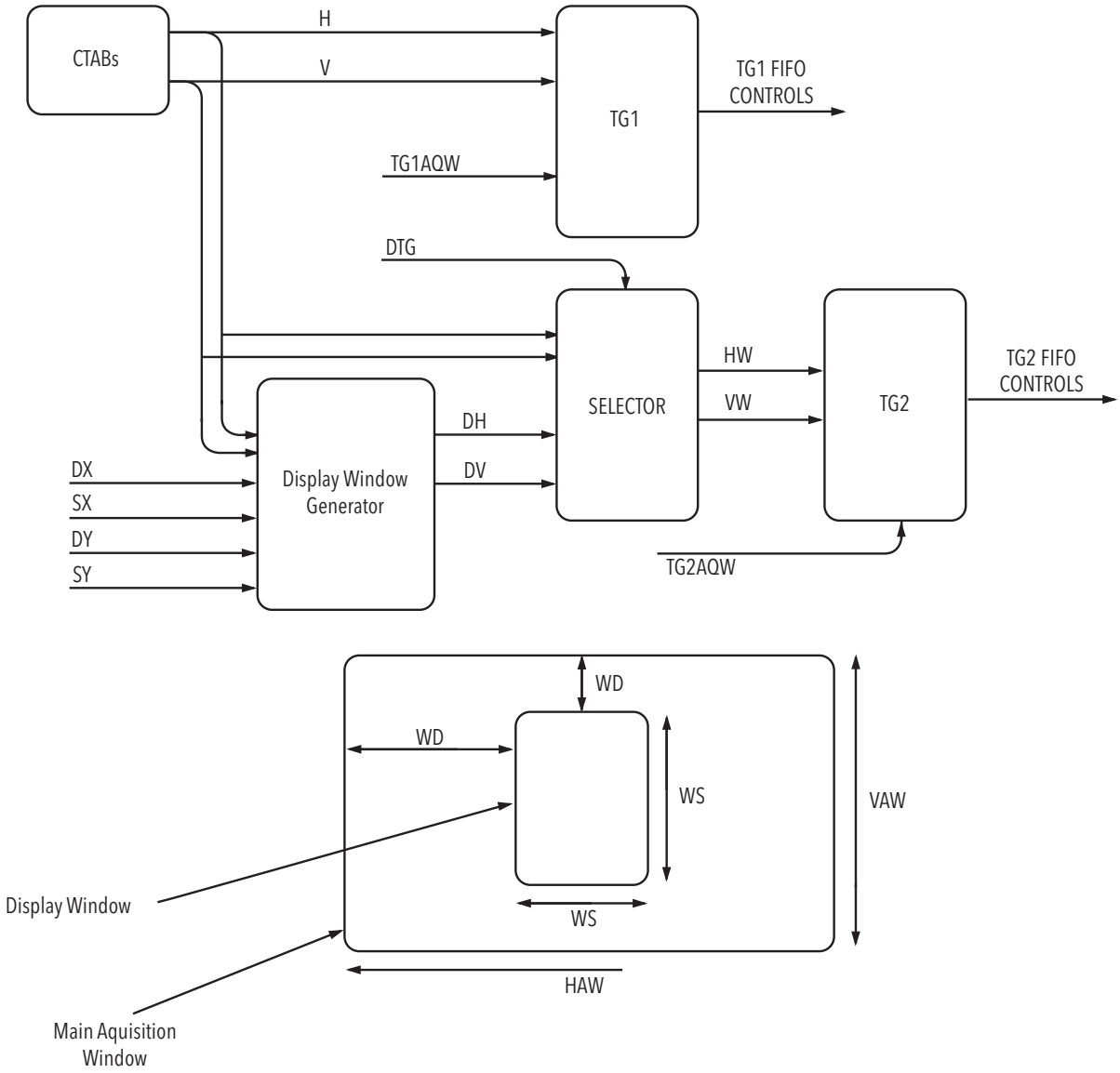


Figure 2-6 Two Timing Generators Structure

TG2 is driven by HW, VW, or by a sub-window of HW, VW. This sub-window is generated by the "display window generator." The sub-window is also called the "display window," as its main use is for display purpose. The TG2AQW0..1 will determine the acquisition width for TG2. These two bits are set by the host. There is a 2:1 selector that select between the full window or the display window for TG2. This selector is controlled by the DTG bit. The size of the display window and its coordinates in the main window are determined by WSX, WSY, WDX, WDY. These values are computed from four registers: SX, SY, DX, DY that are written by the host. Figure 2-7 shows how the hardware computes WSX, WSY, WDX, WDY from SX, SY, DX, DY. The description is for the vertical axis. For the horizontal axis, the circuit is similar.

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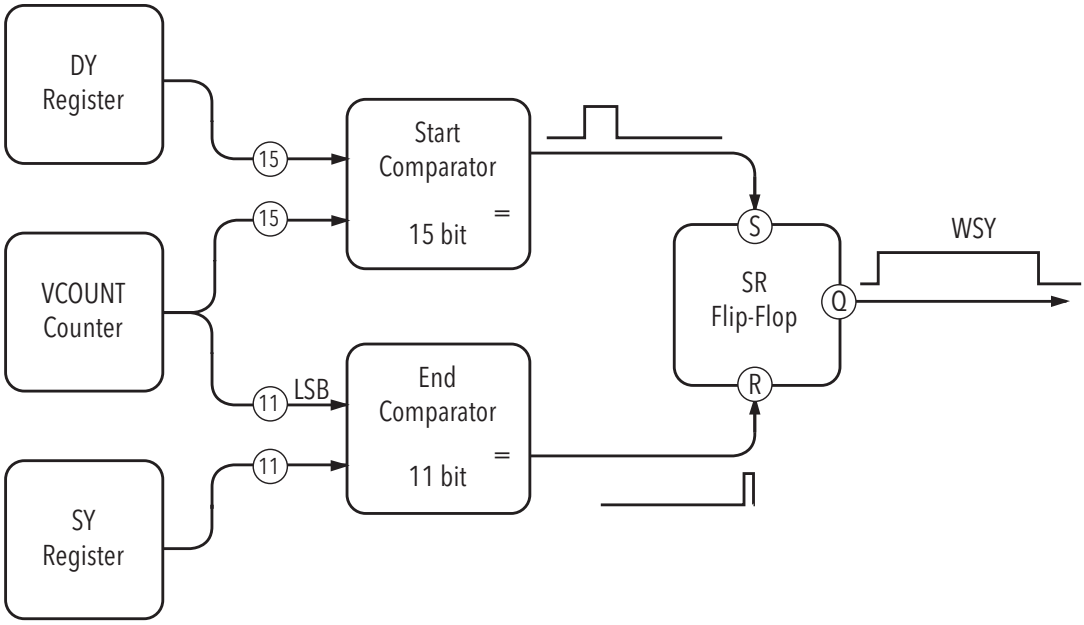


Figure 2-7 Computation of WSY, WDY from DY, SY

VCOUNT is the address counter for the vertical CTAB. It is 15-bit and counts up to 32K. The Start comparator will compare the VCOUNT with the value in register DY. When VCOUNT reaches the value of DY, the Start comparator will detect that and set a flip-flop, Q.

The End comparator will compare the 11 LSBs of VCOUNT to the value in register SY. When it detects equality, it will reset the Q flip-flop. Q will mark the vertical display window. DY, SY will be a function of the vertical acquisition window programmed in the vertical CTAB.

Example:

Lets assume a vertical acquisition window of 1K, starting at address 800H in the vertical CTAB. We want to have a display window of the middle 512 lines, from line 256 to line 767. DY will be set to 900h, SY to 300h.

SY needs some comments. In the example above, you would want to set SY to B00h to detect the end of the display window. If you know that you want a vertical display window of maximum 2K, 11 bits is enough. 300H are the 11 LSBs of B00h.

Lets call Vstart the starting coordinate of the vertical acquisition window. The general formula linking Vstart, WDY, WSY to DY, SY is:

DY = Vstart + WDY
SY = MOD2048(DY + WSY)

Where MOD2048 means computations done modulo 2048.

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For the horizontal case we get:

DX = Xstart + WDX
SX = MOD512(DX + WSX)

Xstart is the starting coordinate of the horizontal acquisition window in the horizontal CTABs. In the horizontal axis we have MOD512 because it is clocked by 1/4 the pixel clock (see the CTAB section).

Each one of the FIFO channels A,B,C,D has an associated control bit: TGA, TGB, TGC, and TGD that will select between TG1 and TG2.

The horizontal size resolution of the main window and display windows is on boundary of four pixels. The vertical size resolution of the main and display windows is on boundary of one pixel.

DX is on boundary of four pixels. DY is on boundary of a single pixel.

The maximum size of SX is 512. The maximum size of SY is 2K.

DX,DY,SX,SY are latched at the beginning of the next vertical active if an acquisition command has been written.

Lets try to describe the sequence of events needed to continuously acquire an image in system memory and to display a portion of that image on the VGA. While displaying, we would like to pan/scroll the display window over the whole image.

As a strategy, we could ping-pong between the two Descriptor banks. In each bank, the descriptors are alternating between display and host memory. While acquiring/displaying from Descriptors bank 0, bank 1 will be updated with descriptors with the next position/size of the display window. Once this is done, the host will have to write the corresponding new DX, DY, SX, SY for the display window. Now remember that these will be latched at the beginning of the first frame after an acquisition command has been written. When this happens we would also like the DBANK bit to point to bank 1. DBANK will be latched at the beginning of a DMA sequence, i.e., before processing the first descriptor in that sequence.

Special care is needed when writing the acquisition command and the DBANK bit. You must guarantee that both will take effect on the same frame, otherwise the descriptors will not match the display window. The “danger zone” is immediately before and after the start of the frame. There is a variable amount of time between the start of the frame and the start of the DMA of that frame. You might write the AQ bits just before and the DBANK after the start of the frame and miss the DBANK. This situation can be prevented by pausing the DMA process until after the DBANK gets written. You could write the AQ bits and the DBANK just after the start of the frame. AQ missed the current frame, but DBANK could make it. The safest point in time is after the start of the frame and after the start of the first descriptor in the sequence. That will give us almost a whole frame time to write two registers. There are a couple of ways to do this. One way would be to have the first descriptor issue an interrupt. Another way would be to mark a safe descriptor and poll. The two extra attribute bits could be used for this purpose.

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Interfacing

Chapter 3

3.1 Input Signals

The trigger and the encoder input signals on the Road Runner/R3 board have been designed to interface to both TTL and RS422 signals. Figure 3-1 shows the electrical structure for the receiver.

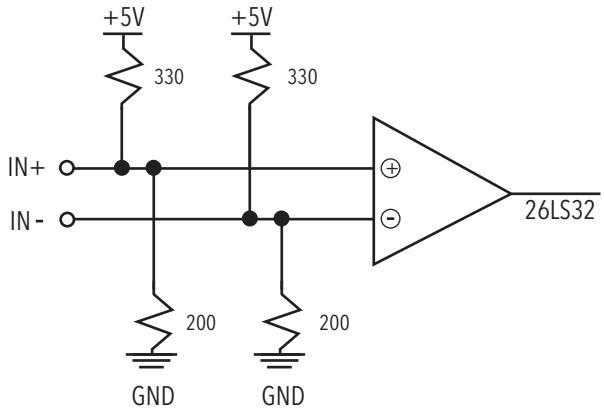


Figure 3-1 Input Circuit for the Encoder and Trigger Signals

Each differential input is biased at ~2V. For a RS422 input signal, connect to the IN+ and IN- inputs. For a TTL signal, connect the single ended input to IN+ (or IN-) and leave the other input unconnected. The unconnected input will be biased at ~2V, the TTL signal will swing between 0.8V and 2.4V. The ground of the TTL signal must be connected to the Road Runner's ground (pin 6 on the P5 connector, pin 5 on the CON-RUN-IO connector).

The minimum drive requirement for the TTL driver is 2 mA source at 2.4V and 10 mA sink at 0.4V. A 74F125 device or equivalent is adequate. Please note that an open collector device will not do work. You will have to add a pull-up resistor of about 100 Ohm.

The trigger and the encoder inputs are edge detected. The minimum pulse width is 15 nanoseconds.

Figure 3-2 illustrates the proper connection for a TTL trigger or TTL encoder source to a Road Runner/R3 board.

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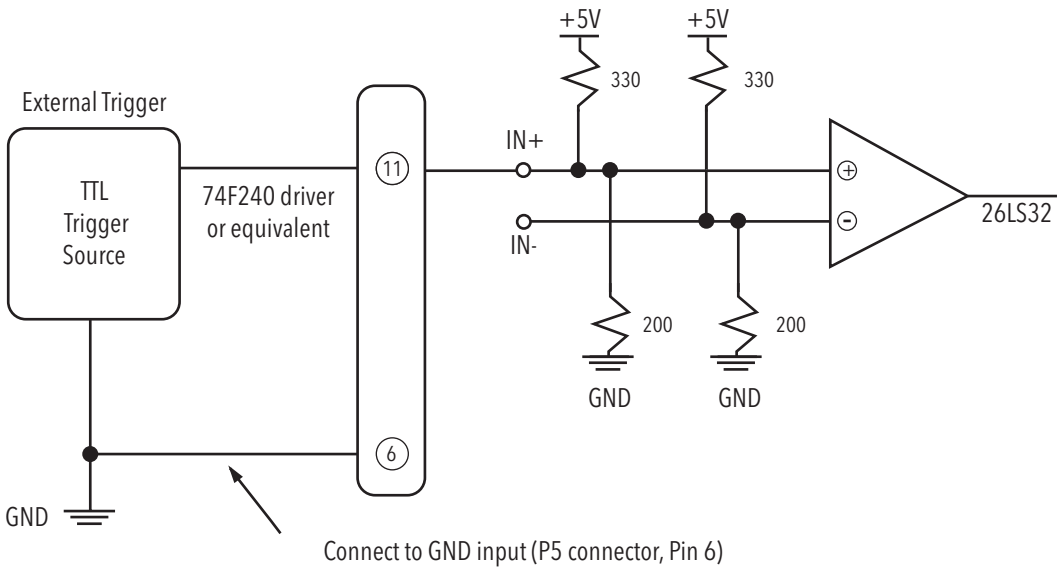


Figure 3-2 Connecting an External TTL Trigger or Encoder to a Road Runner Board

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PCI Interface

Chapter 4

4.1 Introduction

The registers, LUTs, CTABs and the PCI90x0 registers will take up 2 Mbytes (Mb) of memory on the local bus. On the PCI side, this 2 Mb will be located at the address assigned by the BIOS. On the local bus mapping registers will place the 2 Mb at address 000h. Only address bits 20-0 will be needed to access all registers on the local bus.

All accesses to the board should be done as 32-bit long words.

The PCI90x0 registers are available on the local bus and on the PCI bus, except for the DMA register that are available on the local bus only. The PCI can access the DMA registers by doing an access to the local bus.

Note: The PCI90x0 takes up to two distinct address spaces on the PCI bus: one for its internal registers, and one for the local bus.

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4.2 Board Addressing

The following is an address map of the local bus:

Table 4-1

Address (hex)	
0000 0000	PCI90x0 chip,130x32
000A 0000	CTABS, 32Kx32
000C 0000	Descriptors Table, 32Kx32
000F 0000	Video FIFO
000E 0004	Read LUT address
000E 0008	Read LUT data port
000E 000C	CON0, Control register 0
000E 0010	CON1
000E 0014	CON2
000E 0018	CON3
000E 001C	CON4
000E 0100	CON5
000E 0104	CON6
000E 0108	CON7
000E 010C	CON8
000E 0110	CON9
000E 0114	CON10
0008 0000	CON11
000E 0118	CON12

4.2.1 Example 1:

The range for PCI to local address will be loaded with the value FFE0 0000h from the EEPROM. This will tell the BIOS that the Road Runner needs 2 Mb of address space. The remap register will be loaded with the value 0000 0000h, which means that on the local bus, the 2 Mb window will be mapped at address 0.

Lets assume the BIOS assigned the Road Runner a PCI base address of 1220 0000h.

Lets assume the PCI wants to access register CON3. On the local bus, CON3 is at address 000E 0018h. The host should assert on the PCI address 122E 0018h.

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4.2.2 Example 2:

Now lets assume the host wants to access the DMA Command/Status register. This register can be accessed only from the local bus. The PCI can access this register by doing an access to the local bus. The register is at offset 128h from the PCI90x0 base address (chip select) on the local bus. On the local bus, the PCI90x0's base address (chip select) is mapped at address 0000 0000h. To access this register from the local bus, address 0000 0128h must be asserted on the local bus. For the host to access this register, it will have to assert on the PCI address 1220 0128h.

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4.3 Road Runner Non-Register Memory

This section contains descriptions of all of the memory on the Road Runner/R3 that is not used for control registers.

4.3.1 CTABS

HCTAB in bits 7-0, VCTAB in bits 15-8. Both LUTs accessed as one 32-bit word. Table size is 32K.

4.3.2 LUTADDR

This is a LUT address pointer. Addresses are for two lanes of 16in-16out, two lanes of 2in-16out, or four lanes of 8in-8out, depending on the memory installed and BY8 bit. For the four lanes of 8in-8out, the LUTADDR[31..0] holds four 8-bit address pointers. For the two lanes of 12in-16out, the LUTADDRR[31..0] holds two 12-bit address pointers. The two address pointers are right justified in the LSW and in the MSW. For the two lanes of 16in-16out, the LUTADDRR holds two 16-bit address pointers.

The bank pointed to is determined by the BANK bit.

4.3.3 LUTDATA

LUT data port, either 4x8 or 2x16, 1x32.

4.3.4 QTABS

Descriptor Tables, a 32Kx32 memory (Road Runner only).

4.3.5 VFIFO

This is the output of the Video FIFO. In DMA, the video channel selected will be determined by the MCHSEL in the attribute register.

In direct slave access, the channel the video channel selected will be determined by the SCHSEL bits in CON2. This mode is for testing purposes only.

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Register Specifications

Chapter 5

5.1 Introduction

This section enumerates all of the bitfields in all of the registers on the Road Runner/R3. All of the registers are 32 bits wide. These wide registers are named CON0, CON1, etc. Each registers is broken into one or more bitfields. Bitfields can be from one to 32 bits wide. Each bitfield controls a specific function on the board.

5.1.1 Bitfield definitions

What follows is an explanation of bitfield definition sections.

BITFIELD R/W, CON0[7..0

Bitfield explanation.

The definitions is broken into three sections.

Table 5-1

Section	Meaning
Bitfield name	This is the name of the bitfield. This name is used to program this bitfield from software or from within a camera configuration file. When programming bitfields from software using a Peek or Poke function, the bitfield is preceded with "REG_". For example the bitfield CFREQ is referred to in software as REG_CFREQ.
Bitfield details	This section describes how the bitfield is accessed. The first part describes the how the bits can be accessed. For example R/W means the register can be both read and write. See the next table for details. The second part is the wide register that the bitfield is located in. In the example above this bitfield is in CON0. The part in square brackets indicate which bits in this register the bitfield takes up. For example, [7..0] means the bitfield has 8 bits, and it occupies bit positions 0 to 7 in CON0.
Bitfield explanation	This section explains the purpose of the bitfield in detail. Usually the meaning of every possible value of the bitfield is listed.

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Table 5-2

Access	Meaning
R/W	Bitfield can be read and written.
RO	Bitfield can only be read. Writing to this bit has no effect.
WO	Bitfield can only be written. Reading from this bit will return meaningless values.

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5.2 CON0 Register

Bit	Name
0	MUXA
1	MUXA
2	MUXA
3	MUXB
4	MUXB
5	MUXB
6	MUXC
7	MUXC
8	MUXC
9	MUXD
10	MUXD
11	MUXD
12	SYNCSEL
13	SYNCSEL
14	SYNCSEL
15	PROGFIFO
16	CLKCON
17	CLKCON
18	CLKCON
19	CFREQ
20	CFREQ
21	CFREQ
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

Note: See the document "Mux Codes.pdf" for alternate MUX codes.

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MUXA R/W, CON0[2..0]

These bits control the multiplexing of Channel A:

MUXA	Function	Packing	
0 000b	T0	1 → 4	8-bit pixels packed into 32-bit word
1 001b	T1,T0	2 → 4	16-bit pixels packed into 32-bit word
2 010b	T3,T2,T1,T0	4 → 4	32-bit pixels transferred direct
3 011b	T1	1 → 4	8-bit pixels packed into 32-bit word
4 100b	T1,T0	2 → 4	10-bit pixels shifted by 2 and packed as 4, 8-bit pixels
5 101b	T1,T0	2 → 4	12-bit pixels shifted by 4 and packed as 4, 8-bit pixels
6 110b	T3,T2,T1,T0	2 → 4	Two odd/even 10 bit pixels both shifted by 2 and packed as 4, 8-bit pixels
7 111b	T2,T0	2 → 4	16-bit non-inverting taps

MUXB R/W, CON0[5..3]

These bits control the multiplexing of Channel B:

MUXB	Function	Packing	
0 000b	T0	1 → 4	8-bit pixels packed into 32-bit word
1 001b	T1,T0	2 → 4	16-bit pixels packed into 32-bit word
2 010b	T3,T2,T1,T0	4 → 4	32-bit pixels transferred direct
3 011b	T1	1 → 4	8-bit pixels packed into 32-bit word
4 100b	T1,T0	2 → 4	10-bit pixels shifted by 2 and packed as 4, 8-bit pixels
5 101b	T1,T0	2 → 4	12-bit pixels shifted by 4 and packed as 4, 8-bit pixels
6 110b	T1,T0	2 → 4	Two odd/even 10 bit pixels both shifted by 2 and packed as 4, 8-bit pixels
7 111b	T3,T1	2 → 4	16-bit inverting taps

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MUXC R/W, CON0[8..6]

These bits control the multiplexing of Channel C:

MUXC	Function	Packing	
0 000b	T2	1 → 4	8-bit pixels packed into 32-bit word
1 001b	T3,T2	2 → 4	16-bit pixels packed into 32-bit word
2 010b	T3,T2,T1,T0	4 → 4	32-bit pixels transferred direct
3 011b	T3	1 → 4	8-bit pixels packed into 32-bit word
4 100b	T3,T2	2 → 4	10-bit pixels shifted by 2 and packed as 4, 8-bit
5 101b	T3,T2	2 → 4	12-bit pixels shifted by 4 and packed as 4, 8-bit
6 110b	T3,T2	2 → 4	14-bit pixels shifted by 6 and packed as 4, 8-bit
7 111b	T0	1 → 4	8-bit pixels packed into 32-bit word

MUXD R/W, CON0[11..9]

These bits control the multiplexing of Channel D:

MUXD	Function	Packing	
0 000b	T2	1 → 4	8-bit pixels packed into 32-bit word
1 001b	T3,T2	2 → 4	16-bit pixels packed into 32-bit word
2 010b	T3,T2,T1,T0	4 → 4	32-bit pixels transferred direct
3 011b	T3	1 → 4	8-bit pixels packed into 32-bit word
4 100b	T3,T2	2 → 4	10-bit pixels shifted by 2 and packed as 4, 8-bit
5 101b	T3,T2	2 → 4	12-bit pixels shifted by 4 and packed as 4, 8-bit
6 110b	T3,T2	2 → 4	14-bit pixels shifted by 6 and packed as 4, 8-bit
7 111b	T1	1 → 4	8-bit pixels packed into 32-bit word

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SYNCSEL R/W, CON0[14..12]

These bits, together with the SYNCMASTER bit, will select the source of the video to the board including: the main camera from the 62-pin connector, the auxiliary camera from the 60-pin connector, the Sync bus, or a synthetic image.

If SYNCMASTER = 1, the board drives the Sync bus. In this case, the board can select camera 0, camera 1, or an internally-generated synthetic image and synthetic controls. Whatever controls are selected, they will be broadcast on the Sync bus. The control signals involved are PCLK, LEN, FEN, FI.

SYNCSEL	Meaning
0 000b	Gets controls from main camera on the 62-pin connector.
1 001b	Gets controls from the auxiliary camera on the 26-pin connector.

The codes below are for testing. They will disconnect controls and data from the two cameras and generate synthetic controls (LEN, FEN) and data. The clock will be determined by setting CLKCON = 111B and selecting a frequency with CFREQ.

SYNCSEL	Meaning
2 010b	Ramp
3 011b	00000000h
4 100b	FFFFFFFh
5 101b	AAAAAAAAh
6 111b	55555555h
7 111b	ABCDEFABh

If SYNCMASTER = 0, the board is a slave on the Sync bus. It will receive the control signals from the Sync bus. Data will be from the four 8-bit ports. A slave on the Sync bus cannot generate a synthetic image.

PROGFIFO RW, CON0[15]

This bit is used to program the FIFOs on the R3 Boards.

PROGFIFO	Meaning
0	Normal FIFO operation
1	Program FIFOs

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CLKCON R/W, CON0[18..16]

These bits control the PCLK (Pixel Clock), the video sampling clock. Basically, PCLK is derived from CLCKIN, the clock received from the camera. CLCKIN can be trimmed, to take in account the skew between the clock and the data on the transmission lines.

CLKCON	Meaning
0 000b	Use rising edge of CLKIN
1 001b	Use rising edge of CLKIN delayed by 10 ns
2 010b	Delay CLCKIN by 20 ns
3 011b	Reserved
4 100b	Use falling edge of CLKIN
5 101b	Invert CLKIN, delay 10 ns
6 110b	Invert CLKIN, delay 20 ns
7 111b	Use the internal clock generator (this is a test mode)

CFREQ R/W, CON0[21..19]

These bits control the frequency of CLCKOUT, the internal clock generator. This clock can drive a camera.

CFREQ	Meaning
0 000b	0
1 001b	2.5 MHz
2 010b	5 MHz
3 011b	7.5 MHz
4 100b	10 MHz
5 101b	15 MHz
6 110b	20 MHz
7 111b	30 MHz

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5.3 CON1 Register

Bit	Name
0	AQCMD
1	AQCMD
2	AQSTAT
3	AQSTAT
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	TOPA
14	TOPB
15	TOPC
16	TOPD
17	AEFA
18	AEFB
19	AEFC
20	AEFD
21	FI
22	FIRSTFI
23	FI_CON
24	FACTIVE
25	FCOUNT
26	FCOUNT
27	FCOUNT
28	EFA
29	EFB
30	EFC
31	EFD

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AQCMD R/W, CON1[1..0]

The acquisition command can be written any time by the host. After it has been written, it will be latched by the first start of the frame (end of vertical blank).

The AQCM bit will read back the last command written, until it gets latched. After it gets latched, the AQCMD will read 11 for GRAB, 00 for all other cases. The rationale is that the ACMD bits will give you the state of the next frame.

Note: The acquisition command bits have been grouped in a register with RO bits. Being the only bits written in the register, there is no need for a R-M-W cycle. The assumption is that whenever we change command, we will always write the two bits together.

There is another reason the AQCMD bits are the only bits written in this register: we must know when a new acquisition command gets written, even if it is identical to the previous command. The effect of writing to this register will start the state machine controlling the acquisition logic.

AQCMD	Command
0 00b	FREEZE
1 01b	ABORT
2 10b	SNAP (field/frame, depending on AQFRM bit)
3 11b	GRAB continuously

AQSTAT RO, CON1[3..2]

Acquisition status.

AQSTAT	Status
0 00b	FREEZE
1 01b	Reserved
2 10b	SNAP (field/frame, depending on AQFRM bit)
3 11b	GRAB continuously

TOPA, TOPB, TOPC, TOPD RO, CON1[13], CON1[14], CON1[15], CON1[16]

Internal states of FIFO's control. For diagnostics.

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AEFA, AEFB, AEFC, AEFD RO, CON1[17], CON1[18], CON1[19], CON1[20]

FIFO's Almost Empty Flags.

AEFA,AEFB,AEFC,AEFD	Meaning
0	Eight or more than eight entries in FIFO
1	Less than eight entries in the FIFO

FI RO, CON1[21]

Field index. Definition of Odd/Even depends on the camera.

FIRSTFI RO, CON1[22]

This bit is the FI bit latched at the beginning of the acquisition. This information is needed so that the software can correctly display an interlaced image.

FI_CON RO, CON1[23]

This bit is the instantaneous value of the FI input signal (P1 pins 12 and 13). Note the bit FI above is the value of the FI input signal latched at the end of the VB. The following register must be set in order for this bit to work correctly: SYNCSEL = 0 and FISEL = 0.

FACTIVE RO, CON1[24]

Active video bit.

FACTIVE	Meaning
0	Camera is in the vertical inactive (i.e. vertical blank)
1	Camera is in the vertical active area

FCOUNT RO, CON1[27..25]

Frame counter. This 3-bit counter is incremented every frame. The register is incremented at the end of the frame, when the VCTAB column VEND, goes high.

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EFA, EFB, EFC, EFD

RO, CON1[28], CON1[29], CON1[30], CON1[31]

Video FIFO's empty flags.

EFA,EFB,EFC,EFD	Meaning
0	FIFO not empty
1	FIFO empty

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5.4 CON2 Register

Bit	Name
0	GPOUT0
1	GPOUT1
2	GPOUT2
3	ENGPOUT0
4	ENGPOUT1
5	ENGPOUT2
6	ENCT0
7	ENCT1
8	ENCT2
9	NORLUTS
10	ADVANCE
11	BURST
12	BURST
13	FRZFIFO
14	ONEQTB
15	QTBSRC
16	GRNTCTL
17	INT_DMA
18	INT0_CTAB
19	INT1_FIFO
20	INT2_HW
21	SCHSEL
22	SCHSEL
23	LTEOX
24	LTMBANK
25	LTMBYPASS
26	LTMBY8
27	LTMCHSEL0
28	LTMCHSEL1
29	LTFLUSH
30	TRIGINT
31	TRIGSTAT

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GPOUT0, GPOUT1, GPOUT2

R/W, CON2[0], CON2[1], CON2[2]

General purpose bits for camera control are available on P1 and P2. On the P1 connector, those bits can be either TTL or RS422 depending on the setting of the switch S2. On the P2 connector, they are available in both RS422 and TTL format. The TTL version can be tristated by the ENGPOUT bits.

ENGPOUT0, ENGPOUT1, ENGPOUT2

R/W, CON2[3], CON2[4], CON2[5]

Enable the corresponding GPOUT.

ENGPOUT0, ENGPOUT1, ENGPOUT2	Meaning
0	GPOUT tristated
1	GPOUT driven

ENCT0, ENCT1, ENCT2

R/W, CON2[6], CON2[7], CON2[8]

Enable the corresponding CT.

ENCT0, ENCT1,ENCT2	Meaning
0	CT tristated
1	CT driven

NORLUTS

R/W, CON2[9]

This bit will disable the Read LUTs and set them in BYPASS for SLAVE and DMA modes. Useful in testing and with the Model 11 which does not have any LUTs mounted.

NORLUTS	Meaning
0	Read LUTs mode set by BYPASS SLAVE/DMA
1	Read LUTs always in BYPASS mode

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ADVANCE R/W, CON2[10]

This bit will enable to advance the Video FIFO pointer with each SLAVE read.

ADVANCE	Meaning
0	Read video FIFO in SLAVE mode without advancing read pointer
1	Advance video FIFO read pointer after each SLAVE mode read

BURST R/W, CON2[12..11]

These bits control the length of the burst on the PCI bus. The control circuitry will start the DMA when there are at least eight entries in the video FIFO. For video sources that are slow, this can result in inefficient transfers over the PCI, i.e., many short bursts. The BURST can insert additional waiting time after the video FIFO accumulated eight entries. During this time the video FIFO will receive more data. This will result in fewer, but longer bursts.

BURST	Delay
0 000b	No delay
1 001b	128 clocks
2 010b	256 clocks
3 011b	512 clocks

FRZFIFO R/W, CON2[13]

This bit controls the video FIFOs and the DMA in case of overflow. The bit will be set by the rising edge of INT1_FIFO, which is the overflow interrupt. It can be reset by the host by writing a 0. For the host to be able to reset this bit, the CMDWRITE code should be 10b. This will enable a reliable R/M/W operation.

FRZFIFO	Meaning
0	No overflow occurred
1	Overflow occurred

When this bit gets set, the DMA operation will be inhibited. This will guarantee that no corrupted data from the FIFOs will be read. As an overflow interrupt has been issued, the application can gracefully recover. It can reset the DMA and acquisition registers and then restart. This is very useful for display.

Note: If the INT_DMA is not enabled, the DMA will not be stopped.

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ONEQTB R/W, CON2[14]

The host sets up descriptor blocks in the Descriptor Table. This table is a SRAM on the local bus 32Kx32. When accessed from the host, the Descriptor Table looks like a continuous 32Kx32 block. When in DMA mode, the Descriptor Table is divided into two banks: bank 0 and bank 1, each one 16Kx32. In DMA mode, the active bank is selected by the DBANK (Descriptor Bank) bit. This bit will actually set address bit 15 of the Descriptor Table. DBANK is written by the host anytime. It is latched by any one of the following two conditions:

The DMA GO bit is written by the host (PC190x0 DMA Command/Status register bit.

Beginning of a new sequence, for more details refer to the Acquisition section.

The idea behind the two banks is to have the capability to change sequences in real time.

In certain cases, there is a need for a larger Descriptor Table. The ONEQTB bit in CON2 will control the structure of the tables: for ONEQTB = 0, the Descriptor Tables are structured as two banks of 16Kx32, as described above. For ONEQTB = 1, the Descriptor Tables will consist of a single bank, 32Kx32. The DBANK bit will have no effect in this case.

QTBSRC R/W, CON2[15]

This put puts the board DMA engine (PLX9080 only) in host QTAB mode. When the board is in host QTAB mode, the quads that make up the scatter gather table are stored in host memory, instead of on the boards QTAB banks. The DMA engine reads the quads directly from host memory then performs the DMA operation. If the quad is part of a chain, the DMA engine will read each quad and execute it in turn. The advantage of host QTAB mode is that there is virtually no limit to the size of image that can be DMAed using a single QTAB. Also chains of QTABs can be built up so that very large sequences of images can be DMAed without CPU intervention.

QTABSRC	Meaning
0	Board is in board QTAB mode
1	Board is in host QTAB mode

GRNTCTL R/W, CON2[16]

This bit controls the bus grant on the local bus. It is used to flush video FIFO on continuous acquisition.

GRNCTL	Meaning
0	Grant bus to PCI90x0 according to FIFO almost empty bit
1	Grant bus to PCI90x0 if FIFO not empty

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INT_DMA RO, CON2[17]

This bit is the DMA interrupt bit from the PLX90x0. It can be reset in the PLX chip (see the PLX manual).

INT_DMA	Meaning
0	No DMA interrupt
1	DMA interrupt asserted

INT0_CTAB, INT1_FIFO, INT2_HW R/W, CON2[18], CON2[19], CON2[20]

Interrupt bits. This will be generated from the sources listed below. Host and source can set the interrupt if its corresponding interrupt enable bit is set. Host cannot clear the interrupt if the corresponding interrupt enable bit is not set. For the host to access INT0_CTAB, INT1_FIFO, INT2_HW bits, one more condition must be fulfilled: the corresponding CMDWRITE code must be set (see CON4).

Interrupts are generated on the local bus. For DMA interrupts, see the PCI90x0 manual.

Interrupt	Source
INT0_CTAB	CTABs
INT1_FIFO	Video FIFO overflow
INT2_HW	HW exception

SCHSEL R/W, CON2[22..21]

These two bits will control the channel select during direct slave access to the FIFO. When manually reading data out of the FIFO (not DMAing), set these bits to get the data from the channel that you are interested in. When DMAing, these bits are set automatically by the current quad.

SCHSEL	Channel Selected
0 000b	Channel A
1 001b	Channel B
2 010b	Channel C
3 011b	Channel D

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LTEOX, LTMBANK, LTMBYPASS, LTMBY8, LTMCHSEL, LTFLUSH

RO, CON2[23], CON2[24], CON2[24], CON2[25], CON2[26], CON2[28..27], CON2[29]

These bits are the current LaTched attributes. The control circuitry snoops the local bus and intercepts the attributes when the 90x0 reads the DMA local address. These attributes are used for the current DMA process. The "LT" attributes are the ones that have been intercepted and latched in the control circuit. This is useful for testing and debugging.

TRIGINT

R/W, CON2[30]

This bit changes to source of the CTAB interrupt from the IRQ column in the CTABs to the TRIGGERA input. When this bit is set, the CTAB interrupt occurs every time the TRIGGERA signal changes state (i.e. both rising and falling edges). You can find out which transition occurred by peeking the TRIGSTAT bit. If TRIGSTAT is 1 then TRIGGERA went high, if it is 0 then it went low. This trigger interrupt only works when the trigger is internally disabled on the board (i.e. when ENXTRIG = 0). If the trigger is enabled, it works as with previous releases.

TRIGINT	Meaning
0	CTAB interrupt comes CTAB IRQ column
1	CTAB interrupt comes from change in trigger level

TRIGSTAT

RO, CON2[31]

This bit reflects the level of the TRIGGERA external trigger input.

TRIGSTAT	Meaning
0	Trigger input is low
1	Trigger input is high

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5.5 CON3 Register

Bit	Name
0	VF_MRST
1	SEN
2	FWSI
3	LD_FIFO
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	SW
9	SW
10	CLKDRVSEL
11	LENPOL
12	FENPOL
13	TRIGPOL
14	ENCPOL
15	TPSEL0
16	TPSEL1
17	TRIGINTB
18	TRIGSTATB
19	TRIGLT
20	TRIGLTB
21	Reserved
22	Reserved
23	Reserved
24	PROT
25	PROT
26	PROT
27	PROT
28	PROT
29	PROT
30	PROT
31	PROT

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VF_MRST WO, CON3[0]

Master video fifo reset.

VF_MRST	Meaning
0	Normal mode
1	Completely reset programmable FIFOs (should only be used on power up)

SEN R/W, CON3[1]

Used for programming FIFOs.

FWSI R/W, CON3[2]

Used for programming FIFOs.

LD_FIFO R/W, CON3[3]

Used to program FIFOs.

LD_FIFO	Meaning
0	FIFO is in normal mode
1	FIFO is in program mode

SW RO, CON3[9..8]

Two on-board mechanical switches used to identify multiple boards in the same system.

CLKDRVSEL R/W, CON3[10]

Clock drive selector.

Note: This bit is only functions on the R3 models.

CLKDRVSEL	Meaning
0	Clock output is RS422
1	Clock output is LVDS

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LENPOL R/W, CON3[11]

LEN polarity.

LENPOL	Meaning
0	Use rising edge of LEN
1	Use falling edge of LEN

FENPOL R/W, CON3[12]

FEN polarity.

FENPOL	Meaning
0	Use rising edge of FEN
1	Use falling edge of FEN

TRIGPOL R/W, CON3[13]

Controls the polarity of both TRIGGERS A and B.

TRIGPOL	Meaning
0	TRIGGERA and TRIGGERB active on rising edge
1	TRIGGERA and TRIGGERB active on falling edge

ENCPOL R/W, CON3[14]

Controls the polarity of both encoders A and B.

ENCPOL	Meaning
0	Use rising edge of encoders
1	Use falling edge of encoders

TPSEL0 R/W, CON3[15]

Control bit 0 for readout of test points in the "SYNC" PAL.

TPSEL1 R/W, CON3[16]

Control bit 1 for readout of test points in the "SYNC" PAL.

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TRIGINTB R/W, CON3[17]

Controls whether or not TRIGGERB can cause an interrupt.

TRIGINTB	Meaning
0	Level change onTRIGGERB does not cause interrupt
1	Level change onTRIGGERB causes interrupt

TRIGSTATB R/W, CON3[18]

The current level of TRIGGERB

TRIGSTATB	Meaning
0	TRIGGERB is low
1	TRIGGERB is high

TRIGLT R/W, CON3[19]

The state of TRIGGERA when last caused an interrupt.

TRIGLT	Meaning
0	TRIGGERA went high when it caused the last interrupt.
1	TRIGGERA went low when it caused the last interrupt.

TRIGLTB R/W, CON3[19]

The state of TRIGGERB when last caused an interrupt.

TRIGLTB	Meaning
0	TRIGGERB went high when it caused the last interrupt.
1	TRIGGERB went low when it caused the last interrupt.

PROT R/W,CON3[31..24]

Software protection PAL. Contact the factory for details.

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5.6 CON4 Register

Bit	Name
0	ENINT0_CTAB
1	ENINT1_FIFO
2	ENINT2_HW
3	SYNCMSTR
4	SYNCBUSY
5	CMDWRITE
6	CMDWRITE
7	LTAACTIVE
8	LTBACTIVE
9	LTCACTIVE
10	LTDACTIVE
11	LTQBANK
12	OVF
13	CONTINTPOL
14	TRIG_FILTER
15	FORCEABORT
16	SWRESET
17	SWTRIGB
18	SWTRIGA
19	AQFLD
20	AQFLD
21	DBANK
22	AQFRM
23	VFRESET
24	AACTIVE
25	BACTIVE
26	CACTIVE
27	DACTIVE
28	TRIGAQCMD
29	HBYPASS
30	HBANK
31	HBY8

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ENINT0_CTAB, ENINT1_FIFO, ENINT2_HW R/W, CON4[0], CON4[1], CON4[2]

Individual enable interrupt bits related to the acquisition process. The interrupts can be active (from its source or from the host), only if it has been enabled.

ENINT0_CTAB, ENINT1_ FIFO, ENINT2_HW	Meaning
0	Corresponding interrupt disabled
1	Corresponding interrupt enabled

SYNCMASTER R/W, CON4[3]

Setting this bit will make this board the master on the Sync bus, if there is not already another master on the Sync bus. The host can find this out by reading the SYNCBUSY signal (see SYNCBUSY). If there is another master enabled on the Sync bus, and the host will try to write the SYNCMASTER bit, it will not take effect.

SYNCMASTER	Meaning
0	This board is not master on the Sync bus
1	This board is master on the Sync bus

SYNCBUSY RO, CON4[4]

This bit will tell if there is an active master on the Sync bus.

SYNCBUSY	Meaning
0	No master on the Sync bus
1	There is a master on the Sync bus

CMDWRITE R/W, CON4[6..5]

These bits will enable the host to write to interrupt bits that can be modified by on-board circuitry. Disabling the host access to those bits will allow reliable read-modify-write operations to control bits residing in the same control register.

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Below are the CMDWRITE codes:

CMDWRITE	Host access enabled to
0 00b	None
1 01b	INT0_CTAB
2 10b	INT1_FIFO and FRZFIFO
3 11b	INT2_HW

The AQCMD bits do not need a CMDWRITE protection feature because they are in a register by themselves.

The logic of the interrupt generated by the PCI90x0 DMA is such that it does not need the features of the CMDWRITE bits. There is a dedicated bit for resetting the interrupt.

The advantage of having the CMDWRITE logic is that the host cannot only reset the interrupt source, it can also set the interrupt source. This is a handy tool for debugging and simulating hardware interrupts from the software.

LTAACTIVE, LTBACTIVE, LTCACTIVE, LTDACTIVE, LTQBANK

RO, CON4[7], CON4[8], CON4[9], CON4[10], CON4[11]

These bits are the LaTched A,B,C,DACTIVE and QBANK. The ACTIVE bits are latched with the acquisition command, and the QBANK is latched with the DMA GO bit. The bits can be read out in this register for testing and debugging.

OVF

RO, CON4[12]

This is the video FIFO's overflow bit. This bit is not latched. If the overflow condition goes away, the OVF bit will be de-asserted.

OVF	Meaning
0	No overflow in any one of the FIFO channels
1	Overflow in one or more of the FIFO channels

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CONTINTPOL R/W, CON4[13]

In continuous acquisition mode, TRIGCON = 10b. The acquisition is controlled by TRIGGERA and the CTABs are disabled. In this mode, the interrupt from the CTABs is replaced with an interrupt from the TRIGGERA. CONTINTPOL determines on which edge of TRIGGERA the interrupt will occur.

CONTINTPOL	Meaning
0	Assert interrupt on falling edge of TRIGGERA, i.e., at the end of the acquisition
1	Assert interrupt on rising edge of TRIGGERA, i.e., at the beginning of the acquisition

TRIG_FILTER R/W, CON4[14]

The filter is of the "pulse swallower" type. A pulse less than 0.6 microseconds will be discarded. For the trigger to be recognized, it must be asserted for at least 0.6 microseconds. Also, for the trigger to be recognized as de-asserted, it must be de-asserted for at least 0.6 microseconds. The filter introduces a delay of 0.6 microseconds on the trigger.

Note: This filter is not implemented on all board models. Contact BitFlow for more information.

TRIG_FILTER	Meaning
0	Filter on HW trigger disabled
1	Filter on HW trigger enabled

FORCEABORT R/W, CON4[15]

This is a special bit used to abort DMA when the FIFO is already empty. Under normal circumstances there is not need to use this bit.

FORCEABORT	Meaning
0	Normal operation
1	DMA abort operation does not stall on FIFO empty

SWRESET WO, CON4[16]

This is a software reset to the board. It should be asserted each time the board is initialized. It resets the CTABs address counters and the timing generators.

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Note: This bit will always read back 0.

SWRESET	Meaning
0	No effect
1	Asserts software reset

SWTRIGB WO, CON4[17]

This bit is dedicated to the software trigger. It is always active HI and will be ORed with the TRIGGER_B. It does not have to be enabled by the TRIGAQ bit. Writing a "1" will unconditionally generate a trigger on TRIGGER_B.

Note: This bit will always read back 0.

SWTRIGB	Meaning
0	No effect
1	Assert software trigger B

SWTRIGA WO or R/W, CON4[18]

This bit is dedicated to the software trigger. It is always active HI, and will be ORed with the TRIGGER_A. Does not have to be enabled by the TRIGAQ bit. Writing a "1" will unconditionally generate a trigger on TRIGGER_A.

If the board is a Sync bus master, the SWTRIGA will go on the Sync bus as BUSTRIG. If the board is a slave on the Sync bus, SWTRIGA will be substituted with the BUSTRIG.

SWTRIGA, TRIGCON = 0, 1, 3	Meaning
0	No effect
1	Assert software trigger A

This bit will always read back 0 if TRIGCON = 0, 1, 3.

This bit has an additional mode of operation, if TRIGCON = 2. In this mode SWTRIGA is level sensitive. Data will be acquired as long as SWTRIGA is asserted. When SWTRIGA is latched, it will read back the last value written to. It is worth noting that for the continuous acquisition case, TRIGGGERB will also be treated as "level sensitive."

SWTRIGA, TRIGCON = 2	Meaning
0	Do not acquire
1	Acquire

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AQFLD R/W, CON4[20..19]

Controls acquisition for interlaced cameras.

Note: Currently the Road Runner/R3 do not support acquisition from interlaced cameras and this register must be set to 0.

AQFLD	Acquire
0 00b	Start acquire on next field
1 01b	Start acquire on odd field
2 10b	Start acquire on even field
3 11b	Reserved

DBANK R/W, CON4[21]

While the PCI90x0 is doing DMA, this bit will determine the bank the descriptors (QTABs) are read from. This bit will actually be the address bit 15 of the 32Kx32 Descriptor Table.

The bit can be written by the host anytime. It will get latched when the host writes the DMA GO bit, or when a new sequence starts. In the latter case, this bit is latched when a quad (usually the last) has the EOX attribute set.

When the host accesses the Descriptor Tables, the DBANK bit has no effect. The host can access the whole 32Kx32 Descriptor Table.

DBANK	Meaning
0	Access descriptors in the range 0-16K
1	Access descriptors in the range 16K-32K

AQFRM R/W, CON4[22]

Acquire one or two fields.

Note: Currently the Road Runner/R3 do not support acquisition from interlaced cameras and this register must be set to 0.

AQFRM	Meaning
0	Acquire one frame
1	Acquire two fields

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VFRESET WO, CON4[23]

Writing a 1 to this bit will reset all the video FIFOs. This bit is not latched.

Note: This bit will always read back a 0.

VFRESET	Meaning
0	No effect
1	Assert RESET to all video FIFOs

AACTIVE, BACTIVE, CACTIVE, DACTIVE R/W, CON4[24], CON4[25], CON4[26], CON4[27]

These bits mark the active video channels. Video will be clocked only in the FIFOs that are active.

The host can write these bits anytime. They will be latched at the beginning of the active video, when a new acquisition command is latched. On read back, you read the last values you wrote, not the ones that have been latched.

AACTIVE, BACTIVE, CACTIVE, DACTIVE	Meaning
0	Channel inactive, no video will be clocked in that FIFO
1	Channel active, video will be clocked in that FIFO

TRIGAQCMD R/W, CON4[28]

Set for triggered acquisition mode. After the rising/falling edge of the selected trigger, the current acquisition command will be executed. TRIGCON select the trigger, TRIGPOL will select the polarity.

TRIGAQCMD	Meaning
0	Normal acquisition mode (non-triggered)
1	Triggered acquisition mode

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HBYPASS R/W, CON4[29]

This bit will enable to bypass the read LUT when reading the FIFO in Direct Slave mode.

HYPASS	Meaning
0	Data from FIFOs will pass through the LUT
1	Data from FIFOs will bypass the LUT

HBANK R/W, CON4[30]

This bit will select the LUT bank, when the LUTs are accessed from the host. In master mode, the bank is controlled by the BANK in the attribute register.

HBANK	Meaning
0	Select bank 0
1	Select bank 1

HBY8 R/W, CON4[31]

This bit will set the read LUT to 4x8in-8out or 2x12in-16out. Used only in slave mode, for programming the read LUTs. In master mode, the 8/12 mode is controlled by BY8 in the attribute register.

Note: On boards that have a 2x16in-16out LUT this bit must be set to 0.

HBY8	Meaning
0	LUTs set as 2x12in-16out
1	LUTs set as 4x8in-8out

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5.7 CON5 Register

Bit	Name
0	CTABHOLD
1	HSTOP
2	VSTOP
3	TRIGCON
4	TRIGCON
5	ENCDRCON
6	ENCDRCON
7	ENHLOAD
8	VTRIGRST
9	CT0CON
10	CT0CON
11	CT1CON
12	CT1CON
13	CT2CON
14	CT2CON
15	ENXTRIG
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

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CTABHOLD R/W, CON5[0]

This bit will freeze the outputs of the CTABs. When the CTABs are frozen, both the horizontal and the vertical counter will not increment nor respond to any external signals, and the CTs and STROBE outputs will be held at their current levels.

CTABHOLD	Meaning
0	CTABs run
1	Output of CTABs frozen

HSTOP R/W, CON5[1]

This bit will determine if the HCTAB address counter will free run. If HSTOP = 1, the HCOUNT will be reset by the HRESET signal and stay at 0 until an ENCODER signal is asserted.

HSTOP	Meaning
0	HCOUNT is free running
1	After HCOUNT is reset, wait for an ENCODER to continue

VSTOP R/W, CON5[2]

This bit will determine if the VCTAB address counter will free run. If VSTOP is 1, the VCOUNT will be reset by the reset signal (VSTART=VEND=1) and stay at 000 until a TRIGGER comes in. If VSTOP is 0, the VCOUNT will be free running.

VSTOP	Meaning
0	VCOUNT is free running
1	After VCOUNT is reset, wait for TRIGGER to continue

TRIGCON R/W, CON5[4..3]

These bits control the operation of the two triggers, A and B.

TRIGCON	Meaning
0 00b	TRIGGERA active, B disabled
1 01b	Start Grab on A, Stop Grab on B
2 10b	Continuous acquisition
3 11b	Triggered Termination (Start-Stop mode)

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Triggered Termination, TRIGCON = 11b

This mode is used to terminate the acquisition immediately, without waiting for the end of the frame. It is slightly different than the assertion of the ABORT command. It will end the acquisition process and the DMA process in a graceful way. Acquisition can be started normally with a GRAB command and triggered by TRIGGERA. The acquisition can be terminated by TRIGGERA or TRIGGERB, depending on the setting of bit TRIGASTOP in CON10.

TRIGASTOP	Meaning
0	Terminate acquisition assertion of TRIGGERB
1	Terminate acquisition with de-assertion of TRIGGERA

In the second mode, the acquisition is started by the assertion of TRIGGERA and terminated by the de-assertion of TRIGGERA. Polarity of assertion depends on TRIGPOL.

The difference between the two modes is that with TRIGASTOP =1, the start and the end of the acquisition process can be controlled by a single wire, TRIGGERA.

In Triggered Termination, when the termination trigger is asserted, the VCOUNT will be reset to 0. This mode is also called start-stop line scan mode. The CTABs should be programmed to issue an interrupt. It will not abort the acquisition process (in contrast to the ABORT command).

ENCDRCON R/W, CON5[6..5]

These bits control the operation of the two encoders, A and B.

ENCDRCON	Meaning
0 00b	Encoder A active, B disabled
1 01b	TBD
2 10b	TBD
3 11b	TBD

ENHLOAD R/W, CON5[7]

This bit will determine if the HCTAB address counter, HCOUNT, should be loaded by LEN. Useful for cameras that do not give back LEN.

ENHLOAD	Meaning
0	HCOUNT is free running
1	LEN will load the HCOUNT

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VTRIGRST R/W, CON5[8]

This bit will enable the trigger to reset the VCTAB address counter. Do not use this mode when VSTOP = 1 or TRIGAQCMD = 1 since these modes give the board conflicting instructions.

VTRIGRST	Meaning
0	Normal mode
1	VCTAB counter will reset to 0000h when trigger is asserted

CT0CON R/W, CON5[10..9]

These bits control the output of CT0.

CT0CON	Meaning
0 00b	Dynamic, defined by CTABs
1 01b	TBD
2 10b	0
3 11b	1

CT1CON R/W, CON5[12..11]

These bits control the output of CT1.

CT1CON	Meaning
0 00b	Dynamic, defined by CTABs
1 01b	TBD
2 10b	0
3 11b	1

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CT2CON R/W, CON5[14..13]

These bits control the output of CT2.

CT2CON	Meaning
0 00b	Dynamic, defined by CTABs
1 01b	TBD
2 10b	0
3 11b	1

ENXTRIG R/W, CON5[15]

This bit will enable the external hardware TRIGGERA and B. The purpose of this signal is to be able to shut off these triggers. If an input is left unconnected, the output of the its receiver will float, resulting in unpredictable triggering behavior. This bit avoids this problem by disconnecting the external triggers from the acquisition circuitry.

ENXTRIG	Meaning
0	External TRIGGERA and B disabled
1	External TRIGGERA and B enabled

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5.8 CON6 Register

Bit	Name
0	STRAIGHT
1	DTG
2	TRIM
3	TRIM
4	FISEL
5	TG1AQW
6	TG1AQW
7	TG2AQW
8	TG2AQW
9	TGA
10	TGB
11	TGC
12	TGD
13	HSTICK
14	DLY
15	DLY
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

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STRAIGHT R/W, CON6[0]

This bit will control the selection between straight and scan reversed video.

STRAIGHT	Meaning
0	Pass T1,T3 scan reversed
1	Pass T1,T3 straight from the camera

DTG R/W, CON6[1]

This bit selects the display window for TG2. The bit can be written by the host anytime. It will be latched at the start of the active video when a new acquisition command is latched.

Note: The second timing generator is not longer support with the latest release of the BitFlow SDK.

DTG	Meaning
0	Use main acquisition window for TG2
1	Use display window for TG

TRIMP4, TRIM R/W, CON9[15], CON6[3..2]

The horizontal CTABs and the control functions work off PCLK/4. If the data from the camera is misaligned relative to LEN by one, two, or three pixels, we will not be able to correct that with the CTABs. This will have adverse effect especially for multi-tap cameras. TRIM, together with TRIMP4, will delay LEN relative to the data by one to seven pixels (TRIMP4 which resides in CON9 is the MSB on the trimming code).

TRIMP4, TRIM	Delay
0 000b	No delay
1 001b	One pixel
2 010b	Two pixels
3 011b	Three pixels
4 100b	Four pixels
5 101b	Five pixels
6 110b	Six pixels
7 111b	Seven pixels

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FISEL R/W, CON6[4]

Selects between the FI supplied by the camera or the FI detected by the CTABs.

Note: Contact BitFlow about Road Runner support for interlaced cameras.

FISEL	Meaning
0	Use FI from camera
1	FI detected by CTABs

TG1AQW R/W, CON6[6..5]

Acquisition width for TG1.

These bits can be written by the host anytime. They are latched at the beginning of the active video, when a new acquisition command is latched.

TG1AQW	Meaning
0 00b	8 bits
1 01b	16 bits
2 10b	32 bits
3 11b	8 bits subsampled 1:2, i.e., zoom by ½

TG2AQW R/W, CON6[8..7]

Acquisition width for TG2.

These bits can be written by the host anytime. They are latched at the beginning of the active video, when a new acquisition command is latched.

Note: Contact BitFlow about Road Runner support for interlaced cameras.

TG2AQW	Meaning
0 00b	8 bits
1 01b	16 bits
2 10b	32 bits
3 11b	8 bits subsampled 1:2, i.e., zoom by ½

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TGA, TGB, TGC, TGD R/W, CON6[9], CON6[10], CON6[11], CON6[12]

This bit selects the timing generator for Channel A, B, C and D.

TGA, TGB, TGC, TGD	Meaning
0	Use TG1 for corresponding channel
1	Use TG2 for corresponding channel

HSTICK R/W, CON6[13]

This bit controls the behavior of the Horizontal Control Table. If the horizontal counter is clocked up to 7f8h before LEN is asserted, it will stop, if this bit is set. The horizontal counter will remain at 7f8h until LEN is asserted.

HSTICK	Meaning
0	Normal operation
1	Horizontal counter sticks at 7f8h until LEN is asserted

DLY R/W, CON6[15..14]

These two bits will control the delay of Channels B and D relative to Channels A and C when the invert mode is on (see STRAIGHT).

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5.9 CON7 Register

Bit	Name
0	FM_LEVEL
1	FM_LEVEL
2	FM_LEVEL
3	FM_LEVEL
4	FM_MAX
5	FM_MAX
6	FM_MAX
7	FM_MAX
8	Reserved
9	H_ERR
10	FM_RESET
11	Reserved
12	Reserved
13	ROTINV0
14	ROTINV1
15	ROTINV2
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

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FM_LEVEL RO, CON7[3..0]

This registers indicates the current FIFO level in units of 1/16th of the FIFO size. This register is useful for gather statistics on how close the FIFOs are to overflowing based on system load. Reading this register takes about 10 PCI bus clock cycles. This register should not be read more than 1000 times per second, exceeding this value can degrade DMA throughput.

FM_MAX RO, CON7[7..4]

These bits indicate the maximum FIFO level in units of 1/16th of the FIFO size. The maximum value is reset by writing a one to FM_RESET. A reset must be issues before issuing an acquisition command. This register is useful for gathering statistics on how close the FIFOs are to overflowing based on system load.

H_ERR RO, CON7[9]

This bit is used for internal testing

FM_RESET WO, CON7[10]

This bit resets the FIFO monitoring circuitry. In order to have an accurate reading from FM_MAX, the circuitry must be reset by writing a 1 to this bit, before an acquisition command is issued.

ROTINV R/W, CON7[15..13]

These bits add delay to the pixels that are coming from the STACK. They are used to synchronize lines that are inverted in the STACK with lines that are not inverted.

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5.10 CON8 Register

Bit	Name
0	Reserved
1	Reserved
2	Reserved
3	Reserved
4	Reserved
q	Reserved
6	Reserved
7	Reserved
8	ENC_FILTER
9	LAL
10	TRIG_FREE
11	HCTAB_X16
12	FENHRESET
13	STCON
14	STCON
15	VSTICK
16	Reserved
17	reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

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ENC_FILTER R/W, CON8[8]

The filter is of the "pulse swallower" type. A pulse less than 0.6 microseconds will be discarded. For the encoder pulse to be recognized, it must be asserted for at least 0.6 microseconds. Also, for the encoder to be recognized as de-asserted, it must be de-asserted for at least 0.6 microseconds. The filter introduces a delay of 0.6 microseconds on the trigger.

Note: This filter is not implemented on all board models. Contact BitFlow for more information.

ENC_FILTER	Meaning
0	Filter on encoder disabled
1	Filter on encoder enabled

LAL R/W, CON8[9]

This bit changes how the VCOUNT register works. Normally VCOUNT indicates the instantaneous value of the vertical CTAB counter. However, when LAL is set to 1, the VCOUNT register returns the maximum value the vertical CTAB counter reached at the end of the frame. The VCOUNT register will continue to read this maximum value until the next end of frame. This mode is useful for determining the size of an image when the board is in triggered termination mode (start stop line mode). The reason being is that the VCOUNT register will indicate the size of the previous frame, and will continue to return this value during the entire time that the next frame is being acquired.

LAL	Meaning
0	VCOUNT reads the instantaneous value of the vertical CTAB counter
1	VCOUNT read the maximum value of the vertical CTAB counter from the previous frame

TRIG_FREE R/W, CON8[10]

This bit effects how the trigger works when the board is in triggered termination mode (start-stop line mode). When this bit is set to one, and the board is in one shot mode (VSTOP = 1), and the vertical active window starts at the beginning of the VCTAB, the board will continue to acquire as long as the external trigger is asserted. Previously, the board would only acquire one frame when the trigger was asserted. Essentially this bit changes the trigger input from edge triggered mode to level trig-

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gered mode. Please also note that this new mode only works when all the conditions mentioned above are met. Finally this mode also works in start-stop mode (TRIGCON = 3).

TRIG_FREE	Meaning
0	One frame per trigger edge in start-stop mode
1	Board continues to acquire frames as long as trigger is asserted

HCTAB_X16 R/W, CON8[11]

This bit controls how the HCTAB counter is incremented. When this bit is 0 the HCTAB counter is incremented every 4 pixel clocks, when this bit is 1 the HCTAB counter is incremented every 16 pixel clocks. Effectively, this bit controls the maximum size line that can be acquired. When this bit is 0, the HCTAB size is 32K pixels, when this bit is 1 the HCTAB size is 512K pixel.

HCTAB_X16	Meaning
0	HCTAB counter incremented every 4 pixel clocks
1	HCTAB counter incremented every 16 pixel clocks

FENHRESET R/W, CON8[12]

This bit controls how the HCTAB counter is reset when FEN is asserted.

FENHRESET	Meaning
0	HCTAB counter is not effected by FEN assertion
1	HCTAB counter is reset to 0 by FEN assertion

STCON R/W, CON8[14..13]

These bits control the functionality of the STROBE signal.

STCON	Meaning
0 00b	VSTROBE * HSTROBE
1 01b	TBD
2 10b	0
3 11b	1

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VSTICK R/W CON8[15]

This register controls what happens with the vertical control table counter reaches 0ff0h. Normally the counter jumps to 1000h when the FEN is asserted. However, under certain circumstances (e.g., long exposure periods) there may be more than 1000h lines before FEN is asserted. In these cases, set this bit so that the counter will stick indefinitely at 1ff0h until FEN is asserted. Writing a 1 to SWRESET will also un-stick the counter, but in this case the counter will jump to 0.

VSTICK	Meaning
0	The VCTAB counter proceeds normally
1	The VCTAB counter sticks at 0ff0h until FEN is asserted

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5.11 CON9 Register

Bit	Name
0	TRIG_DELAY
1	TRIG_DELAY
2	TRIG_DELAY
3	TRIG_DELAY
4	TRIG_DELAY
5	TRIG_DELAY
6	TRIG_DELAY
7	TRIG_DELAY
8	TRIG_DELAY
9	TRIG_DELAY
10	EN_TRIG_DELAY
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	TRIMP4
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

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TRIG_DELAY R/W, CON9[9..0]

This register sets the delay amount when the board is in trigger delay mode. Trigger delay mode is enable by setting EN_TRIG_DELAY to 1. This trigger delay mode delays any activity on the trigger input line by the programed amount. The delay units are in terms of line times, however, in order to get an acceptable range, a multiplier is used. The delay amount (line times) = 8 x N + 3, where N is the value programmed into TRIG_DELAY.

EN_TRIG_DELAY R/W, CON9[10]

This bit controls trigger delay mode.

EN_TRIG_DELAY	Meaning
0	Trigger action occurs immediately
1	Trigger action delayed, amount controlled by TRIG_ DELAY

TRIMP4 R/W, CON9[15]

The horizontal CTABs and the control functions work off PCLK/4. If the data from the camera is misaligned relative to LEN by one, two, or three pixels, we will not be able to correct that with the CTABs. This will have adverse effect especially for multi-tap cameras. TRIM, together with TRIMP4, will delay LEN relative to the data by one to seven pixels.

TRIMP4, TRIM	Delay
0 000b	No delay
1 001b	One pixel
2 010b	Two pixels
3 011b	Three pixels
4 100b	Four pixels
5 101b	Five pixels
6 110b	Six pixels
7 111b	Seven pixels

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5.12 CON10 Register

Bit	Name
0	Reserved
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	LEN_SIZE
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	TRIGASTOP
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

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LEN_SIZE R/W CON10[10]

This register puts the board in a special horizontal mode. In this mode, the LEN signal only controls the active horizontal window. The CTABs are decoupled from the horizontal active window. When LEN asserts, the board begins acquiring pixels. When LEN, de-asserts, the board stops acquiring pixels.

The purpose of this mode is to allow overlap of exposure control signals (output to the camera) and line readout. Ordinarily, when using an encoder, the exposure time must complete before line readout. When LEN_SIZE = 1, the line can be read out simultaneously with the exposure of the following line.

This mode is only for line scan cameras. The mode only works if the LEN signal asserts for the entire duration of the camera's active pixel readout. In addition, any extra pixels that are output when LEN is asserted will be acquired.

LEN_SIZE	Meaning
0	The HCTAB controls the horizontal acquisition window
1	The LEN signal controls the horizontal acquisition window

TRIGASTOP R/W, CON10[15]

These bits control the operation of the two triggers, A and B. For more information, refer to TRIGCON, R/W (CON5).

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5.13 CON11 Register

Bit	Name
0	Reserved
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	CFGDATA
17	CFGSTATUS
18	CFGGEN
19	CFGDONE
20	CFGCLOCK
21	Reserved
22	OCCONFIG
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

Note: These bits are used to download the firmware in the gate arrays. These should not be used in any user application.

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CFGDATA WO, CON11[16]

This bit is the serial configuration data written to the gate arrays.

Note: On read back this bit will always read 0.

CFGDATA	Meaning
0	Data presented to gate arrays will be 0
1	Data presented to gate arrays will be 1

CFGSTATUS RO, CON11[17]

This bit is the STATUS bit of the first Altera device.

CFGGEN RO, CON11[18]

This bit is the CONFIG bit, an open collector. Through this bit you can read the gate arrays CONFIG bit. Asserting this bit will be done through the OCCNFIG bit (see below).

CFGGEN	Meaning
0	Gate arrays are reset
1	Gate arrays active

CFGDONE RO, CON11[19]

This read-only bit is the DONE bit of the last gate array in the configuration chain.

CFGDONE	Meaning
0	Configuration completed
1	Configuration in process

CFGCLOCK WO, CON11[20]

This is the configuration clock. Writing a 1 to this bit will generate one single clock pulse to the gate arrays.

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Note: On read back this bit will always read 0.

CFGCLOCK	Meaning
0	Clock will not be asserted
1	Clock will be asserted

OCCONFIG R/W, CON11[22]

This bit controls the open collector feature of the CONFIG bit.

OCCONFIG	Meaning
0	CONFIG pin is input mode only, i.e., read-only
1	CONFIG pin is in output mode, asserted 0

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5.14 CON12 Register

Bit	Name
0	VCOUNT
1	VCOUNT
2	VCOUNT
3	VCOUNT
4	VCOUNT
5	VCOUNT
6	VCOUNT
7	VCOUNT
8	VCOUNT
9	VCOUNT
10	VCOUNT
11	VCOUNT
12	VCOUNT
13	VCOUNT
14	VCOUNT
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

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VCOUNT R/O, CON12[14..0]

This register indicates the current value of the vertical control table counter.

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5.15 PCI_COM_PROM_CON Register

Bit	Name
0	Reserved
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	PCI_COM_USERI
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved

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PCI_COM_USERI R/O, PCI_COM_PROM_CON[17]

This bit indicites the level of the external hardware signal connected to the board's GPIN input pin. This signal does not control anything on the board, it a general purpose input.

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Power Requirements

Chapter 6

6.1 Road Runner Current Requirements

Table 6-1 shows the power requirements for the Road Runner. These numbers apply for all options. The Road Runner uses only the +5V power supply.

Table 6-1 Power Requirements

Model	Amps
RUN-PCI-12	3A max
RUN-PCI-14	3.5A max
RUN-PCI-24	4A max
RUN-PCI-44	4.3A max

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6.2 R3 Current Requirements

Table 6-2 shows the power requirements for the R3. These numbers apply for all options. The R3 uses only the +5V power supply.

Table 6-2 Power Requirements

Model	Amps
R3-PCI-DIF	3 A max

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Specifications

Chapter 7

7.1 Introduction

This chapter describes the general specifications of the Road Runner and the R64. The numerical values for the specifications are listed in Table 7-1. If more information is available for a given specification there will be an entry in the column marked "Details".

Table 7-1 Road Runner/R3 Specifications

Specifications	Value	Units	Details
PCI Bus compatible frequencies	33	MHz	
PCI Bus compatible data widths	32	Bits	
PCI Bus compatible voltages	3.3 and 5	Volts	Section 7.2
Maximum Input Pixel Clock Frequency	62.5	MHz	
Minimum Input Pixel Clock Frequency	greater than zero	MHz	
Maximum Pixels Per Line (1 tap)	131,072 (128K)	Pixels	
Maximum Lines Per Frame	32,768 (32K)	Lines	Section 7.3
Minimum clocks between lines	16	Clocks	
Minimum lines between frames	0	Lines	
Minimum pixel clocks between frames	4	Clocks	
Minimum trigger pulse	1	Clock	
Minimum encoder pulse	2	Clock	
Current consumption (+5V)	3 to 4.3	Amps	Section 6.1 & Section 6.2
Temperature range	0 to 50	Degrees Celsius	
Humidity	25% to 80%		
Road Runner Mechanical dimensions	8.7 x 4.2	Inches	
Road Runner Mechanical dimensions	22.10 x 10.67	Centimeters	
R3 Mechanical dimensions	6.6 x 4.2	Inches	

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Table 7-1 Road Runner/R3 Specifications

Specifications	Value	Units	Details
R3 Mechanical dimensions	16.76 x 10.67	Centimeters	
LVDS Reciever	SN65LVDS3486D		
LVDS Transmitter	SN65LVDS31D		
PCI Specification Compliance	2.2		

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7.2 PCI bus compatibility

The R3 will work in both 3.3V and 5V PCI buses. The Road Runner will only work in 5V PCI busses. Please note that this voltage specification is related only to the signalling level on the PCI bus, not the availability of a voltage on the connector. The different voltage PCI connectors have different keying. You cannot plug a 5V board into a 3.3V slot. The R3 is designed as a "universal" board and is keyed so that it will plug into both 3.3V and 5V slots. The Road Runner is keyed so that it will plug into only 5V slots.

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7.3 Maximum Lines Per Frame

For area scan cameras, the maximum number of lines per frame 32,768. For line scan cameras, the board can be set up to continuously acquire lines, with no limit to the number of lines acquire continuous. In the mode, no lines are dropped. An interrupt can be sent to the host every N lines. N can be any number up to the number of lines the host is capable of storing (limited only by RAM in the computer).

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Connector Pinouts

Chapter 8

8.1 Introduction

There are four connectors on the Road Runner models:

P1 - The main camera connector, 62-pin
P2 - The auxiliary camera connector, 60-pin
P5 - The I/O connector, 14-pin
P6 - The Sync bus connector, 14-pin

There are also four connectors on the R3, but they are slightly different:

P1 - The main camera connector, 62-pin
P2 - The auxiliary camera connector, 60-pin
P4 - Test connector
P5 - The I/O connector, 14-pin

The main camera connector is mounted on the bracket. It has all the signals required to connect to a 16-bit camera. These 16 bits connect to the T0 and T1 taps.

The auxiliary camera connector is mounted on the top of the board. It has all the signals required to connect to a 16-bit camera. These 16 bits connect to the T2 and T3 taps.

The I/O connector is mounted on the top of the board. It has control signals that are not directly related to cameras, i.e., STROBE, TRIGGER, etc. These signals usually do not have to be on the same cable that connects to a camera.

The Sync bus is on the top of the board. It has the signals needed to synchronize multiple boards. The master on the Sync bus is determined by the host.

The output and input signalling levels differ for some pins depending on the board family. See Section 8.1.2 for more information on understanding these differences.

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8.1.1 Location of Input Bits and Channels

Table 8-1 Shows how the digital channels (referred to in the MUX registers) maps to the corresponding digital input bits.

Table 8-1 Input Channels to Digital Pins Mapping

Input Channel	Digital Bits	Connector
T0	DIG0 — DIG7	P1
T1	DIG8 — DIG15	P1
T2	DIG16 — DIG21	P2
T3	DIG24 — DIG31	P2

8.1.2 Input and Output Signalling Levels

Table 8-2 shows comments that are used in the pinout tables to describe the outputs.

Table 8-2 Road Runner/R3 Output Types

Comments	Road Runner RS422	Road Runner LVDS	R3
TTL	TTL single ended	TTL single ended	TTL single ended
Diff	RS422 differential	LVDS differential	RS422 differential
Diff or TTL	RS422 or TTL switch-able, depending on S2 and S3	LVDS or TTL switch-able, depending on S2 and S3	RS422 only (no switches on R3)
Diff Sw	RS422 differential	LVDS differential	RS422 or LVDS dif-ferential, depending on the bit CLKDRVSEL

Table 8-3 shows the comments that are used in the pinout tables to describe the inputs.

Table 8-3 Road Runner/R3 Input Types

Comments	Road Runner RS422	Road Runner LVDS	R3
Diff	RS422 differential	LVDS differential	LVDS differential
Diff & TTL	RS422 or TTL depending on how the board is con-nected (See 3.1)	LVDS or TTL depending on how the board is con-nected (See 3.1)	LVDS or TTL depending on how the board is con-nected (See 3.1)

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8.2 P1, The Main Camera Connector

Table 8-4 Shows the pinout for the P1 Connector for the RS422 version of the Road Runner. See Section 8.1.2 for more information on the meaning of the comment column..

Table 8-4 Connector P1 pinout

Pin	I/O	Signal	Comment	Pin	I/O	Signal	Comment
1	In	CLKIN+	Diff	31	In	DIG3+	Diff
2	In	CLKIN-		32	In	DIG3-	
3	Out	CLKOUT	TTL	33	Out	CT1+	Diff or TTL
4	In	DIG8+	Diff	34	Out	CT1-	Diff or TTL
5	In	DIG8-		35	Out	CT2+	Diff or TTL
6	In	DIG9+	Diff	36	Out	CT2-	Diff or TTL
7	In	DIG9-		37	Out	GPOUT0+	Diff or TTL
8	In	DIG10+	Diff	38	Out	GPOUT0-	Diff or TTL
9	In	DIG10-		39	Out	GPOUT1+	Diff or TTL
10	In	DIG11+	Diff	40	Out	GPOUT1-	Diff or TTL
11	In	DIG11-		41	Out	GPOUT2+	Diff or TTL
12	In	FI+	Diff	42	Out	GPOUT2-	Diff or TTL
13	In	FI-		43	In	DIG4+	Diff
14	In	DIG12+	Diff	44	In	DIG4-	
15	In	DIG12-		45	In	DIG5+	Diff
16	In	DIG13+	Diff	46	In	DIG5-	
17	In	DIG13-		47	In	DIG6+	Diff
18	In	DIG14+	Diff	48	In	DIG6-	
19	In	DIG14-		49	In	DIG7+	Diff
20	In	DIG15+	Diff	50	In	DIG7-	
21	In	DIG15-		51	In	TRIG-GERA+	Diff & TTL
22		GND		52	In	TRIG-GERA-	Diff & TTL
23	Out	CLKOUT+	Diff Sw	53	In	Reserved	
24	Out	CLKOUT-		54	In	Reserved	

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Table 8-4 Connector P1 pinout

Pin	I/O	Signal	Com-ment	Pin	I/O	Signal	Comment
25	In	DIG0+	Diff	55		GND	
26	In	DIG0-		56		GND	
27	In	DIG1+	Diff	57	Out	CT0+	Diff & TTL
28	In	DIG1-		58	Out	CT0-	Diff & TTL
29	In	DIG2+	Diff	59	In	LEN+	Diff
30	In	DIG2-		60	In	LEN-	
				61	In	FEN+	Diff
				62	In	FEN-	

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8.3 P2, The Auxiliary Camera Connector, 60-Pin

Table 8-5 shows the pint out for the P2 connector. See Section 8.1.2 for more information on the meaning of the comment column.

Table 8-5 Connector P2 pinout

Pin	I/O	Signal	Comment	Pin	I/O	Signal	Comment
1	Out	CT1	TTL	31	In	DIG30-	
2	Out	CT0	TTL	32	In	DIG30+	Diff
3	Out	GPOUT2	TTL	33	In	DIG29-	
4	Out	GPOUT1	TTL	34	In	DIG29+	Diff
5	Out	GPOUT0	TTL	35	In	DIG28-	
6		GND		36	In	DIG28+	Diff
7	Out	GPOUT2X-		37	In	DIG27-	
8	Out	GPOUT2X+	Diff	38	In	DIG27+	Diff
9	Out	GPOUT1X-		39	In	DIG26-	
10	Out	GPOUT1X+	Diff	40	In	DIG26+	Diff
11	Out	GPOUT0X-		41	In	DIG25-	
12	Out	GPOUT0X+	Diff	42	In	DIG25+	Diff
13	Out	CT2X-		43	In	DIG24-	
14	Out	CT2X+	Diff	44	In	DIG24+	Diff
15	Out	CT1X-		45	In	DIG23-	
16	Out	CT1X+	Diff	46	In	DIG23+	Diff
17	Out	CT0X-		47	In	DIG22-	
18	Out	CT0X+	Diff	48	In	DIG22+	Diff
19	Out	CLKOUTX-		49	In	DIG21-	
20	Out	CLKOUTX+	Diff	50	In	DIG21+	Diff
21	In	LENX-		51	In	DIG20-	
22	In	LENX+	Diff	52	In	DIG20+	Diff
23	In	CLKINX-		53	In	DIG19-	
24	In	CLKINX+	Diff	54	In	DIG19+	Diff
25	In	FENX-		55	In	DIG18-	
26	In	FENX+	Diff	56	In	DIG18+	Diff

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Table 8-5 Connector P2 pinout

Pin	I/O	Signal	Com-ment	Pin	I/O	Signal	Comment
27	In	FIX-		57	In	DIG17-	
28	In	FIX+	Diff	58	In	DIG17+	Diff
29	In	DIG31-		59	In	DIG16-	
30	In	DIG31+	Diff	60	In	DIG16+	Diff

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8.4 P5, The I/O Connector, 14-Pin

Table 8-6 shows the pinout for the P5 connector. See Section 8.1.2 for more information on the meaning of the comment column.

Table 8-6 Connector P5 pinout

Pin	I/O	Signal	Comment
1	In	ENCDRB+	Diff & TTL
2	In	ENCDRB-	Diff & TTL
3	In	TRIGGERB+	Diff & TTL
4	In	TRIGGERB-	Diff & TTL
5	Out	GPOUT2	TTL
6		GND	
7	In	GPIN	TTL
8	Out	STROBE	TTL
9	Out	STROBE+	Diff
10	Out	STROBE-	Diff
11	In	TRIGGERA+	Diff & TTL
12	In	TRIGGERA-	Diff & TTL
13	In	ENCDRA+	Diff & TTL
14	In	ENCDRA-	Diff & TTL

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8.5 P6, The Sync Bus Connector, 14-Pin

Table 8-7 shows the pinout for the p6 connector.

Note: This connecotor is not available on the R3.

Note: All signals on the Sync Bus are TTL. The " _S" suffix means that the respective signal has been edge detected and synchronized. The polarity has also been accounted for, so that all those signals are active HI. FI and CLCKIN are passed through unchanged. MXSYNC is a special synchronization signal (state machines, phases, etc.).

Table 8-7 Connector P6 pinout

Pin	Signal
1	FEN_S
2	FI
3	LEN_S
4	MXSYNC
5	TRIGGERA_S
6	TRIGGERB_S
7	ENCODERA_S
8	ENCODERB_S
9	GND
10	CLKIN
11	GND
12	SYNCBUSY
13	BUSTRIG
14	NC

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