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Tetra-PMC+

High-Speed A/D I/O Card with Reconfigurable FPGA
and TigerSHARC® Link Ports
User's Guide



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BittWare also maintains the following Internet sites:

http://www.bittware.com	Contains product information, technical notes, support files available for download, and answers to frequently asked questions (FAQ).
ftp://ftp.bittware.com	Contains technical notes and support files. Login as "anonymous" and use your e-mail address for the password.

Tetra-PMC+ User's Guide

Hardware Revision 1

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			• Updated clock details	2.2.5, 3.2.2
			• Updated trigger details	Table 2-6
			• Corrected PMC pinout	2.3.6
			• Added table of reset events	Table 3-2
			• Updated TRPM pinout to FPGA on host board	Table 4-1
			• Updated link port interface detail	4.2.6
			• Updated Global ADC Clock control register	Table 4-18
			• Corrected Simulation Control register address	Table 4-19
			• Updated ADC Registers	Table 4-22
			• Corrected address of Decimation Control registers	Table 4-25
			• Corrected address of Pre-Trigger registers	Table 4-27
			• Updated ADC Status register	Table 4-30

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Contents

Chapter 1
Introduction

1.1 Overview of the Tetra-PMC+ 14
1.1.1 Tetra-PMC+ Features 14
1.1.2 Tetra-PMC+ System Overview 14
1.1.3 Tetra-PMC+ Software Overview 16

1.2 About This User's Guide 18
1.2.1 Purpose of This Document 18
1.2.2 Chapter Overviews 18

1.3 Other Helpful Documents and Tools 20
1.3.1 Documents for Further Reference 20
1.3.2 Software Development Tools 20

1.4 Contacting BittWare Technical Support 21

Chapter 2
Preparing the Tetra-PMC+ for Operation

2.1 Unpacking the Tetra-PMC+ 24

2.2 Mounting the Tetra-PMC+ on a Host 25

2.3 Tetra-PMC+ External Connectors 26
2.3.1 User Switch 28
2.3.2 FPGA Debug Header 29
2.3.3 FPGA Programming Header 30
2.3.4 Analog Input Connectors 32
2.3.5 External Clock Signal 32
2.3.6 External Trigger or Clock Out 32
2.3.7 PMC+ Interface 33

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2.4 Tetra-PMC+ Major Components 38
2.4.1 Cyclone II FPGA 39
2.4.2 A/D Converters 39
2.4.3 Amplifiers 40
2.4.4 Clock Options 40
2.4.5 LEDs 41

2.5 Installing the Software Tools 42
2.5.1 Installing the BittWare DSP21k-SF Toolkit 42
2.5.2 Installing Recommended Development Tools 43

2.6 Testing the Board to Make Sure It is Operating Properly 44
2.6.1 Testing the Board with DSP21k Toolkit Utilities 44

Chapter 3
Functional Description

3.1 Board Architecture Overview 46
3.1.1 A/D Interface 46
3.1.2 PCI Interface 47
3.1.3 Link Port Interface 47
3.1.4 JTAG Interface 47

3.2 Analog Interface 48
3.2.1 Analog Inputs 48
3.2.2 Clock Scheme 48
3.2.3 Internal or External Trigger 48

3.3 Cyclone II FPGA 49
3.3.1 A/D Interface 49
3.3.2 Link and Serial Port Interface 49
3.3.3 Local Bus Interface 49
3.3.4 JTAG Interface 50
3.3.5 User Configurable Blocks 50

3.4 PCI Interface 51

3.5 PMC+ Interface 52

3.6 Resetting the Board 53
3.6.1 Resetting via Power On 53

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3.6.2 . . . . . .Resetting via Board Reset53
3.6.3 ADC Event Resets. 53

3.7 Booting the Board 54

3.8 Using the Decimator 55
3.8.1 Enabling the Decimator. 55
3.8.2 Appropriate Sample Rates for the Decimator 55

Chapter 4
Programming Details for the Tetra Control Registers

4.1 System Overview and Sample Usage 58

4.2 External Interfaces 60
4.2.1 ADC Inputs 60
4.2.2 Trigger In/Clock Out 60
4.2.3 Exernal Clock Input 61
4.2.4 PCI Signals 61
4.2.5 PMC+ Pin Usage 61
4.2.6 Link Port Interface. 64

4.3 Memory Map 65

4.4 Register Descriptions 66
4.4.1 Board, Version, Status, Control 67
4.4.2 General Acquisition 74
4.4.3 ADC Registers 77

4.5 FPGA Block Memory Usage 85

Chapter 5
Configuring the Cyclone II FPGA

5.1 Using BitLoader to Configure the Cyclone II 88
5.1.1 Getting Ready to Load from the Host 88
5.1.2 Loading the Cyclone II from the Host with BitLoader 89

5.2 Burning a Cyclone II Program. 90

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5.2.1 Burning the Cyclone II Program into the SPROM 90
5.2.2 Loading the Boot Program via JTAG 90

Appendix A
ATLANTiS Primer

A.1 Overview of the ATLANTiS Architecture 92
A.1.1 The ATLANTiS Switch 93
A.1.2 ADCPerf Example 95
A.1.3 ATLANTiS Configuration Memory Usage 96

A.2 FPGA Implementation and Related Tools 97

A.3 Example of T2 Board–TRPM ATLANTiS Interface 98

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List of Figures

Figure 1-1 Block Diagram of the Tetra-PMC+ 15
Figure 1-2 Block Diagram Illustrating Software Tools Connectivity 16
Figure 1-3 BittWare Software Development Tools Overview 17
Figure 1-4 Block Diagram of the BittWorks Software Development Tools 17
Figure 2-1 Location of the Tetra's Connectors (Top) 26
Figure 2-2 Location of the Tetra's Connectors (Bottom) 26
Figure 2-3 View of Switch On and Off settings 28
Figure 2-4 Location of the Configuration Switch, S1 (Bottom) 28
Figure 2-5 Location of Debug & Programming Headers (J1, J2) (Top) 30
Figure 2-6 Location of the Analog Input, Clock, and Trigger Connectors 31
Figure 2-7 Location of the PMC Connectors (P1–P4) (Bottom) 34
Figure 2-8 Location of the Tetra Major Components (Top) 38
Figure 2-9 Location of the Tetra Major Components (Bottom) 38
Figure 3-1 Block Diagram of the Tetra-PMC+ 46
Figure 4-1 Sample Usage of the Tetra-PMC+ on a T26U Board 58
Figure 4-2 Programmable Components in a Tetra–T2 Setup 59
Figure 4-3 Signal Path of ADC Data on Tetra 60
Figure 4-4 Flag and Interrupt Configuration 61
Figure 4-5 PMC Flag Control Registers 70
Figure 4-6 PMC Interrupt Control Registers 72
Figure 4-7 ADC Acquisition Setup 78
Figure 4-8 FPGA Block Memory Usage 85
Figure A-1 ATLANTiS Architecture as Implemented on most T2 Family BittWare Boards 92
Figure A-2 ATLANTiS Switch Block Diagram 93
Figure A-3 PMC Programming Interface 100

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List of Tables

Table 2-1 PCI Signalling for PMC Interface 25
Table 2-2 External Connector Summary 27
Table 2-3 S1 Inputs to the Cyclone II 29
Table 2-4 FPGA Debug Header Pinout (J1) 29
Table 2-5 FPGA Configuration Header Pinout (J2) 30
Table 2-6 PMC Interface Pinout (P1, P2, P3) 35
Table 2-7 PMC+ Connector Pinout (P4) 37
Table 2-8 Cyclone II LED Connections 41
Table 2-9 FPGA Loader Versions for Various Operating Systems 43
Table 3-1 PMC+ Resource Overview 52
Table 3-2 Tetra Reset Events 53
Table 4-1 Tetra PMC+ Pinout to FPGA on Host T2 Board 62
Table 4-2 ADC 2's Complement (-1V to +1V) 64
Table 4-3 Offset Binary (0V to +2V) 64
Table 4-4 Memory Map 65
Table 4-5 Simulation Memory Format 65
Table 4-6 Register Map Overview 66
Table 4-7 Board, Version, Status, and Control Registers 67
Table 4-8 Contents of Version Info Register (0x02) 68
Table 4-9 Contents of Board Info Register (0x04) 68
Table 4-10 Contents of Board Control Register (0x06) 68
Table 4-11 LED Select Options 69
Table 4-12 Contents of Board Status Register (0x08) 69
Table 4-13 PMC Flag Control Register Format 70
Table 4-14 PMC Flag Select Options 71
Table 4-15 PMC Interrupt Control Register Format 72
Table 4-16 PMC Interrupt Select Options 73
Table 4-17 General Acquisition, applies to all channels 74

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Table 4-18 Contents of Global ADC Clock/Control Register (0x80) 74
Table 4-19 Contents of Simulation Control Register (0x86) 75
Table 4-20 Simulation Memory External Restart Select Signal Options 76
Table 4-21 ADC Registers 77
Table 4-22 Contents of ADC Control Registers (0x100, 0x200, 0x300, 0x400) 79
Table 4-23 Contents of Trigger Control Registers (0x106, 0x206, 0x306, 0x406) 80
Table 4-24 Trigger Select Options 81
Table 4-25 Contents of Decimation Control Registers (0x108, 0x208, 0x308, 0x408) . 82
Table 4-26 Contents of Desired Sample Count Registers (0x110, 0x210, 0x310, 0x410) . 82
Table 4-27 Contents of Pre-Trigger Registers (0x112, 0x212, 0x312, 0x412) 82
Table 4-28 Contents of Holdoff Registers (0x114, 0x214, 0x314, 0x414) 83
Table 4-29 Contents of ADC Threshold Registers (0x116, 0x216, 0x316, 0x416) 83
Table 4-30 Contents of ADC Status Registers (0x180, 0x280, 0x380, 0x480) 83
Table A-1 AdcPerf Batch Files 95
Table A-2 ATLANTIS Configuration Memory Map 96
Table A-3 FPGA Programming Tools 97
Table A-4 FPGA Load File Types 97
Table A-5 ATLANTiS Switch-1 Sources and Sinks 98
Table A-6 ATLANTiS Switch-2 Sources and Sinks 98
Table A-7 User LEDs 99
Table A-8 Digital I/O (DIO) Port Usage 99
Table A-9 ATLANTiS Programming Control Registers 99
Table A-10 GPIO Bit Usage 100

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Chapter 1
Introduction

The Tetra-PMC+ is a high-speed analog input card that provides data capture for four 14-bit, 105 MHz A/D channels and streams the digitized analog signals to an Altera®Cyclone© II FPGA, which provides A/D control, data distribution, and front-end processing capabilities. In addition to providing A/D control and data distribution, the FPGA provides the 32-bit, 66 MHz PCI interface and four TigerSHARC© link ports, making captured data available to the host DSP board.

This chapter covers the following topics:

- The basic architecture of the Tetra-PMC+ system
- An overview of each chapter in this user's guide
- Additional documents that provide more information about the Tetra-PMC+ components and software

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1.1 Overview of the Tetra-PMC+

This section gives a brief overview of the architecture of the Tetra-PMC+ board and describes its software.

1.1.1 Tetra-PMC+ Features

The Tetra-PMC+ features:

- High-performance wideband A/D
  - 4 channels, 14-bit A/D (Analog Devices © AD6645)
  - Up to 105 MHz per channel
- Cyclone II reconfigurable FPGA
  - A/D control and data distribution
  - Configurable pre-processing of high-speed A/D data
- 32-bit, 66 MHz PCI bus interface via Cyclone II
- Four external link ports
  - Configurable for TigerSHARC (TS201S) based boards
  - Available via PMC+ interface
- Internal/external clock and triggering
- Oven-controlled crystal oscillator (OCXO) for high-stability clock (optional)
- Complete software support
- Cyclone II development and customization support

1.1.2 Tetra-PMC+ System Overview

The Tetra-PMC+ is a high-speed analog input board that provides data capture for four 14-bit, up to 105 MHz A/D channels and streams the data directly to a Altera Cyclone II FPGA, which provides A/D control and data distribution and front-end processing capabilities. A 32-bit, 66 MHz PCI interface and four TigerSHARC link ports make the captured data available to the host board.

High-Speed A/D Interface

The high-speed A/D interface features four 14-bit A/D conversion channels, each sampled at up to 105 MHz. Using high-quality 14-bit A/D converters from Analog Devices, the analog interface provides input bandwidth up to 150 MHz and is available with DC coupled inputs. For clocking options, the board features an internal clock and an external

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clock and trigger. The clock is user-configurable to the on-board clock or external clock.

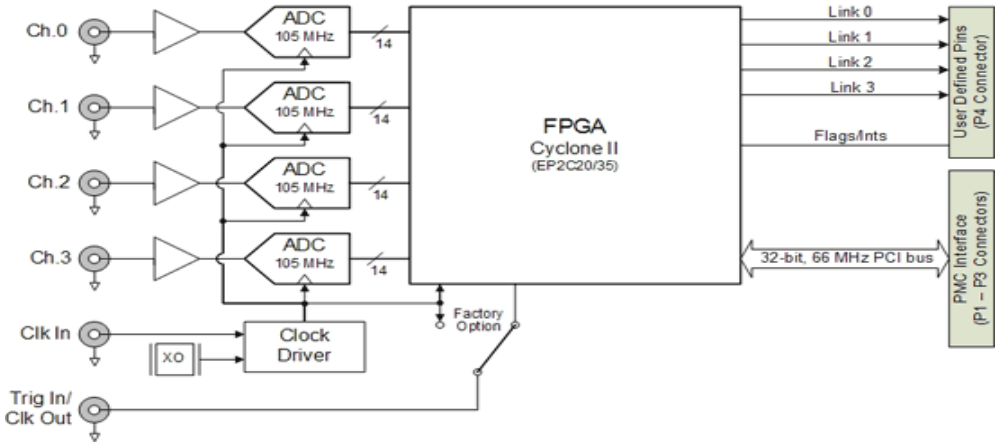
Altera Cyclone II Reconfigurable FPGA

The Cyclone II reconfigurable FPGA (Altera) provides A/D control and data distribution for the Tetra-PMC+ and is available for configurable preprocessing of high speed A/D data, such as digital filtering, decimation, and digital down conversion. To interface the A/D data to the host, the Cyclone II contains a link port interface for directly accessing ADSP-TS201S and a local bus interface to access the PCI host.

PMC+ I/O Interface

The Tetra-PMC+ is fully compatible with any PMC capable base board. When attached to one of BittWare's PMC+ base boards, it also supports BittWare's PMC+ extensions, which include four link ports directly to the Cyclone II FPGA. The PMC+ link ports are configurable for BittWare's T2 (ADSP-TS201S) base boards and are an ideal way to move high-speed data directly to the DSPs. Figure 1-1 is a detailed block diagram of the board.

Figure 1-1 Block Diagram of the Tetra-PMC+

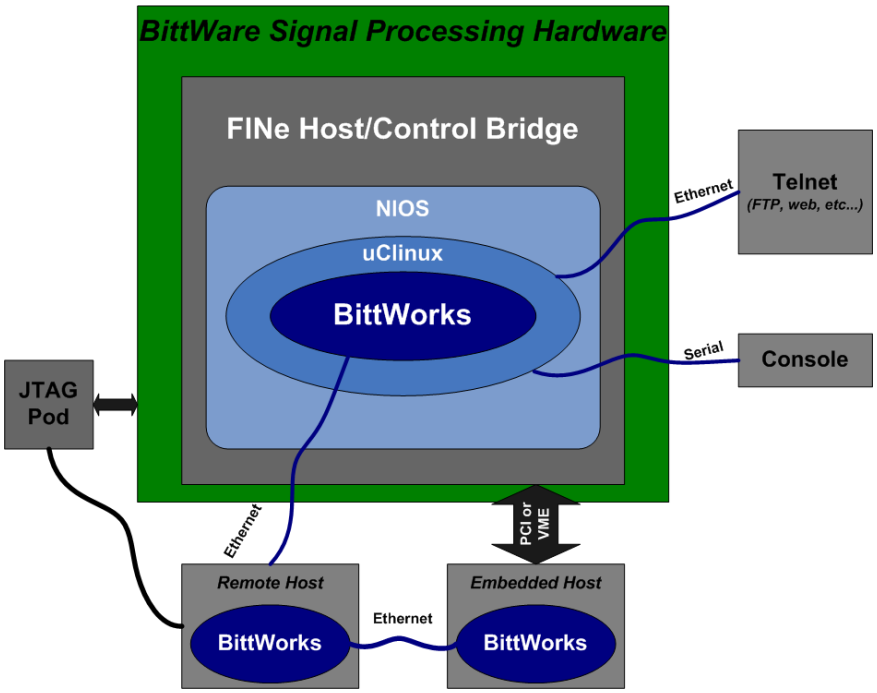


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1.1.3 Tetra-PMC+ Software Overview

BittWare offers complete software development tools that allow designers to easily develop application code and integrate the Tetra-PMC+ into their systems. For user-configured pre-processing, Altera also provides a complete suite of development tools for the Cyclone II. Figure 1-2 through Figure 1-4 are block diagrams of the software development tools for the Tetra-PMC+.

Figure 1-2 Block Diagram Illustrating Software Tools Connectivity



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Figure 1-3 BittWare Software Development Tools Overview

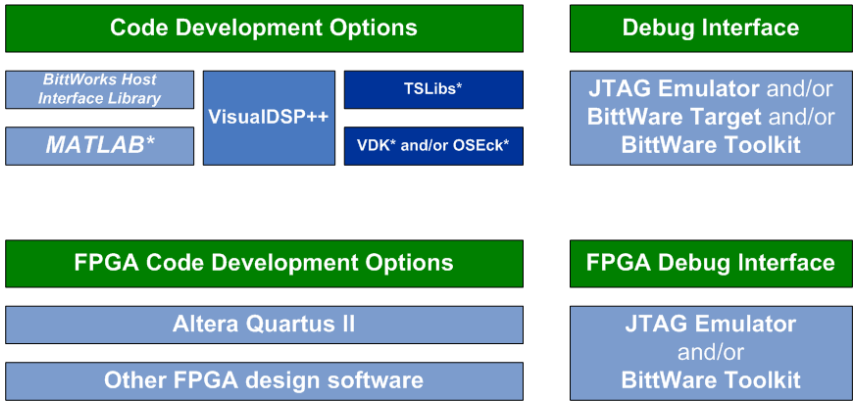
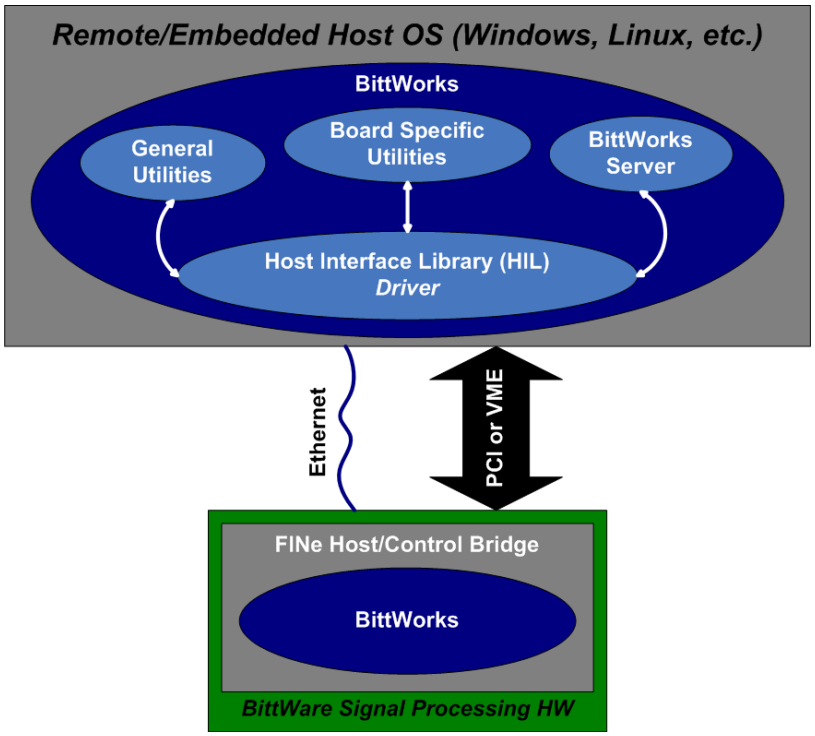


Figure 1-4 Block Diagram of the BittWorks Software Development Tools



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1.2 About This User's Guide

Note *This user's guide describes the Tetra-PMC+ with all connectors populated in the default configuration (see the Order Information section on the product data sheet). Keep in mind that your board may be configured differently, and that some information and settings may not apply to your hardware.*

1.2.1 Purpose of This Document

This user's guide covers hardware revision 1 of the Tetra-PMC+ board. The purpose of this document is to provide details about the board's major hardware components, to describe how to install and properly operate the board, and to discuss important issues that relate to programming the board.

To effectively use this user's guide, you should be familiar with the following:

- The Altera Cyclone II FPGA operation and programming as described in the *Cyclone II Device Handbook* from Altera, Inc. (if you are doing Cyclone II FPGA customization)
- The function of the AD6645 (or AD6644) A/D converter from Analog Devices, Inc.

1.2.2 Chapter Overviews

Chapter 2: Preparing the Tetra-PMC+ for Operation

This chapter shows the location of the Tetra's major components, connectors, and user switch and briefly discusses their function. It also discusses the board software and describes third party tools recommended for use with the Tetra-PMC+.

Chapter 3: Functional Description

This chapter discusses how the board functions. It covers the A/D interface, the Cyclone II FPGA, the PCI interface, the reset circuitry, and the boot procedure.

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Chapter 4: Programming Details for the Tetra Control Registers

This chapter provides programming details for the Tetra-PMC+ Cyclone II FPGA's control registers.

Chapter 5: Configuring the Cyclone II FPGA

Chapter 5 describes the different targets and steps involved in using BittWare's FPGA configuration utility.

Appendix A: ATLANTiS Primer

This appendix gives an overview of the ATLANTiS architecture that is implemented on the T2 host board's Virtex-II FPGA.

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1.3 Other Helpful Documents and Tools

This section gives sources for additional information that applies to the Tetra. It also lists several third party software development tools that you may find useful.

1.3.1 Documents for Further Reference

The documents in the list below provide additional information about the Tetra-PMC+ components and software.

- *DSP21k-SF Toolkit User's Guide* (Version 8.0 and up) – BittWare, Inc.
- *Host Interface Library Reference Manual* (Version 8.0 and up) – BittWare, Inc.
- *Cyclone II Device Handbook, Cyclone II Device Family Data Sheet* – Altera, Inc. (for users who are customizing the Cyclone II)
- *Quartus II® Design Software* – Altera, Inc.
- AD6645 Documentation – Analog Devices, Inc.
- User's guide for your host DSP board

1.3.2 Software Development Tools

BittWare Host Interface Support

BittWare supplies host interface support for the Tetra-PMC+ with the DSP21k-SF Toolkit. Using the Toolkit's C-callable library of routines, you can read from and write to the Tetra-PMC+ control registers and memory and control other board functions. The *DSP21k-SF Toolkit User's Guide* from BittWare, Inc. contains complete information about the DSP21k-SF Toolkit.

Optional IP Cores for Cyclone II

The Cyclone II is available for configurable preprocessing of high-speed A/D data, such as digital filtering, decimation, and digital down conversion. Many standard cores available for the Cyclone II. For details, contact BittWare.

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1.4 Contacting BittWare Technical Support

BittWare is dedicated to providing our customers with superior technical support. We offer the following types of technical support:

- **E-mail:** You can direct questions and feedback to us at support@bittware.com. Please include your name, company, address, phone number, and specific details about your request for technical support.
- **Phone:** You can call us directly at 603.226.0404 between the hours of 8:30 a.m. – 5:30 p.m. Eastern Standard Time.
- **BittWare's website:** Our website at http://www.bittware.com contains anomaly lists and FAQs.

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Chapter 2

Preparing the Tetra-PMC+ for Operation

This chapter describes the Tetra-PMC+ board's major components and connectors. It also discusses installing development software and different methods of testing the board using BittWare's software tools. After reading this chapter, you should be able to:

- Attach any desired external devices to the board
- Mount the Tetra-PMC+ on a host board
- Install the software tools for the Tetra-PMC+
- Identify the major components and connectors on the Tetra-PMC+

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2.1 Unpacking the Tetra-PMC+

Note *The Tetra-PMC+ contains electro-static discharge (ESD) sensitive devices. Be sure to follow the standard handling procedures for ESD sensitive devices, taking proper precautions to ground yourself and the work area before removing the board from its anti-static bag. If you fail to follow proper handling procedures, you could damage the board.*

To unpack the Tetra board,

1. Carefully remove the board from the shipping box. (Save the box and packing materials in case you need to reship the board.)
2. Remove the module from the plastic bag, observing all precautions described in the warning above to prevent damage from electro-static discharge (ESD).
3. Carefully examine the board, checking for damage. If the board is damaged, *do not* install it. Call BittWare technical support.

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2.2 Mounting the Tetra-PMC+ on a Host

Note *Please read the rest of this chapter before installing the Tetra-PMC+ on the host board as there may be additional tasks to complete prior to installation.*

To attach the Tetra-PMC+ to a PMC or PMC+ host board,

1. Orient the Tetra-PMC+ card so that pin 1 on the PMC connectors matches the orientation of pin 1 on the carrier board PMC connectors.
2. Plug the Tetra-PMC+'s PMC connectors into the PMC interface on the carrier board, and press the connectors firmly together.
3. Secure the Tetra-PMC+ to the mounting holes on the carrier board.

For more information about the PMC/PMC+ connectors, see section 2.3.7. Check the required PCI signalling and width to ensure that they fall within the ranges in the table below.

Table 2-1 PCI Signalling for PMC Interface

PMC Connectors	Host Access
P1, P2	32-bit PCI*
P1, P2, P3	32-bit PCI
P1, P2, P4	32-bit PCI and PMC+ extensions
P1, P2, P3, P4	32-bit PCI and PMC+ extensions

* Either 33 MHz or 66 MHz operation

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2.3 Tetra-PMC+ External Connectors

This section describes the external connectors on the Tetra-PMC+ board, gives their pinouts, and shows where they are located.

Figure 2-1 Location of the Tetra's Connectors (Top)

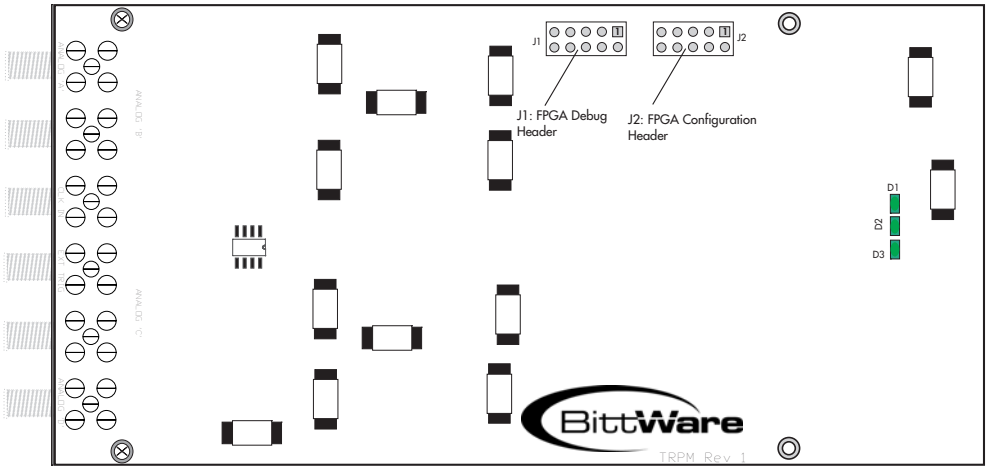
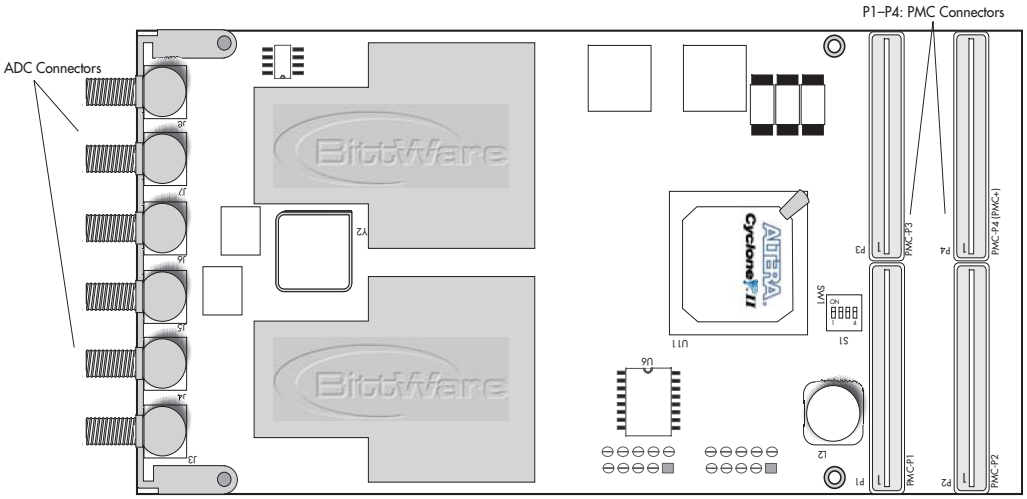


Figure 2-2 Location of the Tetra's Connectors (Bottom)



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Note *This user's guide describes the Tetra-PMC+ with all connectors populated in the default configuration (see the Order Information section on the product data sheet). Keep in mind that your board may be configured differently and that some information and settings may not apply to your hardware.*

Table 2-2 External Connector Summary

Connector	Description	Type	Refer to Section:
S1	FPGA user signals switch	4-DIP Switch	2.3.1
J1	FPGA debug	10-pin header	2.3.2
J2	FPGA program	10-pin header	2.3.3
J3	Analog 1 input	SMA or SMB	2.3.4
J4	Analog 2 input	SMA or SMB	2.3.4
J5	Clock input	SMA or SMB	2.3.5
J6	External Trigger (Clock output)	SMA or SMB	2.3.6
J7	Analog 3 input	SMA or SMB	2.3.4
J8	Analog 4 input	SMA or SMB	2.3.4
P1–P3	PMC interface	64-pin standard PMC*	2.3.7
P4	PMC+ interface	64-pin PMC with BittWare extensions	2.3.7

* P3 signals are not connected on the Tetra-PMC+; therefore, the PCI throughput is 32-bit.

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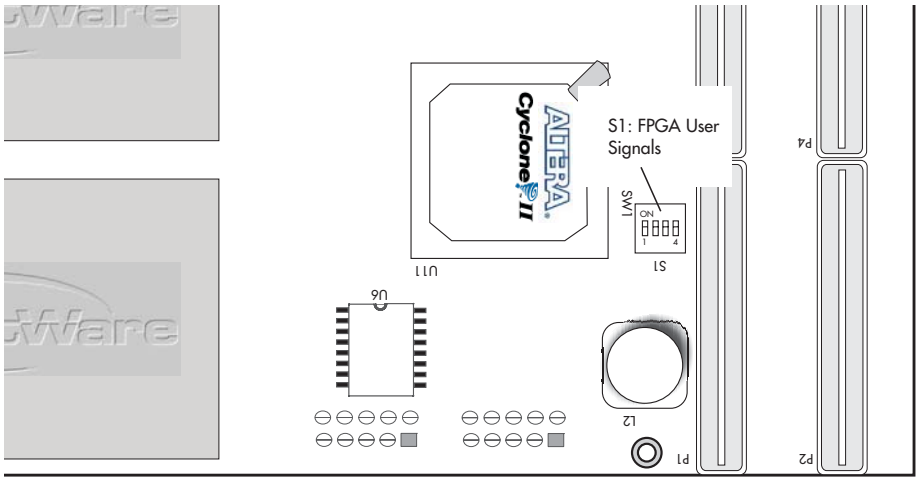
2.3.1 User Switch

The Tetra has a user switch, S1, that is connected to four user-configurable input signals on the Cyclone II FPGA. Set the dips on this switch before installing the Tetra, since the switch is on the bottom (PMC) side of the board. Refer to the *Cyclone II Platform FPGA Handbook* by Altera for details on setting the user-configurable pins. Figure 2-4 below shows the location of S1, and Table 2-3 describes each dip setting and gives the associated Cyclone pin name.

Figure 2-3 View of Switch On and Off settings



Figure 2-4 Location of the Configuration Switch, S1 (Bottom)



Note *You will only need to set the configuration switch if you are doing custom configuration of the Cyclone II. For details on setting these switches, contact BittWare support.*

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Table 2-3 S1 Inputs to the Cyclone II

Dip Switch	Description	ON	OFF	Cyclone II Pin Name
1	SW_USR0	0	1	T8
2	SW_USR1	0	1	R14
3	SW_USR2	0	1	R15
4	SW_USR3	0	1	U13

2.3.2 FPGA Debug Header

J1 is an optional 10-pin header that allows you to debug the FPGA over the JTAG interface. Its pinout is given in Table 2-4. Figure 2-6 on page 31 shows the location of both J1 and J2 headers.

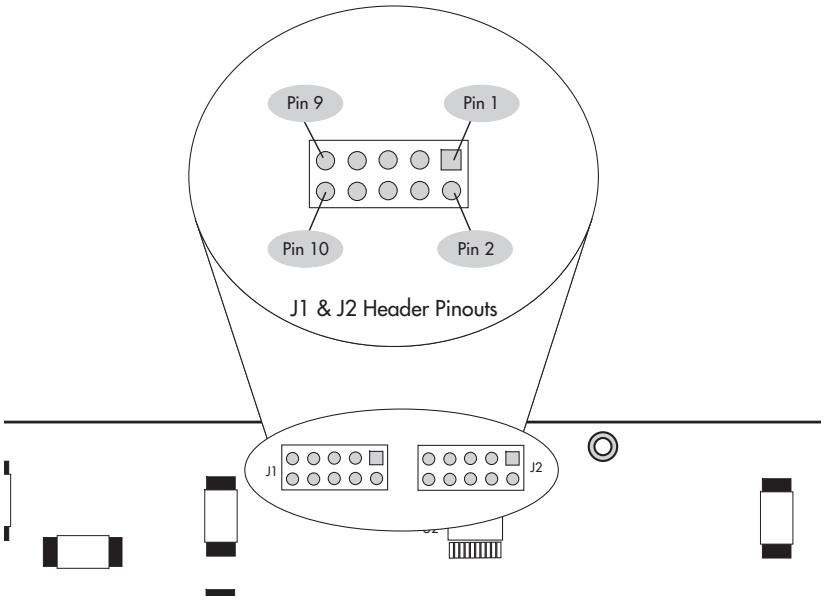
Table 2-4 FPGA Debug Header Pinout (J1)

Signal	Pin	Pin	Signal
JTAG_TCK	1	2	GND
JTAG_TDO	3	4	P3V3
JTAG_TMS	5	6	NC
NC	7	8	NC
JTAG_TDI	9	10	GND

Note *The FPGA test and configuration headers (J1 and J2) violate the PMC height specification and are not accessible in-system while maintaining a single slot.*

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Figure 2-5 Location of Debug & Programming Headers (J1, J2) (Top)



2.3.3 FPGA Programming Header

J2 is an optional 10-pin in-system programming header that allows you to update the FPGA load to the SPROM with the Altera Quartus II Design software and a programming tool such as USB Blaster. In most cases, any changes to the FPGA load should be done over the PCI bus from the host (see section 5.3). Table 2-5 gives the header's pinout. Refer also to Altera's software and programming tool manuals.

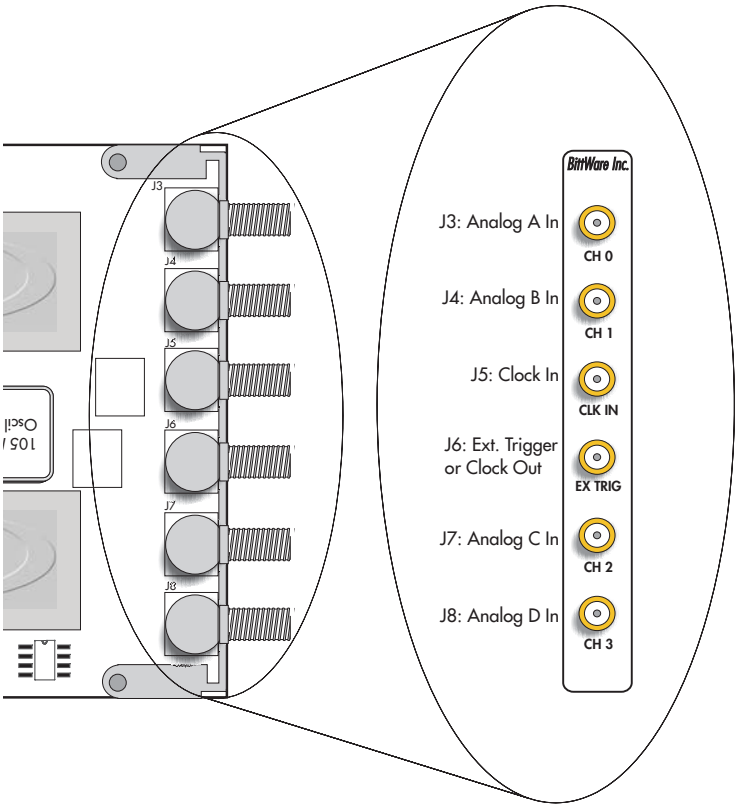
Table 2-5 FPGA Configuration Header Pinout (J2)

Signal	Pin	Pin	Signal
PROG01_FPGA_DCLK	1	2	GND
FLAG3_FPGA_CONF_DONE	3	4	P3V3
PROG04_FPGA_CONFIG	5	6	FLAG1_FPGA_CE
PROG03_FPGA_DATA0	7	8	PROG02_FPGA_CSO
PROG00_FPGA_ASDO	9	10	GND

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Figure 2-6 shows the location and layout of the analog input, clock, and trigger connectors, which are described in sections 2.3.4 through 2.3.6.

Figure 2-6 Location of the Analog Input, Clock, and Trigger Connectors



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2.3.4 Analog Input Connectors

Connectors J3, J4, J7 and J8 are the board's analog inputs, populated with either SMA or SMB connectors.

Connector	Channel	Signal
J3	Analog A	ALG_IN_A
J4	Analog B	ALG_IN_B
J7	Analog C	ALG_IN_C
J8	Analog D	ALG_IN_D

The inputs run at 105 MHz and are routed to a 14-bit A/D converter (Analog Devices AD6645), which is described in section 2.4.2 on page 39. The ADCs are DC coupled and terminated in 50Ω and are factory configured to one of the following options:

- **Bi-polar mode**: input signal is 2V peak to peak, ±1V
- **Uni-polar mode**: input signal is 2V peak to peak, 0V to 2V

2.3.5 External Clock Signal

Connector J5 is an external SMA or SMB connector that allows you to supply an external clock signal to the board. The connector is terminated in 50Ω and is brought directly to a high-speed buffer. The clock speed can be up to 105 MHz. Requirements for an external clock source are a minimum of 10 MHz, maximum of 105 MHz, 0 – 5V square wave. A 0 – 3.3V square wave will work, but a 0 – 5V square wave is optimal. Refer to section 4.2.2 on page 60 for details on the board's clock scheme.

2.3.6 External Trigger or Clock Out

The Tetra-PMC+ has an external SMB connector (J6) that allows you to supply external triggers to the board. The trigger is terminated in 50Ω and uses 3V signaling. It is buffered using a Schmidt-Triggered inverter and is brought to the Cyclone II. Control registers in the Cyclone II configure the operation of the trigger (see "Global ADC Clock/Control Register (0x80)" on page 74). This connector can also be configured as an external clock output, used to drive other boards in a multi-board configuration.

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2.3.7 PMC+ Interface

The PMC connectors are described below, and Table 2-6 on page 35 and Table 2-7 on page 37 provide their pinouts. Additional details about the PMC+ (P4) connector are in section 4.2.5 on page 61.

PMC Connectors

The Tetra's PMC interface features two standard PMC connectors (P1–P2), which provide the 32-bit, 66 MHz PCI interface to the host. Optional PMC connector P3, which normally supports 64-bit PCI throughput, is not connected. Figure 2-7 shows the location of the connectors.

PMC+ Connector

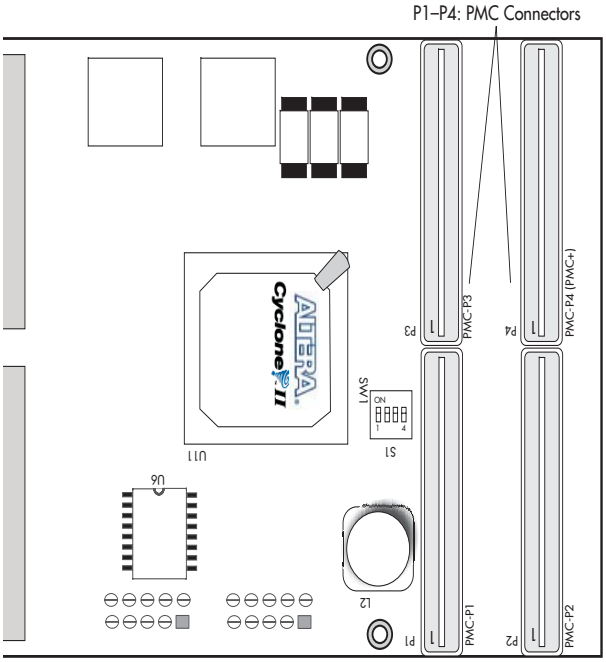
The PMC+ connector (P4), provides BittWare's PMC+ extensions, which include four link ports, flags, and interrupts directly to the DSPs on the host board.

Caution *BittWare uses P4 (PMC-P4) of the PMC connectors for our PMC+ extensions. If you are mounting the Tetra on a non-BittWare carrier board that uses the PMC-P4 connector, the carrier board may have incompatibilities with the PMC+ connector on the Tetra. Call BittWare technical support for assistance.*

Note *The PCI bus on the Tetra-PMC+ board is at its optimal compatibility with T26U and T2V6 boards by BittWare, running on DSP21k-SF software version 8.0 or higher.*

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Figure 2-7 Location of the PMC Connectors (P1–P4) (Bottom)



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Table 2-6 PMC Interface Pinout (P1, P2, P3)

P1 (PMC-P1)				P2 (PMC-P2)			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	NC	2	N12V	65	P12V	66	NC
3	GND	4	$\overline{\text{INTA}}$	67	NC	68	TDO
5	$\overline{\text{INTB}}$	6	$\overline{\text{INTC}}$	69	TDI	70	GND
7	GND	8	PMC_P5VA	71	GND	72	NC
9	$\overline{\text{INTD}}$	10	NC	73	NC	74	NC
11	GND	12	NC	75	NC	76	P3V3
13	CLK	14	GND	77	$\overline{\text{RST}}$	78	NC
15	GND	16	$\overline{\text{GNT}}$	79	PMC_P3V3A	80	NC
17	$\overline{\text{REQ}}$	18	PMC_P5VA	81	NC	82	GND
19	V(I/O)	20	AD[31]	83	AD[30]	84	AD[29]
21	AD[28]	22	AD[27]	85	GND	86	AD[26]
23	AD[25]	24	GND	87	AD[24]	88	P3V3
25	GND	26	$\overline{\text{C/BE3}}$	89	$\overline{\text{IDSEL}}$	90	AD[23]
27	AD[22]	28	AD[21]	91	PMC_P3V3A	92	AD[20]
29	AD[19]	30	P5V	93	AD[18]	94	GND
31	V(I/O)	32	AD[17]	95	AD[16]	96	$\overline{\text{C/BE[2]}}$
33	$\overline{\text{FRAME}}$	34	GND	97	GND	98	NC
35	GND	36	$\overline{\text{IRDY}}$	99	$\overline{\text{TRDY}}$	100	P3v3
37	$\overline{\text{DEVSEL}}$	38	P5V	101	GND	102	$\overline{\text{STOP}}$
39	GND	40	NC	103	$\overline{\text{PERR}}$	104	GND
41	NC	42	NC	105	P3V3	106	$\overline{\text{SERR}}$
43	PAR	44	GND	107	$\overline{\text{C/BE[1]}}$	108	GND
45	V(I/O)	46	AD[15]	109	AD[14]	110	AD[13]
47	AD[12]	48	AD[11]	111	$\overline{\text{M66EN}}$	112	AD[10]
49	AD[09]	50	P5V	113	AD[08]	114	P33V
51	GND	52	$\overline{\text{C/BE[0]}}$	115	AD[07]	116	NC
53	AD[06]	54	AD[05]	117	P3V3	118	NC
55	AD[04]	56	GND	119	NC	120	GND
57	V(I/O)	58	AD[03]	121	NC	122	NC
59	AD[02]	60	AD[01]	123	GND	124	NC
61	AD[00]	62	P5V	125	NC	126	P3V3
63	GND	64	NC	127	GND	128	NC

(Sheet 1 of 2)

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Table 2-6 PMC Interface Pinout (P1, P2, P3) (Continued)

P3 (PMC-P3)			
Pin	**Signal**	**Pin**	**Signal**
1	NC	2	GND
3	GND	4	NC
5	NC	6	NC
7	NC	8	GND
9	VIO	10	NC
11	NC	12	NC
13	NC	14	GND
15	GND	16	NC
17	NC	18	NC
19	NC	20	GND
21	VIO	22	NC
23	NC	24	NC
25	NC	26	GND
27	GND	28	NC
29	NC	30	NC
31	NC	32	GND
33	GND	34	NC
35	NC	36	NC
37	NC	38	GND
39	VIO	40	NC
41	NC	42	NC
43	NC	44	GND
45	GND	46	NC
47	NC	48	NC
49	NC	50	GND
51	GND	52	NC
53	NC	54	NC
55	NC	56	GND
57	VIO	58	NC
59	NC	60	NC
61	NC	62	GND
63	GND	64	NC

(Sheet 2 of 2)

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Table 2-7 PMC+ Connector Pinout (P4)

P4 (PMC-P4)				
Pin	**Signal**	**Pin**	**Signal**	**Connection to DSPs**
1	FLAG0	2	FLAG1_FPGA_CE	
3	IRQ0	4	IRQ1	
5	L0DATA0_N	6	L1DATA0_N	
7	L0DATA0_P	8	L1DATA0_P	
9	L0DATA1_N	10	L1DATA1_N	
11	L0DATA1_P	12	L1DATA1_P	
13	L0DATA2_N	14	L1DATA2_N	
15	L0DATA2_P	16	L1DATA2_P	
17	L0DATA3_N	18	L1DATA3_N	
19	L0DATA3_P	20	L1DATA3_P	
21	LINKVALID_0_N	22	LINKVALID_1_N	
23	LINKVALID_0_P	24	LINKVALID_1_P	
25	LINKACKI0	26	LINKAKI1	
27	L0_BCMP	28	L1_BCMP	
29	FLAG2	30	FLAG3_FPGA_CONF_DONE	
31	IRQ2	32	IRQ3	
33	L2DATA0_N	34	L3DATA0_N	
35	L2DATA0_P	36	L3DATA0_P	
37	L2DATA1_N	38	L3DATA1_N	
39	L2DATA1_P	40	L3DATA1_P	
41	L2DATA2_N	42	L3DATA2_N	
43	L2DATA2_P	44	L3DATA2_P	
45	L2DATA3_N	46	L3DATA3_N	
47	L2DATA3_P	48	L3DATA3_P	
49	LINKVALID_2_N	50	LINKVALID_3_N	
51	LINKVALID_2_P	52	LINKVALID_3_P	
53	LINKACKI2	54	LINKACKI3	
55	L2_BCMP	56	L3_BCMP	
57	PROG00_FPGA_ASD0	58	$\overline{\text{PMC_RST}}$	
59	PROG01_FPGA_DCLK	60	PROG04_FPGA_CONFIG	
61	PROG02_FPGA_CSO	62	CLK_MAST0_N	
63	PROG03_FPGA_DATA0	64	CLK_MAST0_P	

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2.4 Tetra-PMC+ Major Components

Figure 2-8 and Figure 2-9 highlight the major components on the Tetra. The sections that follow describe the features highlighted in the diagrams.

Figure 2-8 Location of the Tetra Major Components (Top)

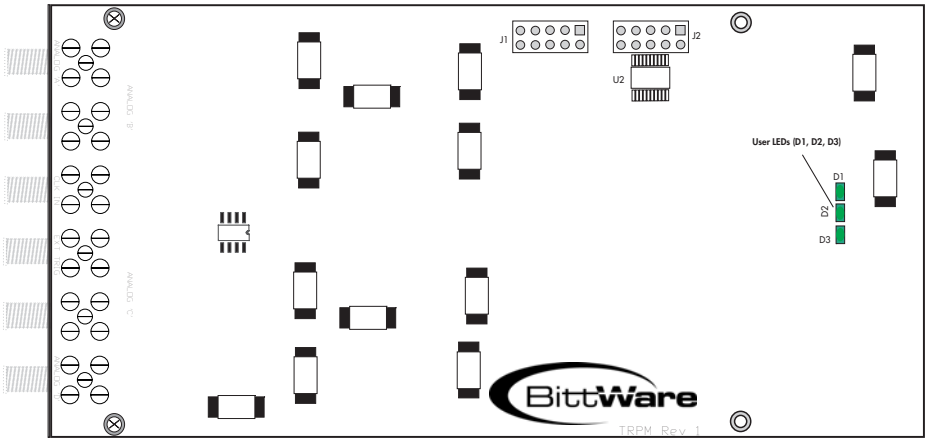
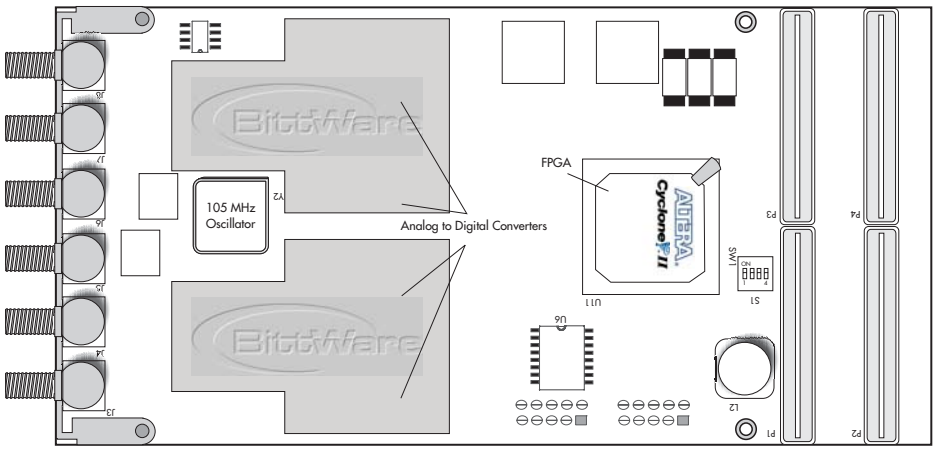


Figure 2-9 Location of the Tetra Major Components (Bottom)



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2.4.1 Cyclone II FPGA

The Cyclone II reconfigurable FPGA from Altera (part number EP2C20F484) provides A/D control and data distribution for the Tetra-PMC+ and is available for configurable preprocessing of high-speed A/D data, such as digital filtering, decimation, and digital down conversion. The FPGA provides the following features:

- A/D control and data distribution
- Configurable pre-processing of high-speed A/D data
- SRAM-based in-system configuration via SPROM or host
- Four TigerSHARC link ports from Cyclone II to PMC+ interface
- FIFOs for storing A/D data
- User-configurable blocks
- Optional third party IP cores

2.4.2 A/D Converters

The Tetra features four AD6645 A/D converters (ADCs) from Analog Devices, Inc. The AD6645 is a high-speed, high-performance, monolithic 14-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on the chip to provide a complete conversion solution. The AD6645 provides CMOS-compatible digital outputs.

The AD6645 maintains 100 dB multitone, spurious-free dynamic range (SFDR) through the second Nyquist band. This breakthrough performance eases the burden placed on multimode digital receivers (software radios) that are typically limited by the ADC. Noise performance is exceptional; typical signal-to-noise ratio is 74.5 dB through the first Nyquist band.

The AD6645 provides the following features:

- SNR =75 dB, fin 15 MHz @ 80 MSPS
- SNR =72 dB, fin 200 MHz @ 80 MSPS
- SFDR =89 dBc, fin 70 MHz @ 80 MSPS
- 100 dB multitone SFDR
- IF sampling to 200 MHz
- Sampling jitter 0.1 ps
- 1.5 W power dissipation
- Differential analog inputs

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- Two's complement digital output format
- 3.3 V CMOS-compatible
- DataReady for output latching

Note *The specifications listed above are for the AD6645 ADC and do not necessarily reflect the performance of the Tetra-PMC+ board.*

2.4.3 Amplifiers

For the ADC inputs, the Tetra-PMC+ features low distortion differential ADC drivers that perform as operational amplifiers (op amps), but can be configured for either single-ended-to-differential or differential-to-differential amplification. The ADC drivers have a 320 MHz bandwidth, and preserve the low frequency and DC information from the ADCs.

2.4.4 Clock Options

On-Board Clock

The Tetra-PMC+ features a standard oscillator (XO) internal clock that drives the A/D converters. The default configuration for this oscillator is 105 MHz (the top speed of the A/D converters), but your board may be configured with a clock operating at 65 MHz or 80 MHz.

External Trigger/Clock Output

Connector J6 is configurable as either an external trigger input (see section 2.3.6) or as a clock output to drive other boards.

Clock Input

Connector J5 provides an additional external clock input as described in section 2.3.5 on page 32.

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2.4.5 LEDs

The Tetra-PMC+ features three LEDs that show the state of signals within the Cyclone II. The LEDs are ON when the corresponding signal is at logic-1. Table 2-8 below lists which signal is connected to which LED, and “Board Control Register (0x06)” on page 68 lists its possible connections.

Table 2-8 Cyclone II LED Connections

LED	Signal
D1	LED0_BUF
D2	$\overline{\text{LED1_BUF}}$
D3	$\overline{\text{LED2_BUF}}$

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2.5 Installing the Software Tools

This section provides an overview of installing the software necessary for operating the Tetra-PMC+ board.

2.5.1 Installing the BittWare DSP21k-SF Toolkit

This section gives a basic overview of installing the BittWare DSP21k-SF Toolkit. The Tetra-PMC+ is compatible with version 8.0 and greater of the Toolkit. For detailed installation instructions, refer to the *DSP21k-SF Toolkit User's Guide*.

Overview of the DSP21k-SF Toolkit

BittWare's DSP21k-SF Toolkit is a set of libraries and utilities that enable you to develop host applications for the Tetra-PMC+ more quickly and easily. It contains a host interface library of C-callable functions for PC-based programs, diagnostic utilities, and demo programs.

Libraries. The primary component of the DSP21k-SF Toolkit is the Host Interface Library (HIL). The HIL is a library of C-callable functions for host programs that allows you to read from and write to the DSP's memory and control other board functions.

Diagnostic Utilities. Diag21k is a character-based diagnostic utility that lets you interactively access the Tetra-PMC+. It also provides assembler level debugging capabilities, including breakpoints.

BitLoader Utility. The BitLoader utility is used to load .rpd and existing logic files onto the Cyclone II FPGA.

Installing the DSP21k-SF Libraries and Utilities

Run the DSP21k-SF Toolkit setup program to install the DSP21k-SF Toolkit libraries and utilities. The *DSP21k-SF Toolkit User's Guide* explains the procedure in more detail.

Installing the BitLoader Utility

Three versions of the BitLoader utility are included on the DSP21k-SF Toolkit CD-ROM to accommodate different operating systems. Refer to Table 2-9 for the file paths for each operating system. To install BitLoader, copy the applicable program file from the example CD-ROM to your local drive using the following path: `%dsp21ksf%\bin`. For Windows and MS-DOS operating systems, you must also copy the driver library file `bitlib.dll` to `%dsp21ksf%\bin`.

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Table 2-9 FPGA Loader Versions for Various Operating Systems

Operating System	Program File Path	Driver Library File Path
Windows	DSP21k-SF Toolkit\bin\BitLoader.exe	DSP21k-SF Toolkit\bin\bitlib.dll
MS-DOS	DSP21k-SF Toolkit\bin\bitldr.exe	DSP21k-SF Toolkit\bin\bitlib.dll
Linux	DSP21k-SF Toolkit\linux\bitldr	n/a

Verifying that the Board is Configured Properly

The BittWare Configuration Manager is a utility included with the DSP21k-SF Toolkit that allows you to install, uninstall, or get and set properties for the Tetra board. The *DSP21k-SF Toolkit User's Guide* explains how to run the BittWare Configuration Manager. Run this program only after attaching the Tetra-PMC+ to your carrier board and installing it in your system.

2.5.2 Installing Recommended Development Tools

BittWare supports and recommends the following development tools:

- Altera Quartus II Development Software
- In-system Programming Header - Altera USB Blaster

FPGA Development Software

BittWare provides support files for the Quartus II Development software, including <<.cdf>> files. Quartus II creates FPGA <<.mcs>> files, which can be loaded to the Cyclone II or SPROM via the PCI interface from the host board. For details on the installation and use of the Altera development suite, refer to the software's user documentation.

Programming Tool

The Tetra-PMC+ provides a 10-pin header compatible with one of the optional in-system programming devices (such as USB Blaster by Altera) that work in conjunction with the Quartus II Development software. This device uses the JTAG interface to download FPGA-logic files to the SPROM. For details about the programming header, refer to section 2.3.3 on page 30.

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2.6 Testing the Board to Make Sure It is Operating Properly

This section discusses running diagnostic tests on the DSPs to make sure the board is operating properly.

2.6.1 Testing the Board with DSP21k Toolkit Utilities

The DSP21k-SF Toolkit contains the Diag21k utility for testing the board to make sure it is operating properly. Diag21k is a character-based diagnostic utility that starts from the MS-DOS command prompt. It lets you interactively access the Tetra-PMC+.

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Chapter 3
Functional Description

This chapter describes how the Tetra-PMC+ board functions. It covers the following topics:

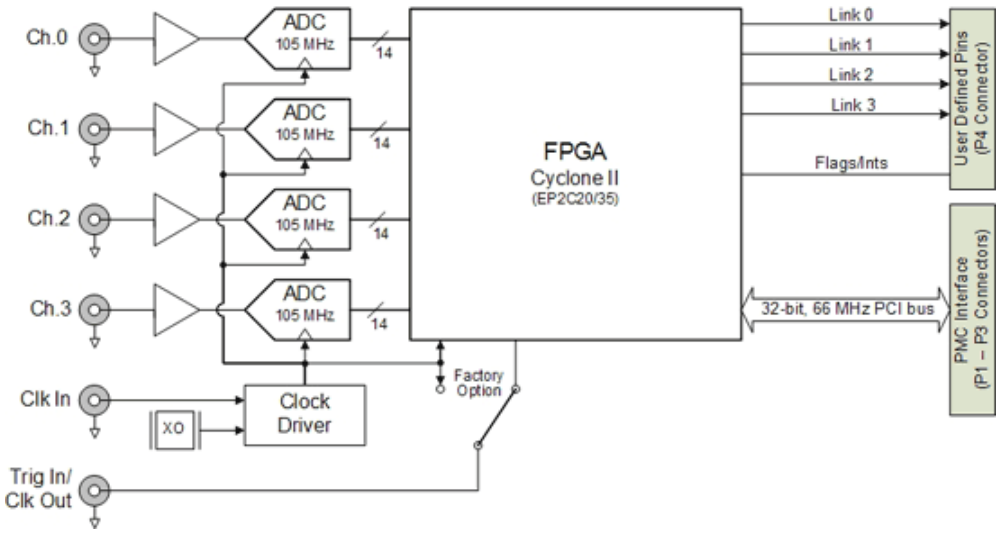
- Overview of the board's architecture (section 3.1 on page 46)
- The function of the A/D interface, clock scheme, and trigger (section 3.2 on page 48)
- The function of the Cyclone II FPGA (section 3.3 on page 49)
- The function of the PCI interface (section 3.4 on page 51)
- The function of the PMC+ interface (section 3.5 on page 52)
- Resetting the board (section 3.6 on page 53)
- Booting the board (section 3.7 on page 54)
- Using the decimator (section 3.8 on page 55)
- The board's power requirements (section 3.10 on page 55)

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3.1 Board Architecture Overview

This section provides an overview of the Tetra-PMC+ board architecture. Figure 3-1 below is a block diagram of the board.

Figure 3-1 Block Diagram of the Tetra-PMC+



3.1.1 A/D Interface

The Tetra-PMC+ features four 14-bit, 105 MHz analog inputs, which provide analog data to four Analog Devices A/D converters (AD6645). The A/D converters stream the converted data to the Altera Cyclone II FPGA, which provides A/D control and data distribution. The Cyclone II stores the data in its FIFOs, where the host can access it via link port or 32-bit, 66 MHz PCI bus.

For clocking options, the board features an on-board clock or an external clock input. The on-board clock is a standard oscillator (XO) operating at up to 105 MHz. A programmable clock divider is available for the on-board clock. An internal (software) or external trigger is also provided.

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3.1.2 PCI Interface

The Cyclone II provides the 32-bit, 66 MHz PCI interface between the host and PMC connectors.

3.1.3 Link Port Interface

The Cyclone II has a link port core that provides four link ports connected directly to the PMC+ interface. The PMC+ interface connects the links directly to the DSPs on a BittWare T2-based (ADSP-TS201S) carrier board running version 8.0 or greater of BittWare's DSP21k-SF Tools.

3.1.4 JTAG Interface

The Tetra features an optional JTAG programming header which interfaces to the SPROM and Cyclone II FPGA.

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3.2 Analog Interface

The Tetra-PMC+ analog interface consists of four A/D input connectors, and four A/D converters (Analog Devices AD6645) which are collectively referred to as ADCs; external clock and trigger inputs; on-board clock, and the Cyclone II A/D interface core.

3.2.1 Analog Inputs

Four SMA or SMB connectors provide the A/D inputs (section 2.3.4 on page 32), which each connect directly to an Analog Devices A/D converter. The A/D converters digitize the data (14 bits, up to 105 MHz) and stream it to the Cyclone II.

3.2.2 Clock Scheme

The Tetra-PMC+ has two options for the clock source: its on-board clock (XO), or an external clock input via J5 (section 2.3.5 on page 32). The ADC Clock Control register selects the source of the clock (see "Global ADC Clock/Control Register (0x80)" on page 74 for complete register description). Depending on the option ordered, the on-board clock can be 65, 80, or 105[1] MHz.

3.2.3 Internal or External Trigger

The Tetra-PMC+ has two trigger options: an internal trigger, which is controlled by the ADC Control registers, or an optional external trigger input via J6 (see section 2.3.6 on page 32). See "Internal Trigger Period A, B (0x82, 0x84)" on page 74 for a complete register description.

1. 105 MHz is the default configuration.

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3.3 Cyclone II FPGA

The Tetra-PMC+ features a Cyclone II reconfigurable FPGA (Altera) to provide A/D control and data distribution. It is available for configurable preprocessing of high speed A/D data, such as digital filtering, decimation, and digital down conversion. To interface the A/D data to the host, the Cyclone II contains a link port interface for directly accessing ADSP-T201S DSPs and a local bus interface to access the PCI host.

3.3.1 A/D Interface

The Cyclone II features an A/D interface core to provide A/D control and data distribution for the Tetra-PMC+. The Cyclone II contains control registers that control the type of data acquisition to be performed. These registers are accessible via the PCI bus. A typical data acquisition process consists of setting the acquisition size, selecting the trigger and clock sources, and activating the acquisition. In addition to these, the Cyclone II also provides a wide variety of options that can be configured in the control registers to initiate a desired transaction.

3.3.2 Link and Serial Port Interface

The Cyclone II has a link port core to provide four link port connections directly to the PMC+ interface. The PMC+ interface provides a direct connection to the DSPs on a BittWare T2 carrier board. The link port connections are as follows (see section 3.5 for more detail):

- PMC+ Link 0 --> Cyclone II Link 0
- PMC+ Link 1 --> Cyclone II Link 1
- PMC+ Link 2 --> Cyclone II Link 2
- PMC+ Link 3 --> Cyclone II Link 3

3.3.3 Local Bus Interface

The Cyclone II has a local bus core to provide a 32-bit PCI bus to the host board. The Data Offload Mode register in the Cyclone II selects whether the data bus or the link ports will provide the data path for the A/D data between the Cyclone II and the host board (see section 4.2.1 on page 60 for complete register description).

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3.3.4 JTAG Interface

An optional programming header (J2) is available to allow the Cyclone II and SPROM to be configured via JTAG using the Altera design software and Altera USB Blaster.

Note that only users who are doing custom configurations of the Cyclone II will need to use this software and device (we recommend the Quartus II Design Software and USB Blaster device).

3.3.5 User Configurable Blocks

Space is available in the Cyclone II for user configurable blocks to allow you to customize the Tetra-PMC+ for nearly any data acquisition application. A variety of third party IP cores are available for use with the Tetra-PMC+. For additional details on customizing the Cyclone II, refer to the Cyclone II documentation from Altera.

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3.4 PCI Interface

The PCI interface is implemented by the Cyclone II FPGA and provides the communication to the host board via the PMC+ interface. The Tetra's PCI interface is 32-bits, 3.3V signalling only, and supports both 33 MHz and 66 MHz.

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3.5 PMC+ Interface

The PMC+ interface is available as an extension of the standard PMC interface. It provides the following signals from the Tetra to the host:

- four link ports
- two flags
- four interrupts
- general purpose signals
- differential clock

The PMC+ interface also provides a reset line from the host to the Tetra. The interface is available via the PMC-P4 (P4) connector of the PMC interface and is compatible only with BittWare host boards populated with ADSP-TS201S (T2) DSPs and running BittWare DSP21k-SF tools version 8.0 or higher. Table 3-1 below outlines the connections to the PMC+ interface.

Table 3-1 PMC+ Resource Overview

PMC+ Resource	Connection on Tetra-PMC+ Board
Link port 1	Cyclone II link port 1
Link port 2	Cyclone II link port 2
Link port 3	Cyclone II link port 3
Link port 4	Cyclone II link port 4
TDM serial port	Cyclone II TDM serial port*
I2C interface†	General purpose
Reset	From T2 Carrier

* Not implemented on Tetra-PMC+.
† Not used on Tetra-PMC+.

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3.6 Resetting the Board

The Tetra-PMC+ will be reset under the conditions listed in Table 3-2 below. The sections that follow provide more detail.

Table 3-2 Tetra Reset Events

By Reset Type	Description	Cause(s)
Power on reset	Reset all registers, FIFOs, links, and PLLs	Power up and/or PCI bus reset
Board reset	Reset all registers, FIFOs, and links	"Board Reset" command in Diag21k or HIL. Or write to Reset address (offset 0x90).
ADC PLL reset	Reset ADC PLL, FIFOs, and links	Automatically when switching to external clock, or forced with Global ADC register bit D3
ADC Global Reset	Reset FIFOs and links	Global ADC register bit D0
ADC Flush	Reset FIFOs and links	Self-clearing register bit. This is done on a per-channel basis in the AdcCtl register. ADC's channels are also flushed when AdcClock PLL is not locked.

3.6.1 Resetting via Power On

When the Tetra-PMC+ is powered on or the PCI bus is reset, the registers, FIFOs, links, and PLLs are reset.

3.6.2 Resetting via Board Reset

Issuing the Host Interface Library or Diag21k board reset command will reset all the registers, FIFOs, and links. Additionally, writing to the Reset Address (offset 0x90) will cause a board reset.

3.6.3 ADC Event Resets

Any of these three ADC events will reset the FIFO and links:

ADC PLL reset: occurs when switching to the external clock or forced with Global ADC register bit D3 ("Global ADC Clock/Control Register (0x80)" on page 74). Also resets ADC PLL.

ADC Global reset: resets when forced with Global ADC register bit D0 ("Global ADC Clock/Control Register (0x80)" on page 74).

ADC Flush: occurs with writes to bit 2 of the self-clearing register bit in any of the four ADC channels ("ADC Control Registers (Ch A: 0x100, Ch B: 0x200, Ch C: 0x300, Ch D: 0x400)" on page 78). The ADC channels are also flushed when the ADC Clock PLL is not locked.

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3.7 Booting the Board

By default, the Cyclone II is set to boot from the SPROM. However, BittWare can provide updates and fixes as .rpd files that you can load and run with BittWare's BitLoader utility. Refer to Chapter 5 for details on loading files with BitLoader.

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3.8 Using the Decimator

The Tetra features a simple decimator to allow you to effectively sample at rates lower than specified for the AD6645 A/Ds. Using the decimator, you can run the converters at a higher speed and decimate to achieve your desired sample rate. For example, with an 80 MHz onboard oscillator, you can achieve 10 MSample/second sampling by using the clock divider to run the converters at 40 MSamples/second, and set the decimator to decimate by 4. There are two important things to note with the decimator.

- First, it is only meant to be used at actual converter clock rates of 52.5 MHz or less (i.e. you cannot run the converters at 105 MHz when using the decimator).
- Second, this is a brute force decimation with no filtering (i.e. samples are simply thrown away).

3.8.1 Enabling the Decimator

The decimator is enabled in the ADC Control register using bit 15. Bits 14:0 of the ADC Control register specify the decimation value. These bits tell the Tetra how many samples to throw away for every sample kept. A value of 0 means no decimation (keep 1, throw away 0), while a value of 3 is a decimate by 4 (keep 1, throw away 3). Do not enable the decimator and use a value of 0, since you are not actually decimating.

3.8.2 Appropriate Sample Rates for the Decimator

The sole purpose for using the decimator is to sample at rates lower than specified by Analog Devices for the AD6645. For details on these specifications, please refer to the data sheets for these parts. Since the decimator is being provided for this purpose, we have not validated the decimator at greater than 52.5 MHz ADC clock rates.

Note that 52.5 MHz is well above the specified minimum sampling rates of the AD6645 (30 MHz). The AD6645-specified minimum sampling frequencies are the minimum frequency at which Analog Devices guarantees the specified performance. However, this does not mean the converters will not operate below these frequencies. In testing at BittWare, we have seen the AD6645 converters perform acceptably at 10 MHz sampling rates. You can decide whether to just run the converters at the slower rate or run them faster and use the decimator. You can use an external clock in combination with the decimator. The 52.5 MHz maximum sample rate still applies, however.

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Chapter 4
Programming Details for the Tetra Control Registers

This chapter provides programming details for the Tetra control registers. For users who are configuring the Cyclone II themselves, additional Cyclone II programming details are available in the Cyclone II documentation from Altera.

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4.1 System Overview and Sample Usage

The Tetra-PMC+ is a 4-channel high-speed ADC interface PMC board. A typical setup includes the Tetra mounted on a BittWare T2-family board, such as the T2-6U-CPCI board (T26U) as illustrated in Figure 4-1.

In this example, the T26U has a Tetra-PMC+ with 4-channels ADC. The data passes between the Cyclone II FPGA on the Tetra and the FPGA on the T26U, through the T26U's DSPs, and then back to the T26U FPGA. Finally, it passes to the Combiner via a custom backplane.

Figure 4-1 Sample Usage of the Tetra-PMC+ on a T26U Board

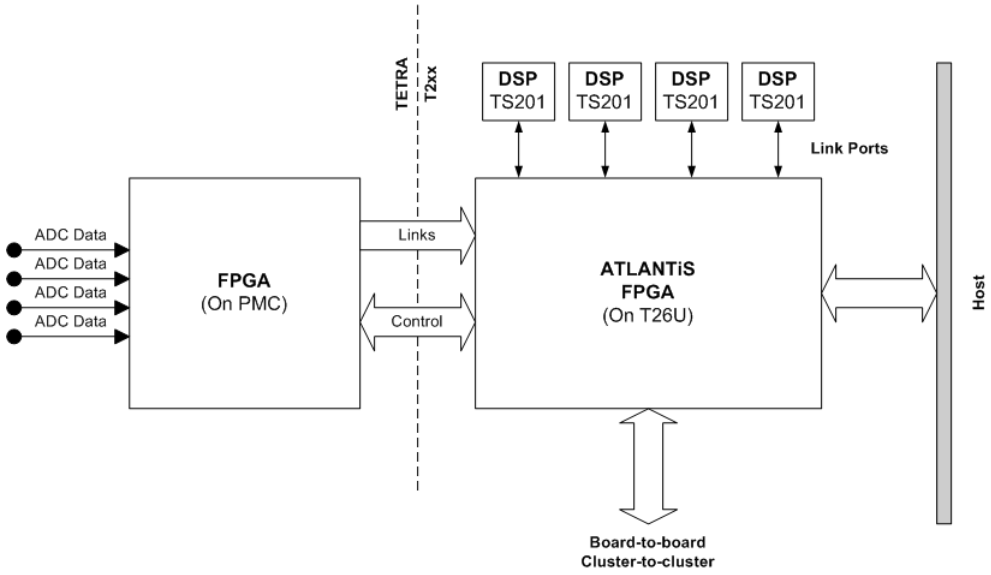
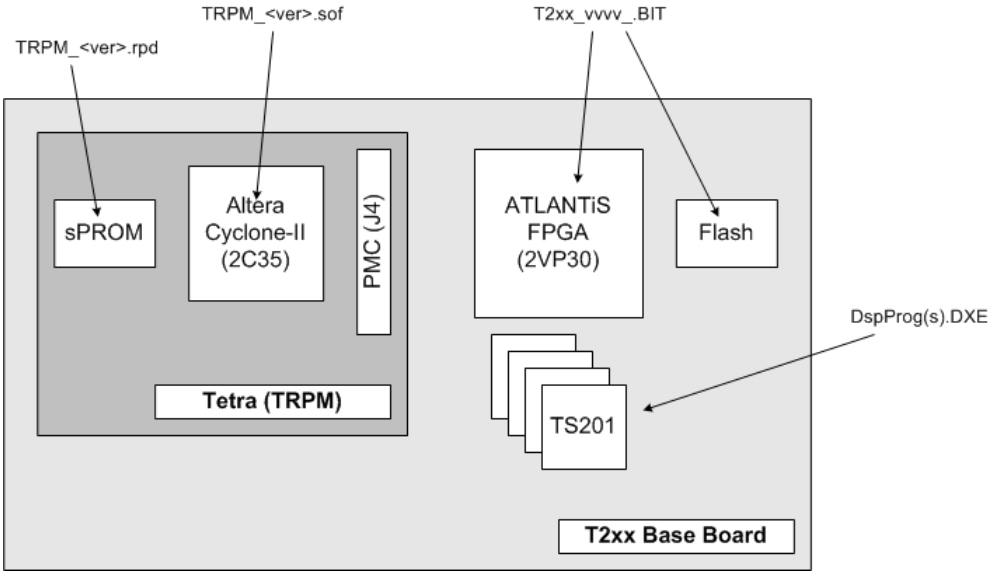


Figure 4-4 on page 61 identifies all the programmable components in a Tetra board system (in this example, the Tetra-PMC+ installed on a BittWare T26U board).

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Figure 4-2 Programmable Components in a Tetra–T2 Setup



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4.2 External Interfaces

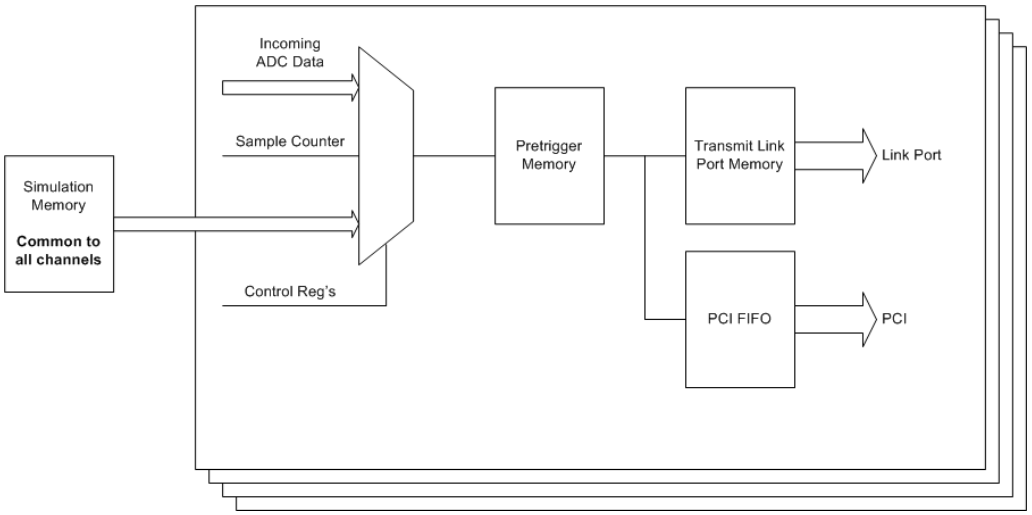
4.2.1 ADC Inputs

Analog signals are input through connectors J3, J4, J7, and J8. From there, they are routed to analog-to-digital converters (ADCs). As input sources dictate, the voltage range can be factory configured to either of the following:

- **Bi-polar mode**: input signal is 2V peak to peak, ±1V
- **Uni-polar mode**: input signal is 2V peak to peak, 0V to 2V

Figure 4-3 illustrates the signal path of the analog data on the Tetra.

Figure 4-3 Signal Path of ADC Data on Tetra



4.2.2 Trigger In/ Clock Out

Connector J6 is an input for an external trigger signal to the board. It can also be configured as a clock output. Registers in the Cyclone II configure the operation of the trigger. Section 2.3.6 describes the connector. “Trigger Control Registers (0x106, 0x206, 0x306, 0x406)” on page 80 describes the trigger registers.

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4.2.3 Exernal Clock Input

Connector J5 allows you to supply an external clock signal to the TRPM. Section 2.3.5 provides the connector detail.

4.2.4 PCI Signals

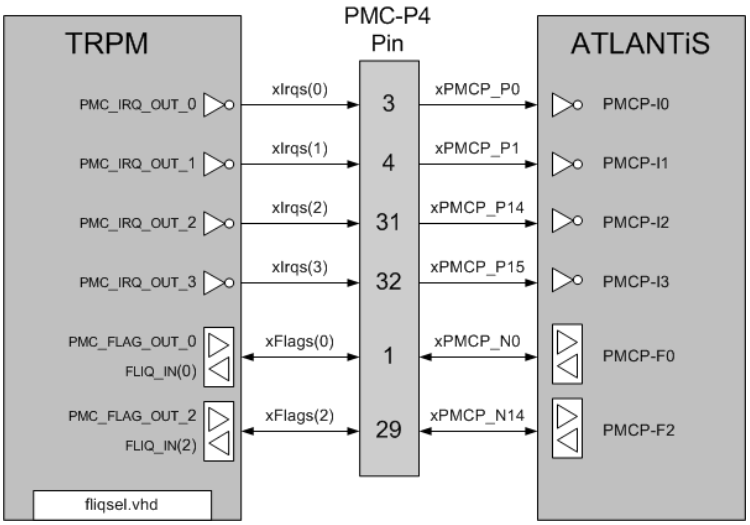
The PCI interface is 32-bits, 3.3V signaling only. It supports both 33 MHz and 66 MHz operation.

4.2.5 PMC+ Pin Usage

As described in section 2.3.7 on page 33 and shown in Table 2-7 on page 37, the Tetra's PMC+ pins (PMC-P4) provide the communication link to the host board. Table 4-1 on page 62 shows the signal assignment for the PMC connector to the host board, which is populated with 6a Virtex-II Pro® FPGA. It includes the following signals:

- Four link ports that are defined at build and/or compile time to be Rx/Tx depending on hardware and/or FPGA
- Two flag pins
- Four interrupt pins
- Five general purpose pins (GPIO)
- One differential clock, from PMC to carrier
- One reset from carrier to PMC

Figure 4-4 Flag and Interrupt Configuration



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Table 4-1 Tetra PMC+ Pinout to FPGA on Host T2 Board

PMC Pin	Tetra Name	Tetra Direction	Signal	V2Pro Name	Usage
1	Flag0	I/O	3.3V SE	XPMCP_N0	
3	Irq0	Out	3.3V SE	XPMCP_P0	
5	L0D0_N	Out	LVDS	XPMCP_N2	Used as TX (reverse all for RX)
7	L0D0_P	Out	LVDS	XPMCP_P2	
9	L0D1_N	Out	LVDS	XPMCP_N4	Links can be either direction as defined by the FPGAs on both the Tetra and the Host.
11	L0D1_P	Out	LVDS	XPMCP_P4	
13	L0D2_N	Out	LVDS	XPMCP_N6	
15	L0D2_P	Out	LVDS	XPMCP_P6	
17	L0D3_N	Out	LVDS	XPMCP_N8	
19	L0D3_P	Out	LVDS	XPMCP_P8	
21	L0VALID_N	Out	LVDS	XPMCP_N10	Data valid (can also be used as gated Lclk for true TS201 links)
23	L0VALID_P	Out	LVDS	XPMCP_P10	
25	L0_ACK	In	3.3V SE	XPMCP_N12	
27	L0_BCMP	Out	3.3V SE	XPMCP_P12	
29	Flag2	I/O	3.3V SE	XPMCP_N14	
31	Irq2	Out	3.3V SE	XPMCP_P14	
33	L2D0_N	Out	LVDS	XPMCP_N16	
35	L2D0_P	Out	LVDS	XPMCP_P16	
37	L2D1_N	Out	LVDS	XPMCP_N18	
39	L2D1_P	Out	LVDS	XPMCP_P18	
41	L2D2_N	Out	LVDS	XPMCP_N20	
43	L2D2_P	Out	LVDS	XPMCP_P20	
45	L2D3_N	Out	LVDS	XPMCP_N22	
47	L2D3_P	Out	LVDS	XPMCP_P22	
49	L2VALID_N	Out	LVDS	XPMCP_N24	
51	L2VALID_P	Out	LVDS	XPMCP_P24	
53	L2_ACK	In	3.3V SE	XPMCP_N26	
55	L2_BCMP	Out	3.3V SE	XPMCP_P26	
57	PROG00_FPGA_ASDO	I/O	3.3V SE	XPMCP_N28	General purpose pins
59	PROG01_FPGA_DCLK	I/O	3.3V SE	XPMCP_P28	programming, or reg's via
61	PROG02_FPGA_CSO	I/O	3.3V SE	XPMCP_N30	I2S, I2C, etc.
63	PROG03_FPGA_DATAO	I/O	3.3V SE	XPMCP_P30	

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Table 4-1 Tetra PMC+ Pinout to FPGA on Host T2 Board (Continued)

PMC Pin	Tetra Name	Tetra Direction	Signal	V2Pro Name	Usage
2	FLAG1_FPGA_CE	I/O	3.3V SE	XPMCP_N1	GP5 – Do not use*
4	Irq1	Out	3.3V SE	XPMCP_P1	
6	L1D0_N	Out	LVDS	XPMCP_N3	
8	L1D0_P	Out	LVDS	XPMCP_P3	
10	L1D1_N	Out	LVDS	XPMCP_N5	
12	L1D1_P	Out	LVDS	XPMCP_P5	
14	L1D2_N	Out	LVDS	XPMCP_N7	
16	L1D2_P	Out	LVDS	XPMCP_P7	
18	L1D3_N	Out	LVDS	XPMCP_N9	
20	L1D3_P	Out	LVDS	XPMCP_P9	
22	L1VALID_N	Out	LVDS	XPMCP_N11	
24	L1VALID_P	Out	LVDS	XPMCP_P11	
26	L1_ACK	In	3.3V SE	XPMCP_N13	
28	L1_BCMP	Out	3.3V SE	XPMCP_P13	
30	FLAG3_FPGA_CONF_DONE	I/O	3.3V SE	XPMCP_N15	GP6 – Do not use*
32	Irq3	Out	3.3V SE	XPMCP_P15	
34	L3D0_N	Out	LVDS	XPMCP_N17	
36	L3D0_P	Out	LVDS	XPMCP_P17	
38	L3D1_N	Out	LVDS	XPMCP_N19	
40	L3D1_P	Out	LVDS	XPMCP_P19	
42	L3D2_N	Out	LVDS	XPMCP_N21	
44	L3D2_P	Out	LVDS	XPMCP_P21	
46	L3D3_N	Out	LVDS	XPMCP_N23	
48	L3D3_P	Out	LVDS	XPMCP_P23	
50	L3VALID_N	Out	LVDS	XPMCP_N25	
52	L3VALID_P	Out	LVDS	XPMCP_P25	
54	L3_ACK	In	3.3V SE	XPMCP_N27	
56	L3_BCMP	Out	3.3V SE	XPMCP_P27	
58	RST*	In	3.3V SE	XPMCP_N29	
60	PROG04_FPGA_CONFIG	N/A	3.3V SE	XPMCP_P29	
62	LCLK_N	Out	LVDS	XPMCP_N31	Link clock (-) continuous
64	LCLK_P	Out	LVDS	XPMCP_P31	Link clock (+) continuous

* Unused pins should be driven or tied to GND.

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4.2.6 Link Port Interface

ADC samples are measured in data words.

Table 4-2 ADC 2's Complement (-1V to +1V)

ADC Sample, 2's Complement	
15:2 ADC Sample (14 bits)	1:0 Programmable*

* Options for over-range and trigger bits are described in the ADC Control Register.

Voltage	ADC Data
-1V	0x8000
0V	0x0000
+1V	0x7FFC

Link Word							
127:112	111:96	95:80	79:64	63:48	47:32	31:16	15:0
ADC(7)	ADC(6)	ADC(5)	ADC(4)	ADC(3)	ADC(2)	ADC(1)	ADC(0)

32-bit Word Offset	Bits	Description
0	31:00	ADC(1) : ADC(0)
1	63:32	ADC(3) : ADC(2)
2	95:64	ADC(5) : ADC(4)
3	127:96	ADC(7) : ADC(6)

Table 4-3 Offset Binary (0V to +2V)

ADC Sample, 2's Complement	
15:2 "0" + ADC Sample (13 bits)	1:0 ADC-D0 Programmable*

* Options for over-range and trigger bits are described in the ADC Control Register.

Voltage	ADC Data
0V	0x0000
+1V	0x4000
+2V	0x7FFC

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4.3 Memory Map

The Cyclone II FPGA is programmable and reconfigurable. This section gives an overview of the memory map and control registers as they are implemented on the Tetra's FPGA.

Table 4-4 Memory Map

Description	Size	Offset (32-bit addresses)*
Registers	32-bits (even addr only)	0x00000 - 0x004FF
Simulation Memory A	1k x 18-bits (even addr only)	0x3000 - 0x37FE

Table 4-5 Simulation Memory Format

Bit	Description	Function
17	Restart	1=Repeats pattern from beginning, if enabled*
16	Stop	1=Holds data until external restart, if enabled*
15:00	Substitute ADC data	

* See simulation control register

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4.4 Register Descriptions

Table 4-6 gives an overview of the general and ADC registers map. The sections that follow describe these registers in more detail.

Table 4-6 Register Map Overview

Description	Base Offset	Max # Reg's*	Refer to:
Board version, status and control	0x000	64	section 4.4.1
General acquisition (applies to all channels)	0x080	64	section 4.4.2
Channel A	0x100	128	
Read/write registers	0x100-0x17E	64	
Read Only status (and read/clear)	0x180-0x1BE	32	
Write Only	0x1C0-0x1FE	32	section 4.4.3
Channel B	0x200	128	
Channel C	0x300	128	
Channel D	0x400	128	

* Only even addresses can be used.

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4.4.1 Board, Version, Status, Control

Figure 4-7 shows size, address, and characteristics of the board, version, status, and control registers. The sections that follow describe the individual registers in more detail.

Table 4-7 Board, Version, Status, and Control Registers

Description	Bits	Offset*	ResetValue	Access†
General-purpose register	32	0x000	0x1234:5678	R/W
Version Info	32	0x002	version	RO
Board Info	32	0x004	board-info	RO
Board Control (inc. LED)	16	0x006	0x0000:0000	R/W
Board Status (inc. switch)	32	0x008	0x0000:0000	RO
Global Flag	1	0x010	0x0000:0000	R/W
Global IRQ	1	0x018	0x0000:0000	R/W
Flag-0 Control	8	0x020	0x0000:0000	R/W
Flag-1 Control	8	0x022	0x0000:0000	N/A
Flag-2 Control	8	0x024	0x0000:0000	R/W
Flag-3 Control	8	0x026	0x0000:0000	N/A
Irq-0 Control	8	0x030	0x0000:0000	R/W
Irq-1 Control	8	0x032	0x0000:0000	R/W
Irq-2 Control	8	0x034	0x0000:0000	R/W
Irq-3 Control	8	0x036	0x0000:0000	R/W

* Diag21k: Diag21k>mr s 0 20 (read 1st 20 reg's)
† RW = Read/Write; RO = Read Only; RC = Read/Clear; WO = Write Only

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General Purpose Register (0x00)

Read/write register, not used for anything internally.

Version Info Register (0x02)

The Version Info is a 32-bit, read only register that is hard-coded into the FPGA when built. This register gives you the version of the FPGA load on the TRPM.

Table 4-8 Contents of Version Info Register (0x02)

D31:D24	D23:D16	D15:D8	D7:D0
Load number	Major Version	Minor Version	Build Number

Board Info (0x04)

The Board Info register is 32-bit, read only and is hardcoded onto the FPGA when built.

Table 4-9 Contents of Board Info Register (0x04)

D31:D24	D23:D16	D15:D8	D7:D0
0x00	0x00	Board Number	Variant (0x00)

Board Control Register (0x06)

The Board Control register includes LED select, reserved, and PMC enable bits. The LED selects are set within the LED Select as shown in Table 4-10.

Table 4-10 Contents of Board Control Register (0x06)

Bit	Description	Function
15:12	LED-3 Select	See LED Select Table*
11:8	LED-2 Select	See LED Select Table
7:4	LED-1 Select	See LED Select Table
3:1	Reserved (write 0)	
0	PMC Enable	0 = Tristate PMC Signals 1 = Enable PMC Signals

* LED Select Table is Table 4-11 on page 69.

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This table shows the different possible LED signals. “1” is ON.

Table 4-11 LED Select Options

LedSelect(3:0)	Signal
0	ON
1	OFF
2	Global Flag
3	Global IRQ
4	ADCLocked
5	PMC Flag 0
6	PMC Flag 2
7	Combined Error
8	ADC-A Error
9	ADC-B Error
10	ADC-C Error
11	ADC-D Error
12	ADC-A Armed
13	ADC-B Armed
14	ADC-C Armed
15	ADC-D Armed

Board Status Register (0x08)

The Board Status is a 32-bit, read only register that gives the status of the user switch.

Table 4-12 Contents of Board Status Register (0x08)

Bit	Description	1	0
15:12	User Switches	Open	Closed
11:4	Reserved, will read 0		
3			
2		Locked	Not Locked
1	Link PLL Status	Locked	Not Locked
0	ADC PLL Status	Locked	Not Locked

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PMC Flag Control Register Format

Table 4-13 shows the format of the 8-bit, R/W PMC Flag Control register. The Source Select bits (3:0) are described in the PMC Flag Select Options Table 4-14.

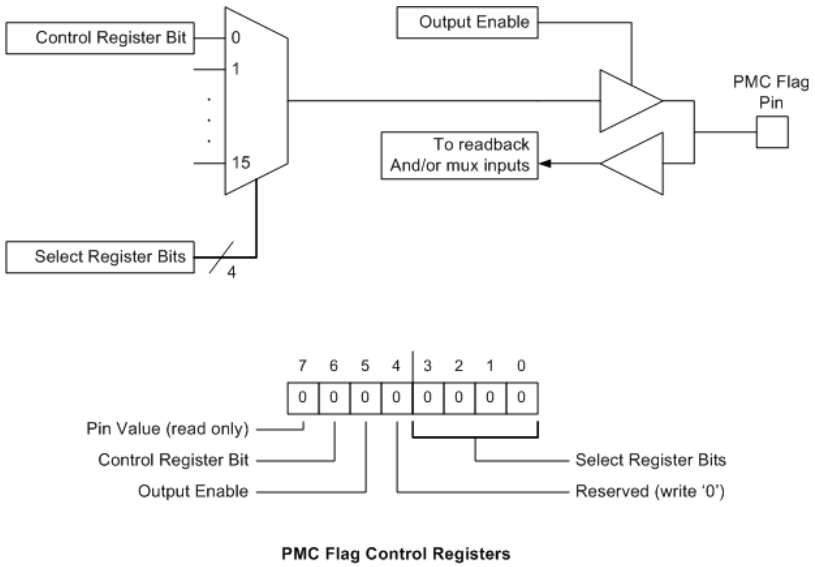
Table 4-13 PMC Flag Control Register Format

Bit	Description
7	Status of pin (read only)
6	Register value (output when select=0 and output enable=1)
5	Output enable (1=TRPM drives pin)
4	Reserved (write '0')
3:0	Source Select (see select tables)

PMC Flag Control

Figure 4-5 below illustrates the PMC Flag Control registers.

Figure 4-5 PMC Flag Control Registers



PMC Flag Control Registers

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Table 4-14 shows the PMC Flag Select options for Flag-0 Control and Flag-2 Control Source Select bits (3:0). (Flag-1 and Flag-3 are not accessible on the Tetra.)

Table 4-14 PMC Flag Select Options

Select Reg	PMC Flag-0	PMC Flag-1	PMC Flag-2	PMC Flag-3
0	Register Bit	Register Bit	Register Bit	Register Bit
1	Global Flag	Global Flag	Global Flag	Global Flag
2	Global IRQ	Global IRQ	Global IRQ	Global IRQ
3	External Trigger	External Trigger	External Trigger	External Trigger
4	Timer-1	Timer-1	Timer-1	Timer-1
5	Timer-2	Timer-2	Timer-2	Timer-2
6	Error/Overrange*	Error/Overrange*	Error/Overrange*	Error/Overrange*
7	RSVD	RSVD	RSVD	RSVD
8	Samps Done A	Samps Done A	Samps Done A	Samps Done A
9	Samps Done B	Samps Done B	Samps Done B	Samps Done B
10	Samps Done C	Samps Done C	Samps Done C	Samps Done C
11	Samps Done D	Samps Done D	Samps Done D	Samps Done D
12	Trigger Event A	Trigger Event A	Trigger Event A	Trigger Event A
13	Trigger Event B	Trigger Event B	Trigger Event B	Trigger Event B
14	Trigger Event C	Trigger Event C	Trigger Event C	Trigger Event C
15	Trigger Event D	Trigger Event D	Trigger Event D	Trigger Event D

* Combination all channels error/over-range indicator (need to read status to determine source).

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PMC Interrupt Control Register Format

Table 4-15 shows the format of the 8-bit, R/W PMC Interrupt Control register. The Source Select bits (3:0) are described in the PMC Interrupt Select Options Table 4-16.

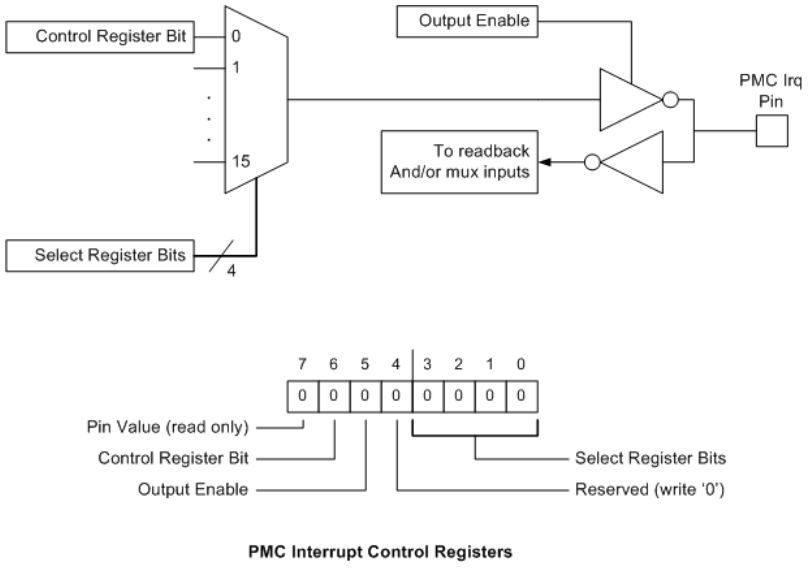
Table 4-15 PMC Interrupt Control Register Format

Bit	Description
7	Status of pin (read only)
6	Register value (output when select=0 and output enable=1)
5	Output enable (1=TRPM drives pin)
4	Reserved (write '0')
3:0	Source Select (see select tables)

PMC Interrupt Control

Figure 4-6 below illustrates the PMC Interrupt Control registers.

Figure 4-6 PMC Interrupt Control Registers



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Table 4-16 shows the PMC Interrupt Select options for IRQ-0–IRQ-3 Control Source Select bits (3:0).

Table 4-16 PMC Interrupt Select Options

Select Reg	PMC IRQ-0	PMC IRQ-1	PMC IRQ-2	PMC IRQ-3
0	Register Bit	Register Bit	Register Bit	Register Bit
1	Global Flag	Global Flag	Global Flag	Global Flag
2	Global Irq	Global Irq	Global Irq	Global Irq
3	External Trigger	External Trigger	External Trigger	External Trigger
4	Timer-1	Timer-1	Timer-1	Timer-1
5	Timer-2	Timer-2	Timer-2	Timer-2
6	Error/Overrange*	Error/Overrange*	Error/Overrange*	Error/Overrange*
7	RSVD	RSVD	RSVD	RSVD
8	Samps Done A	Samps Done A	Samps Done A	Samps Done A
9	Samps Done B	Samps Done B	Samps Done B	Samps Done B
10	Samps Done C	Samps Done C	Samps Done C	Samps Done C
11	Samps Done D	Samps Done D	Samps Done D	Samps Done D
12	Trigger Event A	Trigger Event A	Trigger Event A	Trigger Event A
13	Trigger Event B	Trigger Event B	Trigger Event B	Trigger Event B
14	Trigger Event C	Trigger Event C	Trigger Event C	Trigger Event C
15	Trigger Event D	Trigger Event D	Trigger Event D	Trigger Event D

* Combination of all channels error/over-range indicator (need to read status to determine source).

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4.4.2 General Acquisition

The registers described in this table apply to all channels of ADC. The general acquisition registers described in Table 4-17 are detailed in the following sections.

Table 4-17 General Acquisition, applies to all channels

Description	Bits	Offset*	ResetValue	Access†
Global ADC Clock/Control	16	0x080	0x0000:0000	R/W
Internal Trigger Period A	24	0x082	0x0000:0106	R/W
Internal Trigger Period B	24	0x084	0x00:2904	R/W
Simulation Control	16	0x086	0x0000:0000	R/W
Soft Reset	1	0x090	0x0000:0000	WO

* These registers are mapped into Bar-0, offset 0.
Diag21k: Diag21k>mrr1 0 0 20 (read first 20 registers).
† RW = Read/Write; RO = Read Only; RC = Read/Clear; WO = Write Only

Global ADC Clock/Control Register (0x80)

The Global ADC Clock/Control register is a 16-bit R/W register located at offset 0x080. It resets the PLL, sets the source for the ADC clock, enables the ADCs, and flushes the ADCs..

Table 4-18 Contents of Global ADC Clock/Control Register (0x80)

Bit	Description	1	0
15:8	Reserved, will read 0		
7:4			
3	Force ADC PLL Reset (self-clearing)	Reset PLL	Run
2	ADC Clock Select	External	Internal
1	Global ADC Enable	Run	Reset
0	Global ADC Flush & Link Port Reset	Flush	Run

Internal Trigger Period A, B (0x82, 0x84)

The Internal Trigger Period A and B registers are 24-bit, R/W registers that set the period of the internal trigger timer with the clock base of AdcClk

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(on-board = 105 MHz). An example is using the on board clock to create a 10 kHz timer, set to 0x2904 (105 MHz / 10 kHz).

Simulation Control Register (0x86)

The Simulation Control is a 16-bit, R/W register that enables data capture in simulated data mode. The External Restart selection bits (3:0) must be set from values shown in Table 4-20 on page 76.

Table 4-19 Contents of Simulation Control Register (0x86)

Bit	Description	1	0
6	Simulation Memory Data Restart	Restart when D17=1	Ignore D17
5	Sim Address Counter Enable*	Stop when D16=1	Ignore D16
4	External Restart Enable*	Enable	Disable
3:0	External Restart selection options (see Restart Signal Options table)		

* Stops until next restart event occurs.

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The following table shows the different possible restart signals. If enabled, this condition will reset the simulation memory to location 0.

Table 4-20 Simulation Memory External Restart Select Signal Options

Trig(3:0)	Trigger Signal*
0	OFF
1	Global Flag
2	Global Irq
3	External
4	Timer-1
5	Timer-2
6	PmcFlag-0
7	PmcFlag-2
8	ADC-A "Go"
9	ADC-B "Go"
10	ADC-C "Go"
11	ADC-D "Go"
12	Samps Done A
13	Samps Done B
14	Samps Done C
15	Samps Done D

* As defined elsewhere in Trigger Control register to be rising/falling edge/level.

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4.4.3 ADC Registers

Table 4-21 lists the ADC registers, and the sections that follow describe them further.

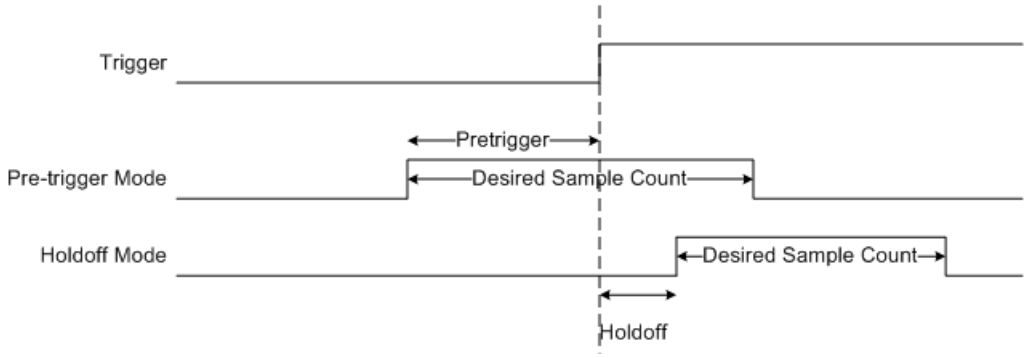
Table 4-21 ADC Registers

Description	Bits	Offset*				ResetValue	Access†
		Ch A	Ch B	Ch C	Ch D		
ADC General Control A	24	0x100	0x200	0x300	0x400	0x0000:0000	R/W
ADC Transfer (link) Control A	4	0x102	0x202	0x302	0x402	0x0000:0000	R/W
ADC A Arm/Go	1	0x104	0x204	0x304	0x404	0x0000:0000	R/W
ADC Trigger Control	16	0x106	0x206	0x306	0x406	0x0000:0001	R/W
ADC Decimation Control	16	0x108	0x208	0x308	0x408	0x0000:0000	R/W
ADC Desired Sample Count A	32	0x110	0x210	0x310	0x410	0x0000:0000	R/W
ADC Pre-trigger A	16	0x112	0x212	0x312	0x412	0x0000:0000	R/W
ADC Holdoff A	16	0x114	0x214	0x314	0x414	0x0000:0000	R/W
ADC Threshold A	16	0x116	0x216	0x316	0x416	0x0000:0000	R/W
ADC Status A	32	0x180	0x280	0x380	0x480	0x0000:0000	RO
ADC Current Block Count A	24	0x182	0x282	0x382	0x482	0x0000:0000	RC
ADC Current Sample Count A	24	0x184	0x284	0x384	0x484	0x0000:0000	RO
ADC Total Sample Count A	24	0x186	0x286	0x386	0x486	0x0000:0000	RC
PCI Data FIFO, ADC-A	32	0x1B0	0x2B0	0x3B0	0x4B0	0x0000:0000	RO
PCI Data FIFO, ADC-B	32	0x1B2	0x2B2	0x3B2	0x4B2	0x0000:0000	RO
PCI Data FIFO, ADC-C	32	0x1B4	0x2B4	0x3B4	0x4B4	0x0000:0000	RO
PCI Data FIFO, ADC-D	32	0x1B6	0x2B6	0x3B6	0x4B6	0x0000:0000	RO
ADC Clear Overrange A	1	0x1C0	0x2C0	0x3C0	0x4C0	N/A	WO
ADC Clear FIFO Overflow A	1	0x1C2	0x2C2	0x3C2	0x4C2	N/A	WO

* Diag21k: Diag21k>mr s 0 20 (read first 20 registers).
† RW = Read/Write; RO = Read Only; RC = Read/Clear; WO = Write Only

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Figure 4-7 ADC Acquisition Setup



ADC Control Registers (Ch A: 0x100, Ch B: 0x200, Ch C: 0x300, Ch D: 0x400)

Table 4-22 on page 79 shows the 24-bit ADC control register, which is the same for all four channels of ADC. This register sets the data acquisition rates as illustrated in Figure 4-7 above, sets the data format, enables simulated data, acquisition mode, and enables the ADCs. See Table 4-22 for bit settings for the ADC Control register.

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Table 4-22 Contents of ADC Control Registers (0x100, 0x200, 0x300, 0x400)

Bit	Description		Function
	Reserved (write 0)		
15:14	D1 substitution (should only be used if data left-justified)		00 : D1=AdcDataIn(1) 01 : Selected Trigger on D1 10 : Over-range on D1 11 : Reserved
13:12	D0 substitution		00 : D0=0 01 : Selected Trigger on D0 10 : Over-range on D0 11 : Reserved
11:10	Simulated data (replaces ADC data) Also see "Simulated Data" (Reg x16)		00 : Live Data 01 : Data replaced by sample counter10 : Data replaced by simulation memory11 : Reserved
9:8	Acquisition Mode Continuous = once triggered, acquire until disabled. Snapshot = acquire desired count and then disarm. Auto snapshot = snapshot with automatic re-arm.		00 : Continuous sampling 01 : Snapshot sampling 10 : Auto snapshot
3	ADC Data Format	2's Comp	Offset Binary
2	Flush		1 = Flush (self-clearing)
1			
0	ADC Enable	Enable	Reset

Transfer Link Control Registers (0x102, 0x202, 0x302, 0x402)

The Transfer (Link) Control register is a 4-bit R/W setting that configures the link/PCI interface.

Arm/Go Registers (0x104, 0x204, 0x304, 0x404)

Arm/Go is a 1-bit R/W register that signals the start and stop of a data acquisition in both continuous and snapshot modes.

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Trigger Control Registers (0x106, 0x206, 0x306, 0x406)

Trigger Control is a 16-bit R/W register that selects the trigger mode, direction, and source for the ADCs. The Trigger Source bits (3:0) must be set from values shown in Table 4-24 on page 81.

Table 4-23 Contents of Trigger Control Registers (0x106, 0x206, 0x306, 0x406)

Bit	Description	Reset	Function
15:10	Reserved (write 0)		
9	Trigger Mode		0 = Edge triggered 1 = Level sensitive
8	Trigger Direction		0 = Rising edge or High level 1 = Falling edge or Low level
7:4	Reserved (write 0)		
3:0	Trigger Source		Trigger select, see Trigger Select Options table

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The following table shows the different possible trigger signals for Trigger Source (3:0). Trigger Mode and Direction apply to all signals except for the Timers since they are only active for a single cycle.

Table 4-24 Trigger Select Options

Trig(3:0)	Trigger Signal
0	RSVD
1	Global Flag
2	Global Irq
3	External
4	Timer-1
5	Timer-2
6	PmcFlag-0
7	PmcFlag-2
8	ADC-A "Go"*
9	ADC-B "Go"
10	ADC-C "Go"
11	ADC-D "Go"
12	ADC-A Trigger Event†
13	ADC-B Trigger Event
14	ADC-C Trigger Event
15	ADC-D Trigger Event

* When using the “Go” bit, also set the TriggerMode to Level.

† As defined elsewhere in this Trigger Control register to be rising/falling/edge/level.

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Decimation Control Registers (0x108, 0x208, 0x308, 0x408)

Decimation Control is a 16-bit R/W register that enables and configures the decimation parameters.

Table 4-25 Contents of Decimation Control Registers (0x108, 0x208, 0x308, 0x408)

Bit	Description	Reset	Function
15	Decimator Enable		1 = Enable Decimation
14:0	Decimation value		Number of samples to "skip" minus 1 E.g., to keep every 4th sample, value = 2

Desired Sample Count Registers (0x110, 0x210, 0x310, 0x410)

This 32-bit R/W register sets the number of desired samples. To get 10 samples, set the register to 9.

Table 4-26 Contents of Desired Sample Count Registers (0x110, 0x210, 0x310, 0x410)

Bit	Description	Setting
31:0	Number of desired samples	Number of samples less 1 E.g., for 10 samples, value = 9

Pre-Trigger Registers (0x112, 0x212, 0x312, 0x412)

The Pre-Trigger register is 16-bit R/W that sets the number of prefetch samples. The Pre-Trigger must not be set to 0.

Table 4-27 Contents of Pre-Trigger Registers (0x112, 0x212, 0x312, 0x412)

Bit	Description	Setting
15:0	Number of Prefetch samples	Number of prefetch samples less 1* E.g., for 16 samples, value = 15

* This is hardware-limited to the max FIFO size

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Holdoff Registers (0x114, 0x214, 0x314, 0x414)

The 16-bit, R/W Holdoff register sets the number of holdoff samples.

Table 4-28 Contents of Holdoff Registers (0x114, 0x214, 0x314, 0x414)

Bit	Description	Setting
15:0	Number of Holdoff samples	Number of Holdoff samples less 1

ADC Threshold Registers (0x116, 0x216, 0x316, 0x416)

The 16-bit read/write Threshold register sets the start for the trigger.

Table 4-29 Contents of ADC Threshold Registers (0x116, 0x216, 0x316, 0x416)

Bit	Description	Setting
15:0	Start Threshold for trigger	2's complement for threshold trigger

ADC Status Registers (0x180, 0x280, 0x380, 0x480)

ADC Status is a 32-bit read only register that gives the status of the ADC overrange, the prefetch ready, and the FIFOs.

Table 4-30 Contents of ADC Status Registers (0x180, 0x280, 0x380, 0x480)

Bit	Description	1	0
31	PCI FIFO Full Status	Full	Not Full
30	PCI FIFO Empty Status	Empty	Not Empty
29:26	Reserved (will read '0')		
25:16	FIFO Read Count (number of words in FIFO)		
15:8	Reserved (will read '0')		
7	Input > greater than threshold	Greater	Less than or Equal
6	ADC Overrange (sticky bit)	Over	OK
5	Prefetch ready	Ready	Not Ready
4	Armed	Armed	Not Armed
3			
2	Data Link FIFO Overflow	Overflow	OK
1	PreFetch FIFO Overflow	Overflow	OK
0	Combined FIFO Overflow (interrupt signal)	Overflow	OK

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Current Block Count (0x182, 0x282, 0x382, 0x482)

The block counter increments after each desired sample count is reached. It is a 24-bit register that is read and clear.

Current Sample Count (0x184, 0x284, 0x384, 0x484)

The sample counter resets after each desired sample count is reached. The counts are sent for transfer as samples. It is a 24-bit read only register.

Total Sample Count (0x186, 0x286, 0x386, 0x486)

The total sample counter is a free-running sample counter. It is a 24-bit read and clear register.

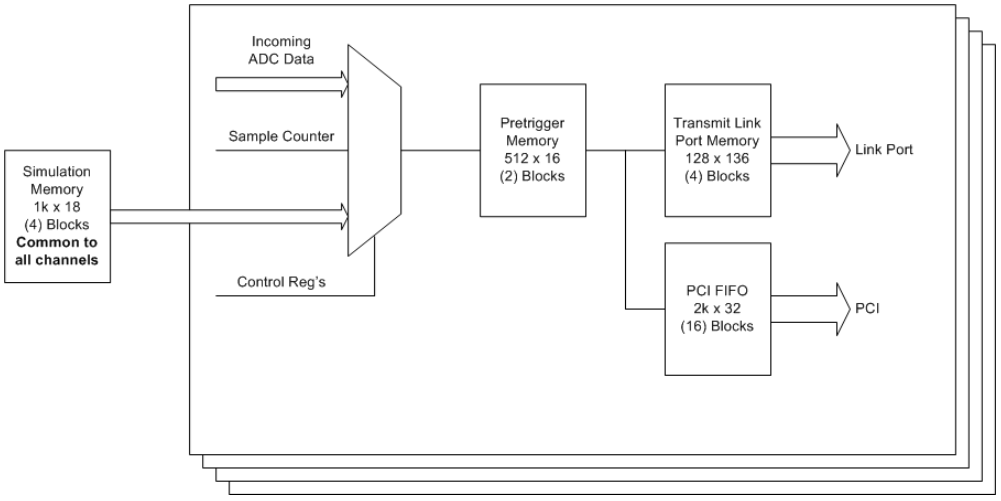
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4.5 FPGA Block Memory Usage

The simulation memory is common for all the channels, and the rest of the blocks are for each channel. There are 105 memory blocks in the FPGA. Block usage is shown in Figure 4-8 below.

60 blocks = (1) * 4 blocks + (4) * 14 blocks

Figure 4-8 FPGA Block Memory Usage



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Chapter 5
Configuring the Cyclone II FPGA

This chapter describes the steps involved in configuring the Cyclone II FPGA. It does not provide instructions on how to create the FGPA program; rather, it describes how to load the program onto it. To make the best use of the instructions in this chapter, you will need to be familiar with the FPGA development tools from Altera, including the Altera Quartus II software and the Altera USB Blaster. You will also need to refer to the *Cyclone II Platform FGPA Handbook*. Figure 5-1 illustrates the file configuration methods, and the sections that follow describe each method in detail.

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5.1 Using BitLoader to Configure the Cyclone II

This section describes how to configure the Cyclone II FPGA by loading an .rpd file to the TRPM via the host board.

Note *The host board must have its FPGA configured so that it can load an .rpd file into the TRPM.*

You will need the information in this chapter when performing field upgrades of the Cyclone II.

5.1.1 Getting Ready to Load from the Host

Before you load files to the FPGA, complete the following steps:

1. Leave the configuration switches in their default setting, which is to load the FPGA via SPROM. (See section 2.3.1 on page 28 for the switch settings.)
2. Install the BitLoader utility.
   To install the BitLoader utility, follow the instructions given in section 2.5.1 on page 42.
3. Create the FPGA logic.
   To write the FPGA logic, use the Altera Quartus II tools to create a .rpd file. Refer to the Quartus II user's manual for details on creating this type of file.

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5.1.2 Loading the Cyclone II from the Host with BitLoader

This section describes the steps for loading a .rpd file into the FPGA using the BittWare BitLoader. This utility loads the .rpd file directly from the host to the Cyclone II FPGA via the PCI bus.

To load the FPGA .rpd file with BitLoader:

1. Install and run the BitLoader utility as instructed in section 2.5.2 on page 45. The BitLoader main window will appear.
2. Select the host board that the TRPM resides on (T26U, T2PC, etc.)
3. From the "Action" drop down, select "Load .rpd file into PMC device FPGA PROM."
4. Select the .rpd file you would like to load to the Cyclone II.
5. Click on "Go."
6. Once the .rpd file has been loaded, you must cycle power on the TRPM. Selecting "Boot PMC device FPGA" will not work.

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5.2 Burning a Cyclone II Program

5.2.1 Burning the Cyclone II Program into the SPROM

To burn the Cyclone II program into the SPROM, use the USB Blaster cable. Connect the cable to the FPGA Programming header (J2) on the TRPM (see section 2.3.3 on page 30 for connector details).

5.2.2 Loading the Boot Program via JTAG

To load the Cyclone II program via JTAG, use the USB Blaster cable. Connect the cable to the FPGA Debug header (J1) on the TRPM (see section 2.3.2 on page 29 for connector details).

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Appendix A
ATLANTiS Primer

This appendix provides an overview of the ATLANTiS architecture as it may be implemented on your BittWare T2 host board. An example of the ATLANTiS test routine AdcPerf is included to demonstrate the configuration process. For specific programming information about your T2 board, refer to its user's guide as well as the BittWare ATLANTiS support documentation:

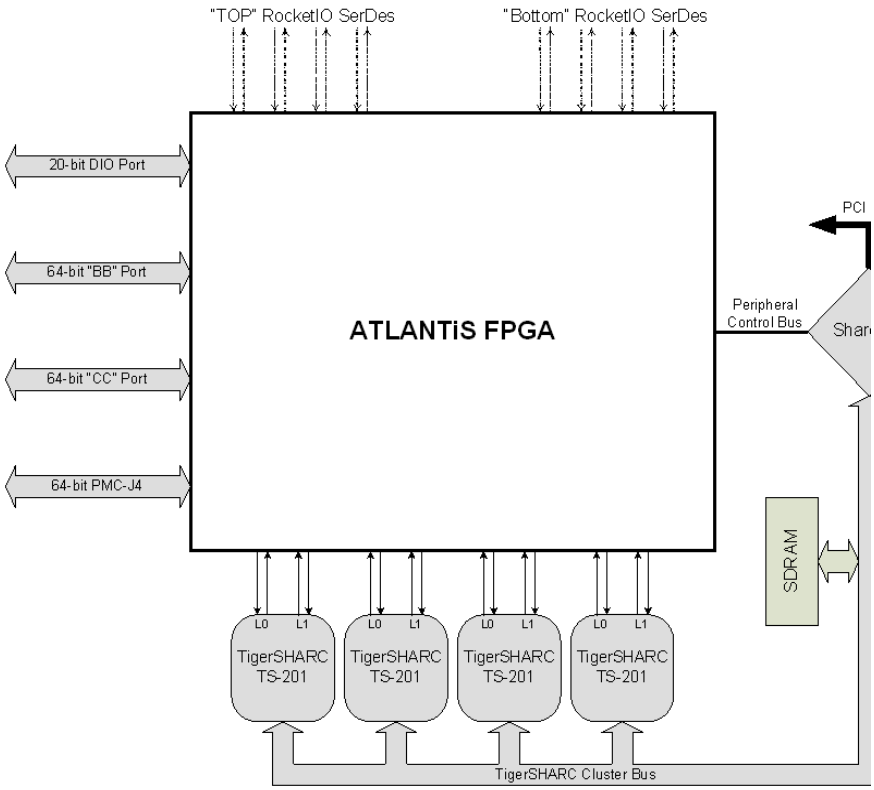
- *ATLANTiS Developer's Guide* – BittWare, Inc.
- *ATLANTiS User's Guide* – BittWare, Inc.
- *ATLANTiS Navigator Guide* – BittWare, Inc.

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A.1 Overview of the ATLANTiS Architecture

BittWare has established an architecture for the ADSP-TS201S family of boards called ATLANTiS. In simple terms, an FPGA is used to connect TS201 processors with each other and other I/O devices.

Figure A-1 ATLANTiS Architecture as Implemented on most T2 Family BittWare Boards



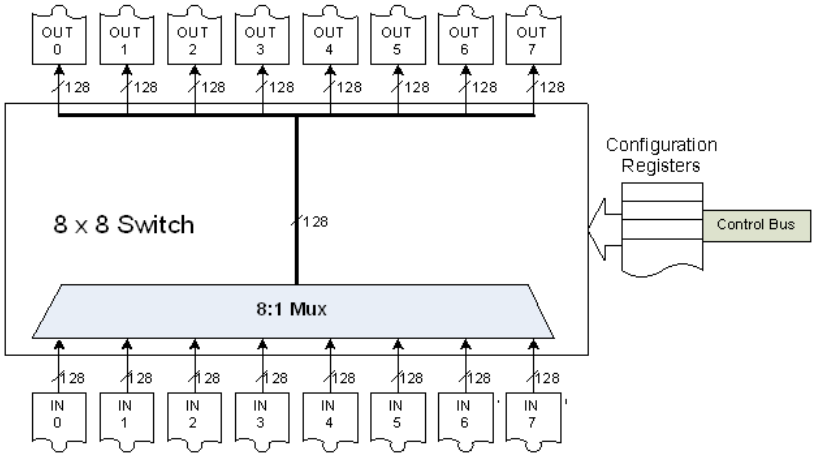
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A.1.1 The ATLANTiS Switch

The heart of ATLANTiS is an internal switch that allows any of its inputs, called *sources*, to be "connected" to one or more of its outputs, called *sinks*. The switch is configured at run time via time slicing. Figure A-2 shows the switch in an 8 x 8 configuration.

One simple and useful way to use ATLANTiS is as a software configurable cable network. By programming the switch, any of the inputs can be connected to any of the outputs and changed as requirements dictate, without recompiling the FPGA or changing any physical cables. The switch also permits any input to be connected to any number of outputs for data broadcast applications.

Figure A-2 ATLANTiS Switch Block Diagram



The ATLANTiS switch features:

- 125 MHz clock rate @ 128 bits (16 Bytes)
- Continuous 2 GByte/s throughput bandwidth
- Bandwidth can be allocated as required to any or all I/Os
- Each "slot" has equal bandwidth (i.e. with 32 slots, each is 62.5 MB/sec)
- Broadcast, multicast, and/or point-to-point
- Configuration registers can be changed "on the fly" (with additional requirements)
- Can support wider ports for sub-band or ECC data

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The ATLANTiS architecture supports the following port rates:

- TS201S link port receiver: 125 MByte/s (125 MHz, 4-bit DDR)
- TS201S link port transmitter: 250 MByte/s (250 MHz, 4-bit DDR)
- RocketIO™: 250 MByte/s payload peak, (2.5 GHz 8B/10B encoded)

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A.1.2 ADCPerf Example

AdcPerf is an example provided to demonstrate how to configure the ATLANTiS switch and access the FPGA registers. Diag21k scripts are included to run the example software on each processor in turn.

The DSP source files are located at the default address
`C:\dsp21ksf\atlantis\devkit\sw\atl_tst`

To run AdcPerf:

From a command window, execute the batch file for the appropriate board (must be device 0). (See Table A-1 below.) There are several user definable parameters for test modes, buffer sizes, etc.

Table A-1 AdcPerf Batch Files

Name(s)	Description
T2pc.bat Dfpc.bat D6pc_nr.bat	Batch file to launch Diag21k and run test on each processor
T2pc.cmd Dfpc.cmd D6pc_nr.cmd	Primary Diag21k script file
T2_sub.cmd Atl_sub.cmd	Script "subroutine" executed on each processor
Atlantis.c/h	Low-level functions to configure switch and manipulate FPGA registers
Atl_cfg.c	Example functions to configure switch for specific boards. Prototypes in atlantis.h.
Lnk_tst.c/h	Functions to send test patterns out a link port and verify data returned
Atl_tst.c/h/dxe	Main program

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A.1.3 ATLANTiS Configuration Memory Usage

You must set DPMx registers prior to issuing a corresponding DPM write command. Write addresses are on 32-bit boundaries (increment by 4 Pbus locations).

Table A-2 ATLANTIS Configuration Memory Map

Address	DPM1 (dest)	DPM0 (source)	Description
0x10000	0x01	0x00	Source-0 to Sink-0
0x10004	0x02	0x01	Source-1 to Sink-1
0x10008	0xC4	0x02	Source-2 to Sink-2, Sink-6, and Sink-7
0x1000C	0x08	0x03	Source-3 to Sink-3
0x10010	0x00	0x04	Source-4 to nothing (Note: it doesn't make sense to do this)
0x10014	0x20	0x05	Source-5 to Sink-5
0x10018	0x00	0x00	No operation
0x1001C	0x00	0x80	No operation and return

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A.2 FPGA Implementation and Related Tools

The ATLANTiS architecture resides on the host board's FPGA and is configured using a variety of tools. Listed here are the programming tools for the Altera Cyclone II FPGA (part number EP2C20F484).

Table A-3 FPGA Programming Tools

Tool	Description
Altera Quartus II	Design software for Cyclone II FPGA; supports VHDL, Verilog, schematic design, block editor, third-party netlist
Nios II Design Suite	Embedded processor design suite; includes software tools, utilities, libraries, and drivers
USB Blaster	Download cable; interfaces a USB port on a host computer to an Altera FPGA on a circuit board
Simulation	Aldec 6.2 sp1 PE. Aldec DO files are included for both functional and timing simulation. A testbench file (tb_xxx.vhd) is included to exercise a number of features including external I/O ports and the ATLANTiS switch(es).
BitLoader ("BitLdr")	BittWare utility for direct programming and flash load of the FPGA

The following file types are used in the design and programming of FPGA loads:

Table A-4 FPGA Load File Types

Extension	File Type
`.npl`	Altera project file
`.sch`	Schematic file (produces VHF)
`.vhf`	VHDL generated from schematic
`.vhd`	VHDL source file or testbench
`.dia`	StateCAD diagram (produces VHD)
`.sym`	Schematic symbol
`.ucf`	Altera constraints file
`<module>_translate.vhd`	Functional simulation file for pre-compiled modules
`.ngc`	Netlist file used for pre-compiled modules
`.rpd`	File used for programming device
`.do`	Macro to initialize simulator

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A.3 Example of T2 Board–TRPM ATLANTiS Interface

The following tables provide the expected signal usage between the Tetra-PMC+ and a T2-based BittWare host board. These values are for example purposes only; please check with BittWare Technical Support for the most current signalling.

Table A-5 ATLANTiS Switch-1 Sources and Sinks

Source Value	Sources (Into FPGA)	Sinks (From FPGA)	Sink Value
0	Tiger-0 Link-0	Tiger-0 Link-0	0x01
1	Tiger-1 Link-0	Tiger-1 Link-0	0x02
2	Tiger-2 Link-0	Tiger-2 Link-0	0x04
3	Tiger-3 Link-0	Tiger-3 Link-0	0x08
4	ADC-A		0x10
5	ADC-B		0x20
6	ADC-C		0x40
7	ADC-D		0x80

Table A-6 ATLANTiS Switch-2 Sources and Sinks

Source Value	Sources (Into FPGA)	Sinks (From FPGA)	Sink Value
0	Tiger-0 Link-1	Tiger-0 Link-1	0x01
1	Tiger-1 Link-1	Tiger-1 Link-1	0x02
2	Tiger-2 Link-1	Tiger-2 Link-1	0x04
3	Tiger-3 Link-1	Tiger-3 Link-1	0x08
4		BB-Link #0	0x10
5		BB-Link #1	0x20
6	CC-Link #0	CC-Link #0	0x40
7	CC-Link #1	CC-Link #1	0x80

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Table A-7 User LEDs

LED	Description	ON	OFF
VPA LED0	DCM Status	All Locked	At least one not locked
VPA LED1	TBD		

Table A-8 Digital I/O (DIO) Port Usage

Name	Usage
DIO	4 Flags, 4 IRQs
Brd2Brd	1 Tx Link, 4 Flags, 4 IRQs
Cluster	2 Rx Links, 2 Tx Links, 4 Flags, 4 IRQs
PMC	4 AdcLinks, 2 Flags, 4 IRQs, 7 GPIO

Table A-9 ATLANTiS Programming Control Registers

Register Name	Offset*	Access	Description
BRD_CTL	0x04	R/W	D0=1 turns on Trigger min gap/assert logic
TSTGEN	0x08	R/W	Min trigger gap value (* 8nS)
TDAT_0	0x58	R/W	Min trigger assert (* 8nS)
GPIO_EN	0x40	R/W	Bitwise output enable
GPIO_DAT	0x41	R/W	Output value (if enabled)
GPIO_IN	0x42	RO	External Pin Status

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Figure A-3 PMC Programming Interface

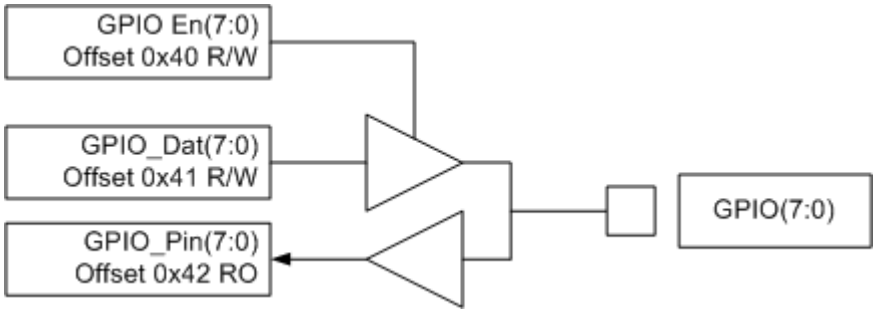


Table A-10 GPIO Bit Usage

GPIO Bit	ATLANTiS Dir	PMC Pin*	Tetra Name
7		N/C	Not used.
6		30	FPGA_CONF_DONE
5		2	FPGA_CE
4		60	FPGA_CONFIG
3		63	FPGA_DATA0
2		61	CPLD_CS0*
1		59	CPLD_DCLK
0		57	CPLD_ADSO

* Sample use pinout only; refer to the hardware user guide for the specific pinout for your board.

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Appendix A

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