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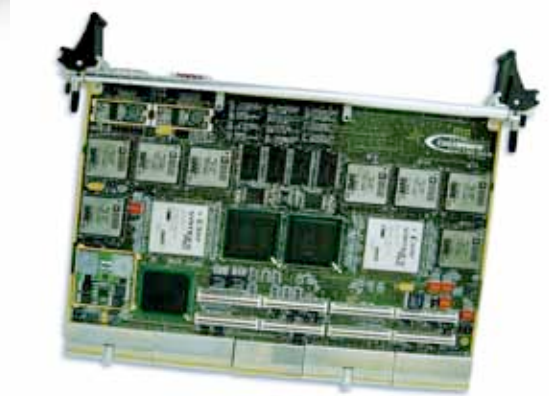
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T2-6U-cPCI

Octal ADSP-TS201S TigerSHARC® 6U CompactPCI Board



High-End Multiprocessing, Scalability, and Unprecedented I/O Bandwidth

The T2-6U-cPCI (T26U) is a 6U CompactPCI board featuring eight ADSP-TS201 TigerSHARC DSPs from Analog Devices. To take full advantage of the high-performance TigerSHARC, the T26U implements BittWare's ATLANTIS, which combines robust TigerSHARC processing with the versatile Xilinx Virtex-II Pro FPGA to offer ultra high performance and unprecedented I/O bandwidth.

Ideal for high-performance applications, such as radar and sonar, the T26U combines the ADSP-TS201 TigerSHARCs and FPGAs with:

- High-bandwidth, low-latency off-board I/O, reconfigurable for nearly any application
- High-speed interprocessor communications to facilitate scalability
- SharcFIN bridge for integrating DSPs with PCI bus and peripherals
- Comprehensive software for ease-of-use

The board also provides two large on-board banks of SDRAM, flash memory for hostless boot, and two PMC sites for adding additional processors and I/O capabilities.

High-Performance TigerSHARC Processing

The T26U features eight ADSP-TS201 TigerSHARC DSPs from Analog Devices, arranged as two clusters of four. The four processors in each cluster share a 64-bit, 83.3 MHz cluster bus. The ADSP-TS201 processor operates at up to 600 MHz, providing 3.6 GFLOPS of peak processing power. Because of its superscalar architecture, the ADSP-TS201 is also efficient at 16-bit fixed-point processing, with each DSP providing 14.4 BOPS of processing. Along with 24 Mbits of on-chip RAM, each DSP also boasts four high-speed LVDS link ports. Each full-duplex link port is comprised of a 4-bit transmit and a 4-bit receive channel, and can support up to 500 MBytes/s per channel for a total maximum throughput of 1 GByte/s. Two link ports from each DSP are used to create an interprocessor communications ring, and the remaining two link ports are routed to the ATLANTIS. When connected to ATLANTIS, the link ports run at 250 MBytes/s (125 MBytes/s per channel).

SharcFIN PCI-DSP Bridge

The T26U features two BittWare SharcFIN PCI-DSP bridge chips, one per DSP cluster, to give the DSPs low-overhead access to the host and PMC site via the 64-bit, 66 MHz PCI interface. The SharcFIN also provides a general purpose peripheral bus that allows the DSPs to access the Flash and the FPGA control registers. It also provides host access to the DSPs, on-board SDRAM, Flash, and FPGA control registers.

Features

- Two clusters of four ADSP-TS201 DSPs @ up to 600 MHz
 - ◆ 28.8 GFLOPS (3.6 GFLOPS of floating-point power per DSP)
 - ◆ 115 BOPS (14.4 BOPS of 16-bit processing per DSP)
 - ◆ 24 Mbits of on-chip RAM per DSP
 - ◆ 16 link ports @ up to 1 GByte/s each
 - ◆ Static superscalar architecture
- Two Xilinx Virtex-II Pro FPGAs (XC2VP20/30) for I/O interfacing, routing, and coprocessing
- ATLANTIS FPGAs featuring 6 GBytes/s of external I/O throughput via Virtex-II Pro routing
 - ◆ 16 link ports @ up to 250 MBytes/s each
 - ◆ 128 high-performance DIO (single-ended and/or LVDS)
 - ◆ 16 channels RocketIO™ high-speed serial transceivers
- Two PMC sites with PMC+ extensions for BittWare's PMC+ I/O modules
- 64-bit 66 MHz PCI interface via BittWare's SharcFIN PCI-DSP bridge
- Up to 512 MBytes of on-board SDRAM
- Two 8 MByte banks of Flash memory for booting DSPs and FPGAs
- Two link ports per DSP dedicated for interprocessor communications
- Two link ports per DSP dedicated for I/O
- 6U CompactPCI form factor
- Complete software support, including remote control and debug, support for multiple run-time and host operating systems, and optimized function libraries



T2-6U-cPCI Board Overview

High-Bandwidth, Low-Latency Off-Board I/O

The T26U boasts a tremendous amount of I/O bandwidth and options: two PMC sites with BittWare's PMC+ I/O extensions, high-performance digital I/O, and eight RocketIO high-speed serial transceivers. Total potential I/O bandwidth is greater than 6 GBytes/s.

Xilinx Virtex-II Pro FPGA

Two Xilinx Virtex-II Pro (XC2VP30) FPGAs, one per DSP cluster, add tremendous flexibility to the board and are useful for routing communications, translating protocols, and implementing algorithms. They connect to eight on-board TigerSHARC link ports and support a variety of external digital I/O (DIO), flags, and interrupts. Each Virtex-II Pro also provides eight RocketIO high-speed serial transceivers, which are brought off-board, for additional external communications. The FPGA also supports pre-processing, post-processing, and co-processing.

ATLANTIS

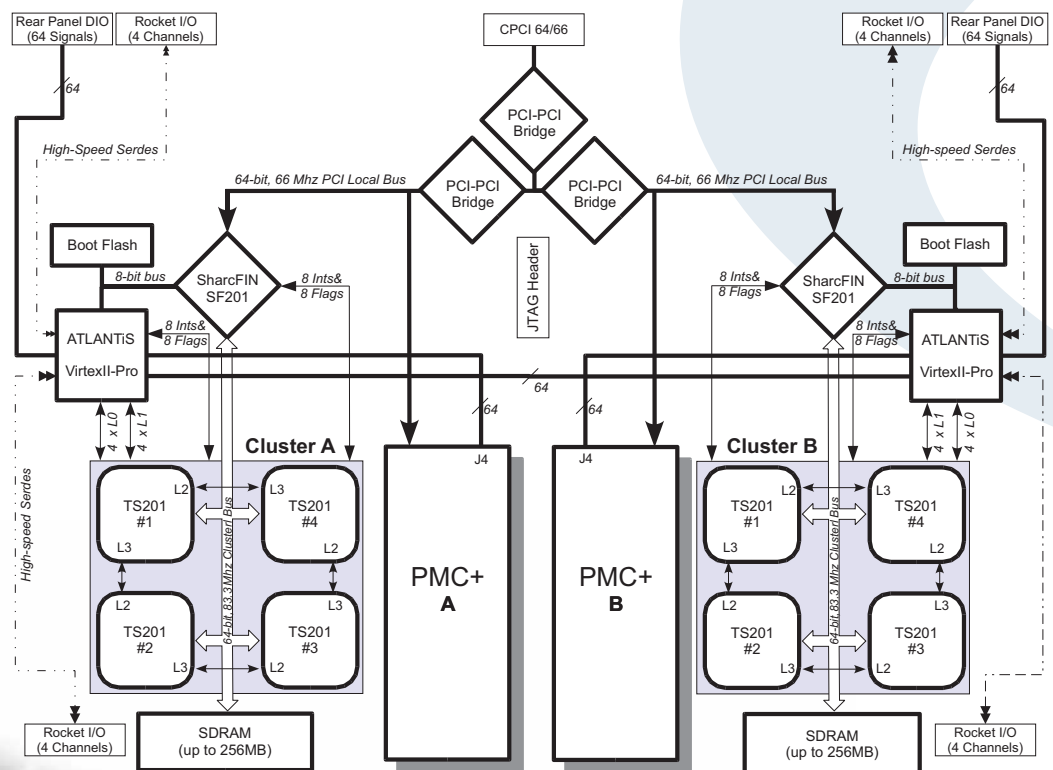
To facilitate off-board I/O and provide communications routing and processing, the T26U features BittWare's ATLANTIS, which is implemented in the Xilinx Virtex-II Pro FPGAs. All off-board I/O for the board, which includes external link ports and digital I/O blocks, is routed through the FPGAs. By tightly integrating the DSPs, PCI bridge, PMC interface, and I/O peripherals with the on-board FPGAs, ATLANTIS gives designers nearly infinite options for configuring and routing the I/O.

The eight bi-directional TigerSHARC link ports routed to each ATLANTIS FPGA provide 2 GBytes/s of data transfer between the DSP cluster and the FPGA. Using its eight RocketIO high-speed serial transceiver channels and its digital I/O blocks, each FPGA can communicate off-board at greater than 3 GBytes/s. It can be configured to connect the I/Os to each other or to the ADSP-TS201 link ports, allowing any combination of inputs and outputs to be routed together. The digital I/O blocks include PMC+ and rear panel connectors. Each digital I/O signal can also be individually configured as single-ended or LVDS.

ATLANTIS adds tremendous flexibility to the DSP subsystem, allowing system designers to route the link ports and digital I/O blocks as their specific applications require.

T2 Board Family

The T26U is part of BittWare's T2 board family, which features the ADSP-TS201 TigerSHARC DSP on a variety of platforms. The boards all feature a common, scalable architecture - ATLANTIS - and are available in PCI-X plug-in, PMC, 6U VME, and 6U CompactPCI form factors.



T26U Architectural Block Diagram

BittWorks Software Tools

BittWare offers a complete suite of software development tools to make developing and debugging applications for the T2 family of DSP boards easy and efficient, regardless of whether the hardware is on the local machine or being accessed remotely.

BittWorks Host Interface and Debugging Tools

BittWare's BittWorks software tools provide host interface libraries and a wide variety of diagnostic utilities and configuration tools. This tool set is comprised of BittWare's DSP21k Toolkit, DSP21k Porting Kit, and BittWare Target.

DSP21k Toolkit

The DSP21k Toolkit is a collection of libraries, applications, and diagnostics that helps users to easily integrate their applications with BittWare hardware. When access to hardware on a remote machine is required, the Toolkit works as though the hardware is on the local machine, creating seamless access for the user. Components of the Toolkit include:

- **Host Interface Library (HIL):** provides a mature and stable API that is compatible with all of BittWare's boards. It makes communication and control easy between the host and DSP by matching addresses supplied to the HIL to the DSP memory map addresses. It is also easily portable; written entirely in C, the same source code compiles for Windows, Linux and Vx Works.
- **BittWare configuration manager:** provides an easy-to-use interface for finding, tracking and displaying information for all BittWare devices in a system.
- **Diag21k:** an interactive diagnostic utility that provides a powerful scripting language for exercising HIL functions without writing a program using the HIL. It also allows users to load programs and examine DSP memory and provides an assembly level single processor software debugger.
- **BitLoader:** a utility for loading new code into an FPGA or EPROM without any special cables, making hardware updates easier.
- **DspTest/DspBAD:** automated diagnostics for testing board functionality, including PCI interface, DSP, and onboard memory tests.

DSP21k Porting Kit

The DSP21k Porting Kit contains the source code for the DSP21k Toolkit to allow designers to port the Toolkit to the operating system of their choice. The Porting Kit provides Project and Makefiles for Windows, VxWorks, and Linux and is written mostly in C for portability.

BittWare Target for VisualDSP++

The BittWare Target is a software debug target for Analog Devices' VisualDSP++ development environment. The BittWare Target has much of the capability of a hardware emulator but provides the extra benefits of a much lower price, faster code-loading time, and easier installation and setup. It allows users to combine any number of processors from multiple DSP boards into a single debugging session. The Target also supports remote debugging sessions for systems that have no direct access to the hardware, using remote access software.

Code Development Tools, Operating Systems, and Libraries

In addition to its BittWorks software, BittWare also supports a range of host software and third party tools from industry leading companies.

Analog Devices' VisualDSP++

VisualDSP++ is an integrated development environment for the ADSP-TS201 consisting of a C++ compiler, source level multiprocessor debugger, and project management utilities.

BittWare's TS-Lib Library

The TS-Lib library is a collection of highly optimized routines for TigerSHARC DSPs. It includes libraries for performing Fast Fourier Transforms (FFTs), windowing, statistics, sorting, histogramming, trigonometry, and timing.

Real-Time Operating Systems

BittWare's T2 family of boards supports the following real-time operating systems (RTOS): Analog Devices' VisualDSP Kernel (VDK) and Enea's OSEck RTOS.

T2-6U-cPCI Technical Specifications

BOARD ARCHITECTURE

Processors

- Eight Analog Devices ADSP-TS201S TigerSHARC DSPs, arranged as two clusters of four
- 600 MHz, 1.67 ns instruction rate DSP core
- 3.6 GFLOPS (32-bit floating point) or 14.4 GOPS (16-bit fixed point) per DSP
- Native support for 32-bit floating point operations or for 1, 8, 16, and 32-bit fixed point operations
- 24 Mbits of on-chip RAM per DSP
- Integrated I/O processor with fourteen-channel DMA controller and four 1 GByte/s LVDS link ports

DSP Cluster Shared Memory

- Two 256MByte banks of SDRAM (one per cluster) available to ADSP-TS201S DSPs
- Two banks of 8 MByte Flash memory for booting DSPs and FPGAs (one bank per cluster)
- 64-bit, 83.3 MHz bus

PMC+ Interface

- Compatible with standard PMC modules
- Additional connector (J4) provides 64 signals to Virtex-II FPGA (can be used as 32 differential pairs)

Link Ports

- 16 link ports (2 per DSP) running @ 250 MBytes/s extend from the ADSP-TS201S DSPs to the Virtex-II FPGAs
- 16 link ports (2 per DSP) running @ 1 GBytes/s dedicated for interprocessor communication

Xilinx Virtex-II Pro (XC2VP30) FPGAs

- 6 million total system gates
- 16 TigerSHARC link ports @ 250 MBytes/s
- Supports various external DIO, flags, and interrupts
- 16 RocketIO™ high-speed serial transceivers, brought off-board

External Connectors

- 8 RocketIO per cluster (16 total) to rear panel
- 8 RocketIO per cluster (16 total) connected to front panel via 2x Infiniband®-type connectors
- 64 DIO per DSP cluster (128 total) to rear panel

SharcFIN™ PCI-DSP Bridges

- 64-bit, 66 MHz PCI rev. 2.2 compliant interface
- SDRAM mapped to PCI memory space
- Programmable interrupt multiplexer: 10 inputs, 7 outputs (supports hardware interrupts in both directions)
- All ADSP-TS201S IOP registers and internal memory are mapped to PCI memory space
- Supports host- and Flash-based booting of ADSP-TS201S

PCI-PCI Bridge

- Interfaces CompactPCI backplane to on-board 64-bit, 66 MHz PCI local bus

Power

- 35 W typical

Size

- 6U single slot (233mm x 160mm, 9.2"x6.3")

SOFTWARE SUPPORT

Host Interface

- BittWare's software development kit for Windows® and Linux contains C-callable libraries for board control and communications routines
- Porting kit available for other operating system platforms

Development Tools

- Analog Devices' VisualDSP tools: kernel (VDK), C compiler, assembler, linker, simulator, and debugger
- BittWare VisualDSP Target for on-board debugging from host without an ICE
- BittWare's FPGA Developers Kit with ATLANTIS modules
- BittWare's TS-Lib optimized function libraries for TigerSHARC
- Analog Devices in-circuit emulators
- Enea's OSEck RTOS

Ordering Information

T26U-RW-XYZZ-AAB-CDEFG

R: Ruggedization C: RocketIO Connectors

0 = Commercial (air cooled) 0 = Not populated (default)
1 = Industrial Temp (air cooled) 1 = Populated*

W: Coating D: PMC+ J4 Connector

U = Uncoated 0 = Not populated
C = Conformal Coating 1 = Populated (default)**

X: Cluster A DSPs E: P3, P4, P5 Rear panel connectors

4 = 4 TS201S DSPs 0 = Not populated (default)
1 = P3 populated*

Y: Cluster B DSPs 2 = P4 populated*
4 = 4 TS201S DSPs 3 = P3 and P4 populated*

ZZ: DSP Speed 4 = P5 populated*

50 = 500 MHz 5 = P3 and P5 populated*
60 = 600 MHz* 6 = P4 and P5 populated*

AA: FPGA Size 7 = All populated (P3, P4, P5)*

20 = XC2VP20* F: SDRAM

30 = XC2VP30 (default) 6 = 128 MB

B: FPGA Speed 7 = 256 MB

6 = Xilinx speed grade 6 (default)

7 = Xilinx speed grade 7*

* Contact BittWare. Special order only.

**PMC site not available on 1U and 1C versions.

Characteristics	Commercial	Level 1U**	Level 1C**
Type	Air-Cooled	Air-Cooled	Air-Cooled
Temperature			
Operating	0°C to 50°C w/ 300 lin.ft./min airflow	0°C to 55°C w/ 300 lin.ft./min airflow	-20°C to 65°C w/ 300 lin.ft./min airflow
Storage	-45°C to 100°C	-55°C to 100°C	-55°C to 100°C
Mechanical			
Vibration	Random; 0.01g ² /Hz 15Hz to 2kHz	Random; 0.04g ² /Hz 15Hz to 2kHz (per MIL-STD-810E)	Random; 0.04g ² /Hz 15Hz to 2kHz (per MIL-STD-810E)
Shock	20g peak sawtooth 11 ms duration	20g peak sawtooth 11 ms duration	20g peak sawtooth 11 ms duration
Conformal Coating	No	No	Yes
Humidity	0 to 95% non-condensing	0 to 95% non-condensing	0 to 100% condensing



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