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PCI 9054RDK-860
Hardware Reference Manual

PCI 9054RDK-860
Hardware Reference Manual

Version 2.3

July 2005

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Order Number: 9054/860-RDK-HRM-P1-2.3

Printed in the USA, March 2005

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About This Manual

This manual provides information about the PCI 9054RDK-860 Rapid Development Kit (RDK), from a hardware perspective. It contains descriptions of all major functional circuit blocks on the board. This manual also includes the complete schematic and bill of materials.

REVISION HISTORY

Date	Version	Comments
April 2000	2.0	Hardware Reference Manual release
June 2002	2.1	Updated Bill of Materials, HRM and Schematic
March 2003	2.2	Corrected EEPROM Register Value Tables
July 2005	2.3	Updated EEPROM values

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1. General Information

The PCI 9054RDK-860 Rapid Development Kit enables designers to learn about PCI 9054 features and design issues before implementing their own designs. When used in conjunction with the PCI Software Development Kit, designers can test and evaluate the PCI 9054 device by using the provided sample software. In addition, designers can implement and test software aimed at specific applications. Through the use of this Rapid Development Kit, designs can be brought to market faster and more efficiently.

1.1 Features

The PCI 9054RDK-860 Rapid Development Kit contains a 12.35" L x 4.20" W circuit board, with the following features:

- PCI 9054 (176-pin PQFP)—PCI v2.2 compliant,
  CompactPCI Hot Swap *Friendly*, I_2O-compatible PCI I/O accelerator
- Motorola MPC860—32-bit RISC-embedded processor
- 32 MB SDRAM memory
- 512 KB FLASH memory
- One external serial RS-232 port, using SCC1 of the MPC860
- Reset switch
- MPC860 JTAG port (6-pin) connector
- MPC860 development port (2x5 pin) connector
- Debug LED
- Prototype area
- POM2 interface connector for MPC860 peripheral devices
- Debug headers

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2. Hardware Installation

2.1 Installation Procedure

Use the following procedure to prevent electrostatic damage to the host computer and to the circuit board while installing the PCI 9054RDK-860 circuit board.

To install the PCI 9054RDK-860 circuit board

1. Log off and shut down the host computer.
2. Turn off power to the computer and disconnect the power cord. Ensure that the chassis and antistatic bag which holds the PCI 9054RDK-860 circuit board are properly grounded, preferably at an antistatic workstation with wrist straps.
3. Ground yourself by touching the computer case.
4. Remove the computer cover.
5. Remove the PCI 9054RDK-860 circuit board from the antistatic bag and place it into an empty PCI slot.
6. Secure the captive screw to ensure proper electrical grounding and mechanical stability.

2.2 Verify Installation

After installation, verify that the PCI 9054RDK-860 circuit board is correctly installed.

To verify that the circuit board is correctly installed

1. Install the PCI SDK (Software Design Kit) onto the computer. Refer to *PCI SDK User's Manual* for software installation.
2. Double click the **PLXMon** icon (located in the C:\PCI SDK folder).
3. When the **PLXMon** application starts, it should select the PCI 9054RDK-860 as default. If the verification is not successful, confirm the hardware is correctly installed, and then reinstall all software.
4. If necessary, contact Customer Support for further assistance (refer to the section, "Customer Support," for information on how to contact PLX).

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3. System Architecture

The purpose of this RDK is to demonstrate the following:

- Connection between the PCI 9054 and MPC860
- Host CPU accesses to all Local resources
- Local CPU (MPC860) accesses to all PCI resources
- Additional features to demonstrate I_2O operations

The PCI 9054RDK-860 features:

- PCI 9054 (PCI Bus Master/Slave Interface chip)
- MPC860 (PowerPC CPU with communications processor)
- Boot ROM (FLASH)
- Memory subsystem (SDRAM)
- Debug port (serial port, MPC860 JTAG, and MPC860 development port)
- MPC860 peripheral port connector

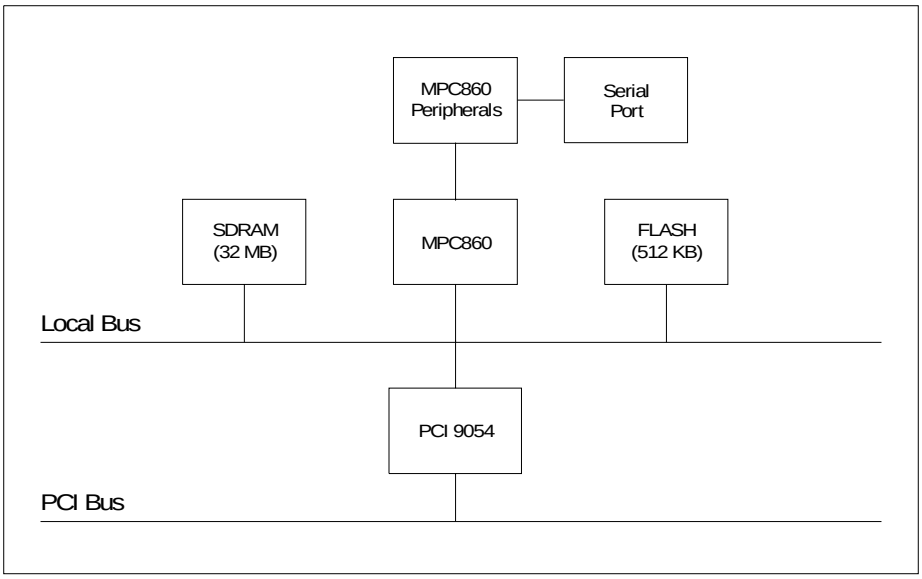


Figure 3-1. PCI 9054RDK-860 System Architecture

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The MPC860 has Read/Write access to the following:

- SDRAM
- FLASH
- MPC860 peripherals
- Serial port
- PCI 9054 internal registers (including DMA registers)
- PCI Bus devices [using the Direct Master (DM) Memory Read and Write, I/O Read and Write, or Configuration Cycle 0 and 1 generation through the PCI 9054]

Any PCI Bus Master device has access to all PCI 9054 internal registers and PCI-to-Local Memory and I/O spaces [(Direct Slave (DS) access)]. PCI Bus Master devices by way of the DS access can access all MPC860 peripherals, including the serial port, SDRAM, and FLASH.

The PCI 9054 DMA controller is the most efficient way to transfer data between the Local Bus and the PCI Bus. In this case, the PCI 9054 is the Master of both the Local and PCI Buses when transferring data.

The combination of the DM, DS, DMA, interrupt generation on the Local and PCI Buses, and I_2O-Ready PCI 9054 architecture enables the PCI 9054RDK-860 to operate as an I_2O-compliant system.

In addition, the PCI 9054RDK-860 provides the complete PCI SDK to aid programmers in developing drivers and applications.

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4. Hardware Architecture

4.1 Hardware Memory Map

Table 4-1. Local Bus Hardware Memory Map

Address Range	Device	Chip Select	Bus Width	Wait State(s)	Comments
FFF7 FFFF FFF0 0000	FLASH	CS0#	8	6	FLASH (Boot Code) — controlled by MPC860 GPCM
FFEF FFFF FF00 0000	Internal Registers and RAM	Internal	NA	NA	MPC860 internal registers (Internal I/O spaces)
FEFF FFFF 8000 0000	Unused				
7FFF FFFF 7000 0000	Unused				
6FFF FFFF 6000 0000	Unused				
5FFF FFFF 5000 0000	DM I/O (PCI 9054)	NA	32	NA	Direct Master I/O space —controlled by MPC860 GPCM
4FFF FFFF 4000 0000	DM Memory (PCI 9054)	NA	32	NA	Direct Master Memory space — controlled by MPC860 GPCM
3FFF FFFF 3000 0000	PCI 9054 Internal Registers	CS3#	32	5	PCI 9054 internal register space (512 bytes) — controlled by MPC860 GPCM
2FFF FFFF 2000 0000	Unused				
1FFF FFFF 1000 0000	Unused				
01FF FFFF 0000 1000	SDRAM	CS1#	32	5-1-1-1	SDRAM space (32 MB) — controlled by MPC860 UPM(A)

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4.2 Main Components

4.2.1 PCI 9054

The PCI 9054 is a PCI Bus Master interface chip (*PCI Bus Specification v2.2 compliant*) with Direct Slave (DS), Direct Master (DM), two DMA controllers, and an I_2O-compliant Messaging Unit. It also is PCI Hot Plug and CompactPCI Hot Swap compliant. It allows for easy interface to the Motorola MPC860, IBM 401XX, and Intel i960XX processor families.

This RDK is configured using the MPC860 MPU M-mode interface. Therefore, J1 pins 3 through 6 should be open. In M mode, glue logic is not required to interface the PCI 9054 to the MPC860.

If the PCI 9054 TEST pin is pulled high (*that is*, J1 pins 1 and 2 are shorted), all PCI 9054 pins become input (except the USERo pin) and the PCI 9054 operates in NANDTREE Test mode.

In a normal operation, J1 should be open (*that is*, no jumper blocks).

The serial EEPROM (93LC56B) is used to configure the PCI 9054 during power-on and to hold Vital Product Data (VPD). The power-on configuration serves as PCI Plug-and-Play (PnP), PCI 9054 configuration, Local Bus and board configuration. The serial EEPROM is a 3.3V part; however, a 5V part can also be used, as the PCI 9054 is 5V I/O tolerant.

Although the PCI 9054 has internal 50K-ohm pull-up resistors on the Address Bus and other input pins, RN1 through RN8 were added to pull up the address lines with 10K-ohm resistors. These resistor networks are optional.

The PCI Bus Power Management Event (PME#) signal and internal registers are included in the PCI 9054 to support PCI Bus Power Management features.

The PCI Bus ENUM# and Local Bus LEDon/LEDin pins are included to support the CompactPCI Hot Swap feature. Refer to *PCI 9054 Data Book* or *CompactPCI 9054RDK-860* for CompactPCI RDK.

The PCI 9054 supports a standard Single cycle (one Address phase per one Data phase) and Burst cycle [one Address phase for one or more Data phases, as MPC860 and its peripherals are limited to four longword (Lword) (32 bit) data bursts at a time] to or from the MPC860. In addition, the PCI 9054 supports a Back-Off mechanism through the MPC860 Retry function. When the PCI 9054 detects a possible Deadlock situation, mainly DS and DM occuring simultaneously, the PCI 9054 asserts the RETRY# signal requesting the MPC860 to Back-Off (the DM releases the current cycle for a later time).

The PCI 9054 also supports the MPC860 IDMA transfer to or from the PCI Bus using the MDREQ# signal. MDREQ# (DMA request to the MPC860 IDMA controller) is asserted by the PCI 9054 as long as the DM FIFO space is available. In other words, MDREQ# is de-asserted only when the DM Write FIFO is full. The software must account for MDREQ# being asserted when the IDMA is not ready to transfer data. Refer to *PCI 9054 Data Book* for more information.

The PCI 9054 has full access to the MPC860 communications and MPC860 memory controller modules. The MPC860 has full access to the PCI 9054 internal registers using the CS3# signal (CS9054# => CCS#) and all PCI resources using the Direct Master Read and Write (DMR and DMW) cycles. Refer to *PCI 9054 Data Book* for more information.

4.3 MPC860

The Motorola MPC860XX is a 32-bit PowerPC-core-based MPU with a programmable communications processor and built-in memory controller modules. The MPC860 includes the JTAG and development ports connector for debugging purposes. The development port supports many different types of Motorola-approved tools including FRZ signal or VFLS[0:1] signal to pins 1 and 6. Refer to the Motorola website for further details on these tools.

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The MPC860 power-on configuration is done while HRESET# is asserted. MODCK[1:2] determines the initial operating frequency, while U34 and the pull up/down resistor network determines the other MPC860 initial operating mode. Any of these power-on configuration settings can be reprogrammed by way of the software after boot up.

Either a 4-MHz or a 50-MHz oscillator is used to generate a reference clock to the MPC860. The MPC860 generates Local Bus Clock Out (CLKOUT) to the clock buffer. In turn, the clock buffer generates all Local Bus clocks, including the PCI 9054 (LCLK), SDRAM (SDRAM_CLK), and PLX Option Module 2 (POM2_CLK) clocks.

***Note**: Refer to the section, "Clock," for further design notes.*

All MPC860 peripheral signals are connected to the POM2 (PLX Option Module 2) for MPC860 peripheral expansion. Only SSC1 is used as the PLXROM debug connection to the remote terminal. All other peripheral expansion is available to the user.

The GPL(A) ports and BS_A port are used to control the SDRAM. The GPL(A)[0:3] signals are connected to all SDRAM control signals, as well as the external address Mux (U31, U32, and U33). BS_A[0:3] are used as a Read/Write Enable signal. Refer to the section, "SDRAM," for more information.

One of the MPC860 internal Chip Selects (CS[3:0]#) is used to access the PCI 9054 internal registers (CS3# or CS9054#). CS0# is assigned to access the FLASH (CSFLASH#), while CS1# is used to access the SDRAM (CSSDRAM#).

For exception process, IRQ1# is connected to the PCI 9054 Local Interrupt In/Out pin in addition to the TEA# and the RETRY# signals from the PCI 9054.

4.4 Clock

The MPC860 accepts the 4 MHz external clock (MODCK[1:2] = 'b11) or 50 MHz external clock (MODCK[1:2] = 'b10), and generates the CLKOUT to clock buffer (U9, CY2305). The CLKOUT frequency is programmable via MPC860 internal clock circuit—4 MHz times 12 (48 MHz), 13 (52 MHz), 50 MHz times 1, or other combinations.

The MPC860 and PCI 9054 are rated at 50 MHz. In turn, the clock buffer generates LCLK to the PCI 9054, POM2_CLK to the POM2 connector, and SDRAM_CLK to the SDRAM. In addition, there is a SPARE_CLK, with a capacitor termination of 10 pF. All clock outputs from U9 (CY2305) should have the same loading to maintain zero delay between input clock (MPC860 CLKOUT) and all outputs.

The phase of the outputs can be adjusted by way of C38, a terminating capacitor on the SPARE_CLK signal. If C38 is larger than the loading of each clock (LCLK, SDRAM_CLK, and POM2_CLK), then the phase shift is negative (*that is*, output leads input). If C38 is smaller than the loading of each clock, the phase shift is positive (*that is*, output lags input). Each clock loading should be 10 to 15 pF (plus trace capacitance).

***Note**: Refer to the section, "Schematics*," *for the clock circuits and optional clock termination circuits.*

4.4.1 PCI Clock

The PCI Bus Clock (PCLK) supports speeds up to 33 MHz.

4.4.2 Local Clock

The Local Bus Clock (CLKOUT) can be any multiple of 4 MHz, programmable with the MPC860 internal clock generator or 50 MHz with the 50 MHz external oscillator. The PCI 9054RDK-860 is built and set to 50 MHz with an external 50 MHz oscillator.

Note: The PCI 9054 and the MPC860 are limited to 50 MHz.

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4.5 Memory

The SDRAM and FLASH are connected to the MPC860 memory controller.

4.5.1 Boot ROM (FLASH)

The Boot ROM (FLASH) is described as follows:

- 512 KB (512 kilobits x 8 bits), 90 ns
- Access type is Single cycle only
- Number of available wait states is six (at 50 MHz, 120 ns FLASH, worst case)

***Note**: The FLASH contents should be copied to SDRAM after initial boot up. Also, turn on the instruction cache feature to improve performance.*

The FLASH contains MPC860 boot code and debug code (PLXMon). The FLASH is accessible by way of the MPC860, as well as the PCI 9054 (Host processor access). The access can be read or write. The MPC860 GPCM is connected to the FLASH with CS0# as the chip select, BS_B0# as the Write Enable signal, and GPL_A1# as the read (OE#) signal. The power supply to U10 (FLASH) can be 3.3 or 5V, selectable by way of R76/R77, depending on the FLASH used. Both the MPC860 and PCI 9054 have a 3.3V supply with 5V-tolerant I/O buffers.

4.5.2 SDRAM

The SDRAM is described as follows:

- 32 MB, 10 ns (100 MHz)
- 4 chips x (2 megabits x 8 bits x 4 banks)
- Access type is Single cycle or Burst 16 bytes [Four Lword (32-bit) bursts only]
- Timing is 5-1-1-1

All SDRAM control signals (UPM(A)—GPL_A[0:3], GPL_A[5], BS_A[0:3], CS1# or CSSDRAM#) originate from the MPC860, with the exception of the CKE signal, which is used to enable or disable the clock signal for power-down purposes. CKE can be enabled or disabled by installing a resistor (R16 or R23, respectively). The CSSDRAM# is connected to the SDRAM chip select [programmable via the MPC860 UPM(A) (user programmable machine A)]. GPL_A0# is connected to the SDRAM AP by way of Mux. GPL_A1# is connected to the SDRAM WE#, GPL_A2# as the SDRAM RAS0#, and GPL_A3# as the SDRAM CAS0#. BS_A[0:3]# are connected to SDRAM DQM[0:3] and act as byte enables.

The GPL_A5# controls the Address Mux unit (U31, U32, and U33). The Mux unit is used to multiplex the row and column address as CAS = A[21:29], RAS = A[9:20]. A[7:8] are used as the bank-select signals.

***Note**: The SDRAM requires a synchronous clock (SDRAM_CLK) and MA10/AP line to indicate the mode of operation (programming). Refer to the section, "*Schematics*."*

SDRAM contains the core of standard DRAM, with a clock pin that synchronizes all inputs and outputs (address, data and control signals) to the system clock. These simplify the control interface and eliminate the need to generate asynchronous RAS and CAS strobes, as required by conventional DRAM.

SDRAM incorporates a burst counter used to increment column addresses on each clock for Burst cycles. The burst length and type (sequential or interleaved) is selected by programming an on-chip mode register. The length of the burst sequence may be set by the user and is programmed for one, two, four, eight, or whole page transfers within SDRAM Mode registers.

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In addition to the programmable burst length and address-mode selection, CAS Latency and Burst Read/Write mode are programmable. The CAS Latency determines how many clocks are required for data to be valid during Read cycles. The Burst Read/Write Mode bit determines the Burst Read/Write capability of the processor accessing the SDRAM.

Therefore, the mode register should contain 'b100010 for burst of four, Sequential Addressing mode, CAS latency of two, and Burst Read/Write operation. (The MAR data is actually 88h because the address lines are shifted by two Least Significant Bits (LSBs) — SDRAM A[0] is actually LA[2] due to the 32-bit Data Bus.) Refer to *SDRAM Data Sheet* for more information.

The following data was generated from UPM860.EXE (UPM860.zip file and *MPC8XX SDRAM Interface Application Note* from the Motorola website).

***Note**: 100 MHz SDRAM were used to meet the MPC860 timing requirements. The SDRAM is accessible by way of the MPC860 or PCI 9054 (Host processor access).*

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The SDRAM Initialization sequence summary is as follows:

```
;Load the UPM(A) data
1. Load the UPM(A) data --- see below for the UPM(A) data.
;Memory Bank 1 initialization
2. Init Option_REG_bank1---[OR1]
3. Init BASE_REG_bank1-----[BR1]
;SDRAM_INIT
4. INIT SDRAM mode register --- [MAR] = 0x88.
5. Run MRS command from UPM data 0x2B --- MCR = 0x8000212B
6. Set the UPMA_MODE_REG
7. Set the MCR for refresh --- MCR = 0x80002130 (0x30 of the UPM(A) data
has the refresh sequence)
8. Set the UPMA_MODE_REG
UPM_Initialize_Values:
; UPM A RAM Array
; Single Read (Offset 0x0)
 .long 0xeffefc04, 0x0ffcfc04, 0xeeefb004, 0x00af3004
 .long 0xeffaf000, 0x0ff0f004, 0xfffffc05, 0xfffffc04
; Burst Read (Offset 0x8)
 .long 0xeffefc04, 0x0ffcfc04, 0xeeefb004, 0x00af3004
 .long 0xf0fff000, 0xf0fff000, 0xe0faf000, 0x0ff0f000
 .long 0xfffff005, 0xfffffc04, 0xfffffc04, 0xfffffc04
 .long 0xfffffc04, 0xfffffc04, 0xfffffc04, 0xfffffc04
; Single Write (Offset 0x18)
 .long 0xeffefc04, 0x0ffcfc04, 0xeeebb000, 0x00a33004
 .long 0xeffaf004, 0x0ff0f004, 0xfffffc05, 0xfffffc04
; Burst Write (Offset 0x20)
 .long 0xeffefc04, 0x0ffcfc04, 0xeeebb000, 0x00a33000
 .long 0xf0fff000, 0xf0fff000, 0xe0faf004, 0x0ff0f004
 .long 0xfffffc05, 0xfffffc04, 0xfffffc04, 0xefdafc34
 .long 0x0fe0fc34, 0xefaab034, 0x1fb57435, 0xfffffc04
; Refresh (Offset 0x30)
 .long 0xeffebc04, 0x0ffc3c04, 0xfffffc04, 0xfffffc04
 .long 0xfffffc04, 0xfffffc04, 0xfffffc04, 0xfffffc05
 .long 0xfffffc04, 0xfffffc04, 0xfffffc04, 0xfffffc04
; Exception (Offset 0x3c)
 .long 0xeffffc04, 0x0ffffc04, 0xfffffc05, 0xfffffc04
```


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4.6 Serial Port

One of the MPC860 serial ports (SCC1) is used as the RS-232 port. A remote terminal can be connected to this RS-232 port to monitor the PLX ROM program, which is stored in the FLASH.

4.7 Debug Port

The PCI 9054RDK-860 supports two MPC860 debug ports — JTAG(J2) and development port (BDM) (J3). The development port supports many different types of Motorola-approved tools, including the FRZ or VFLS[0:1] signals to pins 1 and 6. Refer to the Motorola website for more information.

4.8 Interrupts

This section discusses the PCI and Local Bus Interrupt Controller Unit and routing.

4.8.1 MPC860 Critical Interrupt

The Local System Error interrupt from the PCI 9054 (RETRY# and TEA#) is routed directly to the Critical Interrupt input on the MPC860 processor.

4.8.2 MPC860 External Interrupt

The External Interrupts (RETRY#, IRQ[0:2]3, and IRQ7#) are routed to the MPC860 internal interrupt controller. Interrupts IRQ0#, IRQ2#, and IRQ7# are unused while IRQ1 is connected to the PCI 9054 LINT# pin. LINT# (IRQ1#) can be used to trigger the PCI 9054 DMA Transfer Complete or Doorbell register writes by the Host. The LINT# pin is a bidirectional (input and output) PCI 9054 interrupt pin.

4.8.3 PCI-to-Local interrupt

A PCI Master device can generate the local interrupt through the PCI 9054 Doorbell or Mailbox registers. The PCI 9054 interrupt output is connected to the MPC860 IRQ1# pin. The PCI 9054 Local System error (such as a PCI Master abort) can generate TEA# to the MPC860. Refer to the *PCI 9054 Data Book* for specific interrupts.

4.8.4 PCI Interrupt (INTA#) via the PCI 9054

The bidirectional LINT# pin can be programmed to take the local interrupt source and generate the PCI interrupt (INTA#). INTA# can also be generated from the Local-to-PCI Doorbell register, the DMA Done interrupt, and so forth. Refer to the *PCI 9054 Data Book* for more information.

4.9 LED Indicators

The *Green Debug LED* is connected to the PCI 9054 USERo pin. Therefore, the Green LED can be turned on or off by writing 1 or 0, respectively, to the PCI 9054 internal register USER bit. The USERo pin can also be used for user-specific applications.

The *Red MPC860 Failed LED* is connected to the MPC860 FRZ pin. This signal indicates the MPC860 is in Debug Mode or jumped into Debug mode.

4.10 Power Supply

Most of the components are powered from a 3.3V supply. The main PCI power supply can be 5V or 3.3V, selectable by way of R47/R48 configuration.

- If R47 is present and R48 is not, the PCI Bus connector 3.3V power supply is used. In this case, do not install U27, C47, R48, R49, or R50.
- If 3.3V is not available (or if uncertain whether it is “default”), a 5V to 3.3V voltage regulator, such as a U27, can be used (install R48, but not R47).

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4.11 MPC860 Peripherals Connector (POM2)

The POM2 (PLX Option Module 2) connector contains the necessary signals to utilize all possible MPC860 peripherals, using

- Port A (PA[0:15])
- Port B (PB[14:31])
- Port C (PC[4:15])
- Port D (PD[3:15])
- Input Port B (IP_B[0:7])
- GPL signals
- Timer expired (TEXP)
- Output Port[0:1]

In addition, there are two groups of power supplies with a configurable 3.3 or 5V supply. Refer to the section, “Serial Interface Pinout,” for peripheral connection pinouts.

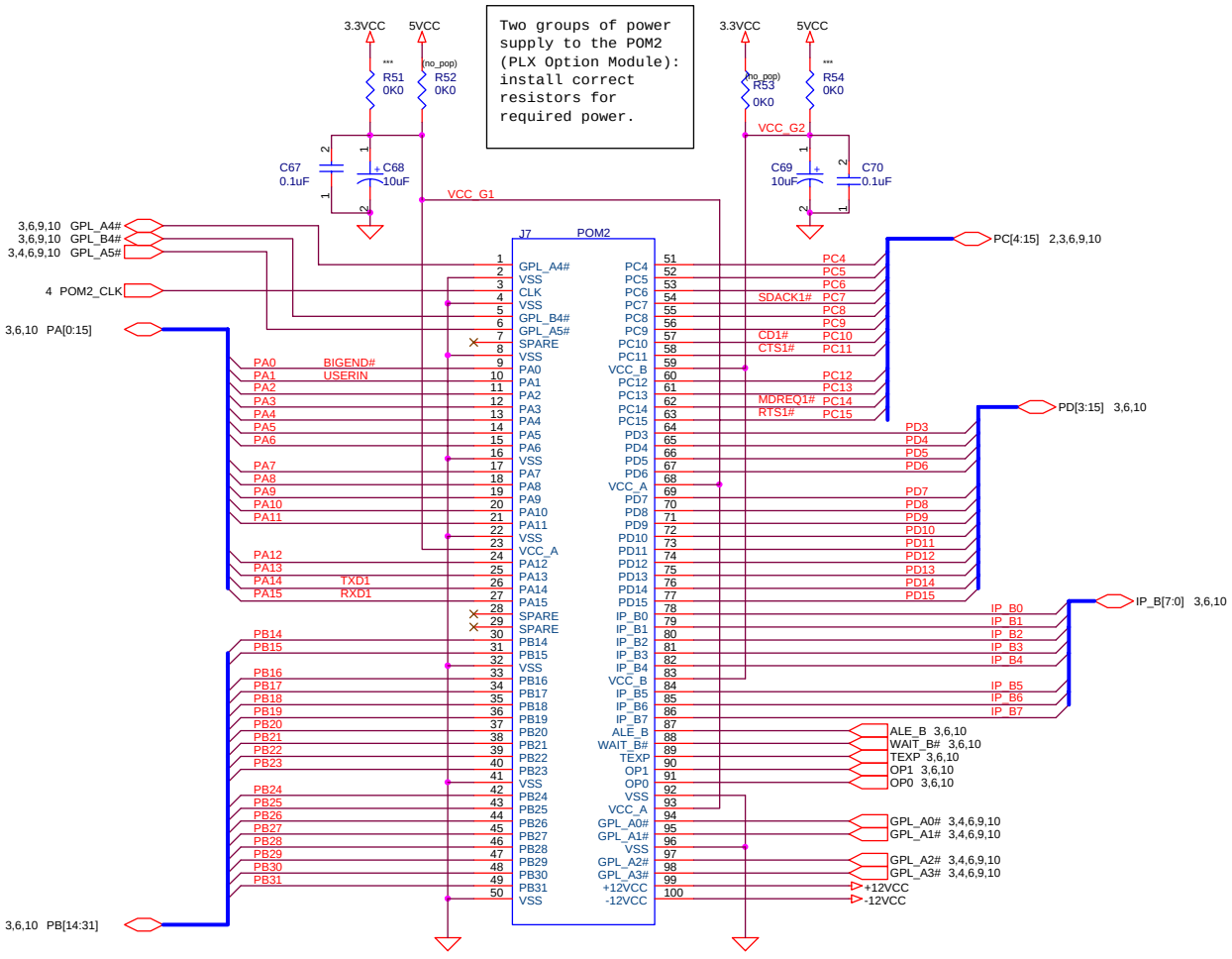


Figure 4-1. MPC860 Peripherals Connector (POM2)

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4.12 Reset Circuitry

4.12.1 Power-On Reset and Pushbutton Reset

The PCI Bus resets when the RST# signal is active during power-on. The PCI 9054 outputs LRESETo# when RST# is active. All Local devices reset with the LRESETo#.

The on-board Pushbutton resets all Local devices, excluding the PCI 9054. The software must reinitialize the PCI 9054 after all resets.

4.12.2 Register Initialization

The PCI 9054 serial EEPROM contains all critical configuration data for normal PCI Bus operations. These include PnP data, PCI memory resource allocation, and end of the PCI 9054 initializations (such as the Init Done bit). In addition to the serial EEPROM data, the Local processor (MPC860 in this case) can reinitialize the PCI 9054, thereby overwriting the data from the serial EEPROM. Refer to *PCI 9054 Data Book* and the following serial EEPROM data example for more information.

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4.12.3 Serial EEPROM Loads

Table 4-2. Long Serial EEPROM Load Registers

Serial EEPROM Offset	Serial EEPROM Value (hex)	Description	Register Bits Affected
0h	1860	Device ID	PCIIDR[31:16]
2h	10B5	Vendor ID	PCIIDR[15:0]
4h	0680	Class Code	PCICCR[23:8]
6h	0001	Class Code, Revision	PCICCR[7:0] / PCIREV[7:0]
8h	0000	Maximum Latency, Minimum Grant	PCIMLR[7:0] / PCIMGR[7:0]
Ah	0100	Interrupt Pin, Interrupt Line Routing	PCIIPR[7:0] / PCIILR[7:0]
Ch	0000	MSW of Mailbox 0 (User Defined)	MBOX0[31:16]
Eh	0000	LSW of Mailbox 0 (User Defined)	MBOX0[15:0]
10h	0000	MSW of Mailbox 1 (User Defined)	MBOX1[31:16]
12h	0000	LSW of Mailbox 1 (User Defined)	MBOX1[15:0]
14h	FF00	MSW of Range for PCI-to-Local Address Space 0	LAS0RR[31:16]
16h	0000	LSW of Range for PCI-to-Local Address Space 0	LAS0RR[15:0]
18h	0000	MSW of Local Base Address (Re-map) for PCI-to-Local Address Space 0	LAS0BA[31:16]
1Ah	0001	LSW of Local Base Address (Re-map) for PCI-to-Local Address Space 0	LAS0BA[15:0]
1Ch	0100	MSW of Mode/DMA Arbitration Register	MARBR[31:16]
1Eh	0000	LSW of Mode/DMA Arbitration Register	MARBR[15:0]
20h	0030	MSW of Local Bus Big/Little Endian Descriptor	PROT_AREA[15:0]
22h	5524	LSW of Local Bus Big/Little Endian Descriptor	LMISC[7:0] / BIGEND[7:0]
24h	0000	MSW of Range for PCI-to-Local Expansion ROM	EROMRR[31:16]
26h	0000	LSW of Range for PCI-to-Local Expansion ROM	EROMRR[15:0]
28h	0000	MSW of Local Base Address (Re-map) for PCI-to-Local Expansion ROM	EROMBA[31:16]
2Ah	0010	LSW of Local Base Address (Re-map) for PCI-to-Local Expansion ROM	EROMBA[15:0]
2Ch	4343	MSW of Bus Region Descriptors for PCI-to-Local Accesses	LBRD0[31:16]
2Eh	0043	LSW of Bus Region Descriptors for PCI-to-Local Accesses	LBRD0[15:0]
30h	FF00	MSW of Range for Direct Master-to-PCI	DMRR[31:16]
32h	0000	LSW of Range for Direct Master-to-PCI	DMRR[15:0]
34h	4000	MSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[31:16]
36h	0000	LSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[15:0]
38h	5000	MSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[31:16]
3Ah	0000	LSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[15:0]
3Ch	0000	MSW of PCI Base Address (Remap) for Direct Master-to-PCI	DMPBAM[31:16]
3Eh	0003	LSW of PCI Base Address (Remap) for Direct Master-to-PCI	DMPBAM[15:0]
40h	0000	MSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCFGA[31:16]
42h	0000	LSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCFGA[15:0]

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Table 4-3. Extra Long Serial EEPROM Load Registers

Serial EEPROM Offset	Serial EEPROM Value	Description	Register Bits Affected
44h	9054	Subsystem ID	PCISID[15:0]
46h	10B5	Subsystem Vendor ID	PCISVID[15:0]
48h	FF00	MSW of Range for PCI-to-Local Address Space 1 (1 MB)	LAS1RR[31:16]
4Ah	0000	LSW of Range for PCI-to-Local Address Space 1 (1 MB)	LAS1RR[15:0]
4Ch	0000	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[31:16]
4Eh	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[15:0]
50h	0000	MSW of Bus Region Descriptors (Space 1) for PCI-to-Local Accesses	LBRD1[31:16]
52h	0043	LSW of Bus Region Descriptors (Space 1) for PCI-to-Local Accesses	LBRD1[15:0]
54h	0000	MSW of Hot Swap Control register	***Reserved***
56h	4C06	LSW of Hot Swap Control register	HS_NEXT[7:0] / HS_CNTL[7:0]

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4.13 Arbitration

PCI Bus arbitration is performed using the PCI Host arbiter when the PCI 9054 needs the PCI Bus, while the Local Bus uses the built-in MPC860 arbiter when the PCI 9054 needs the Local Bus. The PCI Bus arbitration signals are REQ# and GNT#. The Local Bus arbitration signals are BR#, BG#, and BB#.

4.14 Power Management

Power Management uses the PME# pin (four stages) (refer to *PCI 9054 Data Book*). The PCI 9054 does not retain Power Shutdown mode; however, the LCLK (local clock) can be slowed or shut down from the external clock circuit to conserve power. PME# and internal registers for Power Management are used by the Local and Host processors to control board power management. If the clock is removed (0 Hz), the PCI 9054 contains all the configuration data as long as the power is supplied and the clock returns with a smooth transition. If power is removed, the software must reconfigure the PCI 9054.

4.15 Prototype Area

The PCI 9054RDK-860 provides a prototype area that allows users to incorporate custom-designed circuitry. This area contains common surface-mount footprints, including two 44-pin TQFPs, two 20-pin SOs, two 16-pin SOs, a 20-pin PLCC, a 44-pin PLCC, and a 68-pin PLCC.

In addition, a standard 0.100-inch through-hole array is included, as well as connections for +3.3V and ground.

4.16 Test Connectors

All Local Address and Data lines can be monitored by way of J8, and all Local Bus Control signals can be monitored by way of J9.

4.17 Test Points

All schematic signals have test points, which are coincident to board “VIAs.” The PCI 9054RDK-860 is an example of how to implement a circuit board for an Automated Test Unit (ATU) fixture. Refer to the GERBER files on the RDK CD-ROM for details.

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4.18 Jumpers and Connectors Summary

4.18.1 Configuration Jumpers (Resistors)

The following table describes configuration jumpers (resistors).

Table 4-4. Configuration Jumpers (Resistors)

Resistor	Description
R60 and R62, or R61 and R63	Configures the type of Development Port tool used (default). Install R61 and R63 to use the tools requiring VFLS[0:1].
R76/R77	Selects the FLASH power source. Install R76 if FLASH operates with 3.3V (default). Install R77 if FLASH operates with 5V.
R16/R25	Enable/disable the SDRAM clock input. Enables it when R16 is installed (default).
R38/R39	MODCK1 state during power-on. If R38 is installed, MODCK1 = 1. R40/R41 — MODCK2 state during power-on. If R40 is installed, MODCK0 = 1. Install R38 and R40 if 4 MHz OSC is used. (Default) Install R38 and R41 if 50 MHz OSC is used.
R42/R43	D[5] state during power-on. If R42 is installed, D[5] = 1, boot port size is 8-bit (default).
R70/R71	D[7] state during power-on. If R70 is installed, D[7] = 1, initial internal register base address = 0xFF00_0000 (default).
R72/R73, R74/R75	D[9:10] state during power-on. If R72 and R74 are installed, D[9:10] = 11, debug pin configuration (default).
R64/R65, R66/R67	D[11:12] state during power-on. If R64 and R66 are installed, D[11:12] = 11, external bus division factor (default).
R48/R47	Power Source: 1. If R48 is installed, the 3.3V power is regulated from PCI 5V. 2. If R47 is installed, the board uses the PCI Bus 3.3V. (Do not install U27 and R48.)
R51/R52 and R53/R54—POM2	Power source. Refer to the section, ”Schematics, sheet 8.” 1. Default. Install R51 and R54 for POM2 connector 3.3V/5VCC supply. (Do not install R52 and R53.) 2. Connect desired power supply combinations.

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4.18.2 Jumpers, Test Points, and Connectors

The following table describes jumpers, test points, and connectors.

Table 4-5. Jumpers, Test Points, and Connectors

Jumper	Description
J1	PCI 9054 mode and test configuration. 1. Pins 1 and 2 are open (default)—TEST = 0; test function is disabled for normal operation. 2. Pins 3 and 4 are open (default)—MODE1 = 1, and pins 5 and 6 are open (default)—MODE0 = 1. MODE[1:0] are used to program the PCI 9054 Local Bus mode. When these bits have a value of 11, the PCI 9054 operates in M mode (MPC860 mode). Refer to *PCI 9054 Data Book* for more information.
J2	MPC860 JTAG connector.
J3	MPC860 Development Port connector.
J6	PCI edge connector.
J7	POM2 (PLX Option Module 2).
J8	Local Address and Data test points.
J9	Local Bus Control Signal test points.

4.19 Special Considerations

Note the following when using the PCI 9054RDK-860:

- BDIP# is generated only if the BTERM bit is reset (0). Therefore, if more than four Lwords are needed, use the BURST# signal (instead of BDIP#) to terminate the Burst sequence. To burst more than four Lwords, use of synchronous devices is recommended. Refer to *CompactPCI 9054RDK-860 Hardware Reference Manual* for more information on how to use synchronous-burst SRAM.
- The BB# line requires a 3.9K pull-up resistor.
- The EEDI/EEDO pin requires a 1K-ohm pull-down resistor if the serial EEPROM is not present and the MPC860 does not initialize the PCI9054. The 1K-ohm pull-down resistor forces data input to the PCI 9054 to be 0, which is required to bypass the serial EEPROM load. Because the EEDI/EEDO pin is bidirectional, 1K is required to quickly pull down the line because the PCI 9054 is driven high during the last clock.
- The EEDI/EEDO pin requires a 3.9K-ohm pull-up resistor if serial EEPROM is present.

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5. Software Architecture

5.1 PCI SDK

A complete PCI 9054 API library is available from PLX Technology (refer to the section, “Customer Support,” for information on how to contact PLX).

5.1.1 PLXMon (Uses PCI SDK)

PLXMon is used on the Host Bus (PC). PLXMon runs from FLASH memory on the Local Bus.

5.1.2 Windows Device Drivers

Drivers that use the API library are available from PLX Technology (refer to the section, “Customer Support,” for information on how to contact PLX).

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6. Serial Interface Pinout

6.1 SCC1

Table 6-1. UART

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
D17	PA[14]	TXD1	Transmit data output for SCC1
C18	PA[15]	RXD1	Receive data input for SCC1
N19	PB[19]	RTS1#	Request to send modem line for SCC1
J19	PC[11]	CTS1#	Clear to send modem line for SCC1
K19	PC[10]	CD1#	Carrier detect modem line for SCC1

Table 6-2. HDLC Controller

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
D17	PA[14]	TXD1	Transmit data output for SCC1
C18	PA[15]	RXD1	Receive data input for SCC1
M19	PA[7]	CLK1	Clock for SCC
N19	PB[19]	RTS1#	Request to send modem line for SCC1
J19	PC[11]	CTS1#	Clear to send modem line for SCC1
K19	PC[10]	CD1#	Carrier detect modem line for SCC1

Table 6-3. Transparent Controller

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
D17	PA[14]	TXD1	Transmit data output for SCC1
C18	PA[15]	RXD1	Receive data input for SCC1
M19	PA[7]	CLK1	Clock for SCC
N19	PB[19]	RTS1#	Request to send modem line for SCC1
J19	PC[11]	CTS1#	Clear to send modem line for SCC1
K19	PC[10]	CD1#	Carrier detect modem line for SCC1
U18	PB[14]	RSTRT1#	Serial CAM Interface output signals that marks start of a frame
E19	PB[27]	BRG01	BRG1 output clock

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Table 6-4. Ethernet Controller

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
D17	PA[14]	TXD1	Transmit data output for SCC1
C18	PA[15]	RXD1	Receive data input for SCC1
M19	PA[7]	CLK1, RCLK	Clock for SCC
N19	PB[19]	RTS1#, TENA	Request to send modem line for SCC1
J19	PC[11]	CTS1#, CLSN	Clear to send modem line for SCC1
K19	PC[10]	CD1#, RENA	Carrier detect modem line for SCC1
U18	PB[14]	RSTRT1#	Serial CAM Interface output signals that marks start of a frame
L19, K17	PB[22],PB[23]	SDACK2-1	SDMA acknowledge 2-1 (Ethernet CAM interface signal)
K3, J1, J2, H1	IP_B[6], ALE_B, IP_B[2], IP_B[7]	AT0-AT3	Address type 0-3; 1 = CPM transaction initiator, 0 = CPU transaction initiator
C17	PB[31]	REJECT1	SCC1 CAM interface reject pin

Table 6-5. I^2C

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
E19	PB[27]	I^2C SDA	I^2C serial data pin
F19	PB[26]	I^2C SCL	I^2C serial clock pin
M17	PA[6]	BRGLCK1	BRGs external clock inputs

Table 6-6. Centronic Transmitter

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
U18, R17, N16, P18, N17, N19, L16, K16, L19, K17, J18, J16, F19, E19, D19, E16, C19, C17	PB[14:31]	PB[14:31]	General Purpose I/O Port B bits [14:31]

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6.2 SCC2

Table 6-7. UART

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
K16	PB[21]	TXD2	Transmit data output for SCC2
L16	PB[20]	RXD2	Receive data input for SCC2
D18	PC[14]	RTS2#	Request to send modem line for SCC2
L18	PC[9]	CTS2#	Clear to send modem line for SCC2
M18	PC[8]	CD2#	Carrier detect modem line for SCC2

Table 6-8. HDLC

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
K16	PB[21]	TXD2	Transmit data output for SCC2
L16	PB[20]	RXD2	Receive data input for SCC2
D18	PC[14]	RTS2#	Request to send modem line for SCC2
L18	PC[9]	CTS2#	Clear to send modem line for SCC2
M18	PC[8]	CD2#	Carrier detect modem line for SCC2
M17	PA[6]	CLK2	Input clock for SCC

Table 6-9. Transparent Controller

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
K16	PB[21]	TXD2	Transmit data output for SCC2
L16	PB[20]	RXD2	Receive data input for SCC2
D18	PC[14]	RTS2#	Request to send modem line for SCC2
L18	PC[9]	CTS2#	Clear to send modem line for SCC2
M18	PC[8]	CD2#	Carrier detect modem line for SCC2
M17	PA[6]	CLK2	Input clock for SCC
F19	PB[26]	BRG02	BRG2 output clock

***Note**: No RSTRT# support.*

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6.3 SCC3

Table 6-10. UART

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
W18	PD[10]	TXD3	Transmit data output for SCC3
T16	PC[11]	RXD3	Receive data input for SCC3
T15	PD[7]	RTS3#	Request to send modem line for SCC3
M16	PC[7]	CTS3#	Clear to send modem line for SCC3
R19	PC[6]	CD3#	Carrier detect modem line for SCC3

Table 6-11. HDLC

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
W18	PD[10]	TXD3	Transmit data output for SCC3
T16	PC[11]	RXD3	Receive data input for SCC3
T15	PD[7]	RTS3#	Request to send modem line for SCC3
M16	PC[7]	CTS3#	Clear to send modem line for SCC3
R19	PC[6]	CD3#	Carrier detect modem line for SCC3
M18	PC[8]	CLK3	Clock for SCC

Table 6-12. Transparent Controller

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
W18	PD[10]	TXD3	Transmit data output for SCC3
T16	PC[11]	RXD3	Receive data input for SCC3
T15	PD[7]	RTS3#	Request to send modem line for SCC3
M16	PC[7]	CTS3#	Clear to send modem line for SCC3
R19	PC[6]	CD3#	Carrier detect modem line for SCC3
M18	PC[8]	CLK3	Clock for SCC
R17	PB[15]	BRGOUT3	Output clock for BRG3

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6.4 SCC4

Table 6-13. UART

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
W17	PD[8]	TXD4	Transmit data output for SCC4
V17	PD[9]	RXD4	Receive data input for SCC4
V16	PD[6]	RTS4#	Request to send modem line for SCC4
T18	PC[5]	CTS4#	Clear to send modem line for SCC4
T17	PC[4]	CD4#	Carrier detect modem line for SCC4

Table 6-14. HDLC

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
W17	PD[8]	TXD4	Transmit data output for SCC4
V17	PD[9]	RXD4	Receive data input for SCC4
V16	PD[6]	RTS4#	Request to send modem line for SCC4
T18	PC[5]	CTS4#	Clear to send modem line for SCC4
T17	PC[4]	CD4#	Carrier detect modem line for SCC4
P19	PA[4]	CLK4	Clock for SCC

Table 6-15. Transparent Controller

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
W17	PD[8]	TXD4	Transmit data output for SCC4
V17	PD[9]	RXD4	Receive data input for SCC4
V16	PD[6]	RTS4#	Request to send modem line for SCC4
T18	PC[5]	CTS4#	Clear to send modem line for SCC4
T17	PC[4]	CD4#	Carrier detect modem line for SCC4
D19	PB[28]	BRGO4	BRG4 output clock

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6.5 MISC

Table 6-16. SI with TDM (Time Slot Assignor)

MPC860 Pin #	POM2 Signal Name	Signal Name	Description
T17	PC[4]	L1RSYNCA	Receive sync input for serial interface TDM Port A
U17	PD[15]	L1TSYNCA	Input transmit data sync to TDM Channel A
R16	PD[12]	L1RSYNCB	Receive sync input for serial interface TDM Port B
V18	PD[13]	L1TSYNCB	Input transmit data sync to TDM Channel B

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7. Customer Support

Prior to contacting PLX Customer Support, please be situated close to the computer in which the RDK board is installed and be prepared to provide the following information:

- Evaluation board serial number
- PLX PCI RDK board model number
- PLX PCI SDK version
- Operating System version and type
- Description of intended design:
  - PLX PCI chip
  - Processor
  - Local Operating System and version (if any)
  - I/O
- Description of problem and steps to recreate the problem (if reporting a problem)

You may contact PLX Customer Support at:

Address PLX Technology, Inc.

Attn: Customer Support
870 Maude Ave
Sunnyvale, CA 94085

Phone 408-774-9060
800-759-3735
Fax 408-774-2169
Website http://www.plxtech.com

For technical support on the Web, go to http://www.plxtech.com/support/.

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8. References

1. PLX Technology, Inc., *PCI 9054 Data Book,* http://www.plxtech.com

2. Motorola, *MPC860 Data Book*

3. PCI SIG, *PCI Specification Rev. 2.1 and 2.2*

4. Motorola, *SDRAM Data Sheet*

5. I_2O Special Interest Group, *Intelligent I/O (I_2O) Architecture Specification Revision 1.5*

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9. Bill of Materials & Schematics

PLX Part #: 91-0002-300-A

Table 9-1. BOM – Components Should be Assembled

Item#	Qty	Manufacture	Manufacture Part Number	Description	Package Type	Source	Part Reference
3	43	Kemet	C0805C104M5UAC	0.1uF, 50V 20% Capacitor	SMT, 0805	Electrosonic	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C13 C14 C15 C16 C18 C19 C20 C21 C22 C23 C24 C25 C26 C34 C45 C48 C54 C55 C56 C57 C58 C59 C61 C63 C65 C67 C70 C71 C73 C75 C77 C81
4	11	Panasonic	ECS-T1DC106R	10uF, 20V Tantalum Capacitor	SMT, C Case	Newark	C12 C46 C47 C49 C50 C51 C52 C53 C68 C69 C79
5	1	Panasonic	ECJ-2VC1H151J	150pF, 50V 5% Capacitor	SMT, 0805	Electrosonic	C17
6	9	Kemet	C0805C103M5UAC	0.01uF, 50V 20% Capacitor	SMT, 0805	Electrosonic	C27 C60 C62 C64 C66 C72 C74 C76 C78
7	1	Panasonic	ECU-V1H100JCN	10pF, 50V 5% Capacitor	SMT, 0805	Digikey	C28
9	4	Kemet	T491A104K035AS	0.1uF, 35V Tantalum Capacitor	SMT, A Case	Electrosonic	C80 C82 C83 C84
10	1	Agilent Tech.	HSMG-C650	GREEN_LED	SMT	Newark	D1
11	1	Agilent Tech.	HSMS-C650	RED_LED	SMT	Newark	D2
18	1	Molex	15-91-1062	6-Pin header, 3x2 Dual-Row .1",unshrouded header	SMT	FAI	J1
20	1	Molex	15-91-1102	10-Pin header, 5x2 Dual-Row .1", unshrouded header	SMT	FAI	J3
21	1	N/A	N/A	32-bit PCI, Universal Card Edge Connector	N/A		J6
22	1	AMP	1-104652-0	100-Pin Female Squall Connector, 50x2 Dual row	SMT	Digikey	J7
23	2	Molex	15-91-1722	72-Pin header, 36x2 Dual row .1", Unshrouded Header	SMT	FAI	J8 J9
29	43	CTS	742C-08-3-103J	10K Ohm Isolated resistor network	SMT, 0603X4	Digikey	RN1 RN2 RN3 RN4 RN5 RN6 RN7 RN8 RN9 RN10 RN11 RN12 RN17 RN18 RN19 RN20 RN21 RN22 RN23 RN24 RN25 RN26 RN27 RN28 RN29 RN30 RN31 RN32 RN33 RN34 RN35 RN36 RN37 RN38 RN39 RN40 RN41 RN42 RN43 RN44 RN45 RN46 RN47

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Item#	Qty	Manufacture	Manufacture Part Number	Description	Package Type	Source	Part Reference
30	24	Philips	RC11J10K0	10K Ohm, 1/10W, 5% Resistor	SMT, 0805	Electrosonic	R1 R2 R3 R4 R6 R9 R11 R12 R13 R36 R37 R38 R42 R45 R55 R56 R57 R58 R59 R64 R66 R70 R72 R74
31	7	Philips	RC11J1K00	1K Ohm, 1/10W, 5% Resistor	SMT, 0805	Electrosonic	R7 R8 R10 R41 R79 R81 R82
32	10	Philips	RC11J22R1	22 Ohm, 1/10W, 5% Resistor	SMT, 0805	Electrosonic	R14 R15 R17 R18 R19 R21 R22 R24 R68 R69
33	7	Vishay	WSL1206R010FRE4	0 Ohm, 1/4W, 1% Resistor	SMT, 1206	Newark	R16 R48 R51 R54 R61 R63 R76
34	5	Philips	RC11J33R	33 Ohm, 1/10W, 5% Resistor	SMT, 0805	Electrosonic	R20 R23 R26 R27 R28
36	3	Philips	RC11J110R	110 Ohm, 1/10W, 5% Resistor	SMT, 0805	Electrosonic	R44 R46 R49
37	1	Philips	RC11J180R	180 Ohm, 1/10W, 5% Resistor	SMT, 0805	Electrosonic	R50
38	2	Panasonic	ERJ-6GEYJ392V	3.9K Ohm, 1/10W, 5% Resistor	SMT, 0805	Digikey	R80 R83
40	1	Omron	B3S-1002	Tactile Pushbutton Switch	SMT, 4 Pin, 4.2x9.0mmm	Digikey	SW1
43	1	PLX	PCI 9054-AC50PI	PLX PCI9054 Bridge Chip	PQFP-176 Pin	PLX	U1
45	1	Motorola	XPC860MHZP50C1	Motorola MPC860 50Mhz	BGA-357 Pin	FAI	U3
46	1	MTRON	M213TAN50.00	50.00 Mhz Osc, 3.3V	SMT, 4 pin lead	FAI	U4
47	4	Samsung	K4S640832D-TC10	2MegX8X4banks 10ns SDRAM	TSOP-54 Pin		U5 U6 U7 U8
48	1	Cypress	CY2305SC-1	3.3V Zero delay buffer	SOIC-8 Pin	Cypress	U9
49	1	Augat	PCS-032SMU-11	32 Pin PLCC socket	PLCC-32 Pin	Electrosonic	U10
50	1	Maxim	MAX6306UK30D1-T	3.3V Programmable reset device	SOT23-5	Newark	U20
51	3	Fairchild	NC7SZD384P5	1-bit Bus switch	SC70-5	Digikey	U24 U25 U26
52	1	Linear Tech.	LT1587CM	3A Adjustable Voltage Regulator	3 Pin Lead DD PAK	Electrosonic	U27
53	1	Maxim	MAX3245CAI	RS-232 Transceiver	SSOP-28 Pin	Digikey	U28
54	3	Fairchild	74LCX257MTC	Quad 2-input Multiplexer	TSSOP-16 Pin	Digikey	U31 U32 U 33
55	1	Fairchild	74LCX245MTC	Bus Transceiver	TSSOP-20 Pin	Digikey	U34
56	1	PLX	90-0002-300-A	PCB, PCI9054RDK-860 (Use schematic 91-0002-300-A Rev 300)			

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Table 9-2. BOM – Through Hole Components

Item#	Qty	Manufacture	Manufacture Part Number	Description	Package Type	Source	Part Reference
19	1	Leoco	2556P06TA00	6-Pin header, 6x1 Single-Row .1", unshrouded header	Thru hole	Prolex	J2
24	1	Toko	262LY-822K	30mA Inductor, 8RBS Low Profile	Thru hole	Digikey	L1
26	1	SPC	DE-9P-FRS	DE-9 Male PCB mount RS232 connector	Thru hole	Newark	P1
44	1	SPC	MPSL-08T	8 Pin DIP Socket, 300 mil	Thru hole	Newark	U2

Table 9-3. BOM – Manually Inserted Components

Item#	Qty	Manufacture	Manufacture Part Number	Description	Package Type	Source	Part Reference
27	1	Microchip	93LC56B	2K Serial EEPROM	DIP-8 Pin	Newark	P2
28	1	Atmel	AT29LV040-12JC	512K X 8, 120ns, 3.3V Flash Memory	PLCC-32 Pin	Newark	P3

Table 9-4. BOM – Miscellaneous Components

Item#	Qty	Manufacture	Manufacture Part Number	Description	Package Type	Source	Part Reference
1	1	Velostat	2100R/7X15	7" X 15" Antistatic Bag	N/A	FAI	BAG1
2	1			Serial cable, 25 pin Female to 9 pin Female (null modem)	N/A		CABLE1
25	1			PCI 9054RDK-860 PCB Bracket	N/A	DTI	Panel1
39	2	Philips	501-002	Panel screws	N/A	Spaenaur	SCREW1, SCREW2

Table 9-5. BOM – Components Should Not Be Assembled

Item#	Qty	Manufacture	Manufacture Part Number	Description	Package Type	Source	Part Reference
8	5	Panasonic	ECU-V1H220JCN	22pF, 50V 5% Capacitor	SMT, 0805	Digikey	C29 C30 C31 C32 C33
30	1	Philips	C11J10K0	10K Ohm, 1/10W, 5% Resistor	SMT, 0805	Electrosonic	R40
31	9	Philips	RC11J1K00	1K Ohm, 1/10W, 5% Resistor	SMT, 0805	Electrosonic	R5 R39 R43 R65 R67 R71 R73 R75 R78
33	7	Vishay	WSL1206R010FRE4	0 Ohm, 1/4W, 1% Resistor	SMT, 1206	Newark	R25 R47 R52 R53 R60 R62 R77
35	5	Philips	RC11J51R	51 Ohm, 1/10W, 5% Resistor	SMT, 0805	Electrosonic	R29 R30 R31 R32 R33

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The following are the PCI 9054RDK-860 circuit board schematics.

Note: *"Page 5 of 11" of the schematics is intentionally omitted.*

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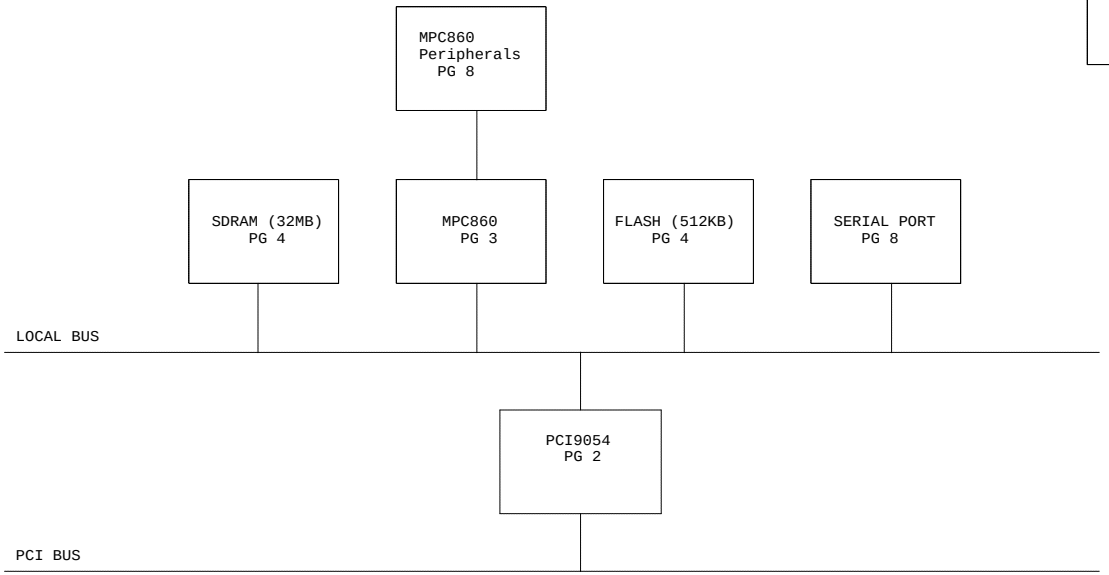
PCI9054RDK-860 BLOCK DIAGRAM

ECN HISTORY

ECN NUMBER	DATE	NOTE
xxx-xxx	04/30/98	1. BDM signals added: R60, R61, R62, and R63 to include VFLS[1:0] and FRZ to the BDM connector. 2. Added pull up to D11 and D12: R64, R65, R66, R67, U29, and U30.
xxx-xxx	06/22/98	1. SDRAM: added ADDR MUX(U31,U32,U33): Changed MA[0:11] to SDRAM, Added R68 and R69 for A7 and A8. Changed WE#(GPL_A1#). 2. FLASH: Added 3.3V or 5V(VCC) PS Option. Changed WE#(BS_B0#). 3. SRAM: added BDIP# signal to the glue. 4. Power UP config: added D7,D9,D10 (U34,U35,U36) for the power up configurations. 5. Changed the PU/PD (R)s for the Power Up Configurations. 6. Added PU/PD (R)s for the MPC860 JTAG Port.
xxx-xxx	07/02/98	Added R78 & R79 (Wait control input to UPM)
xxx-xxx	08/08/98	1. Removed SRAM: Lattice and SRAMs. 2. Changed R5 to 1K (EEDI/O pull down R). 3. Added Pull-Up Resistor(510 ohm) for BB#. 4. Added Pull-Down Resistor for TCK and TRST#(1K ohm). 5. Fixed SDRAM address MUX unit.
xxx-xxx	08/21/98	1. TSIZ0 (pin 92) and TSIZ1 (pin 91) were swapped.
xxx-xxx	6/25/02	1. Correct pull-up resistor at U1-166. It was R81, now is R83 2. Update BOM to reflect PCB board Rev 90-0002-300-A, and Document Number

NOTE: (otherwise specified)
1. All resistors are EIA case style 0805, 5% tolerance.
2. All .1uF caps are EIA case style 0805, 10% tolerance.
3. All 0K0 resistors are 1210 type and less than 0.01 ohms

(*** indicates default, do not install other)

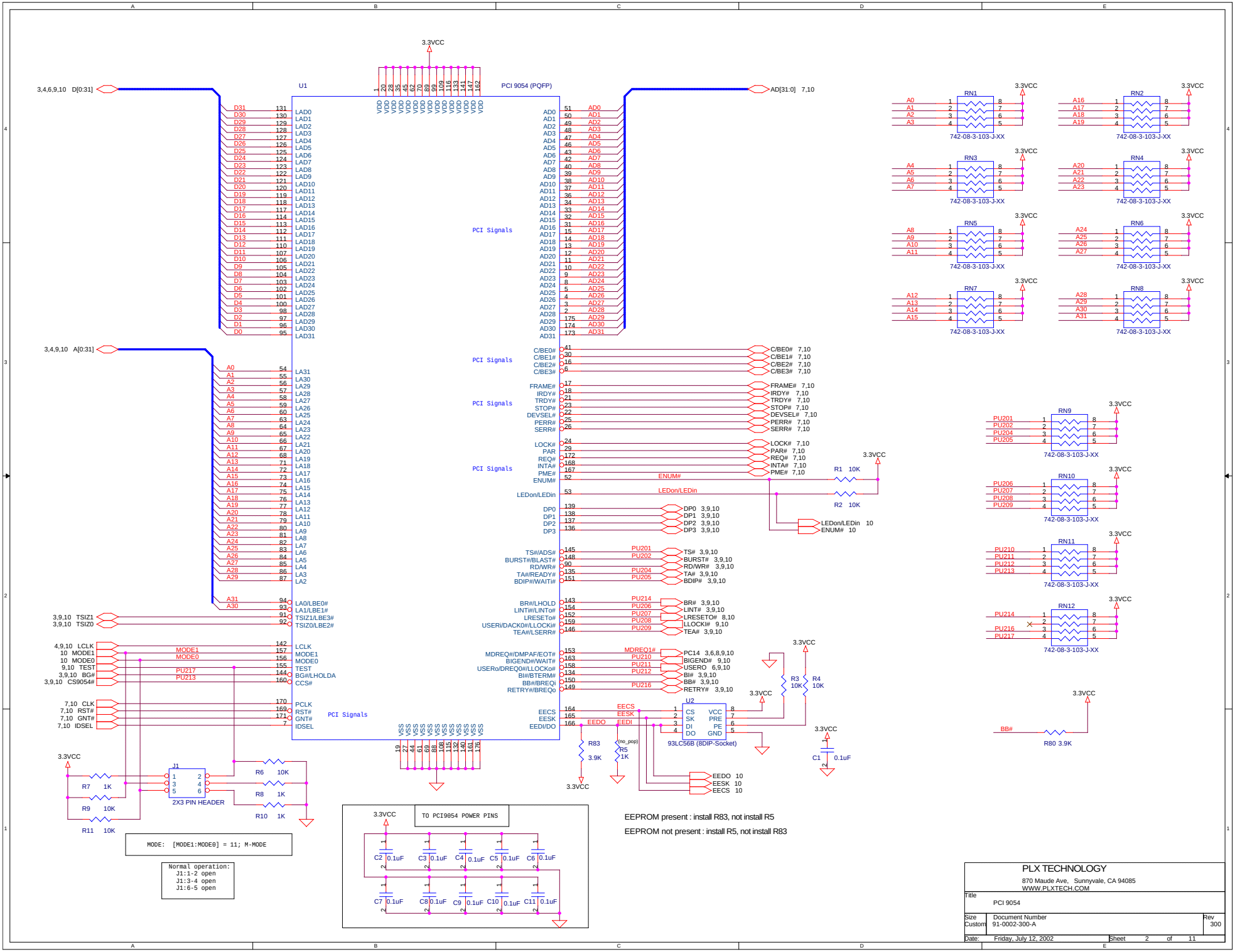


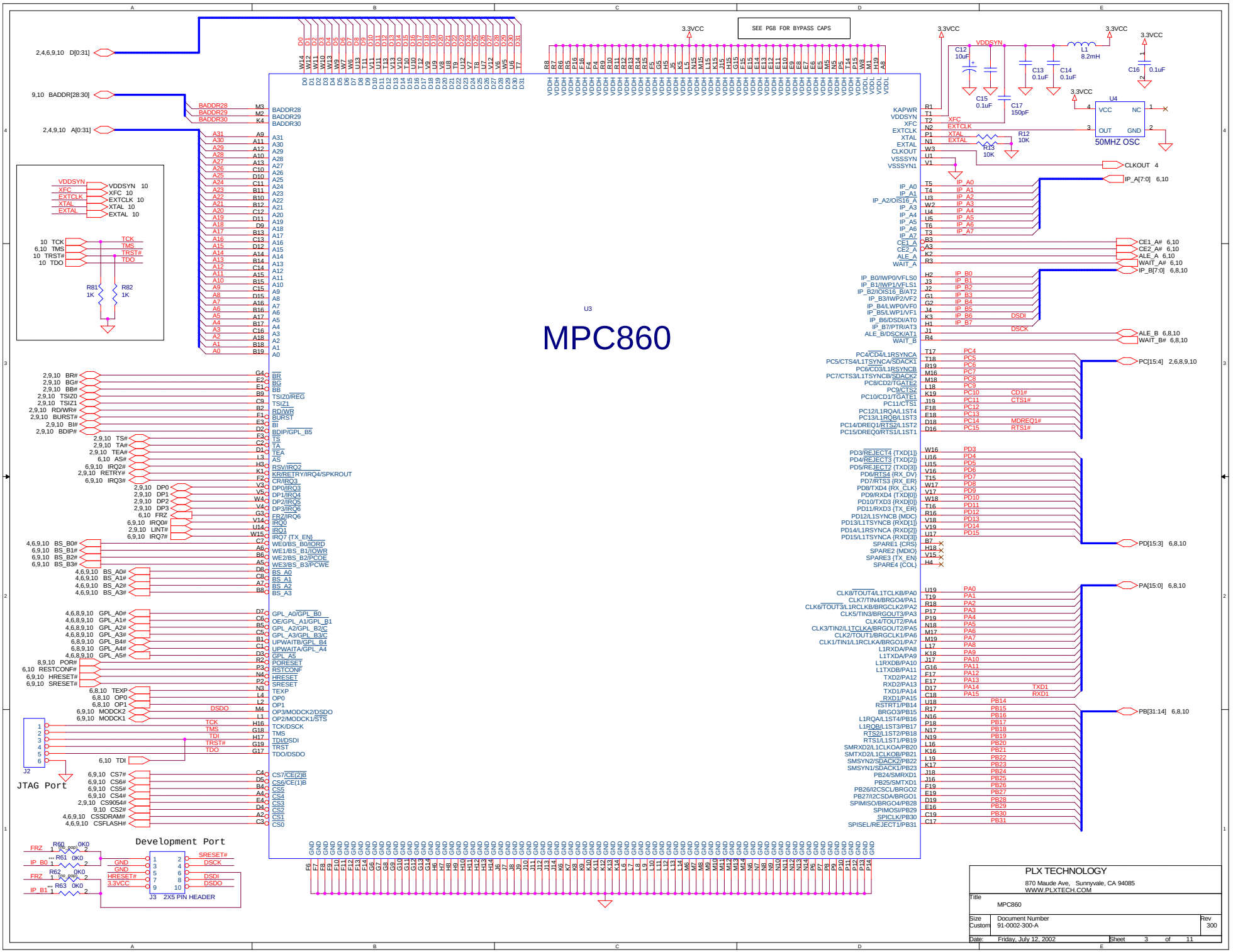
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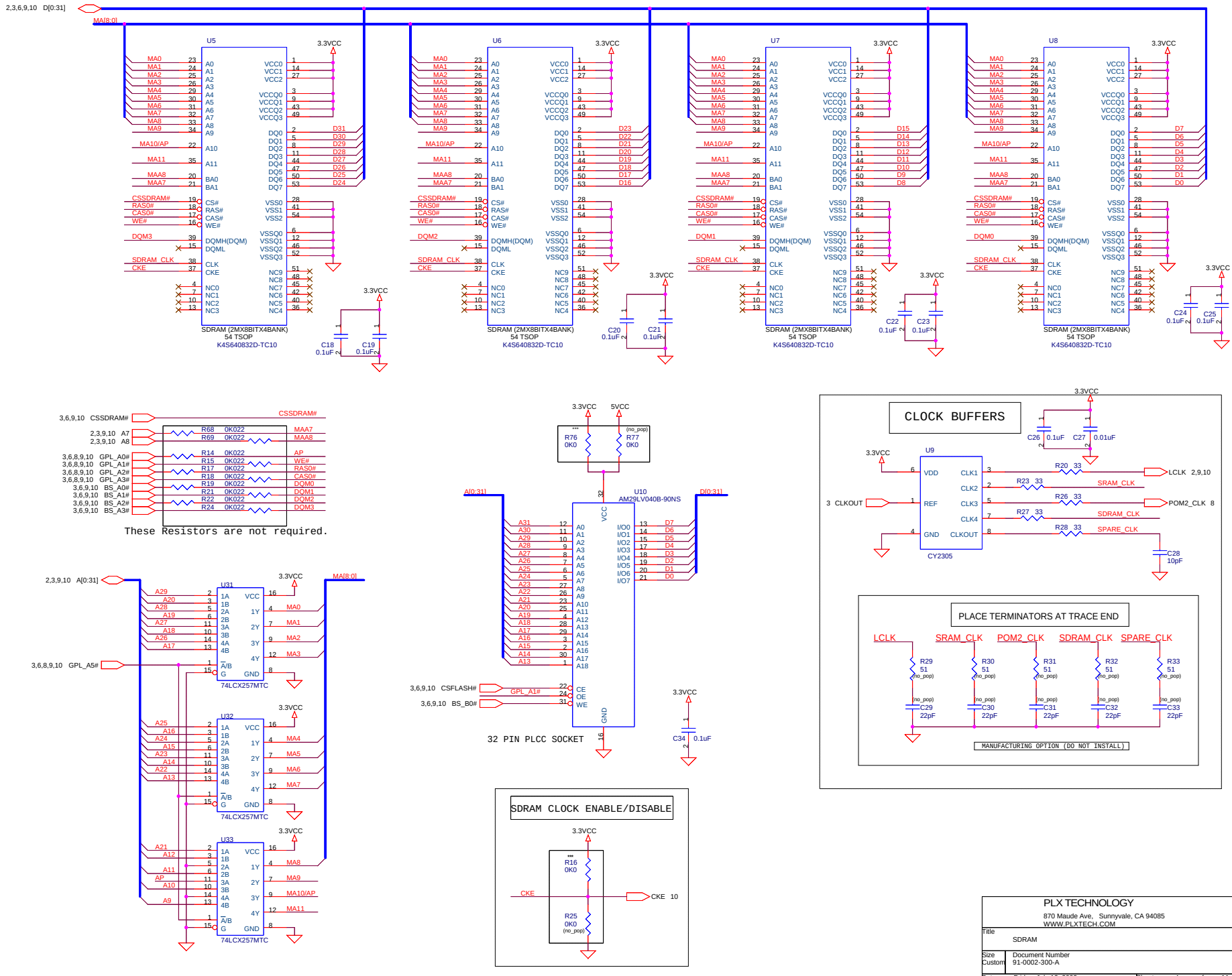
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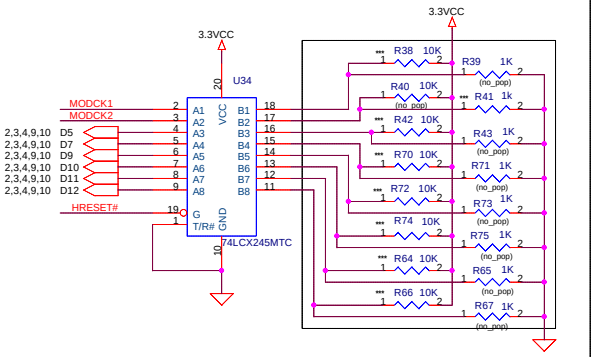

U1
PCI 9054 (PQFP)
3.3VCC
3,4,6,9,10 D[0:31]
AD[31:0] 7,10
3,4,9,10 A[0:31]
PCI Signals
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
LAD8
LAD9
LAD10
LAD11
LAD12
LAD13
LAD14
LAD15
LAD16
LAD17
LAD18
LAD19
LAD20
LAD21
LAD22
LAD23
LAD24
LAD25
LAD26
LAD27
LAD28
LAD29
LAD30
LAD31
LA31
LA30
LA29
LA28
LA27
LA26
LA25
LA24
LA23
LA22
LA21
LA20
LA19
LA18
LA17
LA16
LA15
LA14
LA13
LA12
LA11
LA10
LA9
LA8
LA7
LA6
LA5
LA4
LA3
LA2
LA0/LBE0#
LA1/LBE1#
TSIZ1/LBE3#
TSIZ0/LBE2#
LCLK
MODE1
MODE0
TEST
BG#/LHOLDA
CCS#
PCLK
RST#
GNT#
IDSEL
C/BE0#
C/BE1#
C/BE2#
C/BE3#
FRAME#
IRDY#
TRDY#
STOP#
DEVSEL#
PERR#
SERR#
LOCK#
PAR
REQ#
INTA#
PME#
ENUM#
LEDon/LEDin
DP0
DP1
DP2
DP3
TS#/ADS#
BURST#/BLAST#
RD/WR#
TA#/READY#
BDIP#/WAIT#
BR#/LHOLD
LINT#/LINTo#
LRESETo#
USERi/DACK0#/LLOCKi#
TEA#/LSERR#
MDREQ#/DMPAF/EOT#
BIGEND#/WAIT#
USERo/DREQ0#/LLOCKo#
BI#/BTERM#
BB#/BREQi
RETRY#/BREQo
EECS
EESK
EEDI/DO
VSS
VDD
RN1
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
RN11
RN12
742-08-3-103-J-XX
R1 10K
R2 10K
R3 10K
R4 10K
R5 1K
R6 10K
R7 1K
R8 1K
R9 10K
R10 1K
R11 10K
R80 3.9K
R83 3.9K
C1 0.1uF
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
U2
93LC56B (8DIP-Socket)
CS
SK
DI
DO
VCC
PRE
PE
GND
J1
2X3 PIN HEADER
(no_pop)
TO PCI9054 POWER PINS
MODE: [MODE1:MODE0] = 11; M-MODE
Normal operation:
J1:1-2 open
J1:3-4 open
J1:6-5 open
EEPROM present : install R83, not install R5
EEPROM not present : install R5, not install R83
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11


MPC860
U3
SEE PG8 FOR BYPASS CAPS
3.3VCC
JTAG Port
J2
Development Port
J3 2X5 PIN HEADER
50MHZ OSC
U4
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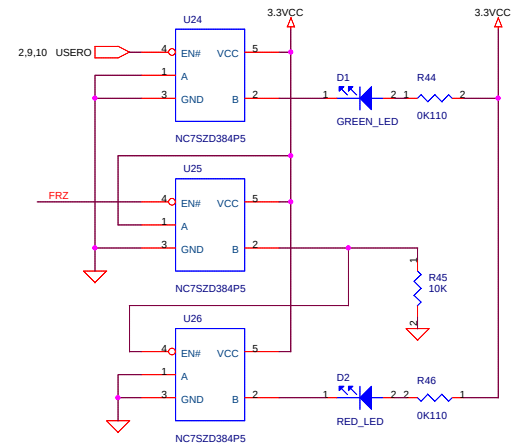

2,3,6,9,10 D[0:31]
MA[8:0]
U5
U6
U7
U8
3.3VCC
SDRAM (2MX8BITX4BANK)
54 TSOP
K4S640832D-TC10
C18 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 0.1uF
C23 0.1uF
C24 0.1uF
C25 0.1uF
3,6,9,10 CSSDRAM#
2,3,9,10 A7
2,3,9,10 A8
3,6,8,9,10 GPL_A0#
3,6,8,9,10 GPL_A1#
3,6,8,9,10 GPL_A2#
3,6,8,9,10 GPL_A3#
3,6,9,10 BS_A0#
3,6,9,10 BS_A1#
3,6,9,10 BS_A2#
3,6,9,10 BS_A3#
These Resistors are not required.
5VCC
U10
AM29LV040B-90NS
32 PIN PLCC SOCKET
3,6,9,10 CSFLASH#
3,6,9,10 BS_B0#
GPL_A1#
2,3,9,10 A[0:31]
3,6,8,9,10 GPL_A5#
U31
U32
U33
74LCX257MTC
SDRAM CLOCK ENABLE/DISABLE
CKE
CKE 10
CLOCK BUFFERS
U9
CY2305
3 CLKOUT
LCLK 2,9,10
POM2_CLK 8
SRAM_CLK
SDRAM_CLK
SPARE_CLK
PLACE TERMINATORS AT TRACE END
LCLK
SRAM_CLK
POM2_CLK
SDRAM_CLK
SPARE_CLK
MANUFACTURING OPTION (DO NOT INSTALL)
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Power Up Configuration

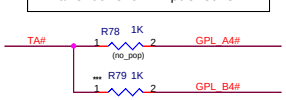
OSC (f)	MODCK1	MODCK2
4Mhz OSC	1	1
50Mhz OSC	1	0

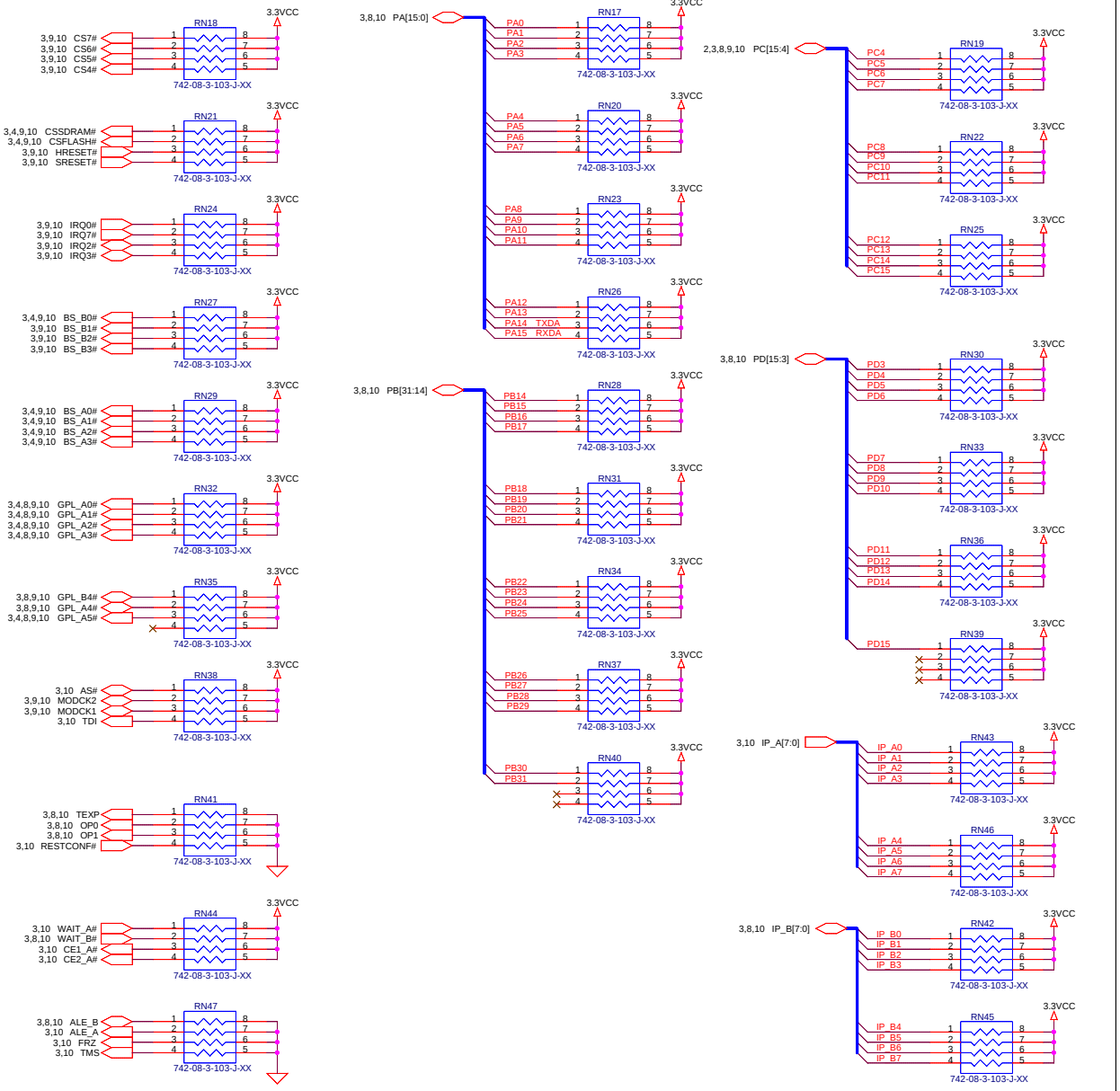


Indicator LEDs



Wait Control Input to UPM





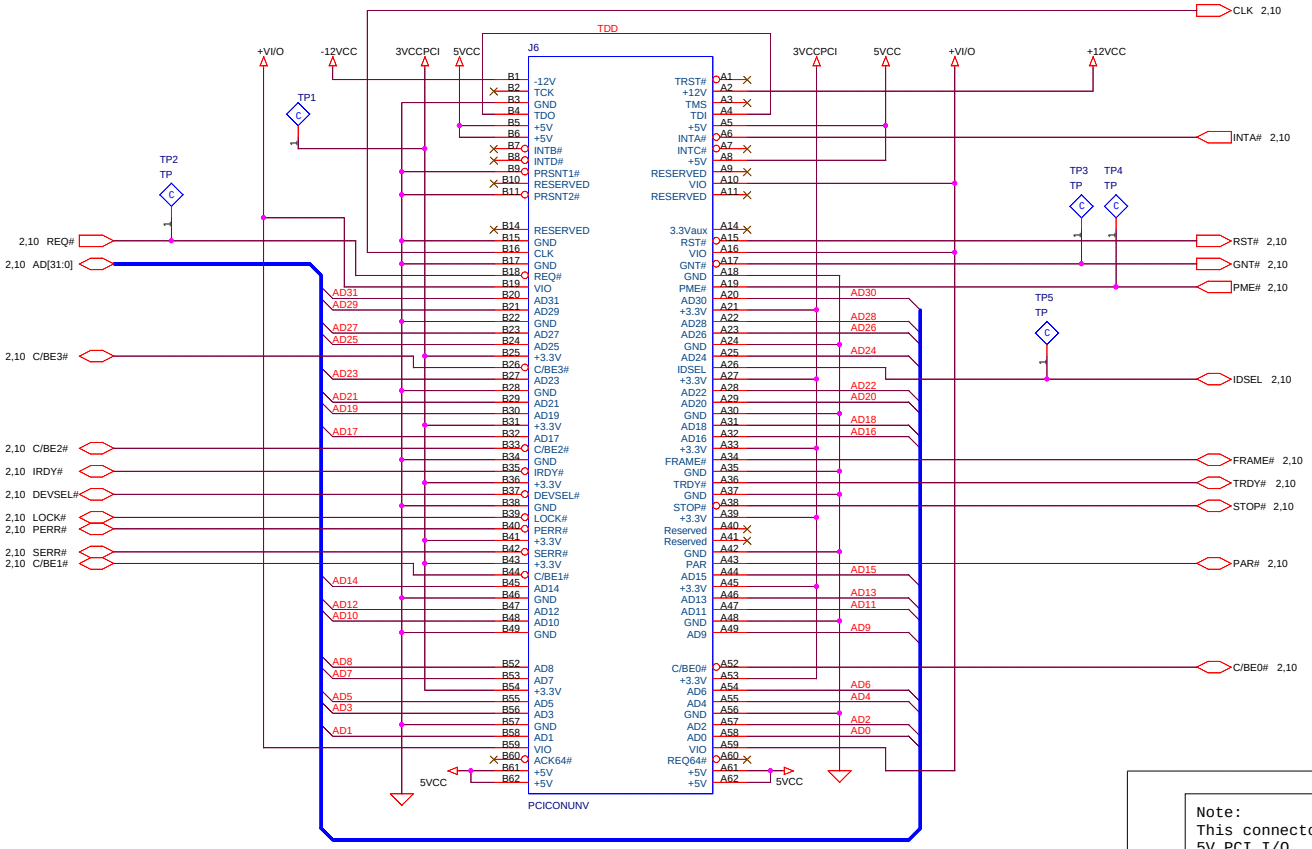
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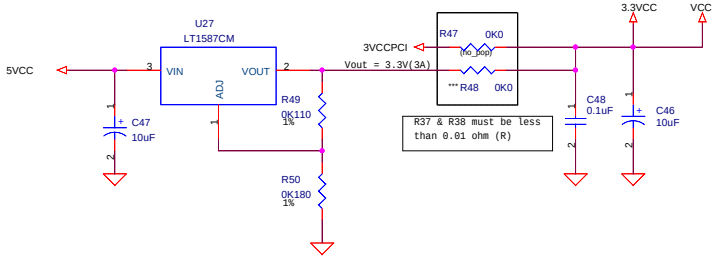
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PCI Edge Connector



Local Bus Power Source



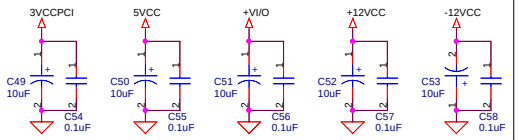
U27 option:
1. If LT1587CM (adjustable) is used, install R49 and R50 (default).
2. If LT1587CM-3.3 is used, do not install R49 and replace R50 with a jumper.

Local Bus 3.3VCC is selectable at manufacturing (R47 or R48):
Populate R47 if using 3.3V supply from the PCI connector
Populate R48 if using 3.3V supply from the Voltage regulator (default)

Note:
This connector is keyed for both 3.3V and 5V PCI I/O

Each power supply group pins must be tied together and have bypass capacitors (+5V, +12V,-12V, and +3.3V).

Each power group has .1uF and 10uF caps.

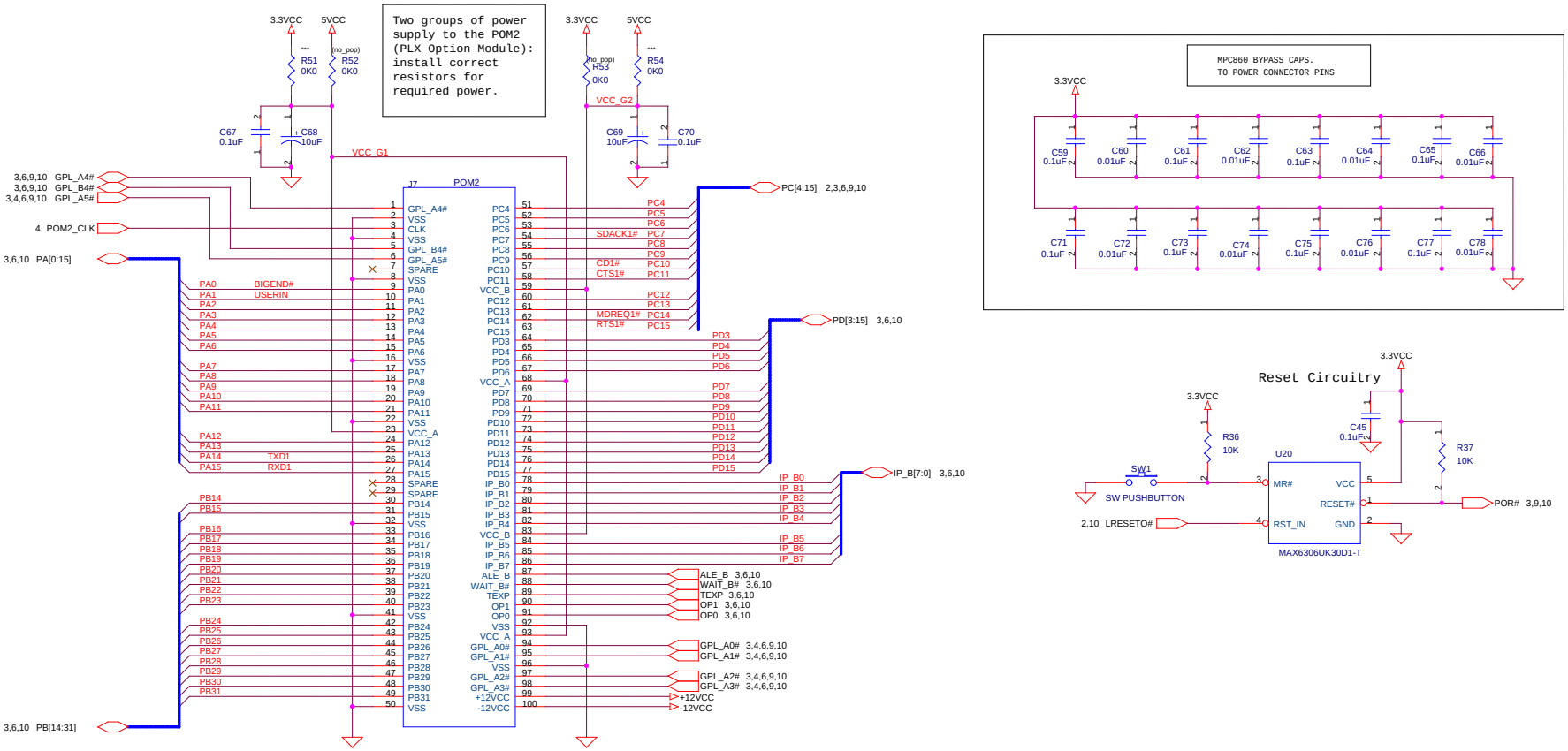


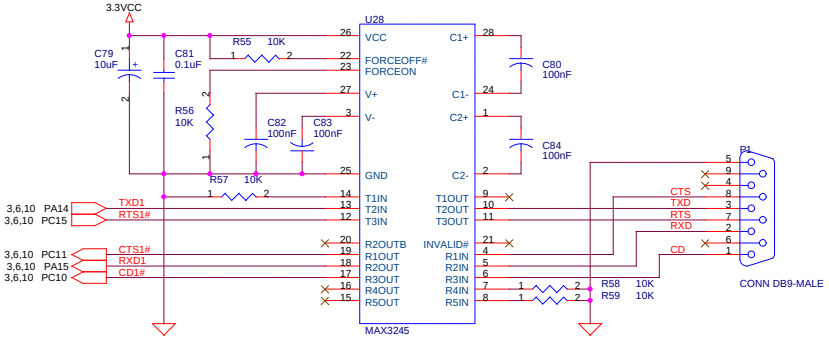
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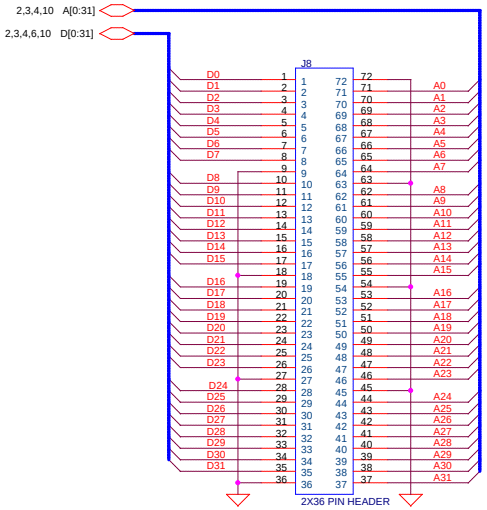
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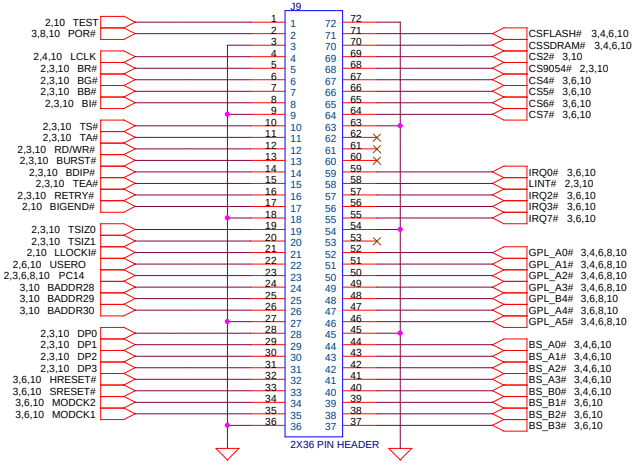
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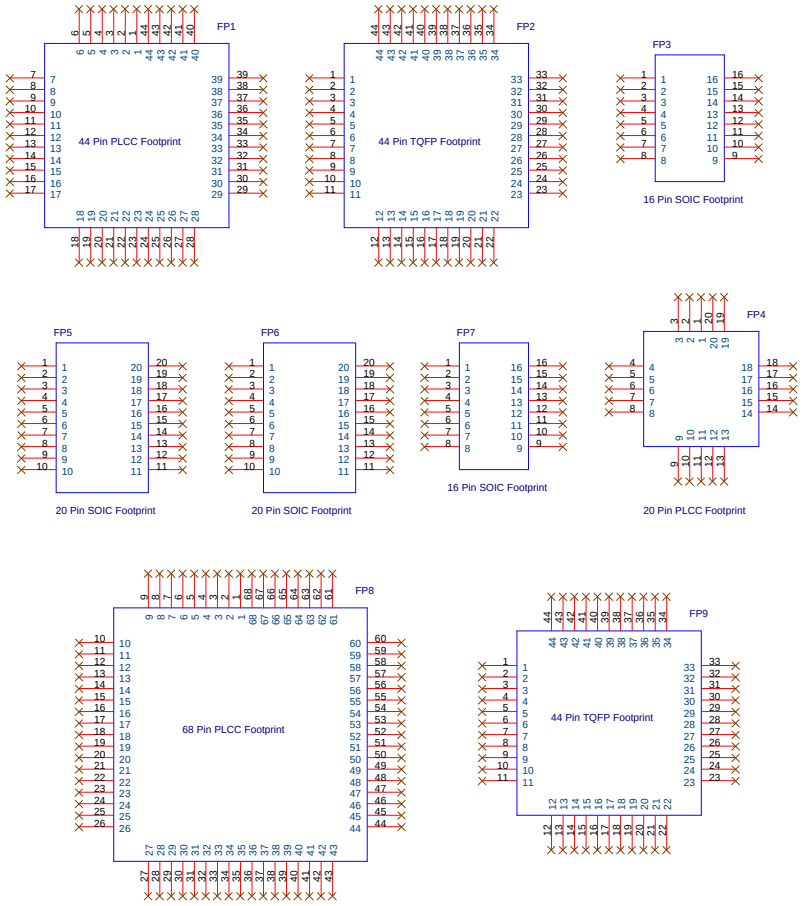
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Prototyping Footprints

Note: Place the 3 PLCC devices co-incident on the board; that is, they share common pins and the 20 fits inside the 44 which fits inside the 68.

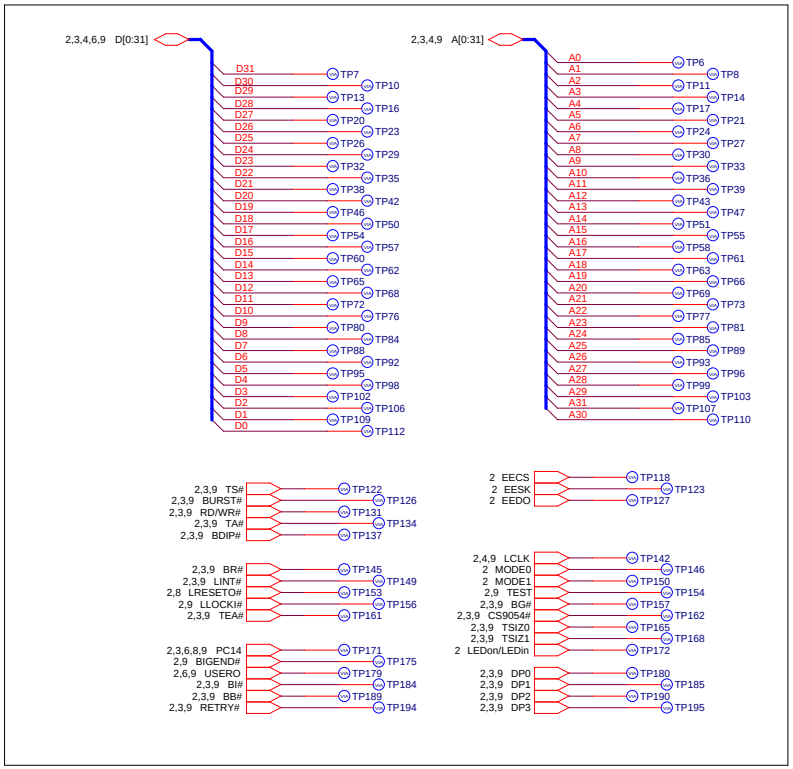


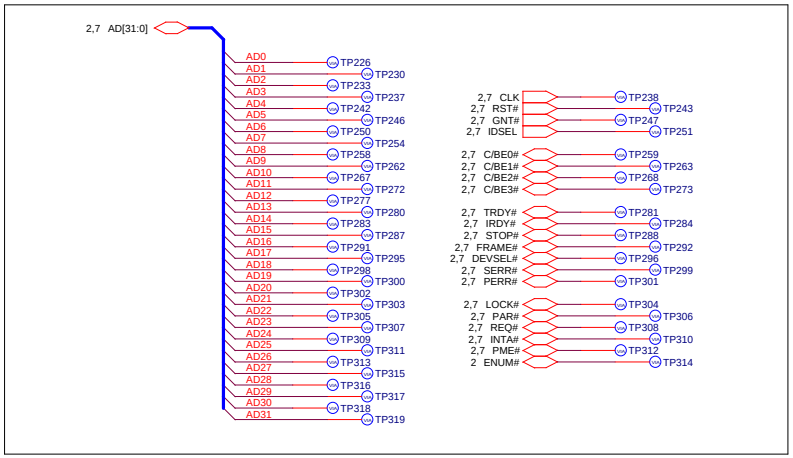
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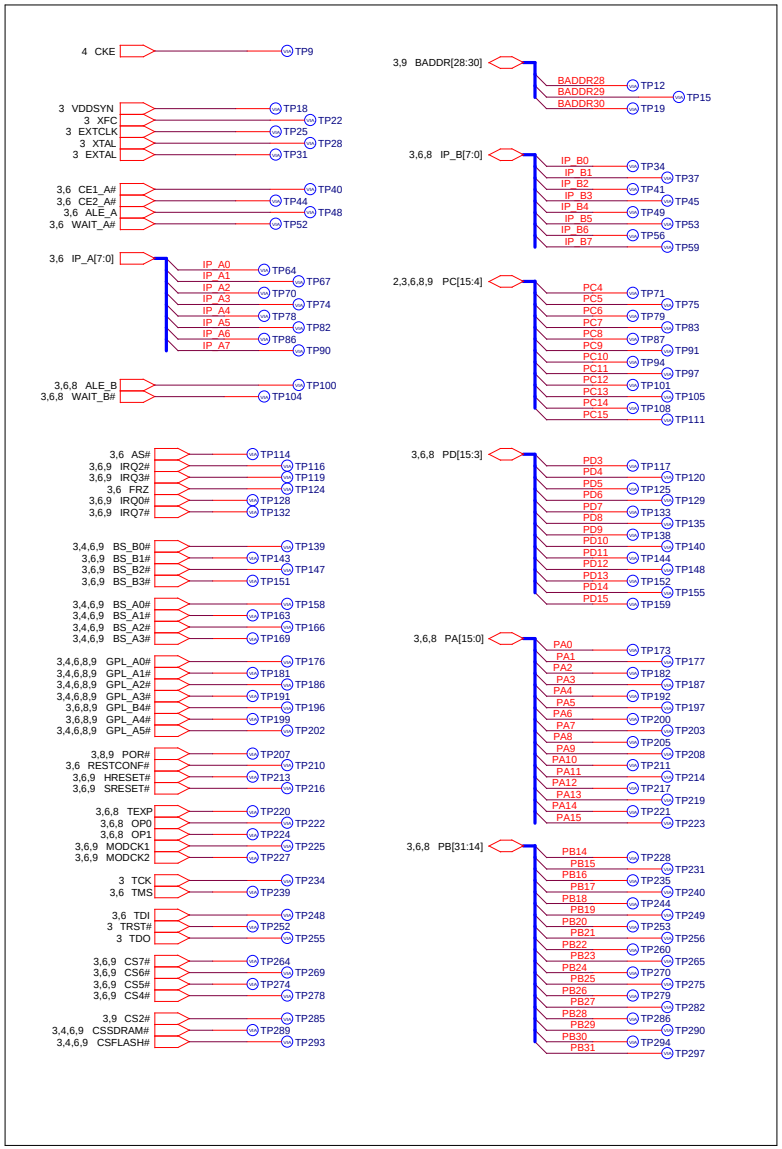
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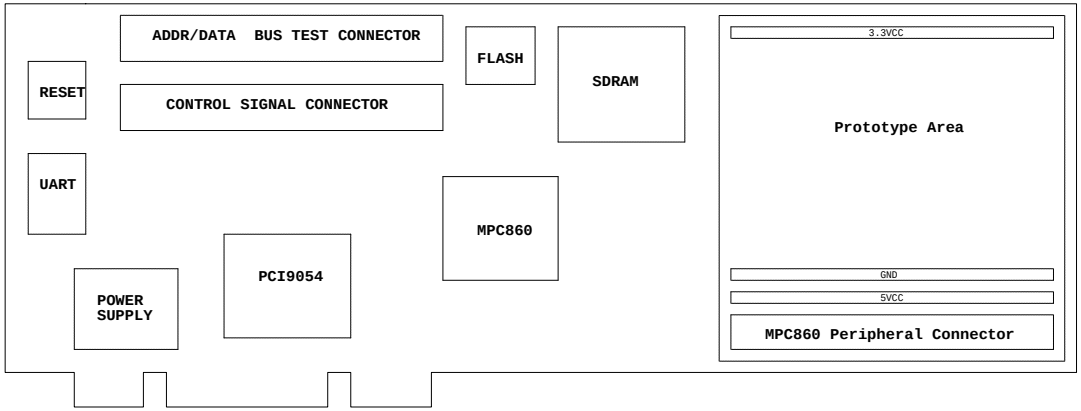
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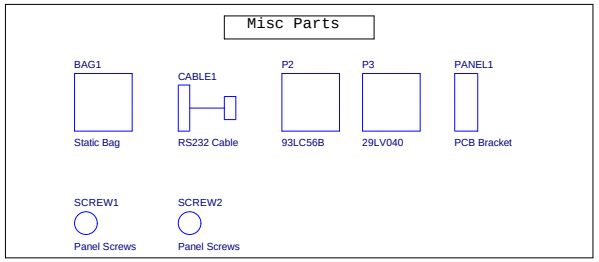
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Universal PCI Connector (3.3V/5V)



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