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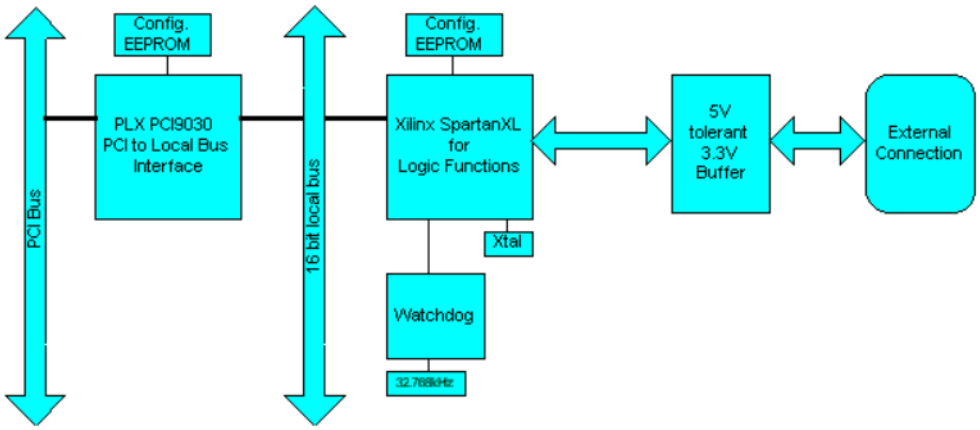
PMC DIO64 64-Bit Digital I/O Module

The PMC-DIO64 is a digital I/O PMC module providing 64 bits of programmable TTL level compatible I/O. A PLX PCI9030 device controls the PCI bus and a Xilinx SpartanXL is used to provide the on-board functionality. The external I/O connections are via 74ABT16245A devices providing 32/64mA source/sink capabilities and can be defined as input or output in blocks of 8 bits. The on-board watchdog has programmable timeout periods up to 2 seconds.

Key Features



- 64-bits of TTL level compatible I/O.
- I/O byte selectable as input or outputs.
- Inputs latched on 33MHz PCI clock.
- Interrupt on change-of-state.
- Change-of-state double-sampled on 33Mhz PCI clock.
- Watchdog period programmable 125ms to 2sec.
- Watchdog interrupt.
- Watchdog tri-states outputs.
- Front panel and rear I/O connections.
- Conforms to PMC standard IEEE P1386.1/Draft 2.3 9th October 2000.
- Conforms to PCI Local Bus Specification Revision 2.2.



Block Diagram

PCI Features

The PMCDIO64 uses a PLX PCI9030 PCI interface to a 16-bit local bus on-board. The general features of the PCI9030 are:

- PCI Local Bus Specification V2.2-compliant 32-bit, 33 MHz Bus Target Interface Device enabling PCI Burst Transfers up to 132 MB/s.
- PCI Bus Power Management Interface Specification V1.1 compliant.
- PCI Local Bus Specification V2.2 Vital Product Data (VPD) configuration support.
- PCI Target Programmable Burst Management.
- PCI Target Read Ahead mode.
- PCI Target Delayed Read mode.
- PCI Target Delayed Write mode.
- Programmable Interrupt Generator/Controller.
- Two programmable FIFOS for zero wait state burst operation.
- Flexible Local Bus provides 32-bit Multiplexed or Non-Multiplexed Protocol for 8, 16, or 32-bit Peripheral and Memory devices.
- Serial EEPROM interface.
- Nine programmable General Purpose I/O (GPIOS).
- Five programmable Local Address spaces.
- Four programmable independent chip selects.
- Programmable Local Bus wait states.
- Programmable Local Read pre-fetch mechanism.
- Local Bus can run asynchronously to the PCI Bus.
- Two programmable Local-to-PCI interrupts.
- Endian Byte Swapping.

Main Logic

The PMCDIO64 uses a Xilinx SpartanXL FPGA connected to the 16-bit local bus to provide the on-board logic functions as described below.

Input Register

A 64-bit Input Register containing a latched version of the I/O pins on the logic device. The signal is latched by the 33MHz PCI clock.

Output Register

A 64-bit Output Register whose contents are output to valid output pins.

Change Flags Register

A 64-bit Change Flags Register where each bit indicates an input that has changed state since interrupt on change-of-state was enabled.

Direction Register

An 8-bit Direction Register where each bit corresponds to a group of 8 I/O bits. If the corresponding bit is set to 1 output is enabled otherwise input is enabled.

Control and Status Register

A 16-bit Control & Status Register where the bits are used to control and monitor the status of the following functions.

- Watchdog Interrupt Control.
- Global Output Control.
- Watchdog Output Control.
- Watchdog Interrupt Status.
- Lock Inputs Control.
- Hold Outputs Control.
- Change-of-State Interrupt Control.
- Change-of-State Status.

Watchdog trigger Register

A 8-bit register which must be written alternately 0 and 1 within ± 25% of the watchdog refresh period.

Watchdog Timer Register

An 8-bit register defining the watchdog refresh period: 125ms; 250ms; 500ms; 1sec or 2sec.

Watchdog Status Register

An 8-bit register which indicates if the watchdog has timed out.

- PCI interface configuration.
- PCI Subsystem and Subsystem Vendor ID.
- BIOS configuration parameters.

I/O Interfaces

The 64-bits of I/O are connected to the outside world via 74ABT16245A buffer devices with 2 bytes per device with separate output enables. These buffer devices have a 32mA source capability or 64mA sink capability when connected to outside signals. The I/O signals may be biased with 10KW pull-up resistors on a per byte basis.

93CS56 EEPROM

The PMCDIO64 is fitted with a 93CS56 EEPROM which is supplied pre-programmed by BVM. The contents of this EEPROM are read by the PCI9030 on coming out of reset and are used to set up the control registers after reset, configuring the PCI interface configuration, PCI Device/Vendor ID's & various other board specific parameters.

18V256 EEPROM

The PMCDIO64 is fitted with a 18V256 EEPROM, which is supplied pre-programmed by BVM. The contents of this EEPROM are read by the SpartanXL FPGA on power up and are used to initialise the logic functions in the FPGA.

Specification

On-Board Functions

PCI9030 PCI Interface

PCI 2.2 compliant 32-bit, 33-MHz Bus Target Interface Device
PCI Target Delayed Read mode disabled
PCI Target Delayed Write mode disabled
Programmable Interrupt Generator
Local Bus provides 32-bit non-multiplexed 16-bit peripheral access

Local Bus zero wait state
Programmable Local-to-PCI interrupt

SpartanXL FPGA

Input Register
Output Register
Change Flags Register
Direction Register
Function Register
Status & Control Register
Watchdog Trigger Register
Watchdog Timer Register
Watchdog Status Register

Local Clocks

32.768KHz timer clock

Board Configuration

LINKS
Pull-Up enables, Common Selection
EEPROMs
PCI Configuration
FPGA Configuration

I/O Interface
64-bits of TTL compatible I/O
I/O direction byte selectable
global output enable
74ABT16245A buffers
32mA source capability
64mA sink capability
re-settable fuse protected at 2.5A

PMC Interface
Bus Interface: PCI 2.2 compliant
Bus Width: 32-bit
Bus Speed: 33MHz
Data Transfer: PCI 2.2 Bus Target
Interrupts: PCI INT #A
Memory Address: BIOS assigned

Operating Environment

Dimensions: 74.0mm x 149.0mm (single PMC size)
Power: +3.3V 215mA typical +5V 5mA typical, excluding external requirements
Environmental: 0 to 70 ° C, 95% humidity non-condensing (extended range to order)

BVM Limited can be contacted by Telephone +44 (0)1489 780144 Fax +44 (0)1489 783589
or email sales@bvmltd.co.uk

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