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U S E R ' S M A N U A L

DIGITAL WORD GENERATOR/ TIMING SIMULATOR MA-MODULE

MODEL MA202

Document Part No: 11027524D

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INTRODUCTION

This manual describes the operation and use of the C&H Model MA202 MA-Module (Part Number 11027520). This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as VME, VXI, LXI, PXI, cPCI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

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1.0 GENERAL DESCRIPTION

The MA202 is a digital word generator and timing simulator module that outputs timing data at a rate up to 10 MHz. As a digital word generator (DWG), the MA202 can generate a serial train of parallel output words at a fixed output clock rate. As a timing simulator (TS), the MA202 can produce almost any conceivable asynchronous digital signal within the 100ns resolution.

The MA202 has up to 16 bits of independently tristateable (high impedance) outputs in the DWG mode, and up to 8 bits of independently tristateable or 16 bits of non-tristateable outputs in the TS mode. The MA202 can use either an internal programmable clock, or an external signal as the time base for outputting data. It can operate in a single cycle mode with a defined number of loops or in a continuous cycle mode where the output sequence continuously loops until stopped.

The module conforms to the ANSI/VITA 12-1996 standard for M-modules, which allows it to be used in a variety of platforms, including VXI, LXI, PXI, VME, PCI, cPCI, and Ethernet, with the use of an M-module carrier.

1.1 PURPOSE OF EQUIPMENT

The MA202 is capable of multi-channel digital word generation and timing simulation.. It can be used in a wide variety of applications including serial bus testing, bus emulation, functional verification of digital systems, signal simulation, design verification, and research and development.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

- Two operational modes, Digital Word Generator (DWG) or Timing Simulator
- 16 channels of output (all 16 channels tristateable in DWG mode, 8 tristateable or 16 non-tristateable in TS mode)
- Up to 10 MHz output data rate
- Programmable internal clock (Max. 10 MHz with 50ns period resolution)
- User selectable clock inputs (programmable internal clock, external front panel signal, or backplane trigger)
- Dynamic data update capability
- Configurable synchronized output signal
- Supports continuous and single cycle modes with controllable number of loops
- Interrupts supported to signal end of cycle
- M-Module identification supported

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1.2.2 Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V (not including output drive)	400	mA
	+12V	60	mA
	-12V	80	mA
Input Voltage (EXTCLK & EXTRUN)	no damage 50Ω input impedance	±6	Vrms
	>100KΩ input impedance	±14	Vrms

AC CHARACTERISTICS

Parameter	Conditions	Limit Min	Typ.	Max	Units
Dynamic Performance					
Time Base	Internal Clock				
- Frequency			40		MHz
- Accuracy			±0.01		%
Programmable Clock					
- Resolution			50		ns
- Range	32-bit	100ns		214s	
- Accuracy			±0.01		%
Channel-to-channel Skew		0		15	ns
Sync Out Timing	EXTCLK to leading edge	15	22	35	ns
	Leading edge to data out	0	5	20	ns
Sync Out Timing (sync on word only)	Trailing edge from data out	0		20	ns
EXTCLK to Data Out	1st word, TS mode only	120		150	ns
Data Output Characteristics					
Output Driver Type	74F125				
Output High Voltage, V_{OH}	I_{OH} = -3ma	2.4			V
	I_{OH} = -12ma	2.0			V
Output Low Voltage, V_{OL}	I_{OL} = 64ma			0.55	V
Output Short Circuit Current	Vout = 0V	-100		-225	mA
Rise/Fall Time	Vout = 0.6V to 2.0V		10		ns
Input Characteristics (EXTCLK & EXTRUN)					
Input Impedance	Switch selectable	48	51	54	Ω
		100K			Ω
Input Threshold	Switch selectable Zero crossing	-0.1	0	0.1	V
	TTL	0.7	0.8	0.9	V
	CMOS	2.3	2.5	2.7	V
Frequency		0		10	MHz
Width		10		∞	ns
Sync Out Characteristics					
Output Driver Type	Three 74F04s in parallel				
Output High Voltage, V_{OH}	I_{OH} = -3ma	2.5			V
Output Low Voltage, V_{OL}	I_{OL} = 60ma			0.5	V
Output Short Circuit Current	Vout = 0V	-180		-450	mA
Rise/Fall Time	Vout = 0.6V to 2.0V		10		ns
Width	Software Selectable	50		75	ns
		900		925	ns
			800		µs

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1.2.3 Electrical

The module requires the +5V, +12V and -12V power from the M-Module interface. The output drivers for the 16 channels are TTL compatible with up to 64ma of output drive capability. The external input signals are switch selectable for TTL, CMOS, or 0V threshold signals. Input impedance is selectable for high-impedance (>100KΩ) or 50Ω.

1.2.4 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for doublewide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 4.183" (106.24 mm) wide.

1.2.5 Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +50°C
Storage Temperature:	-40°C to +70°C
Humidity:	<95% without condensation

Carrier modules may differ in environmental specification. Refer to the carrier's documentation for information.

1.2.6 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for doublewide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D16
Interrupts:	INTA & INTC
DMA:	not supported
Triggers:	Input Trig A and Trig B
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	$0FC1_{16}$
Model Number:	$00CA_{16}$ (202 dec.)
VXI Model Code:	$FE9_{16}$
Revision Level:	0001_{16}

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1.2.7 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

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2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

In most cases the MA202 is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The MA202 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M-MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. M-Modules are installed by firmly pressing the connector on the M-Module together with the connector on the carrier. Secure the M-Module with mounting hardware provided as shown in Figure 1.

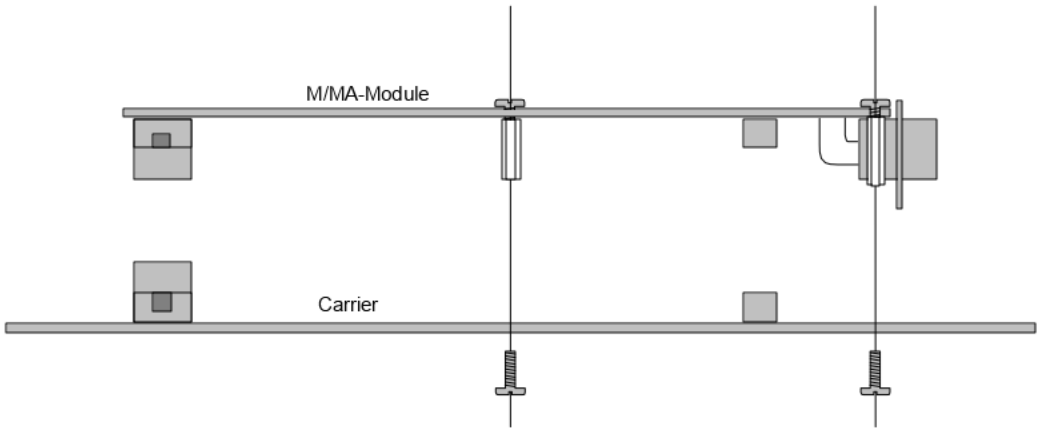


Figure 1. M-MODULE Installation

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2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti static bag. Heat-seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original shipping container and packing material may be re-used if it is still in good condition.

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3.0 FUNCTIONAL DESCRIPTION

3.1 OVERVIEW

The MA202 provides Digital Word Generation (DWG) and Timing Simulation (TS) for up to 16 individually tristateable outputs. A simplified block diagram is illustrated in figure 2.

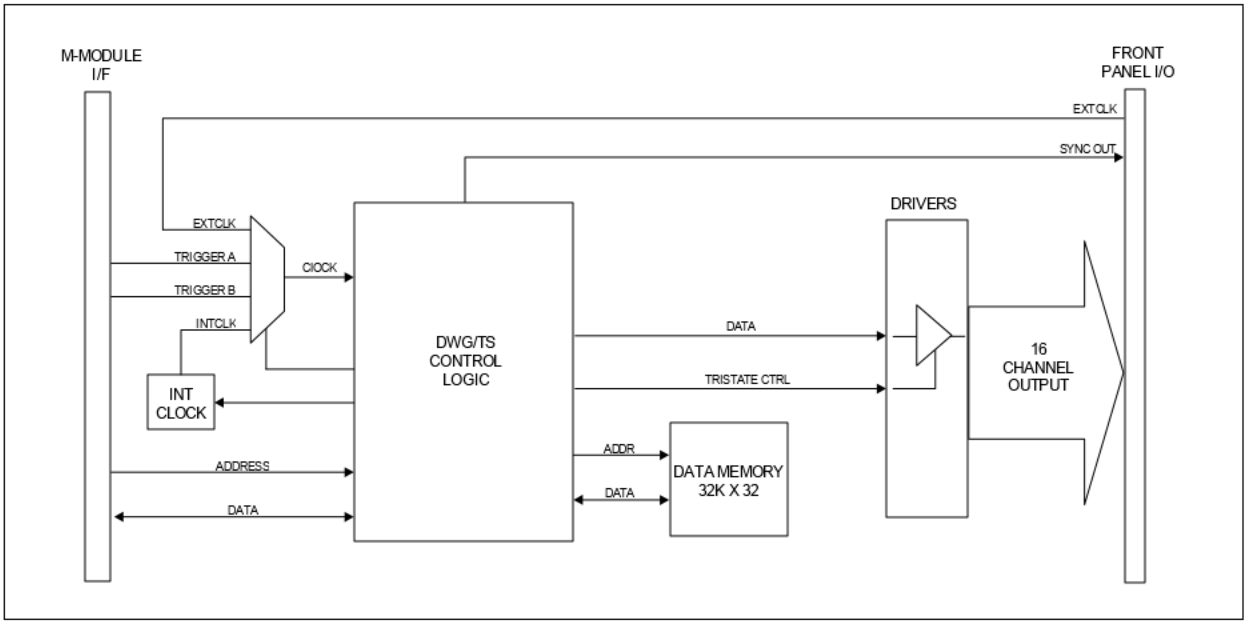


Figure 2. Functional Block Diagram

3.1.1 DWG/TS Control Logic

The control logic is used to control the digital word generator or timing simulator's internal operations such as mode selection, clock selection, and run selection. The control logic is also responsible for fetching data from memory and latching data into a buffer.

3.1.2 Internal Clock

The on-board internal clock is programmable with a period resolution of 50ns up to a frequency of 10MHz.

3.1.3 Clock Input Multiplexer

The source of the time base clock can be an external clock, one of the two M-Module I/F triggers, or the on-board programmable clock. The external clock and triggers can be up to 10MHz.

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3.1.4 Drivers

In DWG mode, the MA202 can output up to 16 bits of independently tristateable data. In the TS mode, it can output either 8 bits independently tristateable or 16 bits non-tristateable data. The output drivers are TTL compatible with up to 64ma of output drive capability.

3.1.5 Data Memory

The module contains 32K × 32 bits of memory for data, control, and timing storage. The memory is accessible to the user through a data port mapped in I/O space.

3.2 OPERATIONAL MODES

3.2.1 Digital Word Generation Mode

The DWG mode provides sixteen channels of independently tristateable data output at a fixed output clock rate. The source of the clock can be an external clock, a backplane trigger, or the internal programmable clock up to a frequency of 10 MHz. This operational mode is typically used where synchronous data patterns are required. Figure 3 shows a typical example output pattern in the DWG mode.

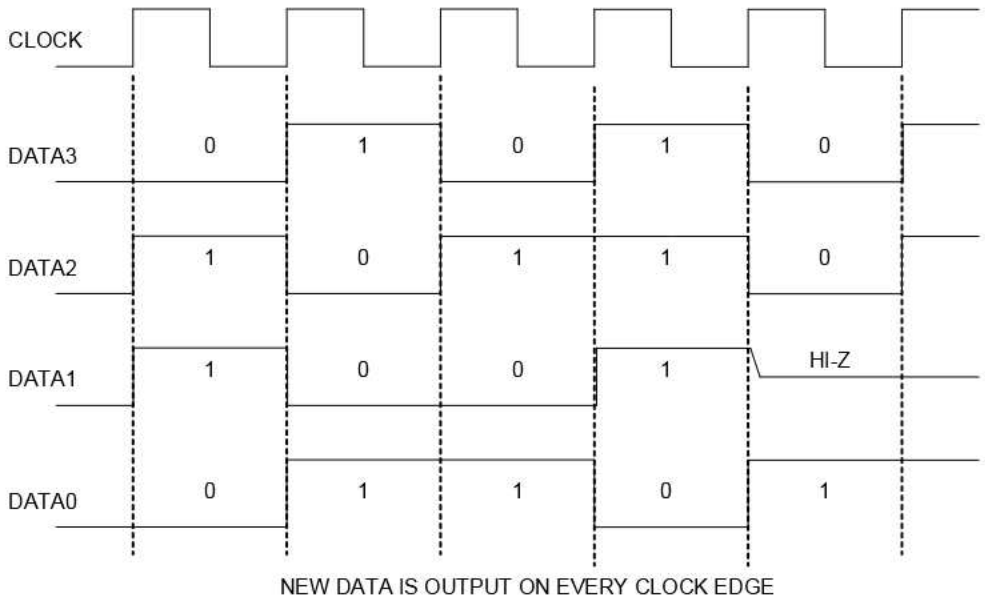


Figure 3. Example Digital Word Generator Output Pattern

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3.2.2 Timing Simulator Mode

The TS mode provides the ability to produce asynchronous data patterns. In this mode, the clock is only used as the time base for specifying when a data pattern is output. A timing value (prescaler and multiplier) is specified in each memory word definition. Sixteen output channels are available if tri-state capability is not needed or eight channels are available with individual tri-state capability. Figure 4 shows a typical example output pattern in the TS mode.

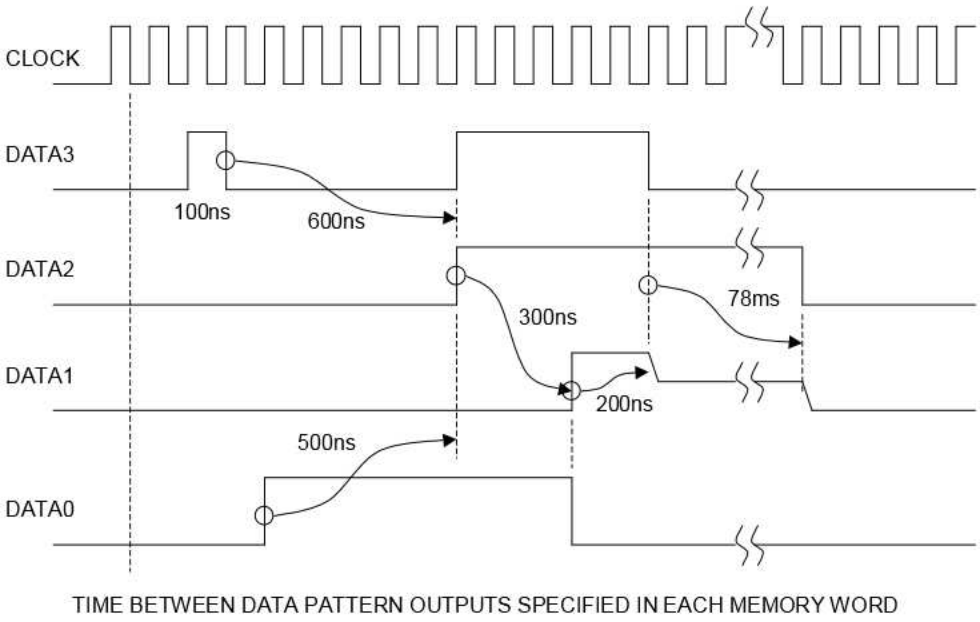


Figure 4. Example Timing Simulator Output Pattern

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3.3 HARDWARE CONFIGURATION

Switch selectable options are shown in Figure 5.

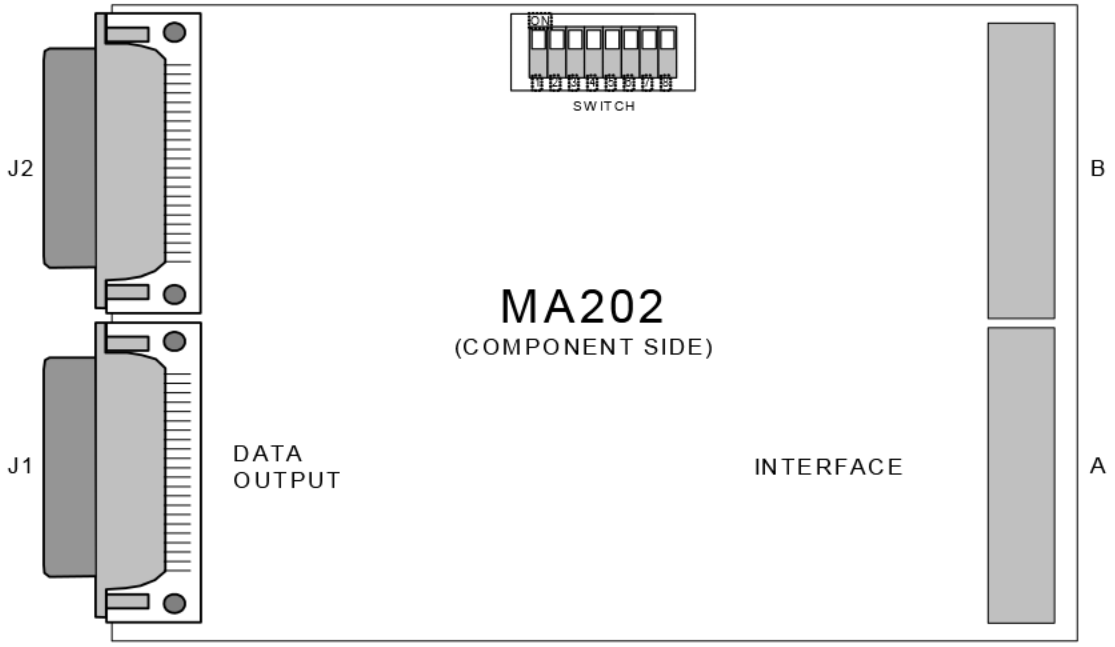


Figure 5. Hardware Configurable Controls

EXTCLK/EXTRUN Impedance (Z) These switches select the input impedance of the EXTCLK and EXTRUN front connector signals.

Impedance	EXTCLK SW3	EXTRUN SW6
50Ω	ON	ON
>100KΩ	OFF	OFF

EXTCLK/EXTRUN Level These switches control the threshold level of the EXTCLK and EXTRUN front connector signals. The level can be set to 0V (zero crossing), TTL (0.8V), or CMOS (2.5V).

	EXTCLK		EXTRUN	
Signal Level	SW1	SW2	SW4	SW5
0V	OFF	OFF	OFF	OFF
TTL	ON	ON	ON	ON
CMOS	ON	OFF	ON	OFF

Output Idle Mode This switch (SW7) controls how the outputs are driven while idle (RUN = 0). When SW7 is:

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ON - the outputs are driven according to the data word pointed to by the User Address Register (IO Reg. 18) (normal).
OFF - the outputs are tristate (high-impedance).

Output Inversion This switch (SW8) controls whether the outputs are logically inverted from the output data word. (OFF = non-inverted (normal), ON = inverted)

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3.4 INPUT/OUTPUT SIGNALS

3.4.1 M/MA-Module Interface

The M/MA-Module interface is provided through a receptacle in accordance with the M-Module specification. Only signals on connector A are used in the MA202 interface as shown in Figure 5.

3.4.2 I/O Signals

The front panel I/O connectors are standard 25-pin D-subminiature male plugs. The signals and functional descriptions are shown below. See APPENDIX A for pin assignments.

EXTCLK — The external clock input allows an external clock source to provide the data rate clock in the DWG mode. The maximum input frequency for guaranteed operation is 10MHz and the minimum pulse width must be greater than or equal to 50ns. The voltage threshold level and input impedance are switch selectable as described in 3.3. The logic is programmable for rising or falling edge operation. In TS mode, EXTCLK can be used as a start signal in single cycle mode.

EXTRUN — The external run input allows an external signal to start and stop the clocking of data. The voltage threshold level and input impedance are switch selectable as described in 3.3. The logic is programmable for active-high or active-low operation.

CH1-CH16 — A SN74F125 tristateable driver drives each output channel. While there are inherent delays in the logic elements, the generator outputs have been designed to minimize signal skew between any two channels.

SYNC OUT — The Sync Output signal is a negative going pulse, which enables the user to synchronize an external device to the MA202.

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3.5 IDENTIFICATION AND CONFIGURATION REGISTERS

3.5.1 M-Module ID PROM Registers

The MA202 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in I/O space and the data is read one bit at a time.

The MA202 also supports the VXI-IDENT function introduced by Hewlett-Packard. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type Registers. Details are shown in Table I.

Table I. M/MA Module EEPROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00CA (202 dec.)
2	Revision Number[1]	0001
3	Module Characteristics[2]	1A68
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (C&H)
18	VXI Device Type[3]	FFE9
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the functional revision level of the module. It does not necessarily correspond to the hardware assembly level.

2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = needs ±12V
11	1 = needs +5V
10	0 = no trigger outputs
9	1 = trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type C
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	$FE9_{16}$ = C&H specified VXI model code

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3.5.2 IO Registers.

There are a variety of registers used to configure and control the MA202 module. The registers are addressable within the I/O Space. An address map of the registers is shown in Table II. The registers provide control, status, internal clock control, and memory information. Details of the registers are provided in Figure 6.

Table II. I/O Address Map/Command Summary

IO REG. (HEX)	REGISTER DESCRIPTION	DATA BITS																NOTE
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	Control/Status	-	RUNSEL			-	CLKSEL			RST	STEP	-	SYNC	TSTRI	TS	CYC	RUN	A
02	Interrupt Control	MIEN	IT	CCIEN	SCIEN	-	-	CCIP	SCIP	INTERRUPT VECTOR								A
04	Reserved	(Reserved)																
06	Start Pointer	A15	START POINTER														A0	I
08	End Pointer	A15	END POINTER														A0	I
0A	Sync On Pointer	A15	SYNC ON POINTER														A0	A
0C	Output Configuration	TSON	IOFF	-	-	SYNC OUT PW				ODD WORD SIZE				WORD SIZE				I
0E	Internal Clock, MSW	D31	INTERNAL CLOCK PERIOD, MSW														D16	A
10	Internal Clock, LSW	D15	INTERNAL CLOCK PERIOD, LSW														D0	A
12	Dynamic Update Pointer	A15	DYNAMIC UPDATE POINTER														A0	R
14	Dynamic Update Data, MSW	D31	DYNAMIC UPDATE DATA, MSW														D16	A
16	Dynamic Update Data, LSW	D15	DYNAMIC UPDATE DATA, LSW														D0	A
18	User Address	D15	USER ADDRESS														D0	A
1A	User Data	D15	READ/WRITE DATA														D0	I
1C	Loop Control	D15	NUMBER OF LOOPS														D0	A

NOTE: Denotes when register can be written, A = Anytime, I = only when idle, R = only when running.

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Control/Status Register (00_{16}) This read/write register provides the main control of the module operation. Bits are provided for control of the modes and clock and run signal sources.

Interrupt Control Register (02_{16}) This read/write register enables interrupts and defines the interrupt vector value returned by the M-Module during an interrupt acknowledge cycle.

Reserved (04_{16}) This register is reserved for factory use.

Start Pointer (06_{16}) This read/write register specifies the starting location of the 32-bit memory where output data is located.

End Pointer (08_{16}) This read/write register specifies the ending address of the cycle.

Sync On Pointer ($0A_{16}$) This read/write register specifies the memory output pointer that will cause a Sync Output (SYNC OUT) pulse, when Sync On Pointer is specified in the Control/Status register.

Output Configuration ($0C_{16}$) This read/write register specifies various output control functions, including the word size, odd word count, Sync Out pulse width, tristate control, and automatic incrementing of the memory address register.

Internal Clock ($0E_{16}$ & 10_{16}) These read/write registers specify the period of the internal clock. The period is programmable to 50ns resolution.

Dynamic Update Pointer (12_{16}) This read/write register specifies the output word pointer for the dynamically updated data value.

Dynamic Update Data (14_{16} & 16_{16}) These read/write registers specify the 32-bit output word value that is written to memory when the Dynamic Update Pointer Register (Reg. 12_{16}) is written.

User Address (18_{16}) This read/write register specifies the memory location that User Data is written to or read from.

User Data ($1A_{16}$) This read/write register stores the data value at the memory location pointed to by the User Address or reads the data from memory at the location specified by the User Address.

Loop Control ($1C_{16}$) This read/write register specifies the number of times a test pattern is output when in single cycle mode.

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Control/Status

00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	RUNSEL			-	CLKSEL			RST	STEP	-	SYNC	TSTRI	TS	CYC	RUN
Read	-	RUNSEL			-	CLKSEL			RST	STEP	-	SYNC	TSTRI	TS	CYC	RUN

RUN	Run (1 = Start cycle)
CYC	Cycle (1 = single cycle, 0 = continuously cycle)
TS	Mode (1 = timing simulator, 0 = word generator)
TSTRI	Timing Simulator Tristate Control (1 = 8-bit data with tristate control, 0 = 16-bit data with no tristate control)
SYNC	Sync Out Control (1 = output a pulse when the output word is on the pointer specified in the Sync On Pointer Register, 0 = output a pulse on each output word)
STEP	Step (1 = starts another cycle in single cycle mode)
RST	Reset (1 = reset)
CLKSEL	Conversion Clock Select

000	Internal Clock	100	Backplane Trigger A (rising edge)
001	Reserved	101	Backplane Trigger A (falling edge)
010	EXTCLK FP signal (rising edge)	110	Backplane Trigger B (rising edge)
011	EXTCLK FP signal (falling edge)	111	Backplane Trigger B (falling edge)

RUNSEL — Run Source Select

000	Software Run bit	100	Backplane Trigger A (low level)
001	(reserved)	101	Backplane Trigger A (high level)
010	EXTRUN FP signal (low level)	110	Backplane Trigger B (low level)
011	EXTRUN FP signal (high level)	111	Backplane Trigger B (high level)

Interrupt Control

02

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	MIEN	IT	CCIEN	SCIEN	-	-	-	-	Interrupt Vector							
Read	MIEN	IT	CCIEN	SCIEN	-	-	CCIP	SCIP	Interrupt Vector							

MIEN	Master Interrupt Enable (1 = enable)
IT	Interrupt Type (0 = Type A, 1 = Type C)
CCIEN	Continuous Cycle Interrupt Enable (1 = enabled)
SCIEN	Single Cycle Interrupt Enable (1 = enabled)
CCIP	Continuous Cycle Interrupt Pending (1 = pending, write a 1 to this bit to clear the interrupt)
SCIP	Single Cycle Interrupt Pending (1 = pending, write a 1 to this bit to the clear the interrupt)
Interrupt Vector	Value presented during interrupt acknowledge cycle

Note: For Type C interrupts, MIEN is automatically cleared during the IACK cycle.

Figure 6. I/O Registers

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Start Pointer

06

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	0	Start Pointer														
Read	0	Start Pointer														

Pointer to the first output memory word to begin the sequence (Sets the starting 32-bit memory location. Can be any value from 0000_{16} to $7FFF_{16}$. This register can only be changed when idle (Reg. 0, RUN bit must be 0))

End Pointer

08

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	0	End Pointer														
Read	0	End Pointer														

Pointer to the last output memory word in the sequence. (Sets the ending 32-bit memory location. Can be any value from 0000_{16} to $7FFF_{16}$. This register can only be changed when idle (Reg. 0, RUN bit must be 0))

Sync On Pointer

0A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	0	Sync On Pointer														
Read	0	Sync On Pointer														

Memory word pointer that will cause a Sync Out pulse. (Generate an Output Sync Pulse on this 32-bit memory location, if proper mode bit in the Control/Status register is selected. Can be any value from 0000_{16} to $7FFF_{16}$. This register can be changed anytime.)

Figure 6. I/O Registers (continued)

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Output Configuration

0C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	TSON	IOFF	-		SOPW				OWC				WS			
Read									OWC				WS			

WS Word Size (only used in word generator mode)

OUTPUT WORD BIT SIZE	WORDS PER MEMORY WORD	Word Size (WS)				OUTPUT CHANNEL(S) FROM WHICH OUTPUT IS TAKEN
		3	2	1	0	
1	16	0	0	0	0	1
2	8	1	0	0	0	1,9
3	4	1	1	0	0	1,5,9
4	4	1	1	0	0	1,5,9,13
5	2	1	1	1	0	1,3,5,7,9
6	2	1	1	1	0	1,3,5,7,9,11
7	2	1	1	1	0	1,3,5,7,9,11,13
8	2	1	1	1	0	1,3,5,7,9,11,13,15
16	1	1	1	1	1	Direct 1 through 16

OWC Odd Word Count (The odd word count is used to specify the number of words used in the last data word read from memory. n = 16 - OWC. (only used in word generator mode)

SOPW Sync Out Pulse Width
- 0001 = Reserved
- 0010 = 50ns sync out pulse
- 0100 = 900ns sync out pulse
- 1000 = 800µs sync out pulse

IOFF Increment Off (1 = inhibit automatic increment of the memory address register 18_{16})

TSON Tristate On (1 = enable the TRISTATE bits)

Note:
1. If word size = 0xF, then OWC is not used.
2. This register can only be changed when the DWG is idle.

Figure 6. I/O Registers (continued)

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Internal Clock MSW

0E

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31							Internal Clock Period								D16
Read	D31							Internal Clock Period								D16

Internal Clock LSW

10

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15							Internal Clock Period								D0
Read	D15							Internal Clock Period								D0

Specifies the period of the internal clock in 50ns increments (minus one). (Period = (value + 1) × 50ns).

Note: If CLKSEL in the Control/Status Register is set to the Internal Clock, the value of the Internal Clock registers must be greater than 0.

Dynamic Update Pointer

12

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Dynamic Update Pointer															
Read	Dynamic Update Pointer															

Specifies the location in 32-bit memory that is dynamic updated. The output word value present in IO Reg. 14 and IO Reg. 16 is dynamically update each time the Dynamic Update Pointer is written.

Dynamic Update Data MSW

14

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31							Dynamic Update Data								D16
Read	D31							Dynamic Update Data								D16

Dynamic Update Data LSW

16

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15							Dynamic Update Data								D0
Read	D15							Dynamic Update Data								D0

In continuous mode, the output word specified in IO Reg. 14 & 16 will be presented at the output port and written to memory each time IO Reg. 12 is written. This feature is active when the DWG is running (IO Reg. 0, RUN is ON). The data in IO Reg. 14 and 16 can be changed anytime.

Figure 6. I/O Registers (continued)

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User Address

18

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	A15							Address								A0
Read	A15							Address								A0

Specifies the physical 16-bit memory address that is written when User Data (IO Reg. 1A) is written or the address that is read when User Data (IO Reg. 1A) is read. This value is automatically incremented each time User Data is written or read, unless this feature is inhibited with the IOFF bit in Output Register (IO Reg. 0C).

Note: When Idle (IO Reg. 00 Run=0) and the Output Idle Mode switch is ON, the output word will be equal to the data value pointed to by the User Address.

User Data

1A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15							Write Data								D0
Read	D15							Read Data								D0

A read or write of this register will either read the data value of the address specified by IO Reg. 18, or write the data value to the address specified by IO Reg. 18. In either case, the User Address in IO Reg. 18 is automatically incremented by 1 after the operation is complete, unless this feature is inhibited with the IOFF bit in Output Register (IO Reg. 0C).

Loop Control

1C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Number of Loops															
Read	Number of Loops															

Specifies how many cycles are to be completed before going idle again. Used in Single Cycle mode only.

Note: Number of loops specified must be one (1) or greater (0 is invalid). Unit will run continuously if zero (0) loops is specified.

Figure 6. I/O Registers (continued)

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4.0 PROGRAMMING INSTRUCTIONS

4.1 INITIALIZATION AND OPERATION CONTROL

4.1.1 Memory Organization and Programming

When defining a digital output pattern and timing sequence it is important to understand the organization of the memory and how the memory is used. The physical memory on the MA202 is addressable as 16-bit words; however, most operations performed by the MA202 internal logic operates on the memory as 32-bit wide words. Memory is read or modified by specifying a 16-bit address in the User Address Register (IO Reg. 18), then writing or reading the value from/to the User Data Register (IO Reg. 1A). To facilitate fast memory operations, the User Address Register is automatically incremented after each read or write of the User Data Register.

Note that the Start Pointer, End Pointer, Sync On Address Pointer, and Dynamic Update Pointer all refer to the 32-bit output memory location NOT the 16-bit physical memory address. The physical memory address is equal to two times the pointer value. An even numbered physical (User) address always refers to tristate control in DWG mode and timing data in TS mode. An odd number physical (User) address always refers to data in DWG mode and tristate/data in TS mode. Thus, in DWG mode, a memory location is defined as:

$$ControlPortionOfPhysical(User)Address = Pointer \times 2 \text{ and}$$

$$DataPortionOfPhysical(User)Address = (Pointer \times 2) + 1$$

where Pointer is the Start Pointer, End Pointer, Sync On Address Pointer, or Dynamic Update Pointer

4.1.2 Clock Setup

The source of the data output clock rate in DWG mode can be the programmable internal clock, an external front panel clock input (EXTCLK), or either M-module I/F trigger (TRIGA or TRIGB). In TS mode, the time base is always the 40MHz internal clock. Any of the clock sources can be configured to clock on the rising or falling edge. The CLKSEL field in the Control/Status Register (IO Reg. 00) is used to select the source and edge of the clock to use.

4.1.3 Loop Control

The MA202 has the capability to repeat a digital output pattern or a timing sequence (steps) for a specified number of cycles. To repeat a sequence of steps for a specific number of times, configure the MA202 for Single Cycle operation, by setting the CYC bit in the Control/Status Register (IO Reg. 00) to '0', then specify the desired number of loops in the Loop Control Register (IO Reg. 1C). Refer to 4.1.4 for details on Single Cycle mode.

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4.1.4 Single Cycle Operation

Single cycle applies in both timing simulator and word generator mode. The following describes single cycle operation.

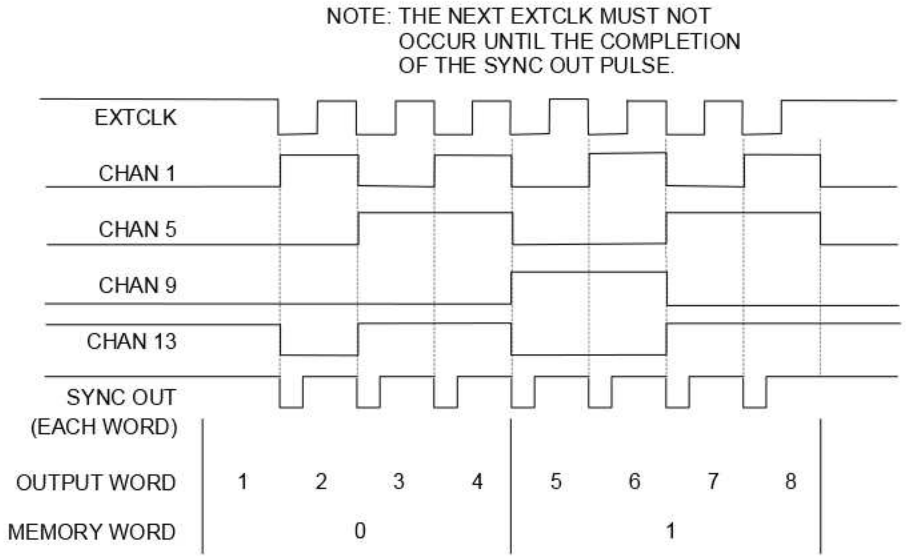
1) The generator remains idle at User Address.
2) Upon receiving either a RUN signal (software run, external clock or trigger), the internal logic begins stepping through the memory words.
3) The generator processes all programmed memory words in the normal fashion.
4) When the last memory address (End Pointer) has been completely processed, the generator steps back to User Address and halts.
5) The sequence may be repeated as desired using the Loop Control Register (IO Reg. 1C).

When idle, the output level is as defined by the data pointed to by the User Address and remains at that level until the following occurs:

1) In timing simulator mode, if EXTCLK is selected as the conversion clock, it acts like a start signal in single cycle mode, therefore, after a cycle completes the next EXTCLK will start another cycle. If EXTCLK is continuous, the MA202 runs continuously.
2) In word generator mode the first memory word is processed in the normal fashion. The data for the User Address is sitting in the output shift register. Upon receiving an external pulse or internal clock, the generator loads the 1st word and begins shifting the data as defined by the Output Configuration Register. It processes the remainder of the memory words in a normal fashion, and completes the cycle by again loading the data pointed to by the User Address, into the output register and then halting.

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Example: Single Cycle Word Generator Mode with Sync Out



The first high to low transition of the EXTCLK pulse starts the signal cycle. However, this edge must be synchronized to the generator's internal clock, thus causing an inherent skew between the falling edge of the EXTCLK and the output data and SYNC OUT pulse. This time skew is 50ns min to 175ns max.

The memory and control registers would be configured as follows:

Register Description	Reg., hex	Value, hex	Comments
Start Pointer	06	0000	
End Pointer	08	0001	2 memory words
Output Configuration	0C	02CC	OWC=16-4=12(C), WS=4 bits
User Address	18	0000	
User Data (Memory Addr 0)	1A	0000	No high impedance outputs
User Data (Memory Addr 1)	1A	DOCA	
User Data (Memory Addr 2)	1A	0000	No high impedance outputs
User Data (Memory Addr 3)	1A	C3CA	
Loop Count	1C	0001	
User Address	18	0001	Set to Start Pointer + 1
Control/Status	00	0303	WG mode, Single Cycle, Ext. Clock, Sync on Word

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4.1.5 Sync Out Operation

SYNC OUT on EACH WORD: This software mode generates a pulse as each output word is generated. In word generator mode a pulse is generated at each output register load and shift. In timing simulator mode, since there are no output register shifts, the pulse occurs only at the output register load time. The pulse width can be programmed to be 50ns, 900ns, or 800µs. Refer to Figure 7 and Figure 8 for the SYNC OUT signal relationships.

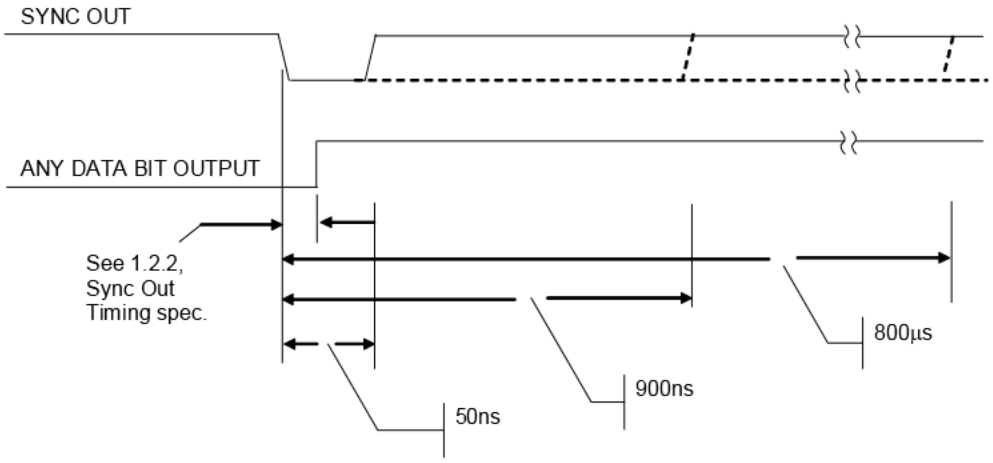


Figure 7. SYNC OUT on EACH WORD (Internal Timing)

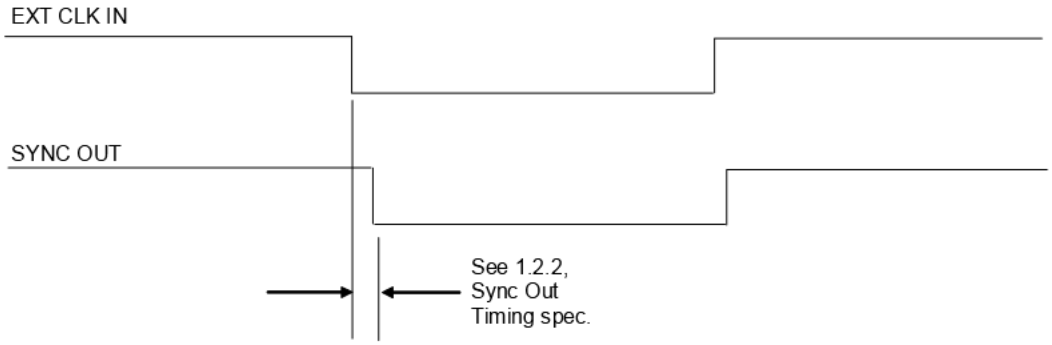


Figure 8. SYNC OUT on EACH WORD (External Timing, WG Mode Only)

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SYNC OUT on SELECTED ADDRESS: This mode generates a pulse when the memory address counter equals the programmed SYNC OUT address. The pulse width is equal to one memory address time. This function is the same for timing simulator and word generator mode. Note that this pulse may encompass several output words in word generator mode since one memory word may contain several output words. Refer to Figure 9 depicting the selected address sync signal.

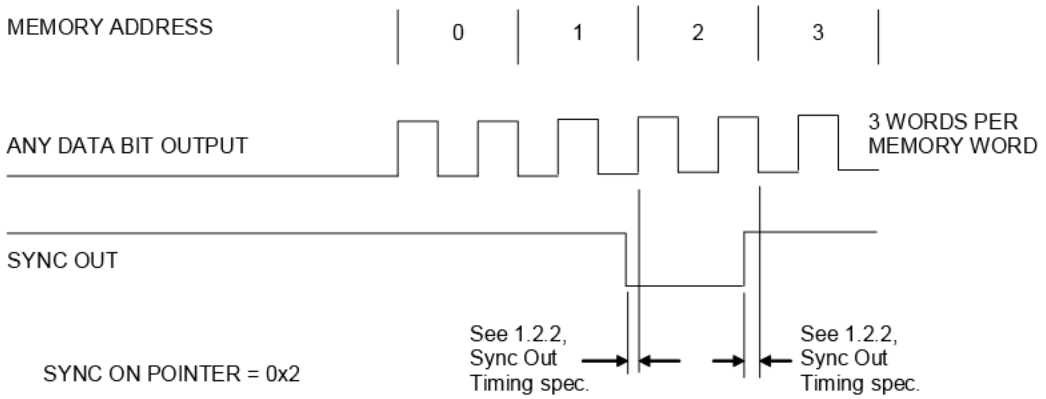


Figure 9. SYNC OUT on SELECTED ADDRESS (Internal & External Timing)

4.1.6 Dynamic Data Update

The dynamic data update capability allows a data pattern or timing value to be dynamically updated while running in Continuous mode. While a digital output pattern or a timing sequence is being output, a memory word (time/data) can be modified. The new 32-bit time/data memory word is specified in Dynamic Update Registers (IO Reg. 14 and 16). The memory is then updated by writing an address to the Dynamic Update Pointer register (IO Reg. 12). This capability can be used to dynamically control the pulse width or time relationship between two signals in TS mode or to dynamically change an output data value in DWG mode.

4.1.7 Interrupt Control

An interrupt can be generated at the end of each sequence of steps in Continuous mode or at the end of the specified number of loops in Single Cycle mode. The Interrupt Control Register (IO Reg. 02) allows either Single Cycle or Continuous Cycle interrupts to be individually enabled. An interrupt vector can be specified that is presented to the host interface during an interrupt acknowledge cycle.

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4.1.8 ID PROM

Refer to 3.5.1 M-Module ID PROM Registers for a description of the ID PROM's function and contents. The ID PROM is a serial device and involves writing and reading a register in a sequential manner to acquire data. Figure **10** is a general description of the code sequence necessary to read the information from the PROM. The PROM is a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*-------------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
addr = 0xFE;                          /* M/MA address for IDPROM */
id_addr = 0x80 | id_addr;             /* 80 is the read opcode for the PROM
*/
write_eebyte (addr, id_addr);
read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
tmpval = rdval << 8;          /* upper byte of sync code word */
read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
tmpval = tmpval | rdval;              /* combine bytes of sync code   */
*value = tmpval;
write_word(addr, 0x0000);             /* lower cs */
return;
}
/*-------------------------------------------------------------------------*/
int write_eebyte (unsigned long addr, unsigned short value){
write_word(addr, 0x0000);             /* insure cs is initially low */
write_word(addr, 0x0004);             /* initialize */
write_eebit(addr, 0x0001);            /* start bit */
temp = value;
for (i=0;i<=7;i++){
write_eebit(addr, ((temp & 0x80)>>7));
temp = (temp << 1);
}
return;
}
/*-------------------------------------------------------------------------*/
int write_eebit (unsigned long addr, unsigned short value){
temp = (0x0004 | (value & 0x0001)); /*  set data bit before clock */
write_word(addr, temp);
Delay(.000005);
temp = (0x0006 | (value & 0x0001)); /*  set data bit & clock */
write_word(addr, temp);
Delay(.000005);
return;
}
/*-------------------------------------------------------------------------*/
int read_eebyte (unsigned short addr, unsigned short *value){
for (i=7;i>=0;i=i-1){
read_eebit (addr, &rdval);
temp = temp | ((rdval&0x01) << i);
}
*value = temp;
return;
}
/*-------------------------------------------------------------------------
*/
int read_eebit (unsigned short addr, unsigned short *value){
write_word(addr, 0x4);                /* lower clock bit */
Delay(.000005);
write_word(addr, 0x6);                /* raise clock bit */
Delay(.000005);
read_word (addr, value);
return;
```

Figure 10. ID PROM Access Routine

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4.2 DIGITAL WORD GENERATOR (DWG) PROGRAMMING

The DWG mode allows the user to generate a serial train of parallel output words. These parallel output words may range from a single bit per output word to 16 bits per output word. Reference is made to two different word types, a memory word and an output word. For a thorough understanding of this mode, the two word types must not be confused.

4.2.1 Output Word Definition

A memory word is 32-bits wide, with 16-bits dedicated to tristate control and 16-bits dedicated to data as shown in Figure 11. The tristate control is always an even memory address and the data is always an odd memory address. An output word is the data presented at the output connector. Each memory word may contain several output words. The Word Size field in the Output Configuration Register (Reg. 0C) is used to program the desired number of output words per memory word. In addition, the Odd Word Count Field in this same register is used to specify the number of output words (i.e., tristate and data control bits) to use in the last data word read from memory. See Figure 6 Reg. 0C for details.

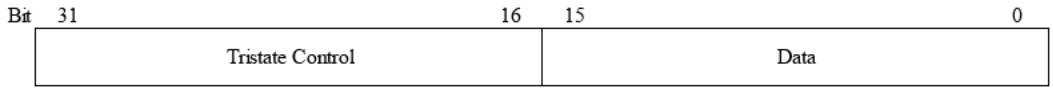


Figure 11. Digital Word Generator

A '1' bit in the tristate control produces a high impedance output regardless of the data value. The lower 16 bits are output as data on the output drivers. Word size is selectable from 1 to 8, or 16 bits. The tristate bits apply the same in all cases. The MA202 contains 32K memory words, which yields 524,288 available bits. This allows a user to program 524,288 output words (1 bit wide), 262,144 output words (2 bits wide), 131,072 output words (4 bits wide), and 65,536 output words (8 bits wide), or 32,768 output words (16 bits wide) as shown in Table III.

Table III. Available Output Words

OUTPUT WORD BIT SIZE	WORDS PER MEMORY WORD	TOTAL NUMBER OF OUTPUT WORDS AVAILABLE	OUTPUT CHANNEL FROM WHICH OUTPUT IS TAKEN FROM
1	16	524,288	1
2	8	262,144	1,9
4	4	131,072	1,5,9,13
8	2	65,536	1,3,5,7,9,11,13,15
16	1	32,768	1 16

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After the output word size is defined in the Output Configuration Register (IO Reg. 0C), the total number of output words must be programmed. This is accomplished by programming the End Pointer Register (IO Reg. 08) and the Odd Word Count (OWC) field in the Output Configuration Register (IO Reg. 0C).

It should be noted, that word sizes which are not binary multiples, may also be programmed (i.e., 3, 5, 6, & 7 bits per output word). These are programmed exactly the same as the 4 or 8 bits per output word with appropriate channels left unused. The data bits in memory corresponding to the unused channels are don't cares.

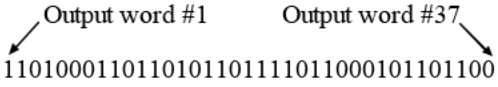
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4.2.2 Programming Examples

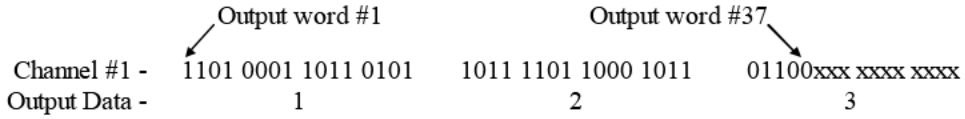
The following examples are presented to provide more familiarity with the word generator mode.

Example 1: One bit per output word (single serial data stream).

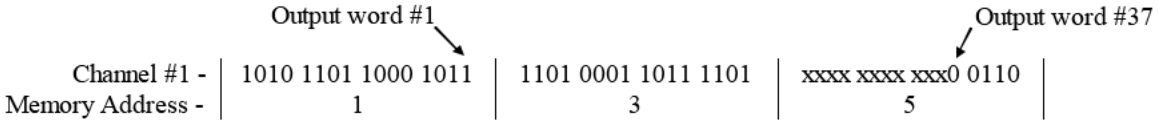
Generate the following thirty-seven word, one bit serial data stream.



For this example, only output channel 1 is used. The DWG data memory is 16 bits wide and the bits can serially be output on channel 1. Thus, the thirty-seven word string can be broken into two memory data words of 16 bits each and one memory data word of 5 bits. The output words are always active, so the tristate control bits are set to '0'.



Since the data at each memory address is loaded into a shift register and shifted right to output, the values represented above must be flipped before loading into memory. For this example, the full 16-bits are flipped.

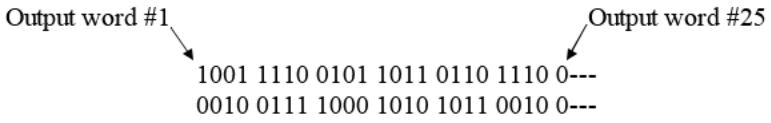


The memory and control registers would be configured as follows:

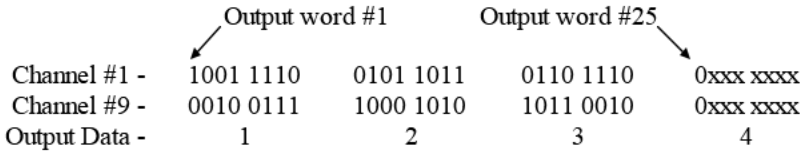
Register Description	Reg., hex	Value, hex	Comments
Start Pointer	06	0000	
End Pointer	08	0002	3 memory words
Output Configuration	0C	02B0	OWC=16-5=11(B), WS=1 bit
User Address	18	0000	
User Data (Memory Addr 0)	1A	0000	No high impedance outputs
User Data (Memory Addr 1)	1A	AD8B	
User Data (Memory Addr 2)	1A	0000	No high impedance outputs
User Data (Memory Addr 3)	1A	D1BD	
User Data (Memory Addr 4)	1A	0000	No high impedance outputs
User Data (Memory Addr 5)	1A	0006	
Program Clock MSW	0E	0000	
Program Clock LSW	10	0001	100ns period
User Address	18	0001	Set to Start Pointer + 1
Control/Status	00	0011	WG mode, Cont. Cycle, Int. Clock, Sync on Addr, SW Run

Example 2. 2 bits per output word. Generate the following twenty-five 2 bit words.

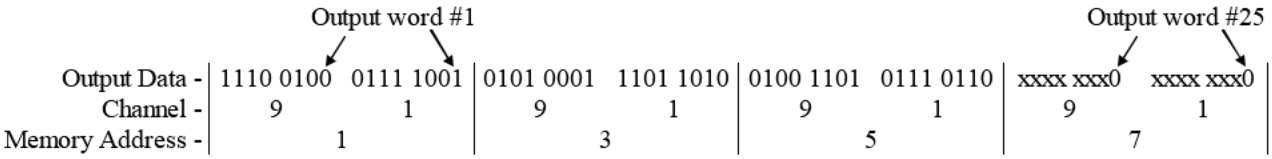
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For this example, output channels 1 and 9 are used. The DWG data memory has 16 bits and 8 of these bits can serially be output on channel 1, while the other 8 can simultaneously be output on channel 9. Thus, the twenty-five word string can be broken up into three memory data words of 8 bits for each output channel and one memory data word of 1 bit for each output channel. The output words are always active, so the tristate control bits are set to '0'.



Since the data is loaded into a shift register and shifted right to output, the values represented above must be flipped before loading into memory. For this example, each of the channels 8-bits are flipped.

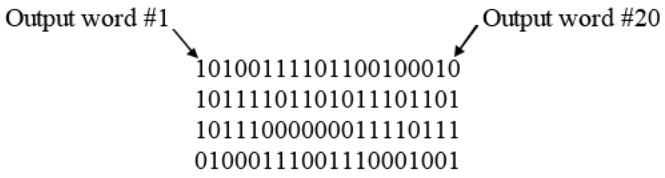


The memory and control registers would be configured as follows:

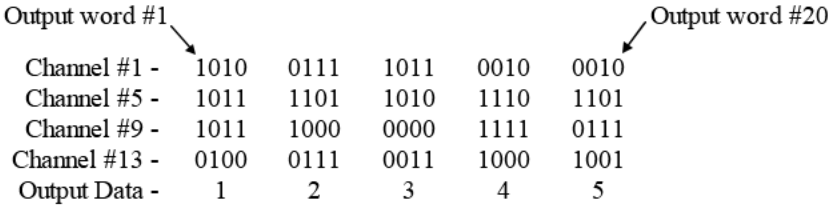
Register Description	Reg., hex	Value, hex	Comments
Start Pointer	06	0000	
End Pointer	08	0003	4 memory words
Output Configuration	0C	02F8	OWC=16-1=15(F), WS = 2 bits
User Address	18	0000	
User Data (Memory Addr 0)	1A	0000	No high impedance outputs
User Data (Memory Addr 1)	1A	E479	
User Data (Memory Addr 2)	1A	0000	No high impedance outputs
User Data (Memory Addr 3)	1A	51DA	
User Data (Memory Addr 4)	1A	0000	No high impedance outputs
User Data (Memory Addr 5)	1A	4D76	
User Data (Memory Addr 6)	1A	0000	No high impedance outputs
User Data (Memory Addr 7)	1A	0000	
Program Clock MSW	0E	0000	
Program Clock LSW	10	0001	100ns period
User Address	18	0001	Set to Start Pointer + 1
Control/Status	00	0011	WG mode, Cont. Cycle, Int. Clock, Sync on Addr, SW Run

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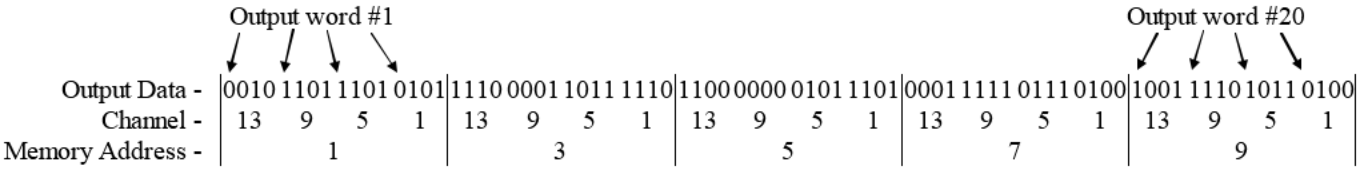
Example 3. 4 bits per output word. Generate the following twenty 4-bit words.



For this example, output channels 1, 5, 9 and 13 are used.



Since the data is loaded into a shift register and shifted right to output, the values represented above must be flipped before loading into memory. For this example, each of the channels 4-bits are flipped.

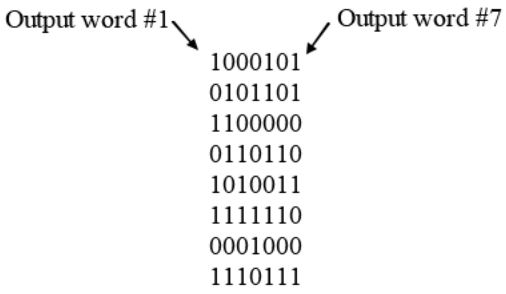


The memory and control registers would be configured as follows:

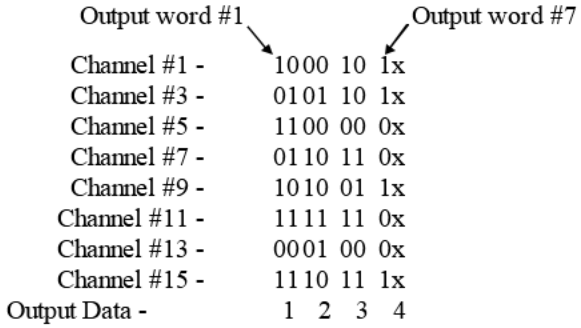
Register Description	Reg., hex	Value, hex	Comments
Start Pointer	06	0000	
End Pointer	08	0004	5 memory words
Output Configuration	0C	02CC	OWC=16-4=12(C), WS=4 bits
User Address	18	0000	
User Data (Memory Addr 0)	1A	0000	No high impedance outputs
User Data (Memory Addr 1)	1A	2DD5	
User Data (Memory Addr 2)	1A	0000	No high impedance outputs
User Data (Memory Addr 3)	1A	E1BE	
User Data (Memory Addr 4)	1A	0000	No high impedance outputs
User Data (Memory Addr 5)	1A	C05D	
User Data (Memory Addr 6)	1A	0000	No high impedance outputs
User Data (Memory Addr 7)	1A	1F74	
User Data (Memory Addr 8)	1A	0000	No high impedance outputs
User Data (Memory Addr 9)	1A	9EB4	
Program Clock MSW	0E	0000	
Program Clock LSW	10	0001	100ns period
User Address	18	0001	Set to Start Pointer + 1
Control/Status	00	0011	WG mode, Cont. Cycle, Int. Clock, Sync on Addr, SW Run

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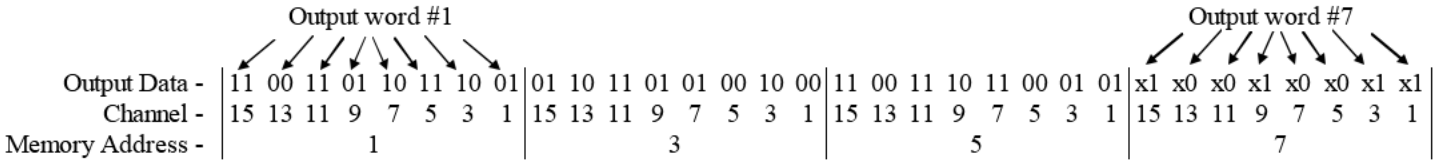
Example 4. 8 bits per output word. Generate the following seven 8-bit words.



For this example, output channels 1, 3, 5, 7, 9, 11, 13 and 15 are used.



Since the data is loaded into a shift register and shifted right to output, the values represented above must be flipped before loading into memory. For this example, each of the channels 2-bits are flipped.



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The memory and control registers would be configured as follows:

Register Description	Reg., hex	Value, hex	Comments
Start Pointer	06	0000	
End Pointer	08	0003	4 memory words
Output Configuration	0C	02FE	OWC=16-1=15(F), WS=8 bits
User Address	18	0000	
User Data (Memory Addr 0)	1A	0000	No high impedance outputs
User Data (Memory Addr 1)	1A	CDB9	
User Data (Memory Addr 2)	1A	0000	No high impedance outputs
User Data (Memory Addr 3)	1A	6D48	
User Data (Memory Addr 4)	1A	0000	No high impedance outputs
User Data (Memory Addr 5)	1A	CEC5	
User Data (Memory Addr 6)	1A	0000	No high impedance outputs
User Data (Memory Addr 7)	1A	4105	
Program Clock MSW	0E	0000	
Program Clock LSW	10	0001	100ns period
User Address	18	0001	Set to Start Pointer + 1
Control/Status	00	0011	WG mode, Cont. Cycle, Int. Clock, Sync on Addr, SW Run

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4.3 TIMING SIMULATOR (TS) PROGRAMMING

The timing simulator mode has been designed such that the user can easily program almost any conceivable digital timing signals. This mode is similar to the word generator mode in that memory words are sequentially taken from memory and loaded into the output register. The Timing Simulator also requires that the user program the associated time intervals into memory. The word generator mode has a constant memory accessing time (i.e., constant word period). The timing simulator mode has a variable memory accessing time (i.e., variable word period).

4.3.1 Configurations

The timing simulator has two types of output configurations. Each type uses a 32-bit word for output and control. Type 1 provides 8-bits of independent tristateable output as indicated in Figure 12. Type 2 provides 16-bits of output with no tristate capability as indicated in Figure 13.

The time base is always the internal 40MHz (25ns period) clock. Each word also offers a 12-bit prescale timing clock value. The prescaler is selected for each timing cycle.

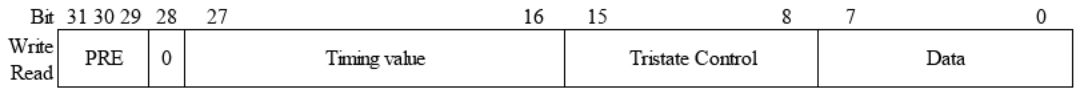
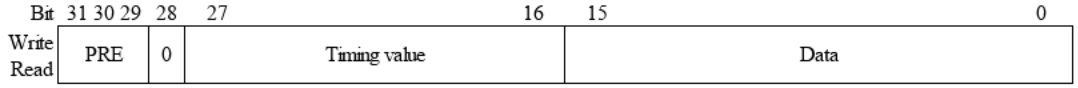


Figure 12. Timing Simulation Tristate Configuration (Type 1)



PRE used to select the prescaler
- 000 – Period of 25ns (minimum timing value = 4)
- 001 – Period of 250ns
- 010 – Period of 2.5µs
- 011 – Period of 25µs
- 100 – Period of 250µs
- 101 – Reserved
- 110 – Reserved
- 111 – Reserved

Figure 13. Timing Simulation Non-Tristateable (Type 2)

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4.3.2 Timing Definition

Programming in the timing simulator mode requires the user to translate his desired timing information to the memory words. The relationship between any timing diagram and the memory words can be complicated and is best described through the examples that follow. The user should become familiar with this relationship to facilitate usage in timing simulator mode.

Defining each memory word consists of the following steps (see example in Figure 14):

1) Draw the desired timing signals.
2) Partition the waveforms at every logic transition.
3) Assign memory word numbers to each partition along with the time duration of each partition.

Each partition defines one memory word, complete with time and output level data. Thus, the relationship between the timing diagram and the memory is defined.

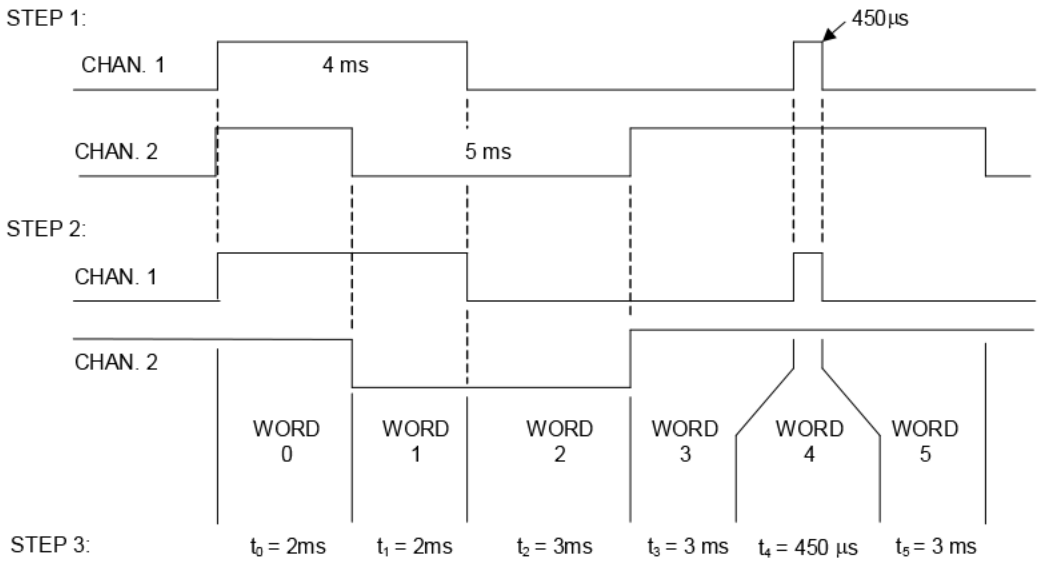


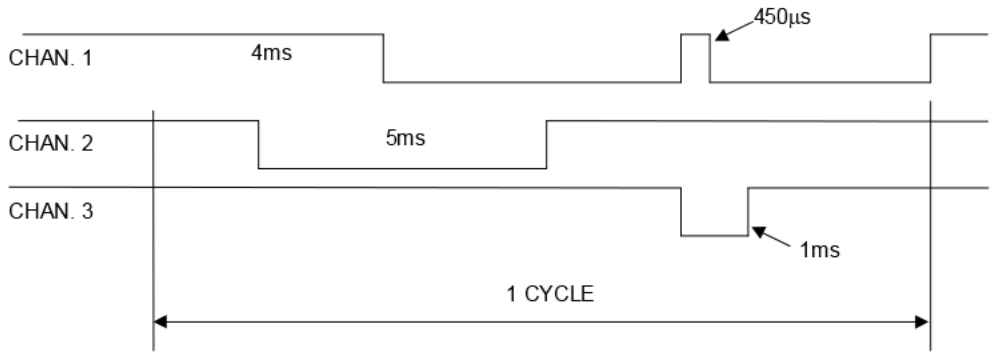
Figure 14. Waveform Definition Example

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4.3.3 Programming Examples

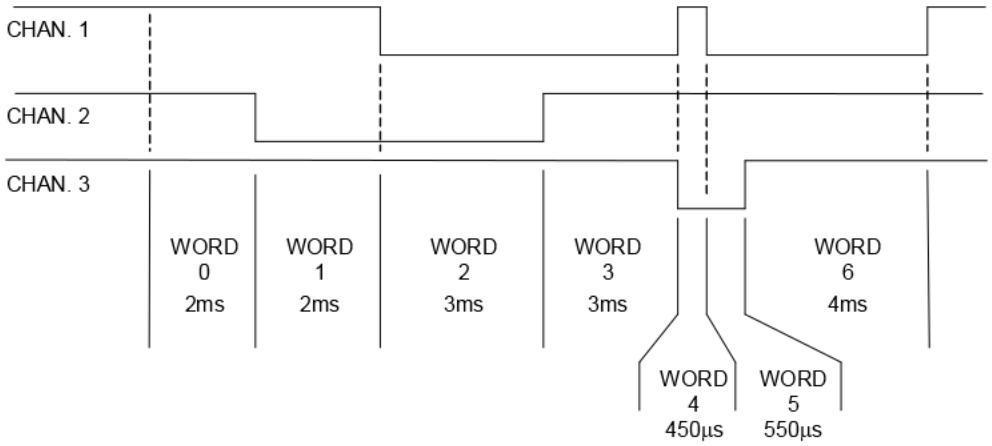
Example 1:

Step 1: Draw the desired timing waveforms.



NOTE: THIS EXAMPLE UTILIZES ONLY 3 OF THE 16 AVAILABLE OUTPUT CHANNELS.

Step 2 and 3: Partition the waveforms at every logic transition on all channels, and define the memory words and time intervals.



This defines the programming, as each partition will define the time and associated data for each programmed word.

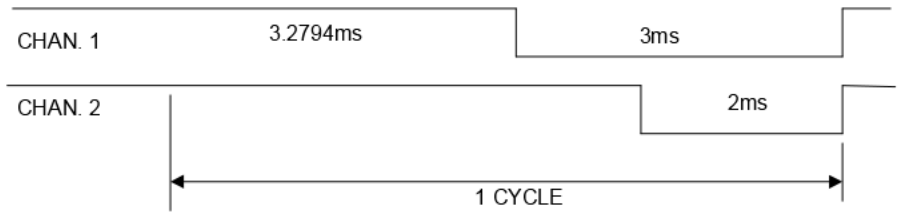
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The memory and control registers would be configured as follows:

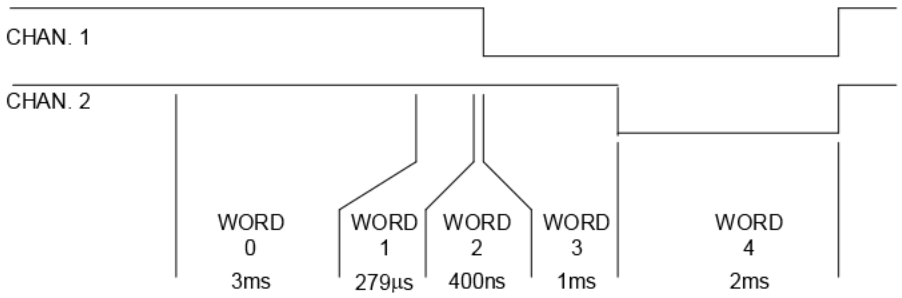
Register Description	Reg., hex	Value, hex	Comments
Start Pointer	06	0000	
End Pointer	08	0006	7 memory words
Output Configuration	0C	02XX	External Clock, OWC & WS = Don't Care
User Address	18	0000	
User Data (Memory Addr 0)	1A	8008	2ms = 250µs(0x8) × 8(0x8)
User Data (Memory Addr 1)	1A	0007	
User Data (Memory Addr 2)	1A	8008	2ms = 250µs(0x8) × 8(0x8)
User Data (Memory Addr 3)	1A	0005	
User Data (Memory Addr 4)	1A	800C	3ms = 250µs(0x8) × 12(0xC)
User Data (Memory Addr 5)	1A	0004	
User Data (Memory Addr 6)	1A	800C	3ms = 250µs(0x8) × 12(0xC)
User Data (Memory Addr 7)	1A	0006	
User Data (Memory Addr 8)	1A	6012	450µs = 25µs(0x6) × 18(0x12)
User Data (Memory Addr 9)	1A	0003	
User Data (Memory Addr 10)	1A	6016	550µs = 25µs(0x6) × 22(0x16)
User Data (Memory Addr 11)	1A	0002	
User Data (Memory Addr 12)	1A	8010	4ms = 250µs(0x8) × 16(0x10)
User Data (Memory Addr 13)	1A	0006	
User Address	18	0001	Set to Start Pointer + 1
Control/Status	00	0015	Software Run, TS mode, Sync On Addr, Cont. Cycle, Run

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Example 2: In some cases the desired timing intervals may not be a multiple of the time register and multiplying factor.



This may be programmed by using several words then serially cascading the time intervals while leaving the data unchanged.



Thus, in this case the timing partitions do not always occur at the logic transitions.

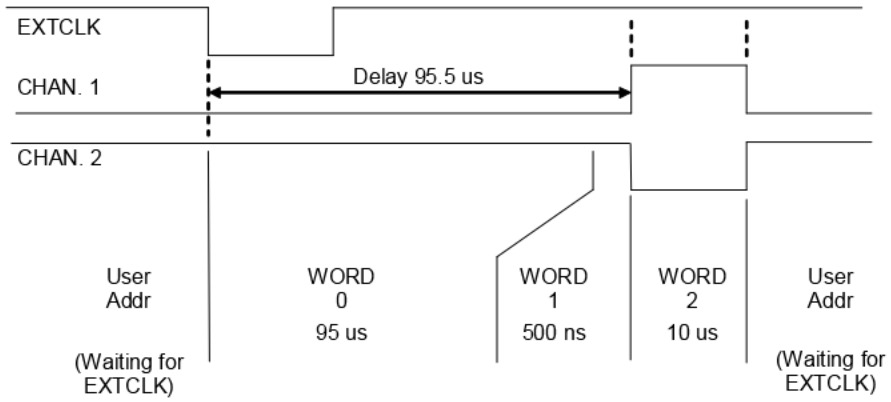
The memory and control registers would be configured as follows:

Register Description	Reg., hex	Value, hex	Comments
Start Pointer	06	0000	
End Pointer	08	0004	5 memory words
Output Configuration	0C	02XX	External Clock, OWC & WS = Don't Care
User Address	18	0000	
User Data (Memory Addr 0)	1A	800C	3ms = 250µs(0x8) × 12(0xC)
User Data (Memory Addr 1)	1A	0003	
User Data (Memory Addr 2)	1A	245C	279µs = 250ns(0x2) × 1116(0x45C)
User Data (Memory Addr 3)	1A	0003	
User Data (Memory Addr 4)	1A	0010	400ns = 25ns(0x0) × 16(0x10)
User Data (Memory Addr 5)	1A	0003	
User Data (Memory Addr 6)	1A	8004	1ms = 250µs(0x8) × 4(0x4)
User Data (Memory Addr 7)	1A	0002	
User Data (Memory Addr 8)	1A	8008	2ms = 250µs(0x8) × 8(0x8)
User Data (Memory Addr 9)	1A	0000	
User Address	18	0001	Set to Start Pointer + 1
Control/Status	00	0015	Software Run, TS mode, Sync On Addr, Cont. Cycle, Run

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Example 3: Digital Delay Generator

The timing simulator may prove useful as a digital delay generator when used in single cycle mode. In this example an external pulse (EXTCLK) starts the delay. The simulator then processes the required memory words to generate the delay and the output pulse or pulses.



The memory and control registers would be configured as follows:

Register Description	Reg., hex	Value, hex	Comments
Start Pointer	06	0000	
End Pointer	08	0002	4 memory words
Output Configuration	0C	02XX	External Clock, OWC & WS = Don't Care
User Address	18	0000	
User Data (Memory Addr 2)	1A	4026	95µs = 2.5µs(0x4) × 38(0x26)
User Data (Memory Addr 3)	1A	0002	
User Data (Memory Addr 4)	1A	2002	500ns = 250ns(0x2) × 2(0x2)
User Data (Memory Addr 5)	1A	0002	
User Data (Memory Addr 6)	1A	4004	10µs = 2.5µs(0x4) × 4(0x4)
User Data (Memory Addr 7)	1A	0001	
Loop Counter	1C	0001	1 loop
User Address	18	0001	Set to Start Pointer + 1
Control/Status	00	0317	External Clock, TS mode, Sync On Addr, Single Cycle

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APPENDIX A: CONNECTORS

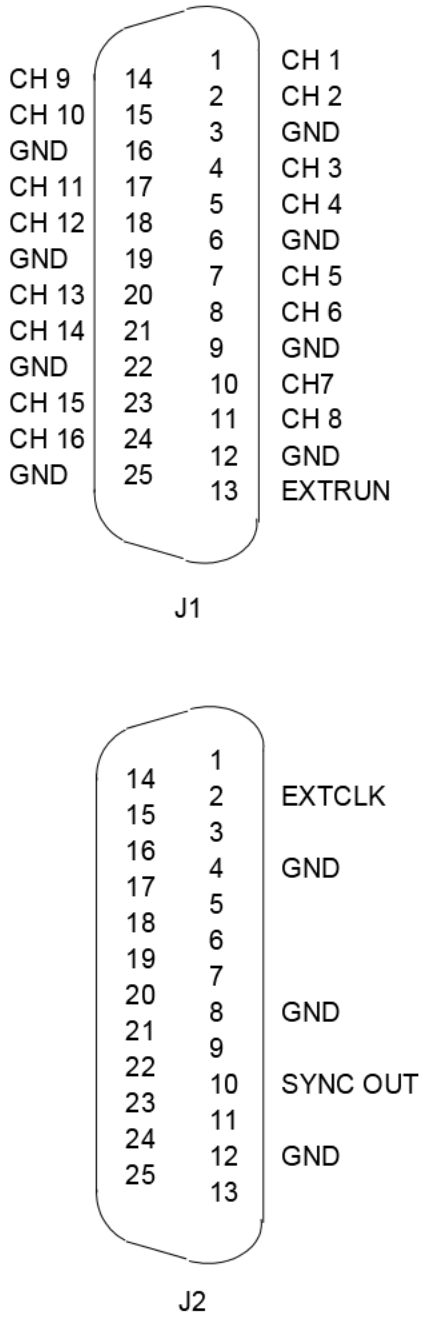


Figure A-1. Front Panel I/O Signals

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Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	/DREQ	(D20)
7	A06	/DACK	(D21)
8	A07	GND	(D22)
9	D08	D00/A08	TRIGA
10	D09	D01/A09	TRIGB
11	D10	D02/A10	(D23)
12	D11	D03/A11	(D24)
13	D12	D04/A12	(D25)
14	D13	D05/A13	(D26)
15	D14	D06/A14	(D27)
16	D15	D07/A15	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	/DS2

Notes: Signals in parentheses ( ) are not used on this module. M/MA Interface Connector B is not used.

Figure A-2. M/MA Interface Connector Configuration

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