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# U S E R  M A N U A L

# VXI
# INDUSTRYPACK®
# CARRIER

# MODEL
# VX403B/C

Manual Part No: 11027004A

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# INTRODUCTION

This manual describes the operation and use of the C&H Model VX403B/C IndustryPack Carrier (Part Numbers 11027000/11027040). This module is one of a number of test and data acquisition/control modules in the VME and VXI format provided by C&H.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.



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## 1.0 GENERAL DESCRIPTION

The VX403B/C is a single slot register-based B/C-size VXIbus compatible carrier module that provides electrical and mechanical support for four single high or two double high IndustryPack® (IPs).

### 1.1 PURPOSE OF EQUIPMENT

This module provides a carrier function for a variety of plug-in modules that vary in functionality from A/D converters, Digital Input/Output, Serial Interfaces, to Memory devices.

### 1.2 SPECIFICATIONS OF EQUIPMENT

#### 1.2.1 Key Specifications

- Up to four (4) Industry Standard IndustryPacks supported
- Individual Logical Addressing of IndustryPacks
- Separate Software Programmable Interrupt Levels
- Isolated and filtered +5V, +12V, and -12V supplies for each IndustryPack
- Front panel connectors for individual IP I/O signal access
- IP input strobe signals can be connected to any VXI TTL Trigger Line allowing IP synchronization
- Both A24 and A32 addressing supported

#### 1.2.2 Electrical

The VX403B/C requires the +5V and +12V power from the VXI back plane. The carrier's peak module current ($I_{PM}$) for the +5 volt supply is 1.2 amps. The ±12 volt supply is not used by the carrier, but may be required by an installed IP. For electrical information on individual IP's, please reference each IP's documentation. The power requirements for each IP installed must be added to these requirements for the total module's requirements.

#### 1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with the VXIbus specification Rev. 1.4 for single slot modules.

'B' Size: The nominal dimensions are 233.35 (9.187 in) high x 160 mm (6.299 in) deep. The module is designed for a mainframe with 20.32 mm (0.8 in) spacing between slots. As required by the VXI bus specification, these dimensions are in accordance with those given in the VME bus specification (Rev. C.1).

'C' Size: The nominal dimensions are 233.35 (9.187 in) high x 340 mm (13.386 in) deep.



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### 1.2.4 Environmental

The environmental specifications of the module are:

| | |
|---|---|
| Operating Temperature: | 0°C to +55°C |
| Storage Temperature: | -40°C to +75°C |
| Humidity: | <95% without condensation |

Installed IPs may differ in environmental specification. Refer to each individual IP's documentation for information.

### 1.2.5 Bus Compliance

The module complies with the VXIbus Specification Revision 1.4 for B/C-size register based modules and with VMEbus Specification ANSI/IEEE STD 1014-1987, IEC 821.

| | |
|---|---|
| Manufacturer ID: | $FC1_{16}$ |
| Model Code: | 'B' size: $FF7_{16}$ |
| | 'C' size: $FF5_{16}$ |
| Access Type: | Register Based |
| Addressing: | A16/A24/A32 |
| Data Transfer: | D8/D16 |
| Sysfail: | supported |
| Interrupts: | IP dependent, programmable levels |
| Bus Arbitration: | BRx tied to BGx |
| Local Bus: | not used |
| TTL Triggers | supported |
| Memory Requirements: | IP dependent |



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## 2.0 INSTALLATION

### 2.1 UNPACKING AND INSPECTION

In most cases the VX403B/C is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the carrier immediately as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

### 2.2 HANDLING PRECAUTIONS

The VX403B/C contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

### 2.3 INSTALLATION OF INDUSTRYPACKS

All IndustryPacks must be installed before the VX403B/C is installed into the VXI system. IndustryPacks are installed by firmly pressing the two connectors on the IP together with the connectors on the carrier. The connectors are keyed to insure the IP can only be installed correctly. Mounting hardware may be provided with the IP, if so follow mounting instructions provided by IP.

There are four possible mounting locations on the carrier: A, B, C, and D. IndustryPacks may be installed into any of the four slots, provided that slot is enabled. Enabling an IP slot is done by following the Hardware Configuration in Section 4.2.1.

Required Memory Switches must be set to their proper values for each IP installed. If an IP does not require memory, these switches should be left in the default position These switches should be set as outlined in Section 4.2.1.

### 2.3 INSTALLATION OF VX403B/C CARRIER

**CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.**

Set the module's logical address and addressing mode as described in Section 4.2.1. Insert the module into the appropriate slot according to the desired priority. Apply power. If no obvious problems exist, proceed to communicate with the module as outlined in Section 4.0 (Operating Instructions).



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## 2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.



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## 3.0 FUNCTIONAL DESCRIPTION

### 3.1 GENERAL

The VX403B/C carrier provides a mechanical and electrical interface between a VXIbus system and four standard IndustryPack modules. The carrier provides VXI register configuration and access to the IndustryPack's ID PROM, I/O Space, and memory (if present). Each IndustryPack is controlled separately and appears as a different Logical Address in the VXI environment. A simplified block diagram of the module is shown in Figure 1.

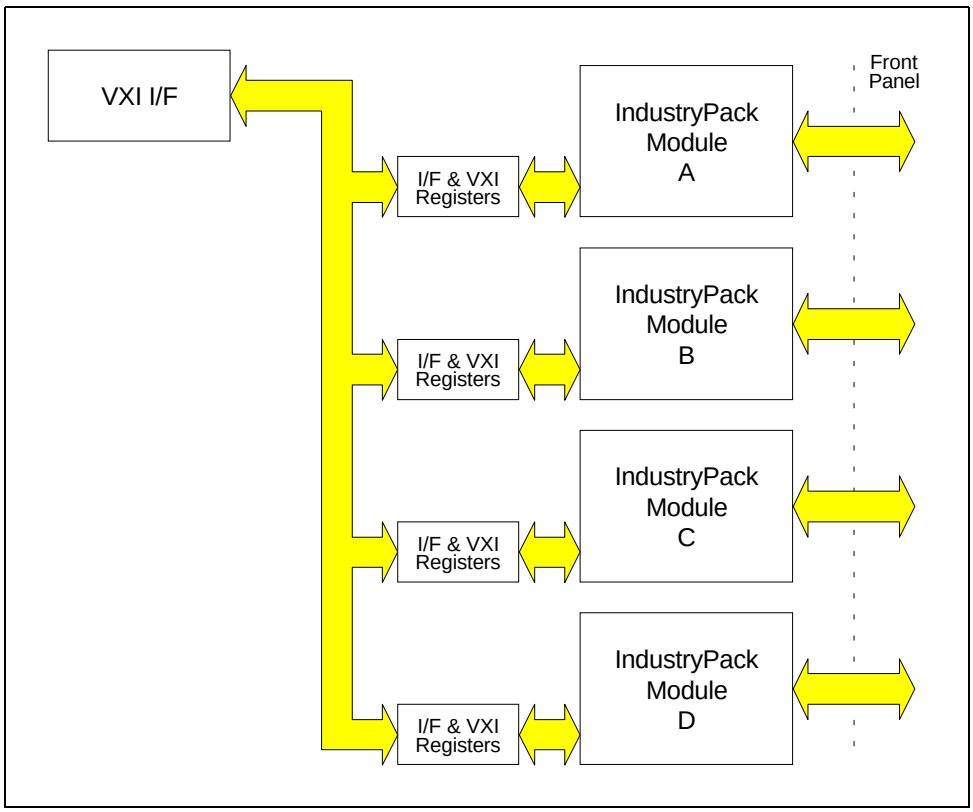



**Figure 1. Functional Block Diagram**

### 3.2 INTERFACES

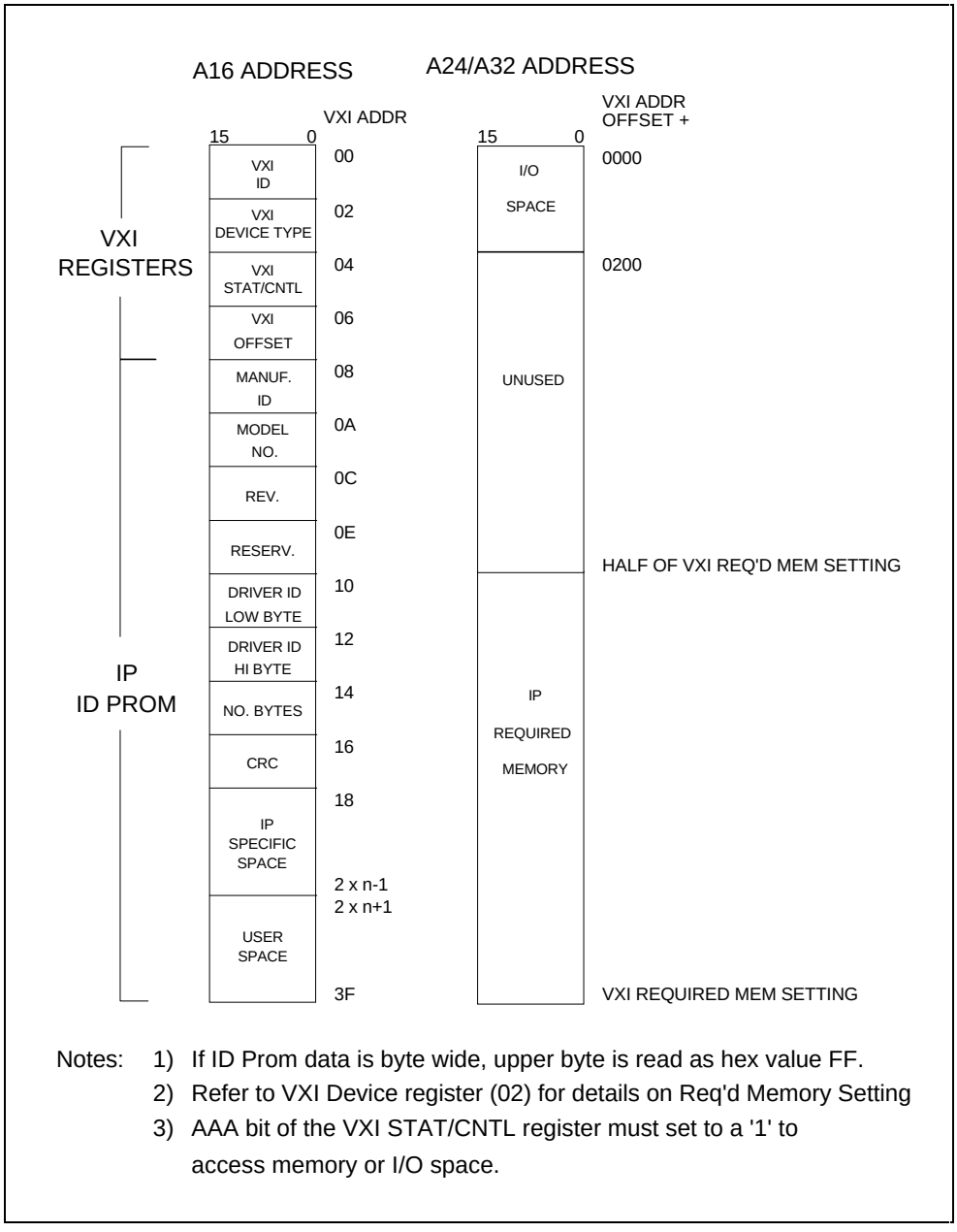
The four IP positions (slots) interface electrically and mechanically with industry standard IndustryPack module meeting the IndustryPack Logic Interface Specification Revision 0.7.1. Each IP interfaces with a 50-pin header that accepts standard IDC sockets and is accessible through the front panel of the VX403B/C.



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## 3.3 I/O AND MEMORY ADDRESSING

The VX403B/C supports both D16 and D8(Even/Odd) data access and A16, A24, and A32 addressing. The VXI registers and ID PROM data of the IPs are accessible in the A16 address space. The ID PROM data is mapped to the upper part of the VXI 64-byte allocation space. Only the low (odd) bytes of the ID PROM contain valid data. The VXI Offset Register is used to map the IP's I/O Space and Memory (if applicable) into the A24 or A32 addressing space. For IP's that support both I/O Space and Memory, the memory begins at the mid-point of the total memory switch setting as shown in Figure 2.




Notes:
1) If ID Prom data is byte wide, upper byte is read as hex value FF.
2) Refer to VXI Device register (02) for details on Req'd Memory Setting
3) AAA bit of the VXI STAT/CNTL register must set to a '1' to access memory or I/O space.

**Figure 2. Memory Organization**



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## 3.4 INTERRUPTS

Each IP can support up to two interrupt requests as specified in the IndustryPack Logic Interface Specification. Each interrupt can be programmed to an individual interrupt level and is handled separately during interrupt acknowledge cycles. A hardware priority for each interrupt level begins with IP A's Interrupt 0 being the highest priority and IP D's Interrupt 1 being the lowest priority.

Individual IndustryPacks provide their own upper byte of the interrupt vector and the interrupt request release mechanism, release on register access (RORA) or release on acknowledge (ROAK). This allows independent control of interrupts.

## 3.5 HARDWARE CONFIGURATION

Logical Address Each IP slot has its own logical address based on a six position switch and the table provided below. The six positions of the switch represent the most significant six bits of the eight bit logical address value. The least significant bits are a fixed value as listed in the table.

IndustryPack Slot A $\Rightarrow$ *switch setting*$_2$ + $00_2$
IndustryPack Slot B $\Rightarrow$ *switch setting*$_2$ + $01_2$
IndustryPack Slot C $\Rightarrow$ *switch setting*$_2$ + $10_2$
IndustryPack Slot D $\Rightarrow$ *switch setting*$_2$ + $11_2$

The switch location is shown in Figure 3.

IndustryPack Enable Four switches are provided to enable the individual IP slots. Each switch corresponds to an IP slot and must be enabled before the carrier will recognize an IP present. These switches are the first 4 positions of an 8 position switch as shown in Figure 3. The remaining four switches are reserved and should be kept in the OFF position.

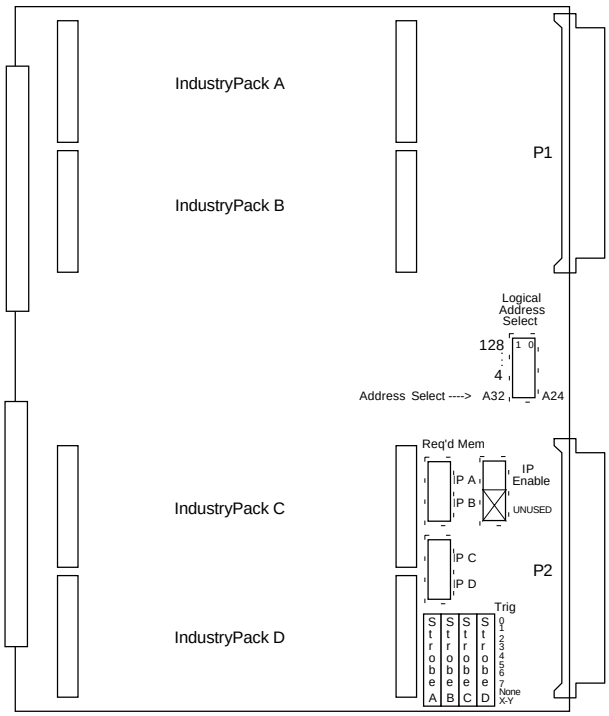
Required Memory Four switches are provided for each IP that allows required memory to be configured for each IP. These switches are combined into two 8-switch packages. The switch locations are shown in Figure 3.

Address Space A single switch is provided that selects either A24 or A32 addressing. This switch is located at position 8 of the logical address switch.

IP Strobe Signals A bank of jumper links or a sliding switch is provided for each IP in order to select a desired input trigger or clock signal using the VXI TTL Trigger lines. If an IP utilizes the optional Strobe, any of the VXI TTL Trigger lines can be configured to control this signal. All IPs on the carrier board can be synchronized by using a single trigger line connected to all IPs.

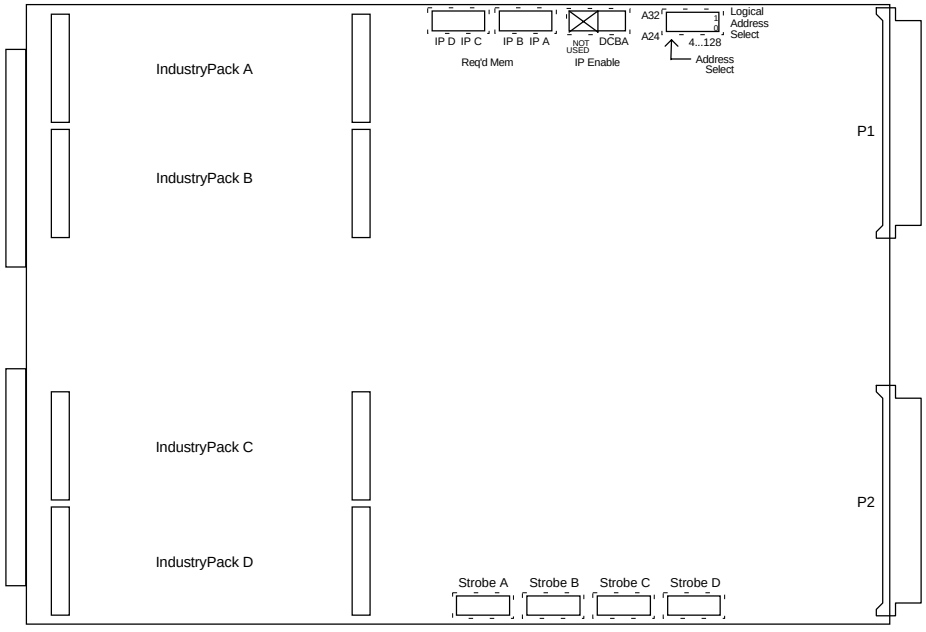


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'B' Size

Note: Additional details on configuring the hardware switches and jumpers may be found in 4.2, Hardware Configuration.




'C' Size

**Figure 3. Hardware Configurable Controls**



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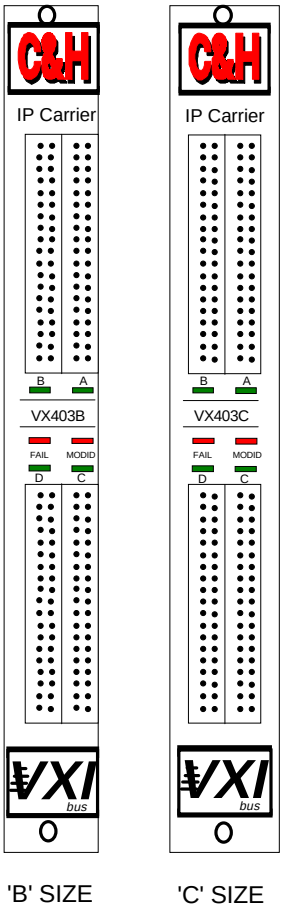



**Figure 4. Front Panel**

## 3.6 INDICATORS

Six LED indicators are provided on the front panel. Their functions are:

FAIL: This front panel LED indicates the PASS/FAIL (SYSFAIL) status. The LED illuminates during reset, initialization, or if there is a failure on the VX403B/C Carrier itself.

MODID: This front panel LED illuminates whenever the host processor applies the MODID signal to the slot the module is occupying.

A, B, C, D: These front panel LEDs illuminate whenever that IP is properly accessed by the host processor.



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## 3.7 CONNECTORS

### 3.7.1 Front Panel Connector

The front panel connectors are 50-pin × 2, stacked "condo" type headers with long ejector latches (3M part number: 3433-D302). These connectors mate with standard IDC sockets and provide a one-to-one connection to the IP's I/O connector with pin one connected to pin one. Refer to the IP documentation for the definition of the I/O signals.

### 3.7.2 Rear Connectors

The P1 and P2 connectors are configured in accordance with the VXI specification. (See Appendix A)

## 3.8 CONFIGURATION REGISTERS

There are a variety of registers used to configure and control the VX403B/C module. The VXI configuration registers provide for control and status as required by the VXIbus specification. The IP ID PROM registers provide information specific to the installed IndustryPack. An address map of the registers is shown in Table I.

**Table I. VXI Register Address Map**

| A16 Address | Register Description | |
|---|---|---|
| Base + 00 | VXI ID | |
| Base + 02 | VXI Device Type | |
| Base + 04 | VXI Status/Control | |
| Base + 06 | VXI Offset Register | |
| Base + 08 | IP Manufacturer ID | |
| Base + 0A | IP Model Number | |
| Base + 0C | IP Revision | |
| Base + 0E | Reserved | Low (odd) Byte Only |
| Base + 10 | IP Driver ID (low byte) | |
| Base + 12 | IP Driver ID (high byte) | |
| Base + 14 | IP Number of Bytes Used, n | |
| Base + 16 | IP CRC | |
| Base + 18 | IP Specific Space | |
| Base + $(2 \times n + 1)$ | IP User Space | |



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### 3.8.1 VXI Configuration Registers

The VXI configuration registers contain basic information needed to configure a VXIbus system. The configuration information includes: manufacturer identification, product model code, device type, memory requirements, device status, and device control. The registers are briefly described below and are detailed in Figure 5.

VXI Identification (ID) Register (Base + $00_{16}$) This read-only register provides the carrier manufacturer identification, device classification (i.e., register based), and the addressing mode (i.e. A32).

VXI Device Type Register (Base + $02_{16}$) This read-only register provides the carrier model code identifier and the IP required memory configuration.

VXI Status/Control Register (Base + $04_{16}$) A read of this register provides the state of P2 MODID* line, the interrupt level for each IP interrupt, SYSFAIL inhibit status, and the Ready and self-test Passed status. A write to this register controls the interrupt level for each IP interrupt, the disabling of the SYSFAIL function, and resetting of the module.

This register also provides a control bit in order to enable writes to the IP ID PROM for future considerations. This bit must be set to a '1' in order to read the IP ID PROM.

VXI Offset Register (Base + $06_{16}$) This read/write register controls the offset value for addressing the IP I/O space and memory.



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## VXI ID

00

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read Only | Device Class | | Address Space | | Manufacturer ID | | | | | | | | | | | |

Device Class ⇨ Device Class (11 = Register Based)
Address Space ⇨ Address Space (00 = A16/A24, 01 = A16/A32, 10 = reserved, 11 = A16 Only)
Manuf. ID ⇨ Manufacturer Identification ($FC1_{16}$ = C & H Technologies)

## VXI Device Type

02

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read Only | Required Memory | | | | Model Code | | | | | | | | | | | |

Model Code ⇨ Model code (VX403B = $FF7_{16}$ , VX403C = $FF5_{16}$)

VXI Required Memory setting ⇨ required memory setting = $256^{a} \times 2^{(23-m)}$, where *a* = Address Space value in VXI ID register and *m* = Required Memory value )

| Mem Rq'd by IP | A32 Settings (VXI Mem) | A24 Settings (VXI Mem) |
|---|---|---|
| 0 bytes | F (64K) | F (256 bytes) |
| 128 bytes | F (64K) | F (256 bytes) |
| 256 bytes | F (64K) | E (512 bytes) |
| 512 bytes | F (64K) | D (1K) |
| 1K | F (64K) | C (2K) |
| 2K | F (64K) | B (4K) |
| 4K | F (64K) | A (8K) |
| 8K | F (64K) | 9 (16K) |
| 16K | F (64K) | 8 (32K) |
| 32K | F (64K) | 7 (64K) |
| 64K | E (128K) | 6 (128K) |
| 128K | D (256K) | 5 (256K) |
| 256K | C (512K) | 4 (512K) |
| 512K | B (1M) | 3 (1M) |
| 1M | A (2M) | 2 (2M) |
| 2M | 9 (4M) | 1 (4M) |
| 4M | 8 (8M) | 0 (8M) |
| 8M | 7 (16M) | - |

**Figure 5. VXI Configuration Registers**



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## VXI Status/Control

04

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | AAA | - | ID | 1 | 1 | ILVL1 | | | 1 | ILVL0 | | | - | - | SI | RST |
| Read | AAA | MID | ID | 1 | 1 | ILVL1 | | | 1 | ILVL0 | | | RDY | Pass | 0 | 0 |

AAA ⇨ A24/A32 Access (0 = disabled)
MID ⇨ Module ID Status (0 = P2 MODID* line is selected)
ID ⇨ ID Prom read enable (1 = enabled, 0 =read disabled/write enabled)
ILVL1 ⇨ One's compliment of the Interrupt Level for IP Interrupt 1 ( 7 = interrupts disabled, 6 = IRQ1, 5=IRQ2, etc.)
ILVL0 ⇨ One's compliment Interrupt Level for IP Interrupt 0 (IRQ 7 = interrupts disabled, 6 = IRQ1, 5=IRQ2, etc.)
RDY ⇨ Ready (1 = ready)
Pass ⇨ Pass/fail indicator (0 = executing or failed, 1 = passed)
SI ⇨ Sysfail Inhibit (1 = inhibit)
RST ⇨ Reset (writing a '1' to this bit resets the IP module; after a minimum 100 µs a '0' must be written to resume normal operation)

## VXI Offset Register

06

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | Offset Value | | | | | | | | | | | | | | | |
| Read | Offset Value | | | | | | | | | | | | | | | |

Offset Value ⇨ Offset to IndustryPack's I/O Space and Memory (if applicable)

**Figure 5. VXI Configuration Registers (continued)**



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### 3.8.2 IndustryPack ID PROM Registers

The IP ID PROM data is mapped to register addresses base + $08_{16}$ to base + $3F_{16}$. The register contents are specified fully in the documentation for a specific IndustryPack and is summarized below. Only the lower (odd) byte is used. The high byte is always $FF_{16}$.

The ID control bit in the Status/Control Register allows for writes to an IP's ID PROM. If ID PROM writes are supported by a particular IP, then setting the ID bit to logical level '0' will enable the write. The ID bit must, however, be set to '1' in order to read an IP's ID PROM. By default ID is read only (ID = 1).

IP Manufacturer ID (base + $08_{16}$) This read-only register provides the Manufacturer ID number of the IP. It is assigned by GreenSpring Computers, Inc.

IP Model Number (base + $0A_{16}$) This read-only register provides the Model Number of the IP. It is set by the manufacturer of the IP.

IP Revision (base + $0C_{16}$) This read-only register provides the Revision of the IP. It is set by the manufacturer of the IP.

IP Driver ID (base + $10_{16}$ & $12_{16}$) These read-only registers provide a 16-bit identifier for the software driver for the IP.

IP Number of Bytes Used (base + $14_{16}$) This read-only register specifies the number of bytes that are used in the ID PROM for fixed data and IP specific data.

IP CRC (base + $16_{16}$) This read-only register provides an 8-bit correction code checksum that can be used to verify that the information in the ID PROM is being read correctly. The CRC is low 8-bits of the FCS as described in CCITT T.30 (Fascicle VII.3) section 5.3.7.



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## 4.0 OPERATING INSTRUCTIONS

### 4.1 GENERAL

The VX403B/C is configured through a series of hardware switches and software controlled registers as described in Section 4.2.1. The switches enable the IP slots, configure the logical addresses of the IPs, and set the memory required by each IP. The VX403B/C has one software controlled register for each IP. Each one provides configuration for interrupts, A24/A32 access, and status for it's IP. All other IP controls are dependent on a specific IP and reside on that IP.

### 4.2 CONFIGURATION

#### 4.2.1 Hardware Configuration

**CAUTION: All hardware configurations must be done only while the power to the module is OFF.**

Logical Address The logical address switch sets the base logical address for the four IPs supported by the carrier. The switch has a range of 4 to 255. Any multiple of four within this range is valid, but care should be taken not to set any of the four logical addresses in this block the same as another module in the system. Position 1 on the switch is the most significant bit and has a weighted value of 128 when the switch is in the off position. Position 6 on the switch is the least significant bit and has a weighted value of 4 when the switch is in the off position. Positions 7 and 8 do not affect the logical address, and their represented bits are replaced by the table given below. The sum of the weighted values of all the switches in the off position along with the values in the table below give the IPs' logical address.

IndustryPack A $\Rightarrow$ *Base Logical Address* + 0
IndustryPack B $\Rightarrow$ *Base Logical Address* + 1
IndustryPack C $\Rightarrow$ *Base Logical Address* + 2
IndustryPack D $\Rightarrow$ *Base Logical Address* + 3

IndustryPack Enable Four switches are provided to enable the individual IP slots. Each switch represents an IP and must be enabled before the carrier will recognize an IP as present. This switch is position 1- 4 of an 8-position switch and corresponds to IP slots A - D respectively. When the switch is in the OFF (open) position the IP slot is disabled. Conversely, the IP is enabled when the switch is ON (closed) position.

Address Select A single switch is provided that selects either A24 or A32 addressing. This switch is located in position 8 of the logical address switch. The OFF position of this switch corresponds to A32 and the ON position to A24.



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Required Memory Setting For IPs that require memory, a set of four switches is provided for each IP. Each set of switches corresponds to half of an 8-switch package and is located as shown in Figure 3. Switch configuration is referenced as a four bit hexadecimal value with switches 8 and 4 being the least significant bit. Switches in the OFF position are logical level '1' and switched in the ON position are logical level '0'.

VXI required memory configuration should always be set to twice the IP required memory, which allows for mapping of the I/O Space into A24/A32 addressing. IP I/O space occupies the lower 128 bytes of the VXI allocated memory beginning at address *Offset* + 0000. IP required memory is mapped into the upper half of the required memory setting, with it's beginning address at the mid-point of the total memory set. Memory switch settings are based on an IP's required memory and the formula given in the VXI Device Type Register description. Proper switch settings are given in the table provided under the VXI Device register description in Figure 5.

IP Strobe Signals If the optional Strobe signal is utilized by an IP, any of the eight VXI TTL Trigger lines can be connected as an input for this signal. A bank of jumpers or a sliding switch is provided for each IP. Moving the jumper (or switch slide) to a numbered location selects that TTL Trigger line as the input. All IPs can be connected to the same trigger line to synchronize the IPs. Additionally, adjacent IP strobe signals may be connected by moving the jumper (or switch slide) to the position marked X-Y (or A-B, B-C, C-D, or D-A). This option is only useful on IP's that support an output strobe signal.

### 4.2.2 Software Configuration

The Status/Control register is 16-bits wide and may be accessed as D8(Even/Odd) or D16. Each IP has its own VXI Status/Control register and is accessed at the same address location ($04_{16}$). The AAA bit (bit 15) must be set high in order to access the IP's Memory or I/O Space. The ID bit (bit 13) must be set high in order to read the ID Prom of an IP. Future capability to write to the ID Prom, on IPs that support this feature, is possible by setting this bit low. The IP interrupt levels are set in this register and are explained in section 4.. All other software control of an IP is IP dependent and is described in the IP's user manual.

## 4.3 INTERRUPTS

The IndustryPack Specification specifies that an IP may generate up to two interrupts. Each interrupt has its own user programmable level set by writing the three-bit one's complement of the desired VXI IRQ level into the appropriate location in the Status/Control register. For example, IP interrupt 0 level is specified in bits 4-6 and IP interrupt 1 level is specified in bits 8-10. Writing a seven (all '1s') disables the interrupt and a setting of *011* sets the level to 4.

The interrupt vector returned during an interrupt acknowledge cycle consist of the IP's logical address in the low byte and an upper byte set by the IP. The setting of the upper byte is different for various IPs, see the IPs user's manual for details. The VX403B/C supports both release on acknowledge (ROAK) and release on register access (RORA). The release mechanism is dependent on the IP.



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## 4.4 UNSUPPORTED IP OPERATIONS

This carrier is NOT a processor based IP carrier, and may not support all functions supported by an IP. For instance, the VX403B/C does not support Direct Memory Access(DMA) or 32-bit wide data with double-sized IPs.



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## 5.0 TROUBLE ANALYSIS

### 5.1 BUILT IN TEST AND DIAGNOSTICS

During power-up initialization, a basic built-in test function is performed. If an initialization failure is detected, the SYSFAIL lamp will light indicating a failure. Sysfail Inhibit can be used to help isolate the cause of the failure.

Enable Sysfail Inhibit and read the Status/Control register.

If a proper value can be read, then verify that the socketed PLCC Xilinx chip and part 11027012 are completely seated in their sockets by first turning off the power and then firmly pressing around the edges of the parts. Verify that the VX403B/C is installed into the VXI system properly, recycle power, and look for SYSFAIL again. If the SYSFAIL LED is illuminated again, please contact C&H.

If after enabling Sysfail Inhibit a proper Status/Control register cannot be read, turn off power and insure that parts 11027013 and 11027015, and the VX403B/C are all firmly installed. Recycle power and if SYSFAIL is still present, please contact C&H.

### 5.2 TROUBLE ANALYSIS GUIDE

The following is a general guide of the most common problems that may be encountered with the VX403B/C, along with a suggestion of the possible causes.

| SYMPTOMS | POSSIBLE CAUSES |
|---|---|
| Bus time out on A16 Access | 1. Logical address incorrectly set.<br>2. Card incorrectly installed.<br>3. IP enable switch set incorrectly. |
| Unable to read IP ID Prom, but can access required VXI registers (0-6) | 1. Incorrectly addressed.<br>2. IP not properly installed. |
| Unable to access IP memory/IO space, but can read ID Prom | 1. Attempting to access an improper address.<br>2. VXI memory switch setting for that IP not set to 2 × IP's required memory.<br>3. AAA bit of Stat/Cntl register not set to allow A32/A24 addressing.<br>4. A24/A32 switch set improperly. |



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# APPENDIX A - CONNECTORS

| PIN | C | B | A |
|---|---|---|---|
| 1 | D08 | - | D00 |
| 2 | D09 | - | D01 |
| 3 | D10 | - | D02 |
| 4 | D11 | BG0IN* | D03 |
| 5 | D12 | BG0OUT* | D04 |
| 6 | D13 | BG1IN* | D05 |
| 7 | D14 | BG10UT* | D06 |
| 8 | D15 | BG2IN* | D07 |
| 9 | GND | BG20UT* | GND |
| 10 | SYSFAIL* | BG3IN* | - |
| 11 | - | BG3OUT* | - |
| 12 | SYSRESET* | - | DS1* |
| 13 | LWORD* | - | DS0* |
| 14 | AM5 | - | WRITE* |
| 15 | A23 | - | - |
| 16 | A22 | AM0 | DTACK* |
| 17 | A21 | AM1 | _ |
| 18 | A20 | AM2 | _ |
| 19 | A19 | AM3 | _ |
| 20 | A18 | GND | IACK* |
| 21 | A17 | - | IACKIN* |
| 22 | A16 | - | IACKOUT* |
| 23 | A15 | GND | AM4 |
| 24 | A14 | IRQ7* | A07 |
| 25 | A13 | IRQ6* | A06 |
| 26 | A12 | IRQ5* | A05 |
| 27 | A11 | IRQ4* | A04 |
| 28 | A10 | IRQ3* | A03 |
| 29 | A09 | IRQ2* | A02 |
| 30 | A08 | IRQ1* | A01 |
| 31 | +12 V | - | -12 V |
| 32 | +5 V | +5 V | +5 V |

**Figure A-1. P1 Pin Configuration**



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| PIN | C | B | A |
|---|---|---|---|
| 1 | - | +5V | - |
| 2 | - | GND | - |
| 3 | GND | - | - |
| 4 | - | A24 | GND |
| 5 | - | A25 | - |
| 6 | - | A26 | - |
| 7 | GND | A27 | - |
| 8 | - | A28 | - |
| 9 | - | A29 | - |
| 10 | GND | A30 | GND |
| 11 | - | A31 | - |
| 12 | - | GND | - |
| 13 | - | +5V | - |
| 14 | - | - | - |
| 15 | - | - | - |
| 16 | GND | - | GND |
| 17 | - | - | - |
| 18 | - | - | - |
| 19 | - | - | - |
| 20 | - | - | - |
| 21 | - | - | - |
| 22 | GND | GND | GND |
| 23 | TTLTRG1* | - | TTLTRG0* |
| 24 | TTLTRG3* | - | TTLTRG2* |
| 25 | GND | - | +5V |
| 26 | TTLTRG5* | - | TTLTRG4* |
| 27 | TTLTRG7* | - | TTLTRG6* |
| 28 | GND | - | GND |
| 29 | - | - | - |
| 30 | GND | - | MODID |
| 31 | - | GND | GND |
| 32 | - | +5V | - |

**Figure A-2. P2 Pin Configuration**



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IP B

| | |
|---|---|
| I/O 50 | I/O 49 |
| I/O 48 | I/O 47 |
| I/O 46 | I/O 45 |
| I/O 44 | I/O 43 |
| I/O 42 | I/O 41 |
| I/O 40 | I/O 39 |
| I/O 38 | I/O 37 |
| I/O 36 | I/O 35 |
| I/O 34 | I/O 33 |
| I/O 32 | I/O 31 |
| I/O 30 | I/O 29 |
| I/O 28 | I/O 27 |
| I/O 26 | I/O 25 |
| I/O 24 | I/O 23 |
| I/O 22 | I/O 21 |
| I/O 20 | I/O 19 |
| I/O 18 | I/O 17 |
| I/O 16 | I/O 15 |
| I/O 14 | I/O 13 |
| I/O 12 | I/O 11 |
| I/O 10 | I/O 9 |
| I/O 8 | I/O 7 |
| I/O 6 | I/O 5 |
| I/O 4 | I/O 3 |
| I/O 2 | I/O 1 |

IP A

| | |
|---|---|
| I/O 50 | I/O 49 |
| I/O 48 | I/O 47 |
| I/O 46 | I/O 45 |
| I/O 44 | I/O 43 |
| I/O 42 | I/O 41 |
| I/O 40 | I/O 39 |
| I/O 38 | I/O 37 |
| I/O 36 | I/O 35 |
| I/O 34 | I/O 33 |
| I/O 32 | I/O 31 |
| I/O 30 | I/O 29 |
| I/O 28 | I/O 27 |
| I/O 26 | I/O 25 |
| I/O 24 | I/O 23 |
| I/O 22 | I/O 21 |
| I/O 20 | I/O 19 |
| I/O 18 | I/O 17 |
| I/O 16 | I/O 15 |
| I/O 14 | I/O 13 |
| I/O 12 | I/O 11 |
| I/O 10 | I/O 9 |
| I/O 8 | I/O 7 |
| I/O 6 | I/O 5 |
| I/O 4 | I/O 3 |
| I/O 2 | I/O 1 |

IP D

| | |
|---|---|
| I/O 50 | I/O 49 |
| I/O 48 | I/O 47 |
| I/O 46 | I/O 45 |
| I/O 44 | I/O 43 |
| I/O 42 | I/O 41 |
| I/O 40 | I/O 39 |
| I/O 38 | I/O 37 |
| I/O 36 | I/O 35 |
| I/O 34 | I/O 33 |
| I/O 32 | I/O 31 |
| I/O 30 | I/O 29 |
| I/O 28 | I/O 27 |
| I/O 26 | I/O 25 |
| I/O 24 | I/O 23 |
| I/O 22 | I/O 21 |
| I/O 20 | I/O 19 |
| I/O 18 | I/O 17 |
| I/O 16 | I/O 15 |
| I/O 14 | I/O 13 |
| I/O 12 | I/O 11 |
| I/O 10 | I/O 9 |
| I/O 8 | I/O 7 |
| I/O 6 | I/O 5 |
| I/O 4 | I/O 3 |
| I/O 2 | I/O 1 |

IP C

| | |
|---|---|
| I/O 50 | I/O 49 |
| I/O 48 | I/O 47 |
| I/O 46 | I/O 45 |
| I/O 44 | I/O 43 |
| I/O 42 | I/O 41 |
| I/O 40 | I/O 39 |
| I/O 38 | I/O 37 |
| I/O 36 | I/O 35 |
| I/O 34 | I/O 33 |
| I/O 32 | I/O 31 |
| I/O 30 | I/O 29 |
| I/O 28 | I/O 27 |
| I/O 26 | I/O 25 |
| I/O 24 | I/O 23 |
| I/O 22 | I/O 21 |
| I/O 20 | I/O 19 |
| I/O 18 | I/O 17 |
| I/O 16 | I/O 15 |
| I/O 14 | I/O 13 |
| I/O 12 | I/O 11 |
| I/O 10 | I/O 9 |
| I/O 8 | I/O 7 |
| I/O 6 | I/O 5 |
| I/O 4 | I/O 3 |
| I/O 2 | I/O 1 |

(As viewed towards front panel)

**Figure A-3. Front Panel I/O Pin Configuration**



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