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U S E R M A N U A L

APERTURE
A/D
MA-MODULE

MODEL
MA200

Document Part No: 11027864C

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INTRODUCTION

This manual describes the operation and use of the C&H Model MA200 MA-Module (Part Number 11027860) revision B and above. This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as VME, VXI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

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1.0 GENERAL DESCRIPTION

The MA200 is a 100KSPS 12-Bit A/D converter module that will sample and selectively store digitally converted differential analog signals at a rate up to 100K samples per second. The module has the ability to convert and store all data at the specified sample rate or selectively store only input values that are outside of a programmed aperture window. This technique provides extensive real-time data compression for transient type input signals. The module is available with the standard common-mode voltage range (-0001) or with a high common-mode voltage range (-0002).

The module is physically implemented on a single wide MA-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules.

The MA200 also supports the addition of an accessory module for input signal conditioning. One such module is the AM102, which provides a programmable anti-aliasing filter (see Appendix B for details). Contact C&H for other input signal conditioning options.

1.1 PURPOSE OF EQUIPMENT

This MA-Module is especially well suited for data acquisition of transient type signals.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

• A/D Resolution:	12-bit
• Conversion Rate:	100KHz (maximum)
• Full Scale Input Range:	±5V or ±10V* Differential
• Common-Mode Voltage:	±13V (-0001) or ±180V (-0002)
• Input Modes:	Unipolar or Bipolar
• Local Memory:	32K 48-bit time-value data pairs
• Sampling Strobe:	Internal (10KHz or 100KHz), Front Panel External or Backplane Trigger (up to 100KHz) (source and prescaler are software programmable)
• Calibration:	Software programmable trim resistors for offset and full-scale

* The -0002 version limits the usable range. See specifications for details.

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1.2.2 Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V (base module only) +12V (base module only) -12V (base module only)	100 20 20	mA mA mA
+5VSUP Supply Current		500	mA.
+12VSUP & -12VSUP Supply Current		100	mA
Maximum Voltage on Analog Inputs (AIN0+ & AIN0-)	-0001 continuous -0002 momentary	±40 ±500	V V
Maximum Voltage on External Inputs (EXTCLK & EXTRUN)	50Ω input impedance >100KΩ input impedance	5 16	Vrms Vrms

SPECIFICATIONS (full operating temperature, unless otherwise specified) [1]

Parameter	Conditions	Limits			Units
		Min	Typ	Max	
A/D					
Resolution				12	bits
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	non missing codes			12	bits
Input Range (switch selectable)	10VPP Bipolar Mode 10VPP Unipolar Mode -0001 -0002 (see note 2) 20VPP Bipolar Mode -0001 -0002 (see note 2)	-5 0 0 -10 -7		+5 +10 +7 +10 +7	V V V V V
Full Scale Error	after calibration 10VPP Mode 20VPP Mode	-0.1 -2.5 -5		+0.1 +2.5 +5	% + mV mV
Common Mode Voltage Range	-0001 -0002	±13 ±180			V V
Common Mode Rejection Ratio	dc to 1KHz	70			dB
Input Impedance	-0001 differential or common-mode -0002 differential -0002 common-mode	10 800 400			MΩ KΩ KΩ
Internal Sample Clock					
Accuracy				±0.01	%
Frequency	see note 3	1		100	KHz
Jitter				±500	ps
External Inputs (EXTCLK/EXTRUN)					
Input Threshold	Switch selectable	-0.2 +0.6 +2.3	0 +0.8 +2.5	+0.2 +1.0 +2.7	V V V
Impedance	Switch selectable	48 100K	50	52	Ω Ω
Frequency	EXTCLK EXTRUN			5 1	MHz MHz

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Specification Notes:

1. These specifications are for operation with no input accessory module installed. If an input accessory module is used, be sure to review the applicable specifications for that module. See Appendix B for specifications of the AM120 Anti-aliasing filter. The input range, error, impedance, and other specifications may be affected.
2. The high common-mode instrumentation amplifier used on the -0002 version has an output range of ±7V minimum, but is typically ±9V.
3. The internal clock rate is software selectable to 10KHz or 100KHz. A prescaler allows further control.

1.2.3 Electrical

The MA200 requires the +5V and ±12V power from the M-Module carrier.

1.2.4 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082"(52.9 mm) wide.

1.2.5 Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +50°C
Storage Temperature:	-40°C to +70°C
Humidity:	<95% without condensation

Carrier modules may differ in environmental specification. Refer to the carrier's documentation for information.

1.2.6 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D16
Interrupts:	INTA
DMA:	not supported
Triggers:	TRIGI
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	$0FC1_{16}$
Model Number:	$00C8_{16}$
Revision Level:	0002_{16} (Functional Level)

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1.2.7 Applicable Documents

ANSI/VITA 12-1996	Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com
AD1674	Data Sheet, 12-Bit 100kSPS A/D Converter, Analog Devices, Rev. C

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2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

In most cases the MA200 is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The MA200 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M-MODULES

> CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.

All M-Modules must be installed into the carrier before the carrier is installed into the host system. M-Modules are installed by firmly pressing the connector on the M-Module together with the connector on the carrier. Secure the M-Module with mounting hardware provided as shown in Figure 1.

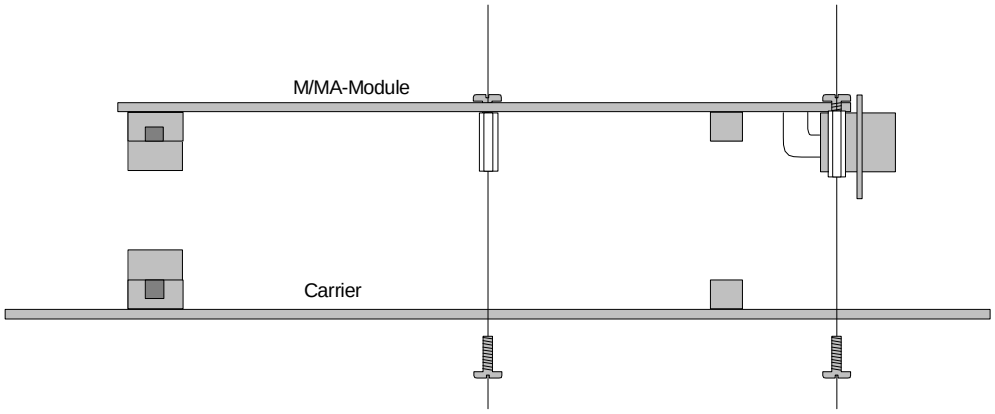


Figure 1. M-MODULE Installation

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2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module-shipping container and packing material may be re-used if it is still in good condition.

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3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

The MA200 provides 100KSPS 12-Bit A/D conversions and can sample and selectively store digitally converted differential analog signals at a rate up to 100K samples per second. When a time-value pair is stored, the aperture window is adjusted to be equal to the stored value. Subsequent data is only stored if it changes more than the programmed window from the last data value stored. Data is stored along with a 31-bit time stamp allowing almost 6 hours of uniquely time stamped data to be monitored at a resolution of 10µs. The time-value pairs of data are stored in memory and retrieved by the user in a first-in first-out (FIFO) manner. Data is read through a single FIFO data port register allowing rapid data retrieval. The most significant bit of the upper time-stamp field indicates data validity (or FIFO empty). A simplified block diagram of the module is shown in Figure 2.

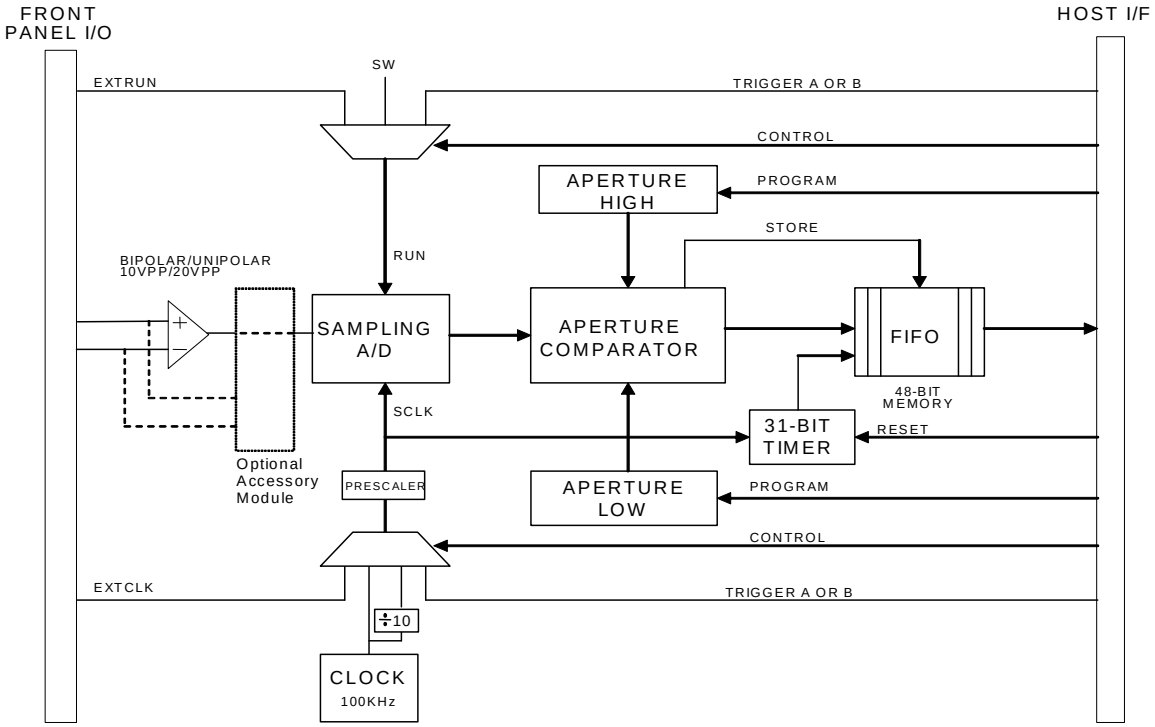


Figure 2. Functional Block Diagram

3.1.1 Differential Input

The differential input circuit provides input signal buffering and over-voltage protection. The circuit consists of a precision unity gain instrumentation amplifier with an input impedance around 10MΩ.

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3.1.2 Sampling A/D

The sampling A/D is a 12-bit 100KSPS analog to digital converter with a front-end sample-and-hold amplifier that supports the full Nyquist bandwidth of the converter. The A/D supports both unipolar and bipolar operation. The A/D interfaces to the aperture comparator logic through a 12-bit data bus.

3.1.3 Aperture Comparator

The aperture comparator logic compares the new data value with the last stored value. If the new value is above the last stored value plus the programmed Aperture High value or it is below the last stored value minus the Aperture Low value, then the new data value is stored in the FIFO memory along with the 31-bit timer value (time-value pair). The first time-value pair captured after the A/D conversion is enabled is automatically stored, since a last stored value may not exist. The last time-value pair captured after the A/D conversion is disabled is automatically stored to give an end point reference value.

3.1.4 Aperture High and Low

The aperture high and low values determine the amount of variation between the last stored value and the new value that is allowed without storing the new value.

3.1.5 31-Bit Timer

The 31-bit timer provides a time stamp of the data stored. The timer increments by one on each rising edge of the sample clock. The timer can be reset independent of the A/D conversion enable or at the same time. Almost 6 hours of uniquely time-stamped data can be captured when running a sample rate of 100K samples per second.

3.1.6 FIFO

The synchronous read/write first-in first-out (FIFO) memory provides data storage for up to 32K time-value pairs. The time-value pairs are stored as 48-bit wide data and retrieved by the user as a three 16-bit word set.

3.1.7 Clock

The clock logic provides an internal time base of 100KHz or 10KHz and the selection of the internal clock, front panel input clock, or backplane trigger signal as the conversion clock. The clock includes a prescaler that can be implemented to change the clock rate.

3.1.8 Optional Accessory Module

The module allows the addition of an accessory module for signal conditioning, such as the AM102 anti-aliasing filter.

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3.2 HARDWARE CONFIGURATION

Switch selectable options are shown in Figure 3.

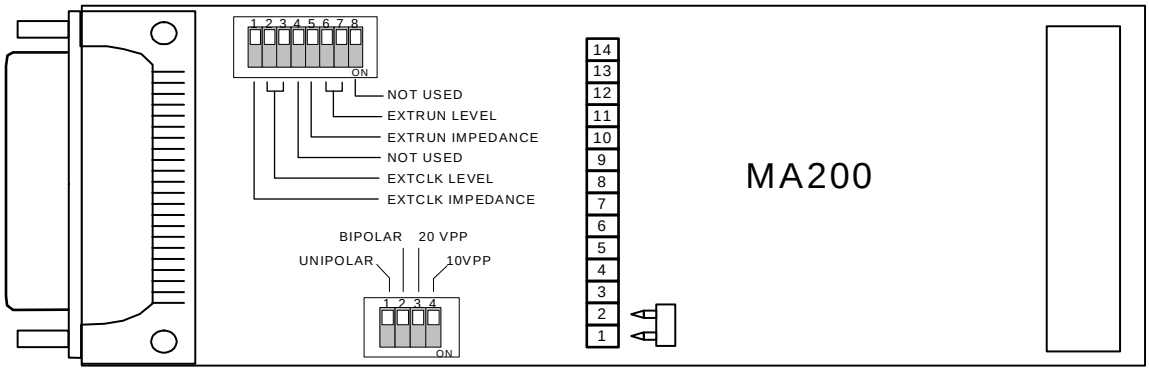


Figure 3. Hardware Configurable Controls

Note: *If an accessory module is not being used, place a jumper into the socket positions 1 and 2 for normal operation.*

UNIPOLAR/BIPOLAR These switches select the input mode of the A/D converter. Refer to the following table for proper switch settings.

Type	Switch 1	Switch 2
Unipolar	ON	OFF
Bipolar	OFF	ON

10VPP/20VPP These switches select the input voltage span of the A/D converter. Refer to the following table for proper switch settings.

Level	Switch 3	Switch 4
10VPP	OFF	ON
20VPP	ON	OFF

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EXTCLK/EXTRUN Impedance (Z) These switches select the input impedance of the EXTCLK and EXTRUN front connector signals. The switches used to control the input impedance are switch 5 (EXTRUN) and switch 1 (EXTCLK). With the switch ON the input impedance is 50Ω. With the switch OFF (default), the impedance is >100KΩ.

EXTCLK/EXTRUN Level These switches control the threshold level of the EXTCLK and EXTRUN front connector signals. The level can be set to 0V (zero crossing), TTL (0.8V), or CMOS (2.5V).

	EXTCLK		EXTRUN	
Threshold	2	3	6	7
0V	OFF	OFF	OFF	OFF
TTL	ON	ON	ON	ON
CMOS	ON	OFF	ON	OFF

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3.3 CONNECTORS

3.3.1 M-Module Logic Bus Connector

The M.MA-Module interface connector contains signal and voltage connections specific to the M-Module interface (see Appendix A for pin assignments).

3.3.2 I/O Connector

The front panel I/O connector is a standard 25-pin D-subminiature female receptacle (AMP 745783-6). Below are the signals and functional descriptions provided on the connector (see Appendix A for pin assignments).

AM0+ to AM7+	Reserved Accessory Module Inputs
AM0- to AM7-	Reserved Accessory Module Inputs
AIN0+	Analog (+) Input *(Input)*
AIN0-	Analog (-) Input *(Input)*
EXTCLK	External Clock. This signal can be used for timing the A/D conversions *(Input, 100KHz max.)*.
EXTRUN	External Run. This signal can be used to enable/disable the A/D conversion. *(Input)*.
GND (LOGIC)	Digital Logic Ground
+5VSUP	+5V supply. Can be used for external buffer, amplifier, or other logic. *(Do not exceed 500mA)*
+12VSUP	+12V supply. Can be used for external buffer, amplifier, or other logic. *(Do not exceed 100mA)*
-12VSUP	-12V supply. Can be used for external buffer, amplifier, or other logic. *(Do not exceed 100mA)*

NOTE: Inputs (AM1+ to AM7+) and (AM1- to AM7-) are reserved for use with an optional accessory module.

3.3.3 Peripheral Interface Connector

The peripheral interface connector allows connection of certain signals to carrier boards that support this option (see Appendix A for pin assignments).

3.3.4 Accessory Module Connectors

These connectors provide the signal interface between the MA203 base module and the signal conditioning accessory modules (see Appendix A for pin assignments).

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3.4 INDENTIFICATION AND CONFIGURATION REGISTERS

3.4.1 M-Module PROM Registers

The MA200 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in sixteen word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in I/O space and the data is read one bit at a time.

The MA200 also supports the VXI-IDENT function introduced by Hewlett-Packard. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type Registers. Details are shown in Table I.

Table I. M/MA Module EEPROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00C8 (200 dec.)
2	Revision Number[1]	0002
3	Module Characteristics[2]	1A68
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (C&H)
18	VXI Device Type[3]	FFEC
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the functional revision level of the module. It does not correspond to the hardware assembly level.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = needs ±12V
11	1 = needs +5V
10	0 = no trigger outputs
9	1 = trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type C (type A also supported)
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	FEC_{16} = C&H specified model code

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3.4.2 IO Registers.

There are a variety of registers used to configure and control the MA200 module. The registers are addressable within the I/O Space. An address map of the registers is shown Table II. The registers provide control, status, and calibration of the A/D, control of the sampling rate and source, control of the aperture value and interrupts, clearing of the time stamp and memory, and reading of the captured time-value pairs. Details of the registers are provided in Figure 4.

Table II. I/O Address Map

IO Address, hex	Register Description
00	Control/Status
02	Interrupt Control
04	Aperture High
06	Aperture Low
08	FIFO Data Port
0A	Calibration
0C	Accessory Module Control
0E	Last A/D Value Stored
10	FIFO Unread Count

Control/Status Register (00_{16}) This read/write register provides the main control of the module operation. Bits are provided for control of the sampling clock and run signal sources, reset of the FIFO and time stamp, manual conversion, and status of FIFO data storage.

Interrupt Control Register (02_{16}) This read/write register individually enables the three types of interrupts.

Aperture High Register (04_{16}) This read/write register defines the allowable variation above the last stored value before time-value pair is stored.

Aperture Low Register (06_{16}) This read/write register defines the allowable variation below the last stored value before time-value pair is stored.

FIFO Data Port Register (08_{16}) This read-only register allows fast reading of the time-value pairs. Three 16-bit words are read in sequential order. The most significant bit (MSB) of the first word determines which word is read on the next read access. If the MSB is 1, Word 2 is read next, and then Word 3 is read. If the MSB is 0, then Word 1 is read. This allows the FIFO to be continuously read until the DV bit goes low. Following reset of the FIFO, Word 1 is always the first word read from the FIFO Data Port.

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Calibration Register ($0A_{16}$) This read/write register allows programming of the offset and full-scale trim potentiometers. The potentiometers are programmed through a series of clock and data write operations.

Accessory Module Control Register ($0C_{16}$) This read/write register is used to control An accessory module. The specific control of this register can be found in the documentation provided with the accessory module.

Last A/D Value Stored Register ($0E_{16}$) This read-only register provides the value of the last A/D value stored in memory. This register is typically only used for calibration or diagnostics purposes.

FIFO Unread Count Register (10_{16}) This read-only register provides a count of the number of time-value pairs that have not been read from the FIFO port. This register is typically only used for diagnostics purposes.

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Status Control Register

00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	DS	FF	HF	PSC		CLKSEL			STA	RUNSEL			CNV	RFF	RTS	RUN
Read	DS	FF	HF	PSC		CLKSEL			STA	RUNSEL			0	0	CSE	RUN

DS ⇨ Data Stored (Reading a 1 = a data value is stored)
(Writing a 1 clears the pending interrupt)

FF ⇨ FIFO full (Reading a 1 = full, no additional time-value pairs are stored when the FIFO is full)
(Writing a 1 clears the pending interrupt)

HF ⇨ FIFO half-full (Reading a 1 = half-full)
(Writing a 1 clears the pending interrupt)

PSC ⇨ Prescaler Control (Selected conversion clock is divided by this prescaler)
- 0 0 Prescaler = 1
- 0 1 Prescaler = 2
- 1 0 Prescaler = 5
- 1 1 Prescaler = 10

CLKSEL ⇨ Conversion Clock Select
- 0 0 0 Internal 10K samples/second
- 0 0 1 Internal 100K samples/second
- 0 1 0 EXTCLK front panel input signal (rising edge)
- 0 1 1 EXTCLK front panel input signal (falling edge)
- 1 0 0 Backplane Trigger A (rising edge)
- 1 0 1 Backplane Trigger A (falling edge)
- 1 1 0 Backplane Trigger B (rising edge)
- 1 1 1 Backplane Trigger B (falling edge)

STA ⇨ Store all (1 = ignore aperture settings and store all values read from A/D)

RUNSEL ⇨ Run Source Select
- 0 0 0 Software Run bit
- 0 0 1 (reserved)
- 0 1 0 EXTRUN front panel input signal (high level)
- 0 1 1 EXTRUN front panel input signal (low level)
- 1 0 0 Backplane Trigger A (high level)
- 1 0 1 Backplane Trigger A (low level)
- 1 1 0 Backplane Trigger B (high level)
- 1 1 1 Backplane Trigger B (low level)

CNV ⇨ Conversion Start (if RUN = 0, then a 1 = perform a single A/D conversion and store data value)

RFF ⇨ Reset FIFO (1 = reset)

RTS ⇨ Reset Time Stamp Clock (1 = reset)

CSE ⇨ Clock Speed Error (1= the conversion clock is exceeding the maximum conversion rate)

RUN ⇨ Run (if RUNSEL = 000, then 1 = enable A/D conversion and storage)

Interrupt Control Register

02

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	DIEN	FIEN	HIEN	-	-	-	-	-	-	-	-	-	-	-	-	-
Read	DIEN	FIEN	HIEN	-	-	-	-	-	-	-	-	-	-	-	-	-

DIEN ⇨ Enable interrupts on data storage

FIEN ⇨ Enable interrupts on FIFO full

HIEN ⇨ Enable interrupts on FIFO half-full

Figure 4. I/O Registers

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Aperture High Register

04

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Aperture High Value												0	0	0	0
Read	Aperture High Value												0	0	0	0

Aperture High ⇨ This value is used to determine if the time-value pair is stored to memory. If the A/D value is above the last stored value *and* the A/D value minus the last stored value is greater than or equal to Aperture High, then the time-value pair is stored to memory.

Aperture Low Register

06

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Aperture Low Value												0	0	0	0
Read	Aperture Low Value												0	0	0	0

Aperture Low ⇨ This value is used to determine if the time-value pair is stored to memory. If the A/D value is below the last stored value *and* the last stored value minus the A/D value is greater than or equal to Aperture Low, then the time-value pair is stored to memory.

FIFO Data Port Register

08

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read 1	DV	Time Stamp (upper half)														
Read 2	Time Stamp (lower half)															
Read 3	A/D Data Value												0	0	0	0

DV ⇨ Data Valid (1 = valid data, 0 = FIFO empty)
Time Stamp ⇨ 31-bit time stamp for A/D data value
A/D Data Value ⇨ 12-bit A/D value presented as a 16-bit data value with the lower nibble zero

Calibration Register

0A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	-	-	-	-	-	-	TRIMSEL		-	-	U/D	CLK
Read	-	-	-	-	-	-	-	-	-	-	TRIMSEL		-	-	U/D	CLK

Trim Select ⇨ Select Trimming Potentiometer

0 0	None
0 1	Full-Scale Trim
1 0	Reserved
1 1	Offset Trim

U/D ⇨ Up/Down (0 = down, 1 = Up)
CLK ⇨ Clock (toggles 0 to 1 to increment or decrement potentiometer)

Figure 4. I/O Registers (continued)

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Accessory Module Control Register

0C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	EN	Reserved											AC3	AC2	AC1	AC0
Read	EN												AC3	AC2	AC1	AC0

EN ⇨ The enable must be set to pass the signal through the accessory module.

ACS(3-0) ⇨ Accessory Module Control (Refer to separate documentation provided with the accessory module for details on the specific control.)

Last A/D Value Stored Register

0E

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(read-only)															
Read	Last Stored															

Last Stored ⇨ Last A/D value stored in memory.

FIFO Unread Count Register

10

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(read-only)															
Read	Count															

Count ⇨ Number of time-value pairs that have not been read by the user.

Figure 4. I/O Registers (continued)

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4.0 OPERATIONAL DESCRIPTION

4.1 DATA ACQUISITION

The MA200 is designed for easy operation keeping the end user in mind. Operation of the MA200 involves setting up the control register and then waiting for a valid piece of data to be returned.

Setting up the MA200 includes setting the aperture window as required, followed by writing a word to the control/status register to initiate the acquisition. Refer to section 3.4.2 for detailed control register and bit definitions. Figure 5 is a flow model to illustrate the data fetch operation.

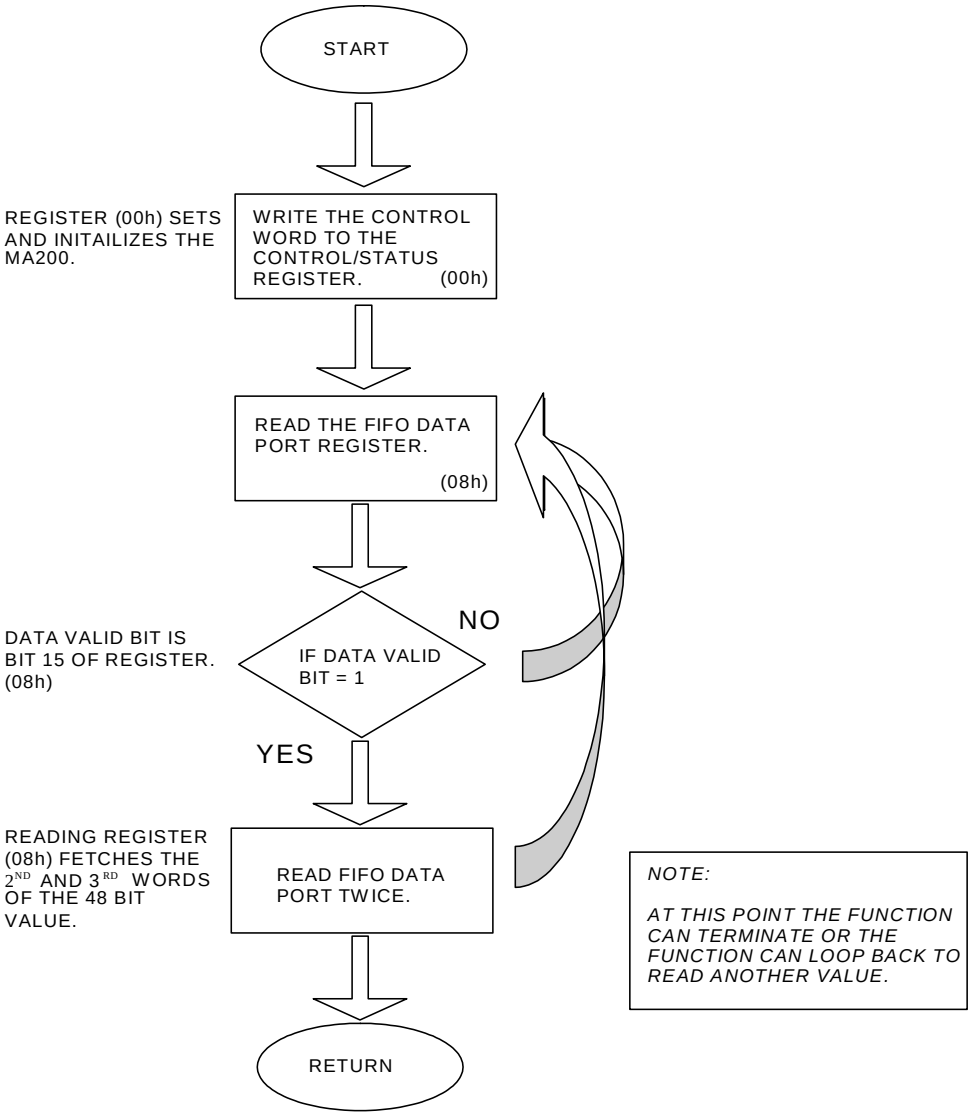


Figure 5. FIFO Data Fetch Operation

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4.2 INTERRUPTS

The MA200 supports Type A interrupts as specified in the M-module specification. The interrupt request line is released on a register access (RORA). The Interrupt Control Register is used to set the interrupt enables. (Refer to section 3.4.2) The MA200 can generate specific interrupts on data stored, the FIFO half full, or the FIFO full.

Data Stored The data Stored bit (DS bit) is set to a one when data is stored, and will remain set until the FIFO is empty. To enable this interrupt a one must be written to DIEN of the Interrupt Control Register. The interrupt request line is released by writing a one to the DS bit in the Status Control Register. This method is best applied if the interrupt service routine is faster than the rate of conversions.

FIFO Half Full The FIFO half full bit (HF bit) is set to a one when the FIFO reaches half full, and will remain set until the FIFO drops below half full. To enable this interrupt, a one must be written to HIEN in the Interrupt Control Register. The interrupt request line is released by writing a one to the HF bit in the Status Control Register. This method is likely to be used in most instances.

FIFO Full Bit The FIFO full bit (FF bit) is set to a one when the FIFO is full, and will remain set until the FIFO reset bit is written in the Status Control Register. To enable this interrupt, a one must be written to FIEN in the Interrupt Control Register. The interrupt request line is released by writing a one to the FF bit in the Status Control Register. This interrupt method is used to detect a FIFO full error.

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4.3 CALIBRATION

The MA200 is switch configurable for bipolar or unipolar mode and for 10VPP or 20VPP voltage range. These switches must be set before calibration. The calibration register is used to control the calibration using software commands. Refer to Figure 4 for a description of the calibration register and to Figure 6 for example code. High level application code may also be available to ease this operation.

NOTE: The module should be calibrated in the input range and polarity mode which it will be used. If an optional accessory module is used, the accessory module must be installed during calibration.

Steps for calibration:

1. Connect a precision voltage source to the AIN+ and ANI- input signals.
2. Set the source voltage according to the full scale table below.
3. Adjust the full-scale offset until the indicated value is returned.
4. Set the source voltage according to the offset table below.
5. Adjust the offset until the indicated value is returned.
6. Repeat steps 2-5 until there is no further adjusting is required.

FULL SCALE

Switch Setting	10 Vpp		20 Vpp	
	-0001	-0002	-0001	-0002
Bipolar	+4.998	+4.998	+9.996	+6.998
Unipolar	+9.998	+6.998	N/A	

OFFSET

Switch Setting	10 Vpp		20 Vpp	
	-0001	-0002	-0001	-0002
Bipolar	-4.998	-4.998	-9.996	-6.998
Unipolar	0.000	0.000	N/A	

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```
/*---------------------------------------------------------------------------*/
/* This function controls the calibration trim potentiometers.               */
int Calibration (int control)
{
#define UB   0x0002
#define DB   0x0000
#define CLK  0x0001
#define FS   0x0010
#define OF   0x0030

   unsigned short value;

   switch (control) {
   case CAL_FS_UP:
      read_word (0xA, &value);
      if ((value & (FS | UB)) != (FS | UB)){  // if not currently doing FS_UP
         write_word (0xA, UB | CLK);          // save setting first
         Delay(0.020);                        // delay 20ms
      }
      write_word (0xA, FS | UB | CLK);
      write_word (0xA, FS | UB);
      write_word (0xA, FS | UB | CLK);
      break;
   case CAL_FS_DN:
      read_word (0xA, &value);
      if ((value & (FS | DB)) != (FS | DB)){  // if not currently doing FS_DN
         write_word (0xA, DB | CLK);          // save setting first
         Delay(0.020);                        // delay 20ms
      }
      write_word (0xA, FS | DB | CLK);
      write_word (0xA, FS | DB);
      write_word (0xA, FS | DB | CLK);
      break;
   case CAL_OF_UP:
      read_word (0xA, &value);
      if ((value & (OF | UB)) != (OF | UB)){  // if not currently doing OF_UP
         write_word (0xA, UB | CLK);          // save setting first
         Delay(0.020);                        // delay 20ms
      }
      write_word (0xA, OF | UB | CLK);
      write_word (0xA, OF | UB);
      write_word (0xA, OF | UB | CLK);
      break;
   case CAL_OF_DN:
      read_word (0xA, &value);
      if ((value & (OF | DB)) != (OF | DB)){  // if not currently doing OF_DN
         write_word (0xA, DB | CLK);          // save setting first
         Delay(0.020);                        // delay 20ms
      }
      write_word (0xA, OF | DB | CLK);
      write_word (0xA, OF | DB);
      write_word (0xA, OF | DB | CLK);
      break;
   case CAL_CANCEL:
      read_word (0xA, &value);
      write_word (0xA, value & 0xFF0F);  // deselect pot, leave U/D & CLK as is
      Delay(0.020);                      // delay 20ms
      write_word (0xA, 0x0000);          // clear register (lowers U/D & CLK)

      break;
   }

   return(0);
```

Figure 6. Calibration Routine

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4.4 ID PROM

Refer to 3.4.1 M-Module PROM Registers for a description of the ID PROM's function and contents.

The ID PROM is a serial device and involves writing and reading a register in a sequential manner to acquire data. Figure 7 is a general description of the code sequence necessary to read the information from the PROM. The PROM is a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*-------------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value)
{
   addr = 0xFE;                         /* M/MA address for IDPROM */
   id_addr = 0x80 | id_addr;            /* 80 is the read opcode for the PROM */
   write_eebyte (addr, id_addr);
   read_eebyte (addr,&rdval);           /* returns first byte of IDPROM */
   tmpval = rdval << 8;                 /* upper byte of sync code word */
   read_eebyte (addr,&rdval);           /* returns first byte of IDPROM */
   tmpval = tmpval | rdval;             /* combine bytes of sync code   */
   *value = tmpval;
   write_word(addr, 0x0000);            /* lower cs */
   return;
}
/*-------------------------------------------------------------------------*/
int write_eebyte (unsigned long addr, unsigned short value)
{

   write_word(addr, 0x0000);            /* insure cs is initially low */
   write_word(addr, 0x0004);            /* initialize */
   write_eebit(addr, 0x0001);           /* start bit */
   temp = value;
   for (i=0;i<=7;i++){
      write_eebit(addr, ((temp & 0x80)>>7));
      temp = (temp << 1);
   }
   return;
}
/*-------------------------------------------------------------------------*/
int write_eebit (unsigned long addr, unsigned short value)
{
   temp = (0x0004 | (value & 0x0001));  /*  set data bit before clock */
   write_word(addr, temp);
   Delay(.000005);                      /* delay at least 5us */
   temp = (0x0006 | (value & 0x0001));  /* set data bit & clock */
   write_word(addr, temp);
   Delay(.000005);                      /* delay at least 5us */
   return;
}
/*-------------------------------------------------------------------------*/
int read_eebyte (unsigned short addr, unsigned short *value)
{
   for (i=7;i>=0;i=i-1){
      read_eebit (addr, &rdval);
      temp = temp | ((rdval&0x01) << i);
   }
   *value = temp;
   return;
}
/*-------------------------------------------------------------------------*/
int read_eebit (unsigned short addr, unsigned short *value)
{
;
   write_word(addr, 0x4);               /* lower clock bit */
   Delay(.000005);                      /* delay at least 5us */
   write_word(addr, 0x6);               /* raise clock bit */
   Delay(.000005);                      /* delay at least 5us */
   read_word (addr, value);
   return;
}
/*-------------------------------------------------------------------------*/
```

NOTE: Functions write_word and read_word are low-level memory access routines that should be replaced with interface specific functions

Figure 7. IDPROM Access Routine

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APPENDIX A – CONNECTORS

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
A14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

Figure A-1. M/MA Interface Connector Configuration

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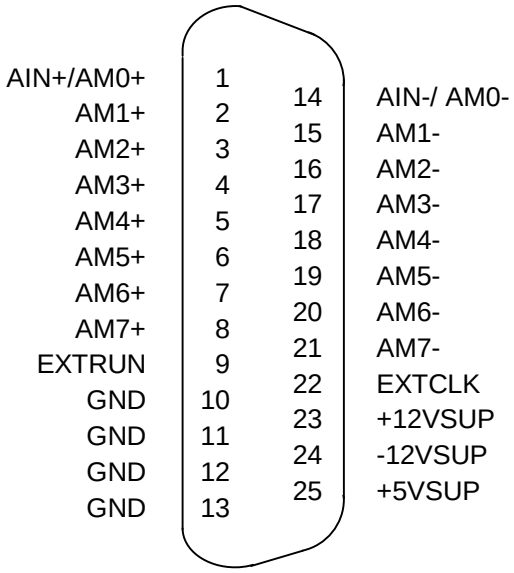
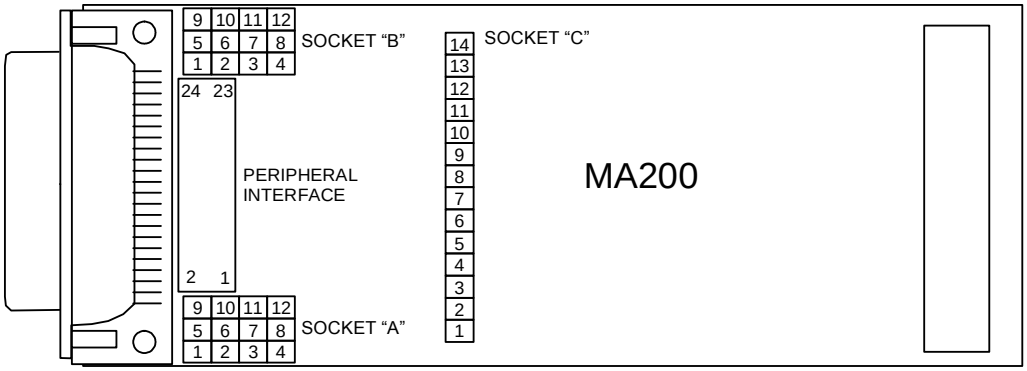


Figure A-2. D-SUB Connector Configuration

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ACCESSORY INTERFACE

SOCKET "A"				SOCKET "B"				SOCKET "C"			
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	AM0+/AIN0+	7	AM3+	1	AM4+	7	AM7+	1	SIGNAL IN	8	-5V
2	AM0-/AIN0-	8	AM3-	2	AM4-	8	AM7-	2	SIGNAL OUT	9	+5V
3	AM1+	9	+5V	3	AM5+	9	+12V	3	ENABLE	10	-12V
4	AM1-	10	-5V	4	AM5-	10	-12V	4	DO	11	+12V
5	AM2+	11	GND	5	AM6+	11	GND	5	D1	12	GND
6	AM2-	12	GND	6	AM6-	12	GND	6	D2	13	SIGNAL OUT
								7	D3	14	GND

PERIPHERAL INTERFACE

PIN	SIGNAL	PIN	SIGNAL
1	AIN0+	2	AIN0-
3	AIN1+	4	AIN1-
5	AIN2+	6	AIN2-
7	AIN3+	8	AIN3-
9	AIN4+	10	AIN4-
11	AIN5+	12	AIN5-
13	AIN6+	14	AIN6-
15	AIN7+	16	AIN7-
17	EXTRUN	18	EXTCLK
19	GND	20	+12VSUP
21	GND	22	-12VSUP
23	GND	24	+5VSUP

Figure A-3. Accessory and Peripheral Interface

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APPENDIX B – AM102 ANTI-ALIASING FILTER

Description

The AM102 accessory module (C&H P/N 11027980) attached to the MA200 and provides anti-aliasing filtering. The module utilizes a three stage Sallen-Key design in a Butterworth configuration to provide a maximally flat band-pass response. The Butterworth response is ideal for instrumentation applications that require minimum deviation throughout the band-pass.

The anti-aliasing filter is a 6-pole low pass active filter with selectable cutoff frequencies. The 6-pole characteristics include a sharp knee at the cutoff frequency, followed by a role off rate of 120 dB per decade. The AM102 can be configured to eight different cutoff frequencies

Specifications

Filter type:	6th order Butterworth
Passband ripple:	< 0.5dB to $0.5 \times f_c$, < 0.7dB to $0.7 \times f_c$
Stopband attenuation:	> 20dB at $2 \times f_c$
Attenuation rate:	120dB/decade
DC offset:	< 20mV
Power consumption:	+12V : 40mA max, -12V : 20mA max
Input Level:	±40V max (no damage)
Input Impedance:	> 10MΩ

Programming

The cutoff frequency is programmed by software through the Accessory Module Control Register (1Ah) discussed in Section 3.4.2. The AC bits (bits 2:0) are used to control the frequency.

Accessory Module Control Register

0C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	EN	Reserved											-	AC2	AC1	AC0
Read	EN												-	AC2	AC1	AC0

EN ⇨ The enable must be set to pass the signal through the accessory module.

ACS(2-0) ⇨ Anti-Aliasing Filter Control

AC2	AC1	AC0	Cutoff Frequency
0	0	0	48 KHz
0	0	1	32 KHz
0	1	0	24 KHz
0	1	1	16 KHz
1	0	0	2.4 KHz
1	0	1	1.6 KHz
1	1	0	240 Hz
1	1	1	160 Hz

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