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Find the *Leonardo DRS / Catalina Research DIREC* at our website: *Click HERE*

DIREC

Digital Receiver and Reconfigurable Computing Board for the VME Bus



Applications:

- Digital Down Conversion
- Baseband Quadrature Sampling
- Hilbert Transforms
- Real and Complex FIR Filtering
- Interpolation and Decimation Filtering
- Reconfigurable Computing

DIREC Benefits & Features

- Dual-channel digital tuner, FIR filter, reconfigurable computing, and DAC capability
- 4HP 6U x 160 mm VME 64x form factor
- VME A24/A32, D32/D64 slave interface
- VME A24/A32, D32/D64 BLT master interface
- CRI's QuickComm64™ (QC64™) high- speed front panel parallel input and output ports for real-time, high-bandwidth I/O (continuous rates beyond 400 MB/sec)
- Front panel arbitration for data routing across multiple boards
- Front Panel Data Port (FPDP) compatible (for interfacing to third party hardware)
- Two 4036XLA and one 4013E series FPGAs per channel for reconfigurable computing (in-circuit programmable)
- One Graychip GC1012 wideband digital tuner ASIC and one GC2011 FIR filter ASIC per channel (on filter daughter card)
- Graychip's GC1012 Digital Tuner supports 50 MSPS input rates (0.1 Hz tuning resolution); the GC2011 Digital Filter supports 80 MSPS input rates (64 taps, 128 taps at ½ I/O rate, 256 taps at ¼ I/O rate)
- Motherboard contains high-speed I/O and is a generic reconfigurable platform for the COTS filter daughter card as well as for tailored daughter cards
- GC1012s and GC2011s operate in stand-alone or cascaded modes
- Support for both continuous and vector operations
- Support for both coherent and non-coherent processing modes
- Real time mode switching
- Each FPGA and Graychip may be bypassed to specifically fit an application's processing and budgetary requirements
- Optional dual-channel digital to analog conversion (DAC) daughter card based upon the Harris HI5741 14 bit, 100 MHz DAC
- Due to daughter card architecture, tailored DAC solutions straight forward to implement
- Application code developed under CRI's Application Program Interface (API) and System Development Framework (SDF)
- Power for fully populated motherboard running at 40 MHz: 6.6A @ +5V worst case (calculated); 2.6A @ +5V typical (measured)
- Power for filter daughter card (two GC1012s and two GC2011s) running at 40 MHz: 4.3A @ +5V worst case (calculated); 2.9A @ +5V typical (measured)

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DIREC Description

DIREC is a 6U x 160 mm single-slot VME board which addresses three application areas:

1) digital receiving and tuning,
2) reconfigurable computing, and
3) digital-to-analog conversion.

DIREC provides two parallel channels. Each channel has an input FPGA (4036XLA), a Graychip GC1012 wideband digital tuner ASIC, another 4036XLA, a Graychip GC2011 digital filter ASIC, and an output XC4013 FPGA. Any of these devices may be bypassed to provide a solution which specifically fits an application's processing and budgetary requirements. Full functionality of the GC1012 and GC2011 is supported, including modes for stand-alone, cascaded, vector data, continuous data, coherent, and non-coherent processing. DIREC supports real time mode switching.

The DIREC motherboard is a generic DSP platform: it contains high-speed front panel I/O and FPGAs. The FPGAs are in-circuit programmable, and have enough capacity to support reconfigurable computing and FPGA-based DSP applications.

The Graychip ASICs (and two more FPGAs) are located on a daughter card. The user may elect to purchase both the motherboard and the daughter card for digital receiver applications, or the motherboard alone for reconfigurable computing applications. The motherboard is also an excellent base on which custom processing daughter cards may be developed.

The DIREC motherboard has two front panel parallel ports. Either may be configured as input or output, and either may be configured as the Front Panel Data Port (FPDP) protocol or CRI's own QuickComm™ (QC64™) interface.

QC64™ is a 64-bit wide port capable of sustaining transfer rates beyond 400 MB/second. FPDP is typically used to interface DIREC to third-party hardware, while QC64™ provides extremely high-bandwidth I/O for demanding applications.

DIREC, via QC64™, also supports and inserts header words into the data stream. The function of the headers may be defined to address customer-specific requirements. The interface also supports data word arbitration, where data vectors may be routed from multiple sources to a single destination or from a single source to multiple destinations.

The flexible front panel interfaces allow DIREC to act as a building block in systems, allowing plug-and-play integration capabilities.

The DIREC board also offers, via an optional daughter card, dual channel digital-to-analog conversion using the Harris HI5741 14 bit, 100 MHz DAC. Front panel SMA connectors provide the analog outputs.

ORDERING INFORMATION

The filter daughter card and DIREC motherboard are ordered as individual units. Multiple configurations exist for both the daughter card and motherboard, providing solutions to fit a variety of processing and budgetary requirements. Please contact CRI for part numbers and pricing information.

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DIREC Block Diagram

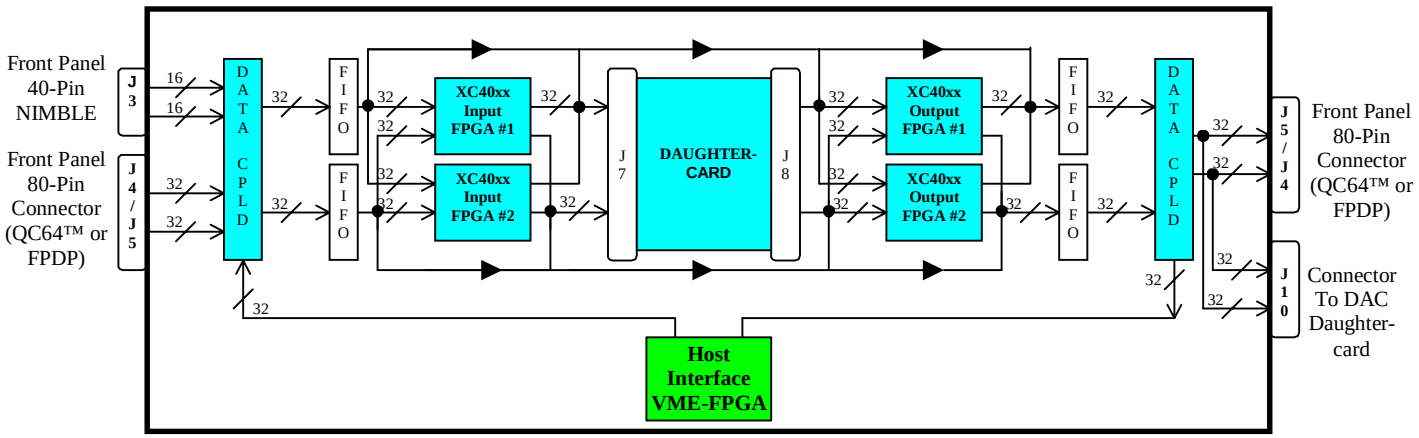


Figure 1: DIREC Motherboard Block Diagram
(daughter card block diagram on next page)

About Catalina Research, Inc.

Catalina Research, Inc., based in Colorado Springs, Colorado, is a customer-driven innovative design and marketing company that provides high-bandwidth, low-latency digital signal processing (DSP) solutions for the most demanding commercial and government applications. Focusing on FFTs and digital receivers, product offerings include ASICs, boards, and systems. COTS board-level products include the highest performance FFT processors, digital receivers, reconfigurable computers, and A/D converters. Form factors and buses supported include VME, RACE, 64-bit PCI and PMC.

Information on this product, along with CRI's entire product line, can be found on CRI's web site at www.catalinaresearch.com.

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DIREC Block Diagram

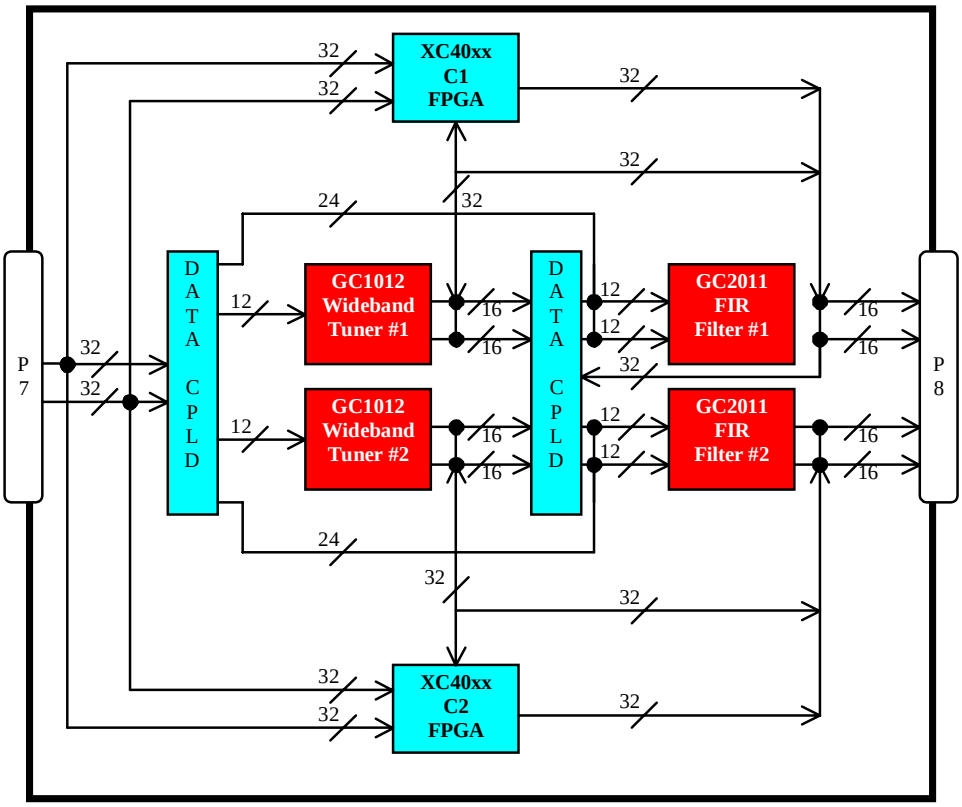


Figure 2: DIREC Daughter Card block diagram

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