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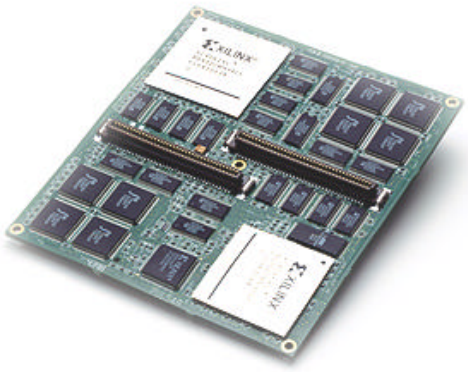
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Find the *Leonardo DRS / Catalina Research Pulsar* at our website: ***Click HERE***

PULSAR

RACEway FFT Compute Element Daughter Card



Applications:

- SAR Processing
- Radar Processing
- Image Processing
- Any RACEway system requiring low-latency FFT Performance

Pulsar Benefits & Features

- Single Type B Daughter Card form factor plugs directly onto Mercury Computer System's H Style RACEway motherboards.
- High performance vector processing accelerates FFTs, IFFTs, correlations, convolutions, and related functions in RACEway systems.
- Low latency.
- One dedicated RACEway interface for input and a second for output provides full RACEway bandwidth for input and output.
- Based upon CRI's Pathfinder FFT ASIC (80 MHz clock).
- CRI Sojourner Address Generator (AG) supports offset/stride addressing and stacked transforms.
- AGs allow the user to time-overlap input data as well as output subsets of a processed vector.
- 32 bit 2's complement block floating point arithmetic.
- Supports data vector lengths from 128 points (complex).*
- Separate input, output, and processing SRAM banks allow concurrent I/O and processing to optimize throughput.
- Window/Reference SRAM bank stores time domain windows and frequency domain filters; may be paged to store multiple sets; 256K complex samples deep.
- Full API control allows PULSAR to act as a "FFT accelerator resource" that other general purpose RACEway CEs (SHARCs and PowerPCs) can access.
- Large capacity FPGAs implement real time pre and post processing of computationally expensive operations; anticipated functions include IEEE floating point conversion and/or magnitude phase conversion.

* Contact CRI for details on smaller sizes.

Pulsar Description

PULSAR is a Compute Element (CE) daughter card based upon Mercury Computer's Type-B form factor. It plugs directly onto Mercury's H-style motherboards and integrates seamlessly into the RACEway compute fabric.

PULSAR is based upon CRI's Pathfinder FFT ASIC and Sojourner address generator (AG) ASIC. The two devices together provide substantial acceleration for frequency domain based algorithms. Table 1 illustrates PULSAR's complex FFT benchmarks.

The Sojourner AG provides full support for radix instructions, real FFTs, 2D FFTs, stacked transforms, vector/complex multiplies, vector/complex adds. All address patterns have offset/stride parameters which allow truly flexible and efficient algorithm implementation.

High speed SRAM banks hang off the various ports of the DSP. Processing is achieved by passing data back and forth between 'A' (input) memories and the 'B' (processing) memory while flowing the data through the processor. The 'A', 'B', and 'Q' memory banks are each 128K x 64 bits. The window/reference memory ('C') provides storage for windows, filters, twiddle factors, and/or temporary data storage. The 'C' bank is 256K x 64 bits, and is based upon Pentium cache RAM technology.

Separate RACEway interface chip sets provide dedicated RACEway paths into and out from PULSAR. Combined with separate input, output, and processing SRAM banks, PULSAR fully supports concurrent I/O and processing. This maximizes the daughter card's performance from both an I/O and processing standpoint.

PULSAR is available with a full support package, including CRI's software API (Application Programming Interface) and System Development Framework (SDF). Also supported is a large class of libraries and digital signal processing functions such as FFTs, fast convolutions, polyphase filters, matched filters and related frequency-domain functions. These libraries, combined with CRI's easy-to-use code generator C++ tool, provide application programmers with the flexibility to address a wide range of digital signal processing problems.

Through the API, the user defines the source and destination of the data to be processed and commands PULSAR to perform an algorithm on that data. The source (a RACEway CE) DMAs data to PULSAR, where it is processed and then DMA'ed to a RACEway CE destination. With this architecture, the processing may change on a vector-by-vector basis.

PULSAR also provides large capacity datapath FPGAs which contain pre and post processing capabilities. Available functions are IEEE floating point conversion and/or magnitude phase conversion. Both of these functions are computationally intensive, yet run in real time in the FPGA. This off-loads other CEs in the RACEway fabric to concentrate on other portions of the real-time signal processing.

PULSAR provides a straight-forward way for the user to easily integrate and take advantage of CRI's FFT technology within Mercury Computers' RACEway environment.

Pulsar FFT Processing Times

FFT Size	FFT Time (microsec.) 80 MHz Clock	Convolution Time (microsec.) 80 MHz Clock
16*	0.6	1.2
32*	0.8	1.6
64*	2.5	5.0
128	4.1	8.2
256	7.3	14.6
512	13.7	27.4
1024	26.5	53.0
2048	78.1	156.2
4096	154.9	309.8
8192	308.5	617.0
16,384	615.7	1231.4
32,768	1230.1	2460.2
65,536	3278.5	6557.0
131,072	6555.3	13,110.6

Table 1: Pulsar FFT Processing Times

*Small FFT Sizes (16, 32 and 64) are custom and assume stacked transforms. Contact CRI for more information.

About Catalina Research, Inc.

Catalina Research, Inc., based in Colorado Springs, Colorado, is a customer-driven innovative design and marketing company that provides high-bandwidth, low-latency digital signal processing (DSP) solutions for the most demanding commercial and government applications. Focusing on FFTs and digital receivers, product offerings include ASICs, boards, and systems. COTS board-level products include the highest performance FFT processors, digital receivers, reconfigurable computing, and A/D conversion. Form factors and buses supported include VME, RACEway, 64-bit PCI and PMC.

Information on this product, along with CRI's entire product line, can be found on CRI's web site at www.catalinaresearch.com.

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Pulsar Block Diagram

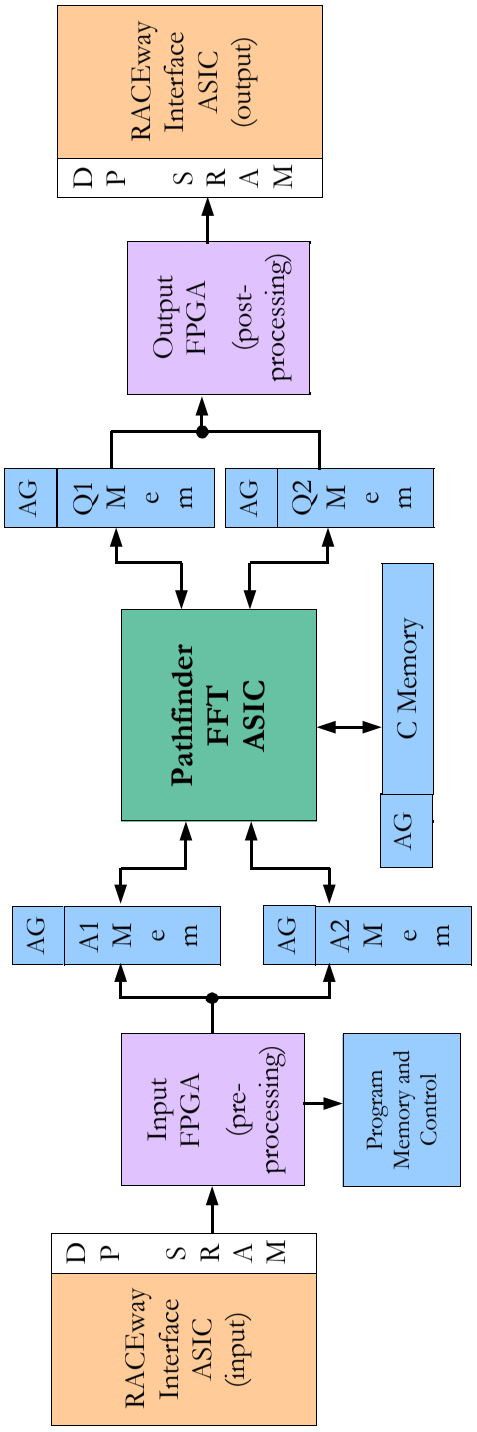


Figure 1: Pulsar Block Diagram

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