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- Based on the [MIO 8261](#) for the CPU kernel (R3052) and the VME interface
- Based on three independent RISC CPU kernels (R3051 / R3052), each dedicated to a specific task (user interface, bus monitoring, BC / mRT functionality)
- VME master / slave
- Compliant with MIL-STD-1553 A and B standards
- Dual redundant buses architecture
- BC, mRT and BM modes simultaneously supported at full bus load
- Error injection / detection capability
- Time stamping logic (1 micro-s resolution)
- Internal / external synchronization
- High performance: short response time (<4 micro-s) and inter-message gap (14 micro-s)

The MIL 8264 is an intelligent VME unit designed by CES around a RIO kernel to meet the requirements of the MIL-STD-1553 bus standard. It is based on standard RISC microprocessors with firmware written in C.

The MIL 8264 provides the principal key of the MIL-STD-1553 bus elements:

- The bus controller (BC), which issues data flow control for all transmissions on the bus
- The multiple remote terminal (mRT) which transfers data in and out of a system and,
- The bus monitor (BM) which listens continuously to the data bus.

The host (VME master) uses a set of registers and different memory structures to communicate with the board. A high-level software interface is used to describe the different configuration of the board. The firmware interprets the high-level commands and translates them to low-level commands without user intervention. This feature provides a short way to build an application.

The MIL 8264 can detect and generate multiple electrical, or protocol errors in various mode: synchro errors, bit errors, phase encoding errors, gap violation, word count errors, parity errors, etc. A diagnostic is delivered with each received message.

A time stamping logic dates each event with a 1 micro-s resolution. Internal / external synchronization starts the stamping logic and its associated counters. A hardware counter provides 16 bits and the firmware implements a 32 bits counter for a complete 48 bits 1 micro-s time stamping logic.

The board is delivered with an EPROM containing the firmware of the board and performing the functions described above.

A complete library of C routines and examples programs are also available on floppy disk.



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