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Mx-RAM
User's Manual

0102-9002A.1

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Chapter one
INTRODUCTION

1.1 Manual Overview

This manual describes the operation of the MD-RAM, MX-RAM, and MR-RAM VMEbus memory boards from Thales Computers. Chapter Two guides the installation process. Chapter Three discusses memory access. Chapter Four describes the power monitor. Appendix A contains board specifications. Appendix B provides parts layouts for the three board configurations.

Throughout this manual the term "Mx-RAM" (with the lower case "x" as a place holder) will be used if the information applies to all of the three functionally related boards.

For additional information on VMEbus architecture, refer to the VMEbus specification. A copy of this specification can be obtained from:

IEEE Service Center
Order Department
445 Hoes Lane
Piscataway, NJ 08854-4150
1-800-678-4333

VITA
10229 N. Scottsdale Road
Suite B
Scottsdale, AZ 85253
1-602-951-8866

1.2 Product Overview

The Mx-RAM provides up to four megabytes of battery-backed, nonvolatile, static random access memory (SRAM) in a double-height (6U) form factor. Available configurations are shown in Figure 1-1. The MD-RAM is intended

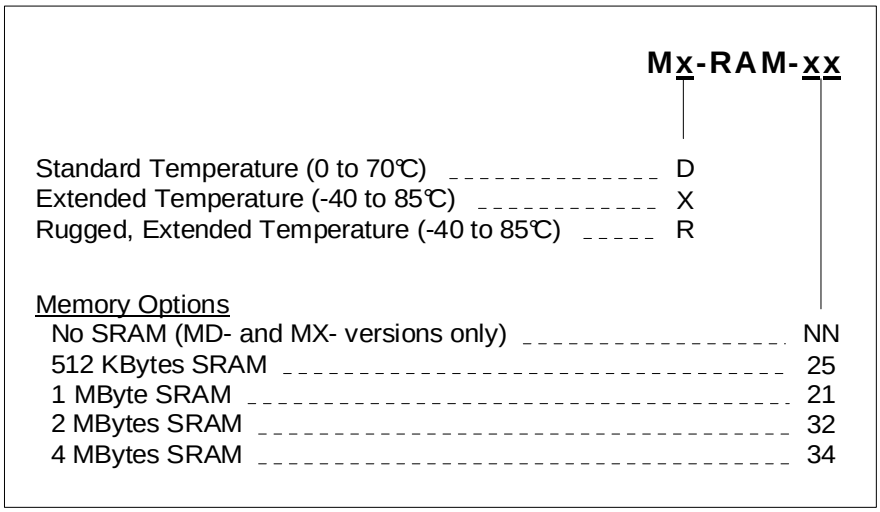


Figure 1-1. Mx-RAM Standard Configurations.

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for use under normal environmental conditions. The MX-RAM can operate over an extended temperature range. The MR-RAM is designed for both extended temperatures and rugged environments. Figure 1-1 also indicates that the MD- and MX-RAM boards are available without memory devices installed. This option allows for on-site user installation of EEPROM devices instead of SRAM. For additional details on board capabilities, refer to Appendix A. Major features of the Mx-RAM include:

- Up to 4 Mbytes of nonvolatile memory.
- Factory installed and tested SRAM devices or unpopulated.
- 128 K x 8, 32-pin or 32 K x 8, 28-pin devices.
- Low-power consumption.
- Battery-backed memory for years of data retention.
- Extended operating temperature versions for -40° to 85°C.

The major functions of the Mx-RAM are shown in Figure 1-2. Mx-RAM memory is organized as two banks of 32-bit memory quads. Each bank has its own battery and power monitor for long-term reliability. Battery status indicators enhance maintainability. Data retention is conservatively rated at ten years

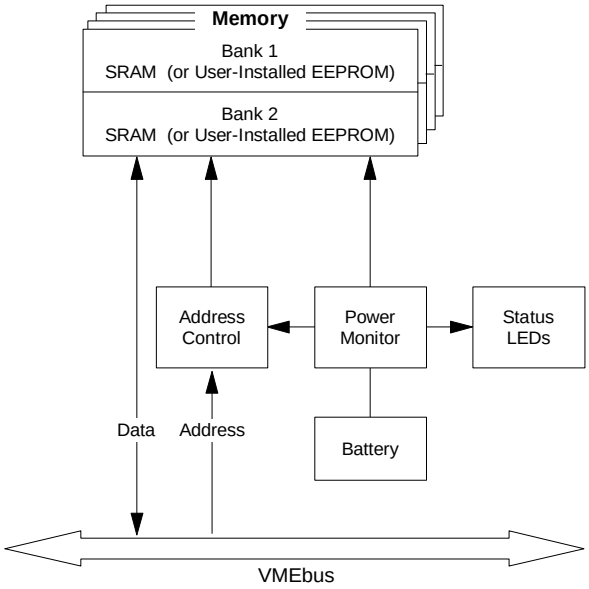


Figure 1-2. Mx-RAM Functional Diagram.

for factory installed SRAM versions (at 25°C, 50% duty cycle). Front panel status display and test switches provide a simple maintenance test and display for battery verification. Through the use of CMOS technology, the Mx-RAM consumes a minimal amount of power. This increases system reliability while limiting power supply requirements.

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Chapter two
INSTALLATION

2.1 Precautions

Many of the components on the Mx-RAM can be damaged by electrostatic discharges. For this reason, keep the board in its protective antistatic bag until it is ready to be configured and/or installed. During installation, and whenever the board is removed from the bag, it is important to follow proper procedures for static protection. The Mx-RAM is factory-configured to operate in most systems without further adjustment. If a particular application requires modification to any of the jumpers, those modifications should be done at an antistatic workstation that includes an operator wrist strap and grounded bench mat. When working with the Mx-RAM, take all necessary precautions for electronic products that may be damaged by electrostatic discharge.

Save the antistatic bag for storing the board and for the possibility of later shipping the board.

Closely inspect the board for any signs of shipment-related damages such as loose components or bent pins. If any evidence of damage is discovered, notify the carrier and Thales Computers immediately.

2.2 Default Settings

The Mx-RAM is factory-configured and ready for use as received (or upon installation of any user-installed memory devices). However, jumper blocks have been provided to allow modification of certain Mx-RAM parameters. These parameters, and the factory default jumper settings, are shown in Table 2-1.

Table 2-1. Factory Default Jumper Settings

Parameter	Factory Default	Jumper Block
ADDRESS MODE	Extended (A32)	J2
BASE ADDRESS	$04000000	J4
MEMORY DEVICE SIZE	Depends on model	J6
WRITE PROTECT	Off	J7

These settings can be changed to accommodate user requirements. Section 2.4 details the options available.

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2.3 Installing the Memory Devices

Mx-RAM memory is configured in two banks of four memory quads. Each quad consists of four memory devices. Figure 2-1 shows the locations of the memory banks, quads, and devices. Either one or both memory banks may be populated. Within a bank, one or more quads will be populated. If a quad is to be populated, it must have all four devices installed.

The Mx-RAM boards may be populated with either 28-pin (32K x 8) or 32-pin (128K x 8), 150 nanosecond (ns) SRAMs or, for MD-RAM and MX-RAM boards only, user-installed EEPROM devices. All memory devices on the board, however, must be of the same size and type. 28-pin memory devices are installed such that pins 1 and 28 of the device are inserted into pins 3 and 30 of the socket respectively.

For the MR-RAM, memory devices are factory-soldered directly into the board and jumper posts are wire-wrapped as required. MD-RAM and MX-RAM boards may be ordered with memory devices installed and tested or unpopulated for on-site memory installation.

A suitable SRAM for the Mx-RAM is the OKI MSM51256, a 32K x 8 device. Use of devices that do not meet the backup current specifications will degrade the data retention time. Board design requires that the installed SRAMs meet the specifications listed in Table 2-2.

EEPROM devices are allowed only in MD-RAM and MX-RAM boards specifically built for EEPROMs. These EEPROMs may be 32K x 8 devices only. Board design requires that the installed EEPROMs meet the specifications listed in Table 2-2.

Table 2-2. Mx-RAM SRAM and EEPROM Specifications

Parameter	SRAM	EEPROM
Access Delay	150 ns or faster	150 ns or faster
Active Current	70 mA or less, 100% duty cycle 30 mA or less, 1 µs cycle time	
Standby Current	3 mA or less	
Backup Current	10 µA or less at Ta = +85°C (MX and MR) 10 µA or less at Ta = +70°C (MD) 1 µA or less at Ta = +60°C 0.5 µA or less at Ta ≤ +25°C	
Operating Temperature	0° to +70°C (MD-RAM) -40° to +85°C (MX- and MR-RAM)	0° to +70°C (MD-RAM) -40° to +85°C (MX-RAM)

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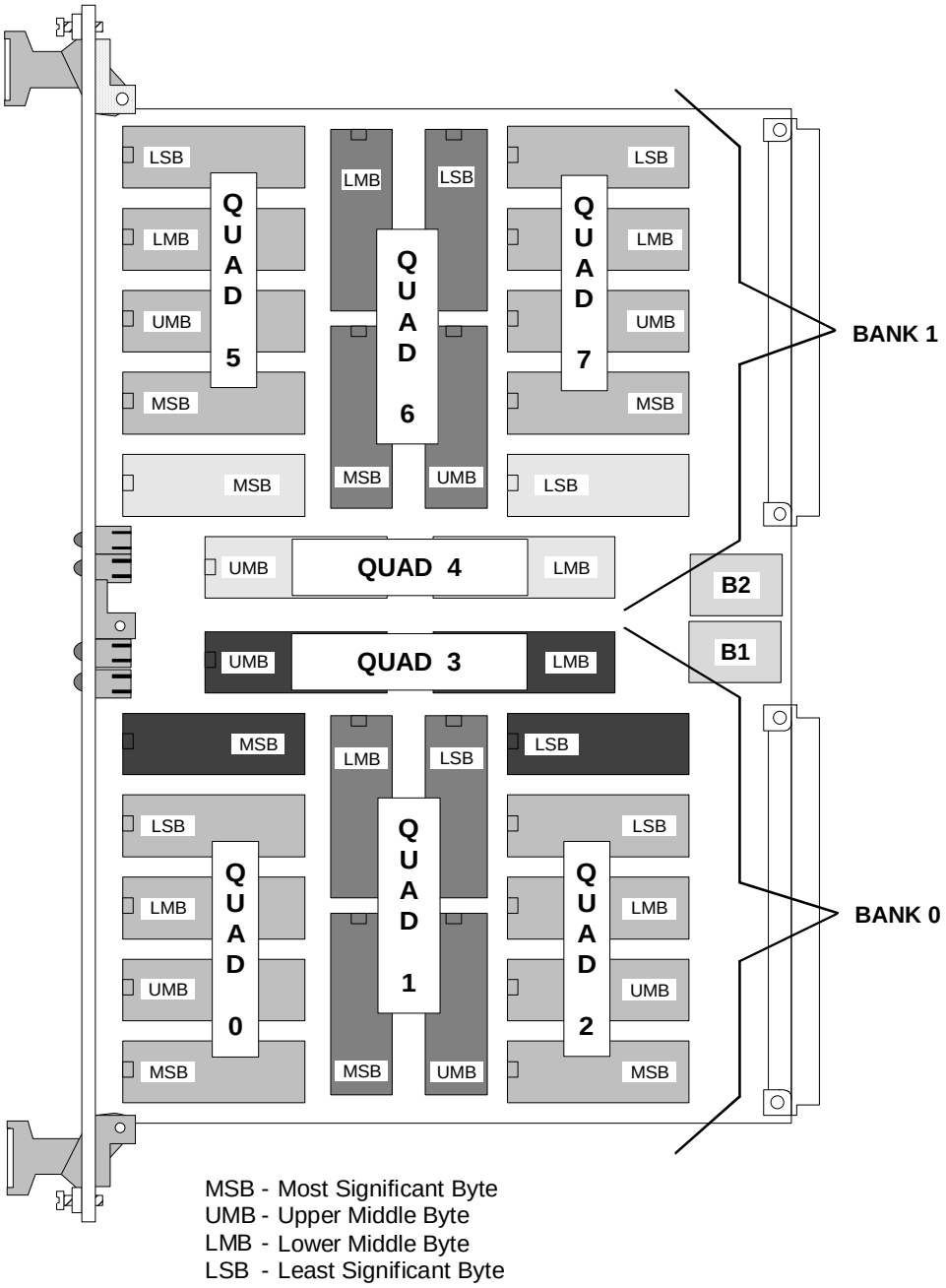
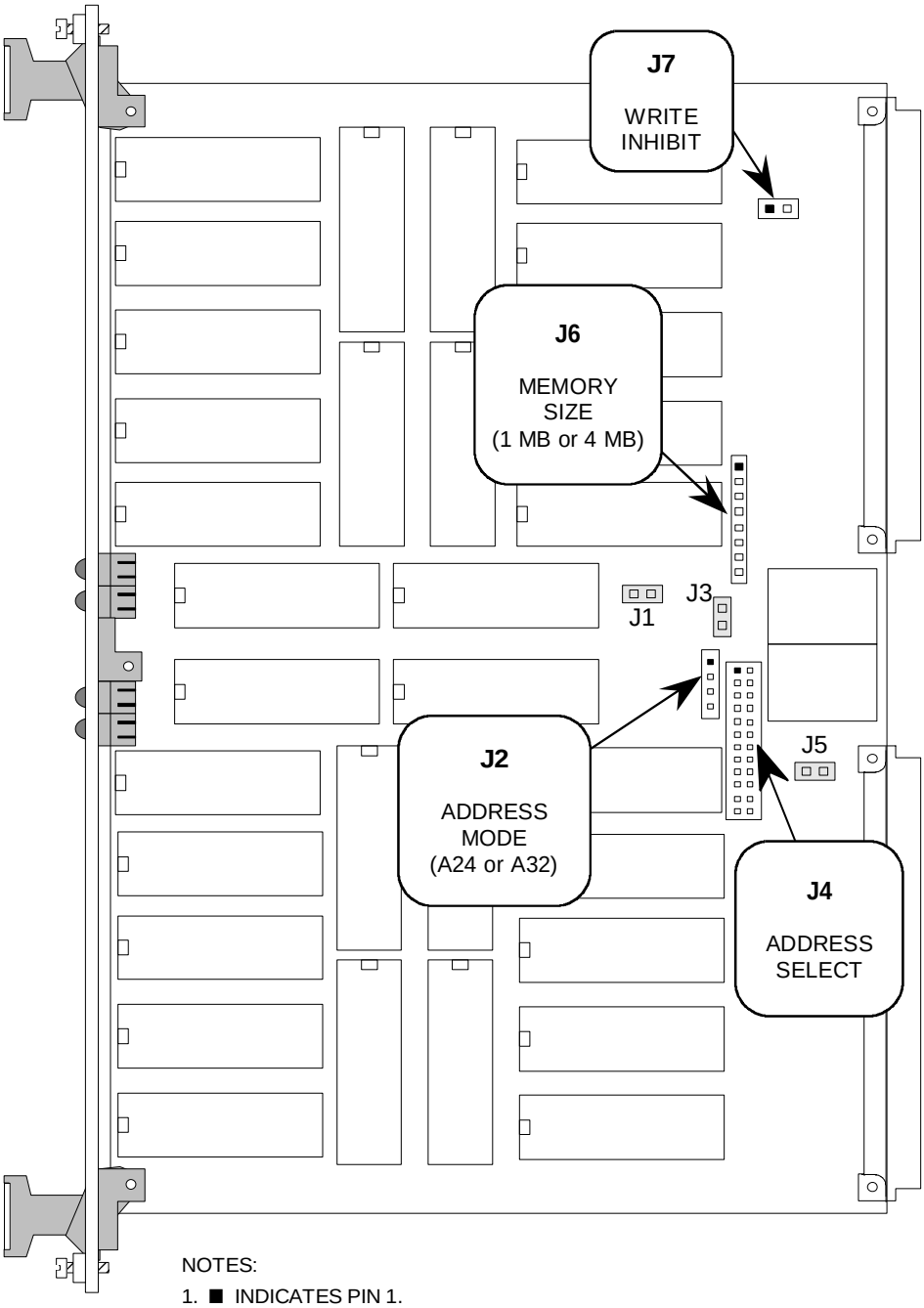


Figure 2-1. Memory Device Layout.

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NOTES:

1. ■ INDICATES PIN 1.
2. FOR J4 ADDRESS SELECT: JUMPER IN = 0, JUMPER OUT = 1.
3. JUMPERS J1, J3, AND J5 FOR FACTORY USE ONLY.

Figure 2-2. Jumper Locations.

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2.4 Setting the Jumpers

In addition to installing memory devices, the user may also modify the operation of the Mx-RAM by setting certain jumpers. Jumper block locations are shown in Figure 2-2. Table 2-1 shows the factory default settings.

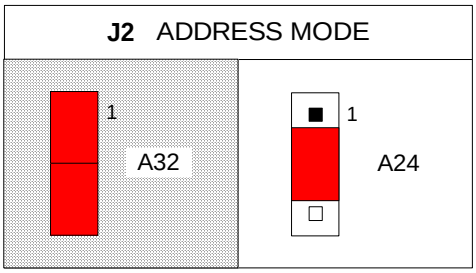


Figure 2-3. Address Mode Select.

Install jumpers in J2 as shown in Figure 2-3 to enable the VMEbus standard address (A24) mode or extended address (A32) mode. In standard mode the board responds to a 24-bit address and ignores the settings for address bits A31..A24. In extended mode all 32 bits of the address are used. A32 address mode is the factory default setting.

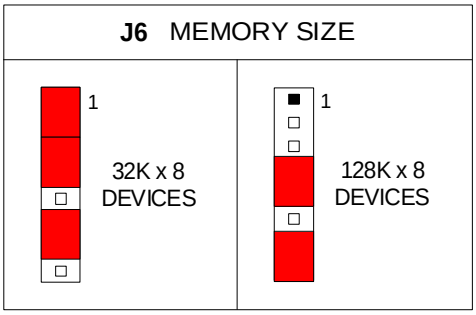


Figure 2-4. Memory Size Select.

Jumper block J6 is used to set the size of the memory devices installed in the Mx-RAM. The options are shown in Figure 2-4. With the jumpers set for 32K x 8 (28-pin) devices, the board address granularity is 1 Mbyte. With the jumpers set for 128K x 8 (32-pin) devices, the address granularity is 4 Mbytes. The default setting is configuration-dependent.

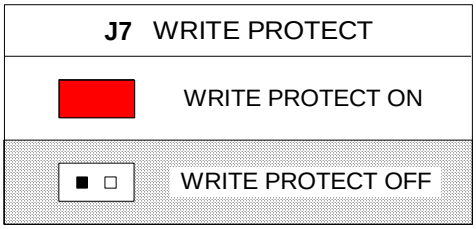


Figure 2-5. Write Protect Select.

Jumper block J7 controls the write protect option as shown in Figure 2-5. No jumper installed (default) permits memory writes to the Mx-RAM in the VMEbus non-privileged space. Install a jumper to protect memory and inhibit writes to the board in the non-privileged address space. If write protection is on, a bus error will be generated when non-privileged writes are attempted.

Jumper block J4 is used to set the Mx-RAM base address as shown in Figure 2-6. For the A24 address mode, only one address digit must be set. The others are ignored. For the A32 mode, all three digits must be considered. The factory default setting (A32 mode) is $04000000. Ensure selected addresses comply with Note 2 of Figure 2-6.

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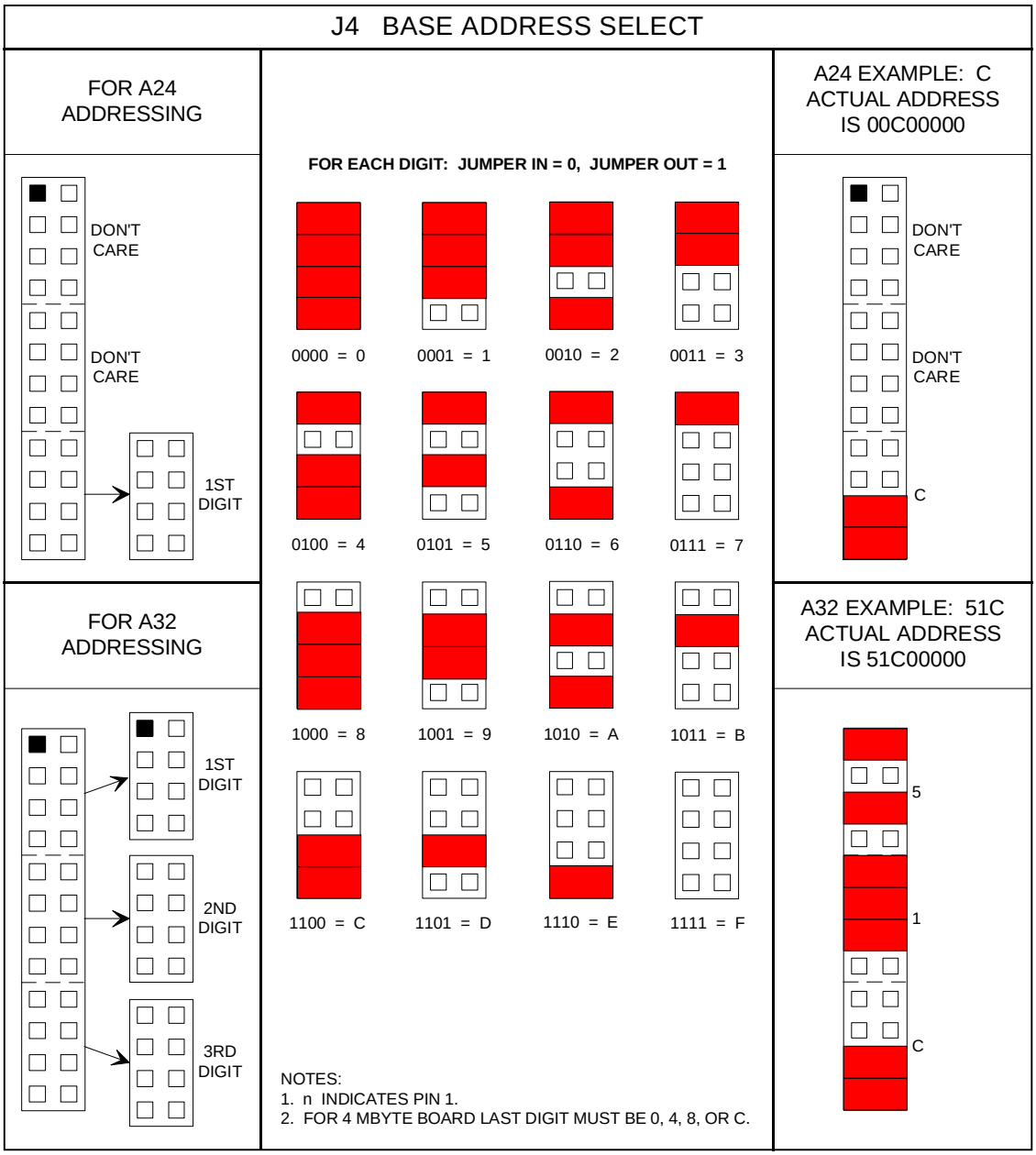


Figure 2-6. Base Address Select.

2.5 Installing the Board

The Mx-RAM may be installed in any slot of the VMEbus system. The board jumpers the VMEbus daisy chains with traces in the printed circuit board. No other preparation is required.

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Chapter three
MEMORY ADDRESSING

3.1 Memory Map

The memory map for an Mx-RAM populated with 32K x 8 SRAMs (1 Mbyte total capacity) and an Mx-RAM populated with 128K x 8 SRAMs (4 Mbyte total capacity) is shown in Table 3-1. The map also applies to 32K x 8 EEPROM devices. The base address is set by J4 in the VMEbus A32 or A24 space. The mapping of the memory quads is shown in the table as an offset from this base address. Data read from an unpopulated quad is indeterminate, and data written to an unpopulated quad is ignored.

Table 3-1. Mx-RAM Memory Map

Address Offset (32K x 8 Devices)	Address Offset (128K x 8 Devices)	Memory Quad
0 0000 to 1 FFFF	00 0000 to 07 FFFF	0
2 0000 to 3 FFFF	08 0000 to 0F FFFF	1
4 0000 to 5 FFFF	10 0000 to 17 FFFF	2
6 0000 to 7 FFFF	18 0000 to 1F FFFF	3
8 0000 to 9 FFFF	20 0000 to 27 FFFF	4
A 0000 to B FFFF	28 0000 to 2F FFFF	5
C 0000 to D FFFF	30 0000 to 37 FFFF	6
E 0000 to F FFFF	38 0000 to 3F FFFF	7

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3.2 Data Transfers

Data may be transferred between a master and the Mx-RAM (a VMEbus slave) with a width up to 32 bits. The data may be aligned or misaligned and follows the conventions for a D32 VMEbus board. The write protect feature may be inhibited by installing jumper J7.

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Chapter four
POWER MONITOR

4.1 Battery Status

Two 750 mAH lithium batteries provide battery backup power for the memory banks. Data retention is conservatively rated at ten years for factory installed SRAM at 25°C and fifty percent duty cycle. Battery B1 powers quads zero through three. Battery B2 powers quads four through seven unless those quads are configured for EEPROMs, in which case B2 and its associated circuitry are not installed on the board.

When VCC drops below 4.75 V, the power monitor inhibits accesses to all memory quads (an access that was in progress is allowed to complete before inhibiting that quad) and places the SRAMs in the data retention mode. When VCC drops below the battery voltage, the power monitor switches the SRAM power to the batteries.

On power up, when VCC exceeds the battery voltage, the power monitor switches the SRAM power to VCC. When VCC exceeds 4.75 V, the power monitor places the memory quads into the standby state. Two hundred milliseconds after VCC exceeds 4.75 V, the power monitor enables accesses to the SRAMs.

Battery status may be checked whenever the system power is applied by looking at the front panel battery status lights. Figure 4-1 illustrates the front panel with indicator lights. If the battery voltage is above 2.0 V, the green "PASS" light will illuminate. If the battery voltage is below 2.0 V, the red "FAIL" light will illuminate. Each battery has its own pair of status lights. For self-test, all lights illuminate whenever the VMEbus SYSRESET* signal is asserted (system reset in progress).

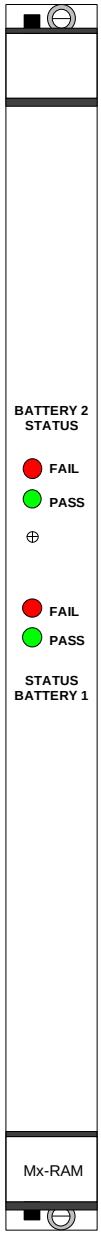


Figure 4-1. Mx-RAM Front Panel.

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Appendix A
SPECIFICATIONS

A.1 VMEbus Compliance

The Mx-RAM fully complies with the VMEbus standard:

ANSI/IEEE Std 1014-1987
IEEE Standard for a Versatile Backplane Bus: VMEbus

A.2 Addressing/Data Transfer Capabilities

The addressing capabilities are SAD032 and SADO24, which include A32, A24, and ADO (address only). The data transfer capability is SD32, which includes D16 and D08 (both even and odd).

A.3 AC Electrical Characteristics

The characteristics listed in Table A-1 apply over the full voltage and temperature range of the Mx-RAM. #1–3 in Table A-1 corresponds to times 1–3 in Figure A-1. All times are in nanoseconds. Typical values shown are at 5.0 Volts, 25°C.

Table A-1. Timing Parameters

#	Description	Typical	Max	Notes
1	Access Delay – Read or Write	275 ns	340 ns	1
2	Termination Delay – Read or Write	45 ns	90 ns	2
3	Cycle	515 ns	575 ns	3

Notes:
1. DSA* low to DTACK* or BERR* low.
2. Both data strobes high to DTACK* and BERR* not driven.
3. This time applies to consecutive accesses.

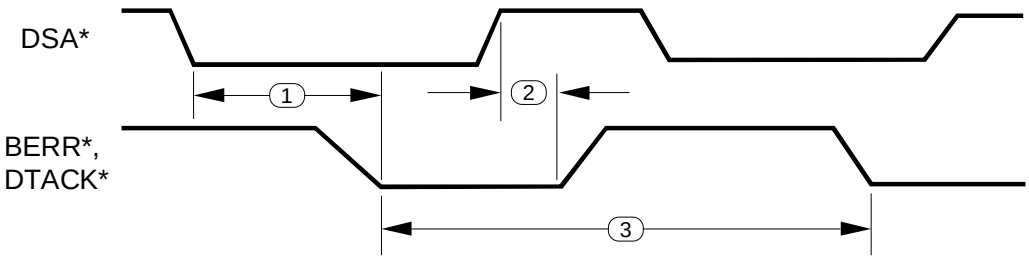


Figure A-1. Mx-RAM Timing Diagram.

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A.4 Power Requirements The power requirements for the Mx-RAM are shown in Table A-2.

Table A-2. Mx-RAM Power Requirements

Source	Min	Max	Units
V_{CC}	4.87	5.25	V
I_{CC} @ V_{CC} = max, Ta = max (no memories installed)		0.53	A

A.5 Environmental Limits The Mx-RAM meets the environmental specifications listed in Table A-3.

Table A-3. Mx-RAM Environmental Limits

	MD-RAM	MX-RAM	MR-RAM
Operating Temperature	0°C to 70°C	-40°C to 85°C	-40°C to 85°C
Storage Temperature	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
Shock: One axis Second axis Third axis	N/A	N/A	>50 Gs, 11 ms 53 Gs, 11 ms 48 Gs, 11.8 ms
Vibration	N/A	N/A	Test Range: 10 to 2000 Hz, 3 Gs First Resonant Frequency: 125 Hz
Relative Humidity (non-condensing)	0% to 90%	0% to 90%	0% to 90%

Note: Shock and vibration testing were conducted by an independent laboratory. The MR-RAM can be further characterized and certified for specific project requirements.

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