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U S E R ' S M A N U A L

16-BIT
DIGITAL I/O
M-MODULE

MODEL
M223

(FORMERLY
HP E2290A)

Document Part No: 11029584

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INTRODUCTION

This manual describes the operation and use of the C&H Model M223 16-Bit Digital I/O M-Module (Part Number 11029580). This module was formerly manufactured by HP (Agilent) as Model E2290A. C&H obtained the manufacturing rights from Agilent and now manufacturers it as C&H Model M223. This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as Ethernet, VME, VXI, PXI, cPCI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

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1.0 GENERAL DESCRIPTION

The M223 provides 16 digital channels on a single wide M-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules. The M223 may be installed on any carrier board supporting the M-Module specification. Carriers are available that allow the M223 to be used in Ethernet, VXI, VME, PCI, cPCI and other system architectures.

1.1 PURPOSE OF EQUIPMENT

The M223 is a digital input/output M-Module containing 16 data/actuator lines. These data lines offer TTL compatible inputs and open-drain outputs up to 30 volts. Each I/O line also provides active pull-up and pull-down for actuating external devices such as:

- Relays and switches
- High frequency coax relays or microwave switches
- Programmable attenuators
- Optical Isolators

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

- 16 digital inputs or outputs. Data that is written (output) may also be read back.
- Each bit is individually addressable.
- Support of interrupts for pattern matching. An interrupt occurs (if enabled) when the incoming data matches a specified pattern.
- Debounce capability for data lines used as inputs. The debounce circuitry allows incoming data to be debounced for a period of 3ms before being latched.
- TTL compatible levels or open-drain outputs. The 16 data lines provide for TTL compatible I/O (open-drain outputs up to 30 Volts, requires external pull-up).
- There are no I/O handshaking lines/modes.

1.2.2 Specifications

The M223 incorporates the standard 40-pin, 20x2 row connector interface to the carrier board for power and data/control, but does not have the 24-pin optional connector for carrying user-connections back onto the carrier board.

User input/output is provided through a standard 44-pin D-subminiature female receptacle (CONEC part number 302A10889X or equivalent). A mating connector kit can be ordered separately as AM111 (C&H Part Number 11029700-0001). The connector pin-outs are shown in Appendix A.

Table I. Specifications

Maximum Output Voltage	+30 VDC (I/O to Chassis or common)
Output Characteristics	Vout (hi): ≥ 2.9 V @ Isource ≤ 20 mA Vout(lo): ≤ 0.4 V @ Isink ≤ 200 mA
Input Characteristics	Vin(hi): ≥ 1.8 V Vin(lo): ≤ 0.8 V

Table II. Power Requirements

Input Supply	IPM (A)	IDM (A)
+5VDC	0.385	0.350
+12VDC	0	0
-12VDC	0	0

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (52.9 mm) wide.

1.2.4 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D16
Interrupts:	supported
DMA:	not supported
Triggers:	not supported
Identification:	IDENT
Manufacturer ID:	$0FFF_{16}$ (See note below)
Model Number:	$069A_{16}$
VXI Model Number:	0260_{16}

Note: C&H obtained the manufacturing rights from Hewlett Packard (Agilent) for this module. The ID's have been retained as Hewlett Packard to provide compatibility with existing SW drivers.

1.2.5 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The M223 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M/MA MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M/MA-Module together with the connector on the carrier as shown in Figure 1. Secure the module through the holes in the bottom shield using the original screws.

CAUTION: M/MA-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M/MA-Module and carrier.

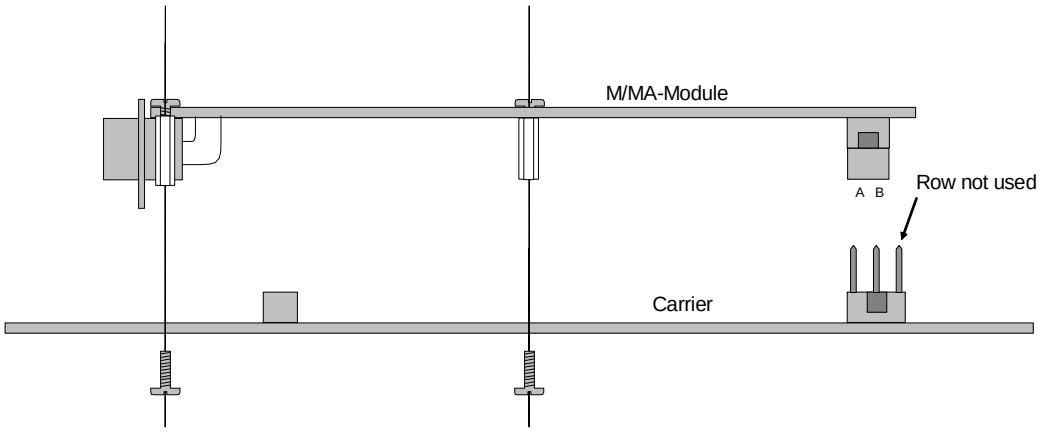


Figure 1. M-MODULE Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 OVERVIEW

A simplified functional block diagram is shown in Figure 2.

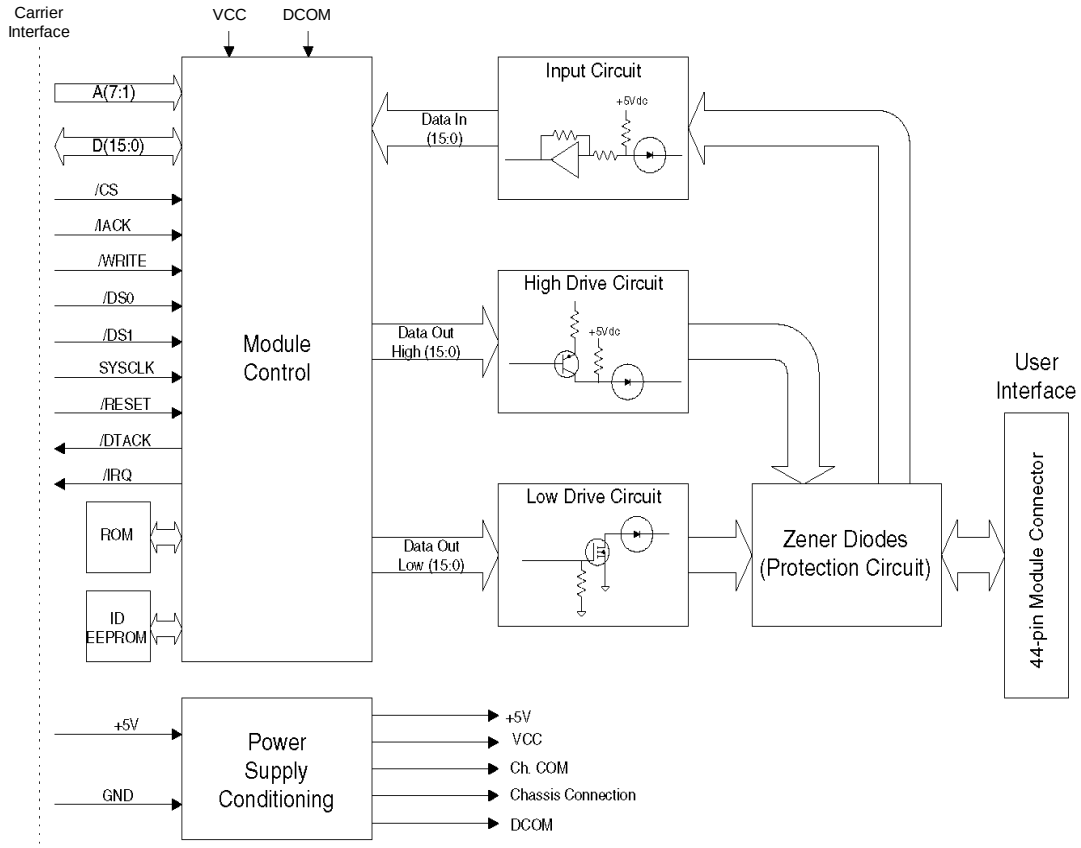


Figure 2. Functional Block Diagram

3.1.1 M-Module Interface

The M-Module Interface allows communication between the M223 and the carrier module. The interface is an asynchronous 16-bit data bus with interrupt capabilities. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for MA modules.

3.1.2 Module Control

This block contains all of the logic for the module including all registers, interrupt control and carrier interface.

3.1.3 ID EEPROM

The EEPROM holds sixty-four 16-bit words of M-Module ID data and VXI M-Module data.

3.1.4 Output Circuit

Figure 3 shows a simplified schematic of one bit of output circuitry and two example applications. A "1" means that the output is driven high (2.9 Vdc or greater, sourcing up to 20 mA); sourcing a "0" means the output is driven low (0.4 Vdc or less, sinking up to 200mA).

CAUTION: Do not exceed the 30Vdc external voltage; doing so may damage the module.

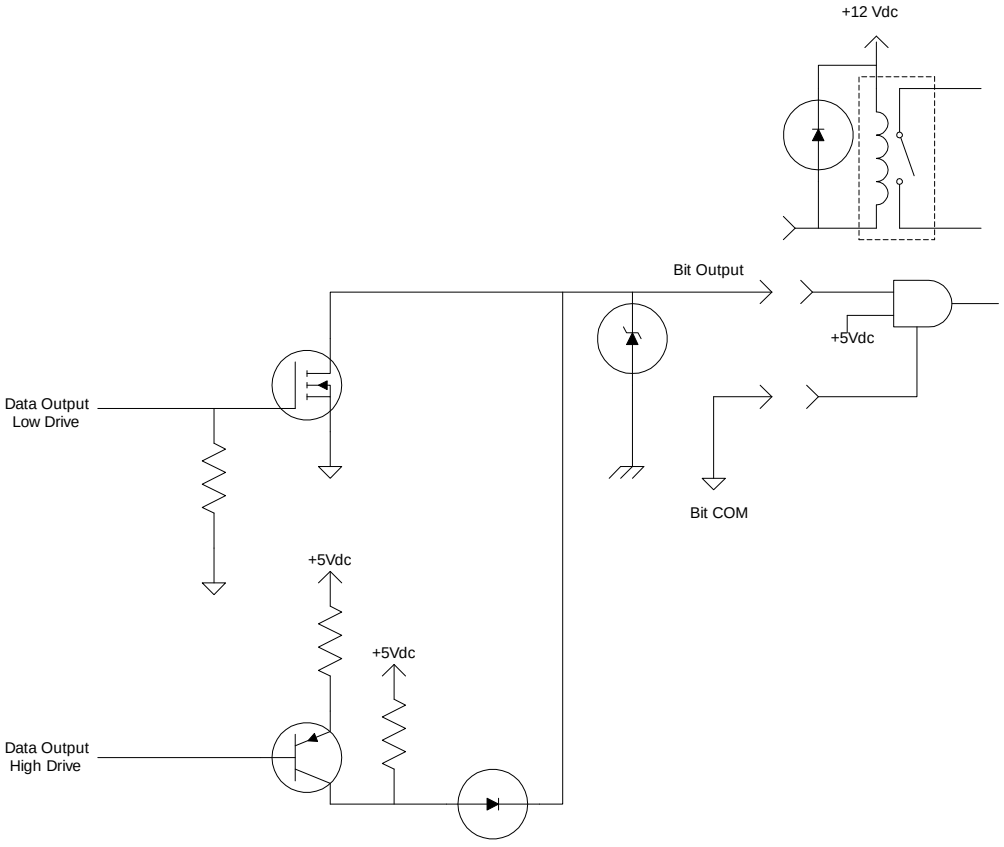


Figure 3. Simplified Digital Output Circuit

3.1.4.1 High Drive Circuit

The high drive circuit (active when sourcing a high, 2.9Vdc) consists of a blocking diode and a PNP transistor circuit for each line. The transistor is in a high impedance state when the line is not output-enabled or the line is driving low.

3.1.4.2 Low Drive Circuit

The low drive circuit (active when sourcing a low, 0.4Vdc) consists of one MOSFET, and a pull-down resistor. The MOSFET is in a high impedance state when the line is not output-enabled or the line is driving high. During a low level output, the MOSFET is turned on creating a low impedance path from the channel input to channel common. The MOSFET can sink up to 200mA.

3.1.5 Input Circuit

A simplified schematic of one bit of the input circuitry is shown in Figure 4. The input comparator maintains correct TTL high and low levels by shifting the input voltages to compensate for the forward voltage drop of the blocking diode. A reference voltage of +1.9Vdc is applied to the inverting input of the comparator. When the input is in the range of 0Vdc to +4.3Vdc the blocking diode is forward biased, and its forward voltage drop is added to the applied voltage. For example, when 0Vdc is applied to the data line, +0.7Vdc is present on the comparator's non-inverting input. Similarly, when the input signal is greater than +1.2Vdc, a voltage greater than +1.9Vdc is applied to the comparator's non-inverting input causing its output to go high. When the applied voltage is less than +1.2Vdc, a voltage less than +1.9Vdc is applied to the comparator causing its output to be low.

The pull-up resistor on the comparator's non-inverting input allows external ground connections and open circuits to be detected.

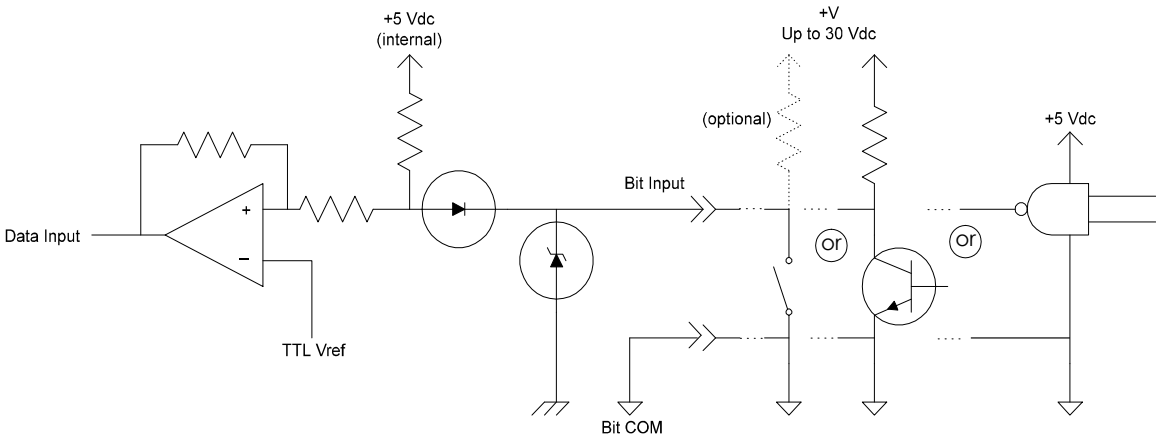


Figure 4. Simplified Digital Input Circuit

3.1.6 Ground and Power Supply Conditioning

This block filters the +5Vdc power to produce the VCC power necessary for the logic circuitry and isolates the various grounds used by the module. The module does not use ±12Vdc power.

3.2 IDENTIFICATION AND CONFIGURATION REGISTERS

3.2.1 I/O Registers

There are a variety of registers used to configure and control the M223 module. These registers are located in the IOSpace. The address map of the registers is shown in Table III. Details of the registers are provided in Figure 5.

Table III. I/O Address Map/Command Summary

IO REG. (HEX)	REGISTER DESCRIPTION	REGISTER TYPE
00	Status	Read Only
02	Control	Read/Write
04 – 0E	Reserved	NA
10	Output Latch	Read/Write
12	Output Enable	Read/Write
14	Input	Read Only
16	Compare Enable	Read/Write
18	Compare Data	Read/Write
1A – 7E	Unused	NA
80 - EF	ID EEPROM	Read/Write

M223 Reg. 00

Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Read-only															
Read	Reserved														INT	RDY

RDY ⇨ Ready (1 = ready to accept read/write instructions, 0 = busy).
INT ⇨ Interrupt Status (1 = interrupt is being asserted, 0 = interrupt is not being asserted)

M223 Reg. 02

Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Reserved													DC	INT	RST
Read	Reserved													DC	INT	RST

RST ⇨ Reset (1 = initiate a soft reset, 0 = terminate soft reset (default))
INT ⇨ Interrupt Enable (1 = interrupt upon a pattern match, 0 = disable interrupts (default))
DC ⇨ Debounce Control (1 = enables the debounce circuitry, 0 = disables debounce circuitry (default))

Figure 5. M223 I/O Registers

M223 Reg. 10

Output Latch

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

D00-D15 ⇨ Data Output Latch (1 = high, 0 = low (default))

M223 Reg. 12

Output Enable

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

D00-D15 ⇨ Data Output Enable (1 = enabled, 0 = disabled (default))

M223 Reg. 14

Input

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Read-only															
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

D00-D15 ⇨ Data Input Lines (1 = high, 0 = low)

Note: If the module is reset, with no loads or signals applied, the input register will contain the value $FFFF_{16}$ because of the internal pull-up resistors. If you source a low and then read the input register the response may still show a low. It takes approximately 5µS after the output is disabled for the pull-ups to bring the input circuit up to the minimum 1.8V for a high indication.

M223 Reg. 16

Compare Enable

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

D00-D15 ⇨ Compare Enable (1 = enabled, 0 = disabled (default))

Note: An interrupt occurs (if enabled) when an input data pattern matches the Pattern stored in the Compare Data Register. You control which data lines will be used in the comparison by enabling/disabling bit s in the Compare Enable Register. Additionally, the Interrupt Enable bit in the Control Register must be high for an interrupt to occur.

Figure 5. M223 I/O Registers (continued)

M223 Reg. 18

Compare Data

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

D00-D15 ⇨ Compare Enable (1 = enabled, 0 = disabled (default))

Note: This register is where you store a data pattern for interrupt pattern matching.

M223 Reg. 80-EF

ID EEPROM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused													CS	CLK	I/O
Read	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	I/O

I/O ⇨ Data In/Out (value from the Data Out pin of the ID EEPROM)
CLK ⇨ Clock (1 = forces the SK pin of the ID EEPROM high, 0 = low)
CS ⇨ Chip Select (1 = selects the ID EEPROM, 0 = deselects the ID EEPROM)

Notes:

1. The ID EEPROM register allows you to access the contents of the ID EEPROM which contains sixty-four 16-bit works of M-Module ID and VXI M-Module data.
2. CAUTION: Do not attempt to write to Bit00 of the ID EEPROM register. You could overwrite the contents of the EEPROM.

Figure 5. M223 I/O Registers (continued)

3.2.2 Module Identification

The M223 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial PROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time. The PROM is compatible with a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet. Data should not be written to the PROM.

The module also supports the VXI-IDENT function. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the PROM to 64 words and includes VXI compatible ID and Device Type Registers. Details are shown in Table IV.

Table IV. M/MA Module PROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	069A
2	Revision Number [1]	0002
3	Module Characteristics [2]	0868
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FFF [3]
18	VXI Device Type [4]	F260 (M223)
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) A Revision Number greater than 1 indicates that the module was manufactured by C&H Technologies.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	0 = does not need ±12V
11	1 = needs +5V
10	0 = no trigger outputs
9	0 = no trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI ID of 0xFFF is the identification value for Hewlett-Packard. C&H has left the ID equal to this value to allow operation with existing E2290A software drivers. The revision number (see note 1) can be used to identify the module as manufactured by C&H.
4) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	260_{16} = C&H specified VXI model code for M223

4.0 OPERATION

4.1 REGISTER PROGRAMMING

The M223 is a register-based instrument that is controlled through a series of I/O registers described in Section 3.2.1. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access.

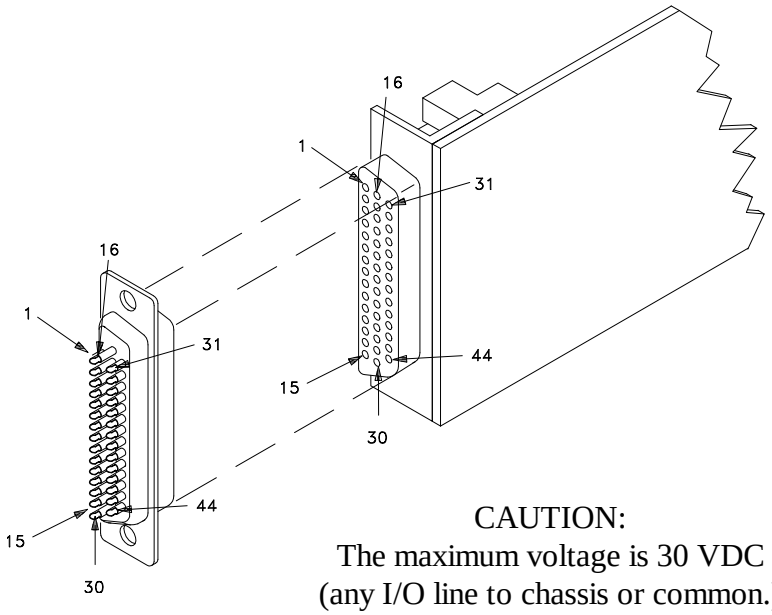
Typically a high level driver is available to aid in control of the module. Refer to the software driver documentation for instructions on using the driver.

4.2 INTERRUPTS

The M223 generates an interrupt request when incoming data matches a specified data pattern. The Compare Enable register specifies which bits are examined and the Compare Data register specifies the data pattern. Interrupts must be enabled in the Control register. Debounce is always active for the input to the pattern match interrupt circuit. The INT bit in the Status register mirrors the status of the /IRG signal on the M-module interface bus. The M223 releases the interrupt request during the interrupt acknowledge cycle (ROAK or hardware-end-of-interrupt type interrupt).

M-module carriers and system controllers treat the interrupts differently. Refer to your carrier and controller documentation to determine how to properly configure them to handle the M223 M-module interrupt request.

APPENDIX A: CONNECTORS



CAUTION:
The maximum voltage is 30 VDC
(any I/O line to chassis or common.)

	Pin #	Use		Pin #	Use		Pin#	Use
Data Port 1	1	Bit 0		16	Bit 0 COM		31	Chassis
	2	Bit 1		17	Bit 1 COM		32	Chassis
	3	Bit 2		18	Bit 2 COM		33	Chassis
	4	Bit 3		19	Bit 3 COM		34	Chassis
	5	Bit 4		20	Bit 4 COM		35	Chassis
	6	Bit 5		21	Bit 5 COM		36	Chassis
	7	Bit 6		22	Bit 6 COM		37	Chassis
Data Port 0	8	Bit 7		23	Bit 7 COM		38	Chassis
	9	Bit 8		24	Bit 8 COM		39	Chassis
	10	Bit 9		25	Bit 9 COM		40	Chassis
	11	Bit 10		26	Bit 10 COM		41	Chassis
	12	Bit 11		27	Bit 11 COM		42	Chassis
	13	Bit 12		28	Bit 12 COM		43	Bit 15
	14	Bit 13		29	Bit 13 COM		44	Bit 15 COM
	15	Bit 14		30	Bit 14 COM			

Figure A-1. Front Panel I/O Signals

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