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U S E R ' S M A N U A L

16-BIT ISOLATED DIGITAL I/O M-MODULE

MODEL M224

(FORMERLY HP E2291A)

Document Part No: 11029594

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INTRODUCTION

This manual describes the operation and use of the C&H Model M224 16-Bit Isolated Digital I/O M-Module (Part Number 11029590). This module was formerly manufactured by HP (Agilent) as Model E2291A. C&H obtained the manufacturing rights from Agilent and now manufacturers it as C&H Model M224. This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as Ethernet, VME, VXI, PXI, cPCI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

TABLE OF CONTENTS

1.0 GENERAL DESCRIPTION 1
1.1 PURPOSE OF EQUIPMENT 1
1.2 SPECIFICATIONS OF EQUIPMENT 1
1.2.1 Key Features 1
1.2.2 Specifications 1
1.2.3 Mechanical 2
1.2.4 Bus Compliance 2
1.2.5 Applicable Documents 2
2.0 INSTALLATION 3
2.1 UNPACKING AND INSPECTION 3
2.2 HANDLING PRECAUTIONS 3
2.3 INSTALLATION OF M/MA MODULES 3
2.4 PREPARATION FOR RESHIPMENT 4
3.0 FUNCTIONAL DESCRIPTION 5
3.1 OVERVIEW 5
3.1.1 M-Module Interface 5
3.1.2 Module Control 6
3.1.3 ID EEPROM 6
3.1.4 Sample Application 6
3.2 IDENTIFICATION AND CONFIGURATION REGISTERS 7
3.2.1 I/O Registers 7
3.2.2 Module Identification 10
4.0 OPERATION 11
4.1 REGISTER PROGRAMMING 11
4.2 INTERRUPTS 11

APPENDIX A: CONNECTORS A-1

LIST OF FIGURES

Figure 1. M-MODULE Installation 3
Figure 2. Functional Block Diagram 5
Figure 3. Sample Application 6
Figure 4. I/O Registers 8

Figure A-1. Front Panel I/O Signals A-1

LIST OF TABLES

Table I. Specifications 1
Table II. Power Requirements 2
Table III. I/O Address Map/Command Summary 7
Table IV. M/MA Module PROM IDENT Words 10

1.0 GENERAL DESCRIPTION

The M224 provides four groups of four isolated output channels on a single wide M-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules. The M224 may be installed on any carrier board supporting the M-Module specification. Carriers are available that allow the M224 to be used in Ethernet, VXI, VME, PCI, cPCI and other system architectures.

1.1 PURPOSE OF EQUIPMENT

The M224 can be used as a simple digital output device or as a driver for external relays. The module has four groups of four isolated output channels. Each group requires its own +5VDC power supply (supplied by the user). All channels are isolated from chassis and have their own ground.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

- Sixteen output channels separated into four isolated groups
- Each channel can sink up to 200mA and switch voltages up to 36VDC
- Programmable Interrupt Delay Timer provides for delayed acknowledgment of command completion

1.2.2 Specifications

The M224 incorporates the standard 40-pin, 20x2 row connector interface to the carrier board for power and data/control, but does not have the 24-pin optional connector for carrying user-connections back onto the carrier board.

User input/output is provided through a standard 44-pin D-subminiature female receptacle (CONEC part number 302A10889X or equivalent). A mating connector kit can be ordered separately as AM111 (C&H Part Number 11029700-0001). The connector pin-outs are shown in Appendix A.

Table I. Specifications

Open Collector-Emitter Voltage	36V Max
Saturation Collector-Emitter Voltage	< 0.5VDC
Sink Current (per Channel)	200mA
Isolation Voltage	42VDC
Programmable Busy Time	0.031875mS to 2089mS

Table II. Power Requirements

Input Supply	IPM (A)	IDM (A)
+5VDC	0.200	0.190
+12VDC	0	0
-12VDC	0	0

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (52.9 mm) wide.

1.2.4 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D16
Interrupts:	supported
DMA:	not supported
Triggers:	not supported
Identification:	IDENT
Manufacturer ID:	$0FFF_{16}$ (See note below)
Model Number:	$069B_{16}$
VXI Model Number:	0261_{16}

Note: C&H obtained the manufacturing rights from Hewlett Packard (Agilent) for this module. The ID's have been retained as Hewlett Packard to provide compatibility with existing SW drivers.

1.2.5 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The module contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M/MA MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M/MA-Module together with the connector on the carrier as shown in Figure 1. Secure the module through the holes in the bottom shield using the original screws.

CAUTION: M/MA-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M/MA-Module and carrier.

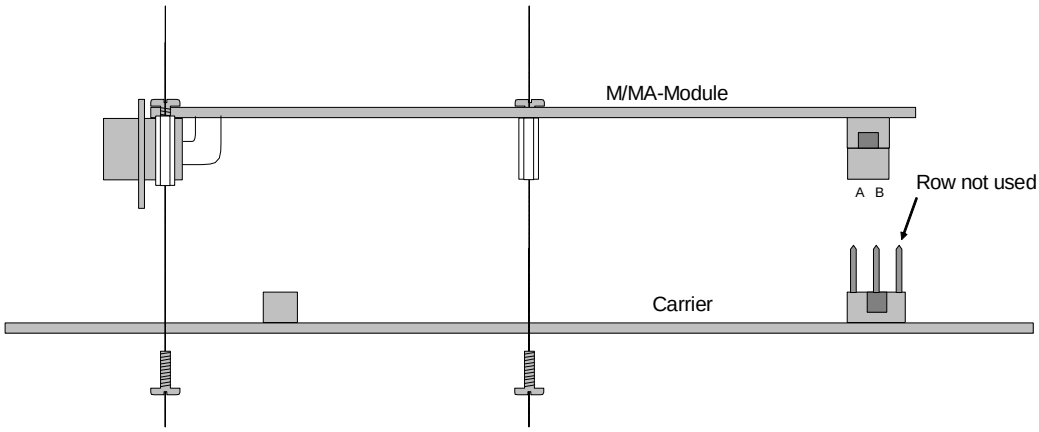


Figure 1. M-MODULE Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 OVERVIEW

A simplified functional block diagram is shown in Figure 2.

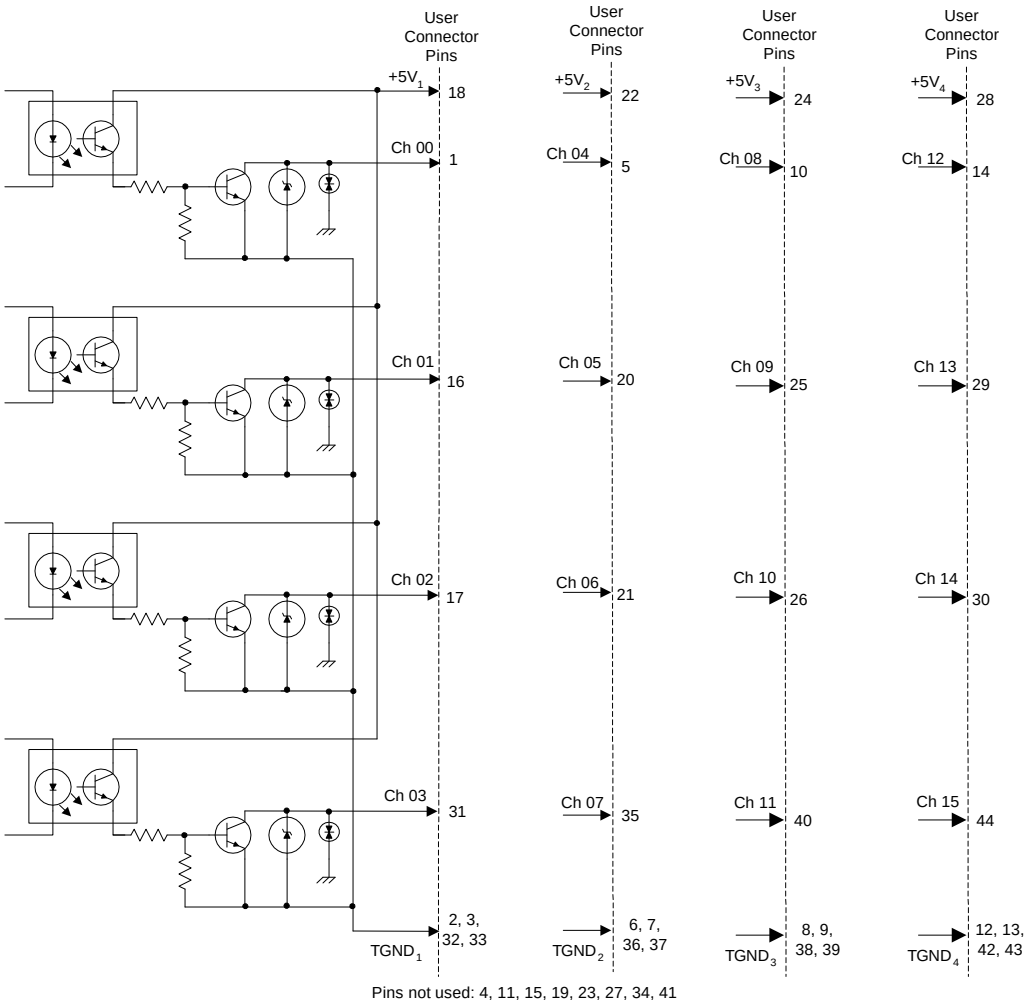


Figure 2. Functional Block Diagram

3.1.1 M-Module Interface

The M-Module Interface allows communication between the M224 and the carrier module. The interface is an asynchronous 16-bit data bus with interrupt capabilities. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for MA modules.

3.1.2 Module Control

This block contains all of the logic for the module including all registers, interrupt control and carrier interface.

3.1.3 ID EEPROM

The EEPROM holds sixty-four 16-bit words of M-Module ID data and VXI M-Module data.

3.1.4 Sample Application

The power supplies power the optical-isolators in each channel. If isolation is not necessary, one power supply can be used for all four groups.

The output of each channel is an open collector NPN transistor (emitter is connected to the TGNDn of each group's isolated power supply). Each channel is zener diode protected to +36VDC, do not exceed this voltage. Each channel's transistor can sink up to 200mA. Figure 3 shows a typical application for the module.

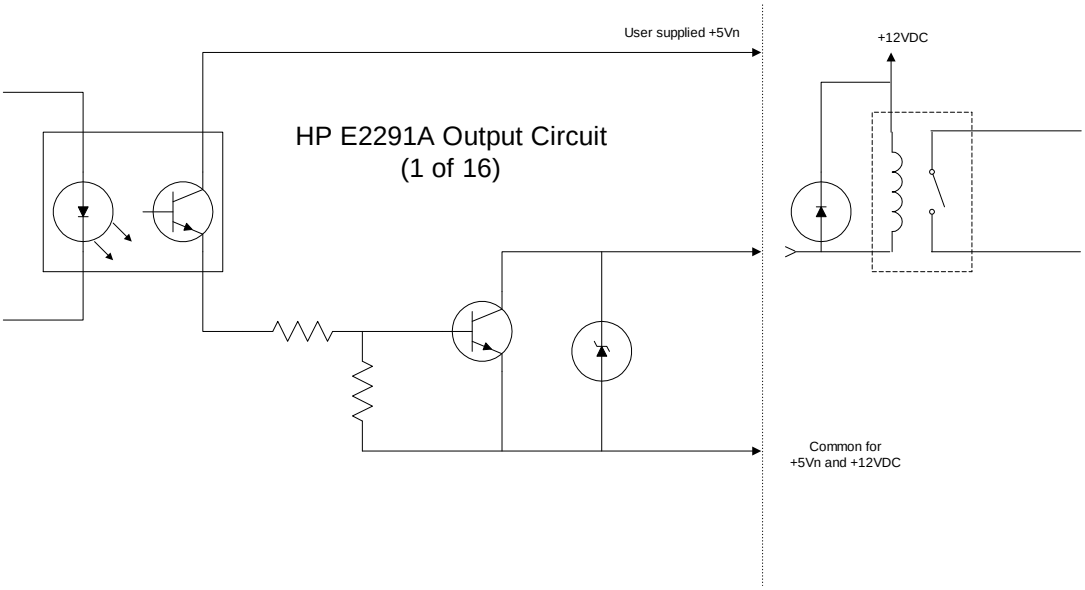


Figure 3. Sample Application

When a command to close a channel or open a channel (CLOSE means the output transistor is biased ON, low collector-emitter impedance; OPEN means the transistor is biased OFF, high collector-emitter impedance) completes execution, the module asserts an interrupt. For some external circuits, you may not want the interrupt until some period of time after the module finishes execution. For example, if you are using the module to control relays with a 13 -15 ms settling time, you can program a delay so that the module does not assert interrupt until after the relays have settled. The delay time is valid for all 16 channels. The time has a programmable range of 0.031875 ms to 2089 ms. The default time is 13 ms.

3.2 IDENTIFICATION AND CONFIGURATION REGISTERS

3.2.1 I/O Registers

There are a variety of registers used to configure and control the M224 module. These registers are located in the IOSpace. The address map of the registers is shown in Table III. Details of the registers are provided in Figure 4.

Table III. I/O Address Map/Command Summary

IO REG. (HEX)	REGISTER DESCRIPTION	REGISTER TYPE
00	Status	Read Only
02	Control	Read/Write
04	Interrupt	Read/Write
06 – 0E	Reserved	NA
10	Unused	NA
12	Delay	Write Only
14	Output	Read/Write
16 – FC	Reserved	NA
FE	ID EEPROM	Read/Write

Reg. 00

Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Read-only															
Read	Not Used								BUSY	Not Used						DIRQ

BUSY ⇨ Busy (0 = delay time not elapsed)
DIRQ ⇨ Delay Interrupt (1 = interrupt pending).

Reg. 02

Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used														DIEN	SRST
Read	Not Used														DIEN	SRST

SRST ⇨ Soft Reset (1 = initiate a soft reset)
DIEN ⇨ Delay Interrupt Enable (1 = interrupt enabled after Delay Timer)

Reg. 04

Interrupt

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used															DIRQ
Read	Not Used															DIRQ

DIRQ ⇨ Delay Interrupt (1 = interrupt pending).

Reg. 12

Delay

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	DLY															
Read	Not Used															

DLY ⇨ Delay Time (Delay Time = (Register Value + 1) * 0.031875mS, where Register Value = 0000_{16} - $FFFF_{16}$,the default time is 13mS)

Reg. 14

Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	CH15	CH14	CH13	CH12	CH11	CH10	CH09	CH08	CH07	CH06	CH05	CH04	CH03	CH02	CH01	CH00
Read	CH15	CH14	CH13	CH12	CH11	CH10	CH09	CH08	CH07	CH06	CH05	CH04	CH03	CH02	CH01	CH00

CH00-CH15 ⇨ Channels 0 - 15 (1 = closes channel (output transistor is biased on, low collector-emitter impedance), 0 = opens channel (output transistor is biased off, high collector-emitter impedance))

Figure 4. I/O Registers

ID EEPROM

Reg. 80-EF Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused													CS	CLK	I/O
Read	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	I/O

I/O ⇨ Data In/Out (value from the Data Out pin of the ID EEPROM)
CLK ⇨ Clock (1 = forces the SK pin of the ID EEPROM high, 0 = low)
CS ⇨ Chip Select (1 = selects the ID EEPROM, 0 = deselects the ID EEPROM)

Notes:

1. The ID EEPROM register allows you to access the contents of the ID EEPROM which contains sixty-four 16-bit works of M-Module ID and VXI M-Module data.
2. CAUTION: Do not attempt to write to Bit00 of the ID EEPROM register. You could overwrite the contents of the EEPROM.

Figure 4. I/O Registers (continued)

3.2.2 Module Identification

The M224 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial PROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time. The PROM is compatible with a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet. Data should not be written to the PROM.

The module also supports the VXI-IDENT function. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the PROM to 64 words and includes VXI compatible ID and Device Type Registers. Details are shown in Table IV.

Table IV. M/MA Module PROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	069B
2	Revision Number [1]	0002
3	Module Characteristics [2]	0868
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	CFFF [3]
18	VXI Device Type [4]	F261
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) A Revision Number greater than 1 indicates that the module was manufactured by C&H Technologies.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	0 = does not need ±12V
11	1 = needs +5V
10	0 = no trigger outputs
9	0 = no trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI ID of 0xFFF is the identification value for Hewlett-Packard. C&H has left the ID equal to this value to allow operation with existing E2291A software drivers. The revision number (see note 1) can be used to identify the module as manufactured by C&H.
4) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	261_{16} = C&H specified VXI model code for M224

4.0 OPERATION

4.1 REGISTER PROGRAMMING

The M224 is a register-based instrument that is controlled through a series of I/O registers described in Section 3.2.1. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access.

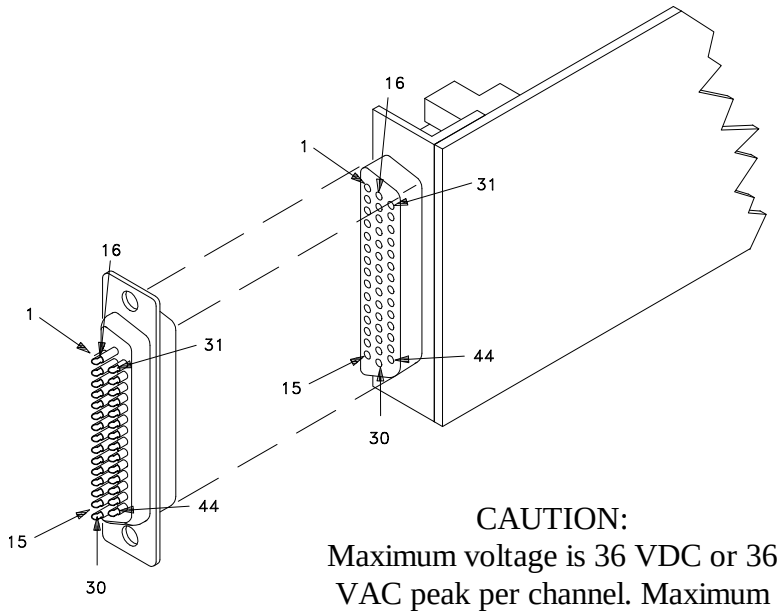
Typically a high level driver is available to aid in control of the module. Refer to the software driver documentation for instructions on using the driver.

4.2 INTERRUPTS

The M224 can generate an interrupt request when a programmed delay time expires. If you are using this M-Module to control relays for example, you may not want the interrupt to be asserted until after the relays have settled. By setting a delay time equal to or greater than the relay settling time, the M-Module will not assert the interrupt until after the relays have settled. The interrupt must be enabled in the Control Register (Reg. 0x02) and the delay time must be programmed in the Delay Register (0x12)

The M224 releases the interrupt request during the interrupt acknowledge cycle (ROAK or hardware-end-of-interrupt type interrupt). M-module carriers and system controllers treat the interrupts differently. Refer to your carrier and controller documentation to determine how to properly configure them to handle the M224 M-module interrupt request.

APPENDIX A: CONNECTORS



CAUTION:
Maximum voltage is 36 VDC or 36 VAC peak per channel. Maximum current is 200mA DC or 200mA AC peak per channel

	Pin #	Use		Pin #	Use		Pin#	Use
Group 1	1	Ch00		16	Ch01		31	Ch03
	2	$TGND_1$		17	Ch02		32	$TGND_1$
	3	$TGND_1$		18	$+5V_1$		33	$TGND_1$
	4	Unused		19	Unused		34	Unused
Group 2	5	Ch04		20	Ch05		35	Ch07
	6	$TGND_2$		21	Ch06		36	$TGND_2$
	7	$TGND_2$		22	$+5V_2$		37	$TGND_2$
Group 3	8	$TGND_3$		23	Unused		38	$TGND_3$
	9	$TGND_3$		24	$+5V_3$		39	$TGND_3$
	10	Ch08		25	Ch09		40	Ch11
	11	Unused		26	Ch10		41	Unused
Group 4	12	$TGND_4$		27	Unused		42	$TGND_4$
	13	$TGND_4$		28	$+5V_4$		43	$TGND_4$
	14	Ch12		29	Ch13		44	Ch15
	15	Unused		30	Ch14			

Channels	**External +5VDc Connections**
00 - 03	+5V1 (Pin 18), TGND1 (pins 2, 3, 32, 33)
04 - 07	+5V2 (pin 22), TGND2 (Pins 6, 7, 36, 37)
08 - 11	+5V3 (Pin 24), TGND3 (Pins 8, 9, 38, 39)
12 - 15	+5V4 (Pin 28), TGND4 (Pins 12, 13, 42, 43)

Figure A-1. Front Panel I/O Signals

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