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U S E R ' S M A N U A L

100MHZ PULSE GENERATOR M-MODULE

MODEL MA209

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Document Part No: 11028794A

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NOTE

The contents of any amendment may affect operation, maintenance, or calibration of the equipment.

REVISION HISTORY

Rev	Date	Description
*	02/08/2006	Original release
A	05/05/2008	Added 1/100PPS disciplining capability (Rev. C and higher assemblies)

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INTRODUCTION

This manual describes the operation and use of the C&H Model MA209 100MHz Pulse Generator M-Module (Part Number 11028790). This mezzanine module is designed to interface within any M-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as VME, VXI, PXI, cPCI, LXI and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

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1.0 GENERAL DESCRIPTION

The MA209 is a fully programmable pulse generator that allows the generation of precisely timed pulses of programmable frequency, pulse width, delay, and amplitude. Operational modes include single, continuous, burst, and follow trigger functions. Single, double, and inverted pulses are supported. Extensive trigger and gating logic provides comprehensive control of pulse timing. The internal base clock can be disciplined to an external reference clock for long term stability.

The module is physically implemented on a single wide M-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules. The MA209 may be installed on any carrier board supporting the M-Module specification. Carriers are available that allow the MA209 to be used in VXI, VME, PCI, cPCI and many other system architectures.

1.1 PURPOSE OF EQUIPMENT

The MA209 can be used in a wide variety of applications including functional verification of digital systems, signal simulation, design verification, and research and development.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

- 0.1Hz - 100MHz
- Programmable Pulse Width, Pulse Delay, and Double Pulse Spacing
- -1.5V to +6.5V Programmable Pulse Output
- Programmable Rise/Fall Time
- Single Pulse or Continuous Pulsing
- Single Pulse, Double Pulse, and Inverted Pulse Modes
- Burst Mode (1 to >2B pulses output on command or trigger)
- Follow Trigger Mode
- External Triggering
- Asynchronous or Synchronous Gating Modes
- On-board can be disciplined to 1PPS*, 100PPS*, or 10MHzexternal clock for long term stability

* Rev. C and higher

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1.2.2 Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V	1500*	mA
	+12V	400*	mA
	-12V	330*	mA
Input Voltage (FPSIGA & FPSIGB)	no damage	12	Vrms

* The power consumption exceeds the ANSI/VITA 12-1996 Specification for M-modules. Be sure check the specifications of the M-module carrier and system environment to ensure that it can handle the rated current load and heat dissipation.

AC CHARACTERISTICS (across operating temperature, unless otherwise specified)

		Limit			
Parameter	**Conditions**	**Min**	**Typ.**	**Max**	**Units**
Dynamic Performance					
Pulse Frequency	Internal Clock				
- Range		0.093		100M	Hz
- Resolution			0.093		Hz
- Accuracy [1]	without reference disciplining		±0.01		%
Pulse Width					
- Range			5 to (period – 3ns)		ns
- Accuracy [2]	at calibration temperature		±(3% + 250ps)		% + ps
Pulse Delay	from Sync Out				
- Range		5ns [3]		5s	
- Accuracy [2]	at calibration temperature		±(3% + 250ps)		% + ps
Double Pulse Spacing					
- Range			(width + 3ns) to (period – width – 3ns)		ns
- Accuracy [2]	at calibration temperature		±(3% + 250ps)		% + ps
Timing	Width, Delay, and Double Spacing				
- Resolution	4 to 13ns		10		ps
	13 to 24ns		20		ps
	> 24ns		(see note 4)		
- Temperature Coefficient	time increases with temperature rise	13	17	23	ppm/°C
Pulse Output Characteristics					
Output Voltage Range	$R_L = \infty$	-1.5		+6.5	V
Output Impedance			50		Ω
Resolution	12 bit		2		mV
Accuracy			±(2.0% + 100mV)		% + mV
Output Current	Source			60	mA
	Sink			60	mA
Short Circuit Current	Dynamic		±120		mA
Rise/Fall Time [5]	SR = 00 (100%)		2.5		V/ns
	SR = 01 (75%)		1.875		V/ns
	SR = 10 (50%)		1.25		V/ns
	SR = 11 (25%)		0.625		V/ns

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AC CHARACTERISTICS (continued)

Parameter	Conditions	Limit Min	Typ.	Max	Units
Input Characteristics (FPSIGA & FPSIGB)					
Input Threshold	Software programmable	-5.0		+5.0	V
Resolution	8 bit		39		mV
Input Impedance	Switch selectable	49 10K	50	51	Ω Ω
Accuracy	mid-point falling/rising		± (5% + 150mV)		% + mv
Hysteresis		50		350	mVpp
Frequency		0		100	MHz
Width		3		∞	ns
Sync Out Characteristics					
Timing [6]	Time from external trigger	20	27	35	ns
Output Impedance			50		Ω
Amplitude	Switch selectable, $R_L = \infty$		5.0 6.5		V V
Output Current	source sink			60 60	mA mA
Short Circuit Current	Dynamic		±120		mA
Rise/Fall Time	Fixed, $R_L = \infty$	2200	2500	2800	V/μs
Width [7]	Software programmable	4 50	5 55	6 60	ns ns
On-Board Clock & External Reference Disciplining [8]					
Frequency Stability	without ext. ref. disciplining with ext. ref. disciplining [9]			50 0.01	ppm ppm
External Ref. Frequency	programmable		1, 100, or 10M		Hz
Time to discipline lock	after 10 minute module warm-up		30	60	sec

Notes:

1. The frequency accuracy and long-term stability can be improved by using an external precision reference clock to discipline the internal oscillator. See External Reference Disciplining specifications for details.
2. Accuracy is within the tolerance specified at the calibration temperature. The calibration temperature is the ambient air temperature flowing across the module. Adequate airflow is assumed. The timing temperature coefficient can be used to correct for temperature variation.
3. The pulse delay can be programmed to zero; however, the minimum Sync Out time to output pulse specification applies. After the minimum time, the accuracy specification applies.
4. For times >24ns, the timing resolution is increases approximately 10ps for every 12ns increase in time.
5. The rise/fall time is specified for a programmed 5Vpp pulse (amplitude low = 0V, amplitude high = 5V) with output terminated into a 50Ω load. The slew rate is specified as the programmed amplitude divided by the 10% to 90% rise/fall time. Given the driver's output impedance of 50Ω, terminating the pulse output into a 50Ω load will effectively cut the voltage in half at the load and reduce the slew rate to half the specified rate. In addition, the slew rate will be slightly less at lower amplitudes.
6. The Sync Out time specified is from the external front panel input to the external front panel Sync Out. Backplane triggering and Sync Out will vary depending on the carrier used.
7. When using long Sync Out, only the leading edge should be used to ensure low jitter to Pulse Out. The falling edge and hence the width of Sync Out varies up to 10ns.
8. Starting with Rev. C of the MA209, the reference disciplining logic was upgraded to include support for a reference input frequency of 1PPS and 100PPS. Prior versions only supported a 10MHZ input frequency. In addition, the disciplining logic was improved to achieve better stability and faster reaction times.
9. The on-board oscillator will discipline to within one decade of the external reference, up to the specified stability.

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1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (52.9 mm) wide.

1.2.4 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules and the M-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	M-Module
Addressing:	A08
Data:	D16
Interrupts:	INTA & INTC
DMA:	not supported
Triggers:	Input/Output Trig A and Trig B
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	$0FC1_{16}$
Model Number:	$00D1_{16}$ (209 dec.)
VXI Model Number:	$0FE2_{16}$

1.2.5 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

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2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The MA209 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M-MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M-Module together with the connector on the carrier as shown in Figure 1. Secure the module through the holes in the bottom shield using the original screws.

CAUTION: M-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M-Module and carrier.

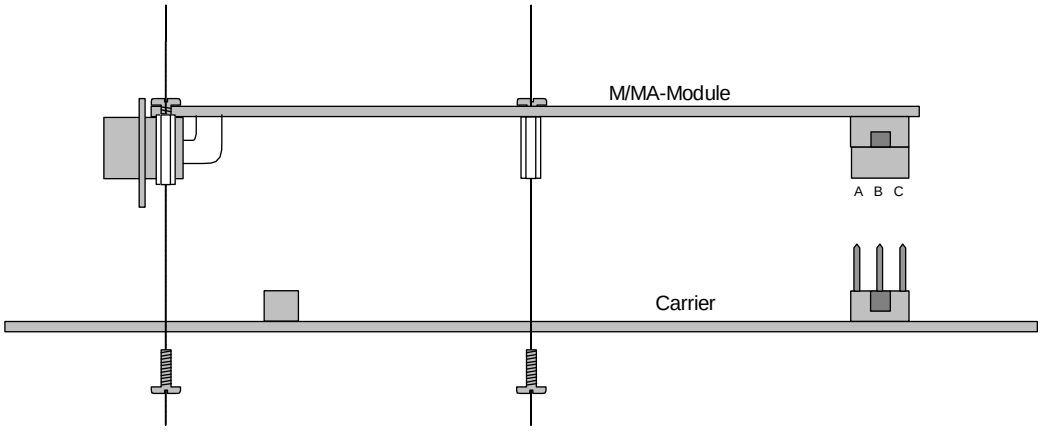


Figure 1. M-MODULE Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

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3.0 FUNCTIONAL DESCRIPTION

3.1 OVERVIEW

The MA209 utilizes programmable gate array logic, a microcontroller, digital/analog converters, pin driver devices, and variety of other digital and analog electronics to provide the pulse generation function. Register-based commands are received through the M-Module interface and acted upon either directly by the pulse generation logic or the microcontroller. In many cases, the microcontroller translates the register data into appropriate DAC or programmable clock values to produce the desired functionality. A simplified block diagram is shown in Figure 2.

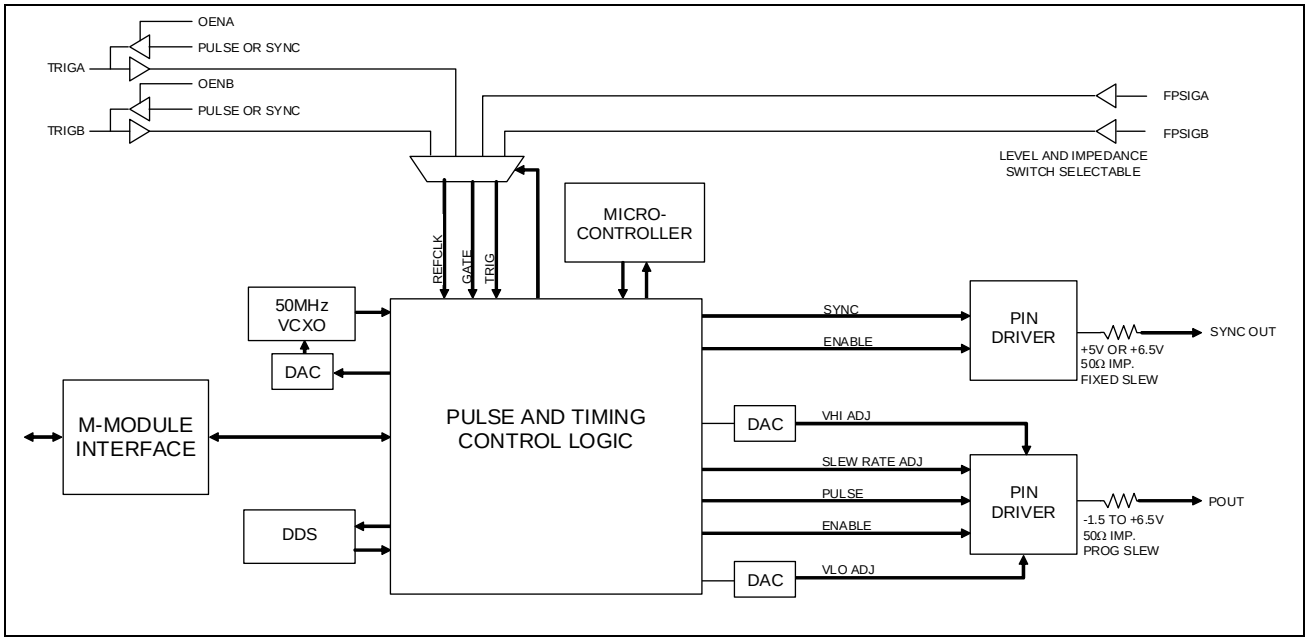


Figure 2. Functional Block Diagram

3.1.1 M-Module Interface

The M-Module Interface allows communication between the MA209 and the carrier module. The interface is an asynchronous 16-bit data bus with interrupt and trigger capabilities. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for MA modules.

3.1.2 Pulse and Timing Control Logic

The pulse and timing control logic provides the main control and generation of the raw pulse. It contains the user programmable control and status registers, the delay lock loop elements for precise clock control, the interface logic for the microcontroller and other functions, and numerous counters and control logic elements for the pulse formatting functions.

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3.1.3 Microcontroller

The microcontroller performs extensive interface functions to program the DDS, DACs, driver, counter registers, and delay values to produce the desired pulse. The DDS and DACs are programmed through the pulse and timing control logic via a serial interface to set the appropriate frequency, delay values, and pin driver amplitude. New values are computed anytime a user modifies a user register.

3.1.4 Direct Digital Synthesizer (DDS)

The DDS produces the main internal clock that controls the output pulse repetition rate. The DDS output is converted to square wave clock using a high speed comparator.

3.1.5 VCXO

The voltage controlled oscillator (VCXO) provides the base clock for the module. Even though the internal VCXO is fairly accurate and stable on its own, it can also be disciplined to a high precision 1PPS*, 100PPS*, or 10MHz external clock, if one is available. (* Rev. C and higher)

3.1.6 Pin Drivers

The pin driver provides the output voltage, current, and slew rate of the output pulse and Sync Out signals. The output impedance of both pulses is fixed at 50Ω.

3.1.7 Front Panel Input Signals

Two front panel trigger signals are provided for trigger, gate, or clock reference control from an external source. The inputs have switch selectable input impedance and threshold level control.

3.1.8 Backplane Trigger Signals

Two backplane M-module trigger signals are provided. As inputs, these signals can be used for external control of the trigger, gate, or clock reference. As outputs, they can be used to output the pulse and Sync Out signals. To utilize this feature, the M-Module carrier must support triggers (third row on M-module interface). Trigger operation differs depending on the carrier; see your carrier's documentation for details.

3.2 OPERATIONAL MODES

The MA209 can be configured for many different operating modes. In order to fully understand the operation, it is important to have a clear understanding of the terminology used and relationship of the various signals as shown in Figure 3.

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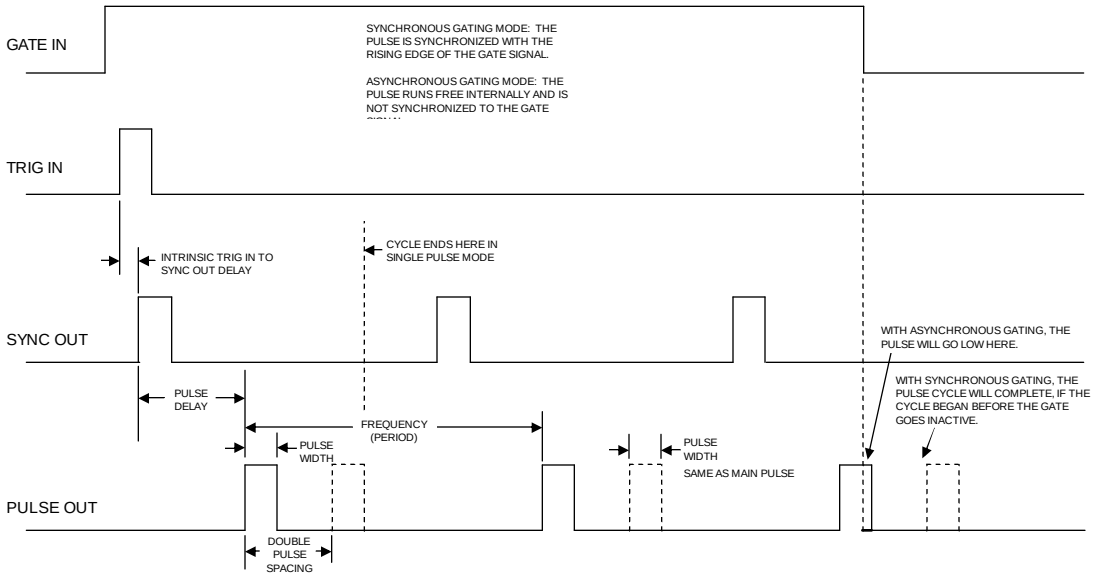


Figure 3. Pulse Terms and Relationships

3.2.1 Frequency (Pulse Repetition Rate)

The frequency of the output pulse can be controlled internally using the frequency value and mode registers or externally using an external trigger signal.

3.2.2 Pulse Width

The width of the output pulse can be controlled internally using the pulse width register or externally using an external trigger signal.

3.2.3 Pulse Delay and Double Pulse Spacing

The time from the Sync Out signal to the first output pulse and the space between the first pulse and second pulse, if Double Pulse is enabled, is programmable using the pulse delay and double pulse spacing registers.

3.2.4 Single Pulse or Double Pulse

The output pulse can be either a single or a double pulse. In Double Pulse mode, the widths of both pulses are the same.

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3.2.5 Run Modes

There are four run modes: single, continuous, burst, and follow trigger. In all cases, except follow trigger, the output pulse can be a single pulse or a double pulse. The run event can be initiated by software or an external trigger. Single pulse mode produces one pulse (or a double pulse) for each software or trigger signal. Continuous mode continues pulsing until software disables the run. Burst mode allows a preset number of pulses to be produced. In the follow trigger mode, the output pulse follows both the pulse width and period of the trigger input.

3.2.6 Pulse Output

The amplitude of the output pulse is programmable using the high and low level amplitude registers. The high level of the pulse and the low level of the pulse are controlled separately. The output can be enabled or disabled (placed in a high-impedance state) and the polarity (active-high or active-low) and slew rate are programmable. The output impedance is fixed at 50Ω.

3.2.7 Sync Out

The Sync Out signal indicates the start (T_0) of the pulse generation internal timing. The signal output can be enabled or disabled (placed in a high-impedance state) and its polarity (active-high or active-low) is programmable. The output level is switch selectable for 5.0V or 6.5V. The output impedance is fixed at 50Ω.

3.2.8 External Trigger

An external signal can be used to control the pulse repetition rate, instead of the internal counter. Either the positive going or negative going transition can be used. Additionally, the output pulse can follow the pulse width and period of the trigger input signal.

3.2.9 External Gate

The module can be configured to enable pulsing only during the presence of an external signal. The gate operation can be asynchronous or synchronous (see 4.1.6 for details). The external gate can be active-high or active-low.

3.2.10 External Reference Clock

An external 1PPS*, 100PPS*, or 10MHz signal can be used to discipline the internal clock. After an initial 10 minute module warm-up period, the internal clock will discipline in typically 30 seconds to within one decade of the external reference, up to the specified stability. Software register bits allow enabling the disciplining operation and provide status of the state of the reference and the internal clock.

* Rev. C and higher

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3.3 HARDWARE CONFIGURATION

The MA209 contains three sets of four switches that select the input impedance of the FPSIGA and FPSIGB front panel inputs, the mode of operation for the pulse generation logic, and the Sync Out level and impedance. The switches are located as shown in Figure 4. The switches are only accessible with the module removed from the carrier.

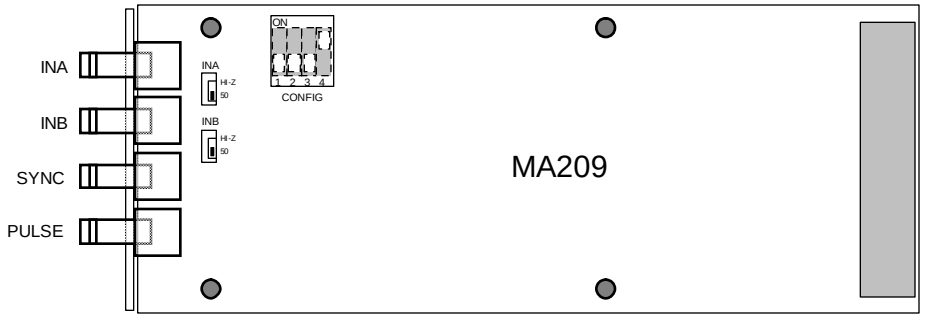


Figure 4. MA209 Hardware Configuration Switches

Front Panel Signals A & B Input Impedance These switches select the input impedance of the signal A and signal B front connector signals.

Input Signal A Impedance	Switch INA
>100KΩ	OFF
50Ω	ON

Input Signal B Impedance	Switch INB
>100KΩ	OFF
50Ω	ON

Sync Out Level These switches control the output level and impedance of the Sync Out signal.

Sync Out Level (no load)	Switch CONFIG 3
+5V	OFF
+6.5V	ON

Mode These switches control special modes of operation. These modes are undefined at this time, but are available for future implementations with special purpose modes.

Special Mode 1	Switch CONFIG 1
Normal	OFF
Factory Debug Mode*	ON

* Rev. C and higher

Special Mode 2	Switch CONFIG 2
Undefined	OFF
Undefined	ON

CONFIG Switch 4 is not used.

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3.4 INPUT/OUTPUT SIGNALS

The front panel input/output signals are as shown in Figure 5 and are briefly described below. The connector shield of each of the connectors are tied to chassis ground.

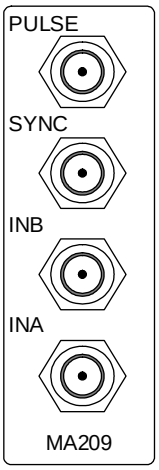


Figure 5. Front Panel

INA This SMA connector is the input signal A. This input is software configurable as the trigger, gate, or reference clock signal. The threshold level and input active high/low are programmable. The input impedance is switch selectable.

INB This SMA connector is the input signal B. This input is software configurable as the trigger, gate, or reference clock signal. The threshold level and input active high/low are programmable. The input impedance is switch selectable.

SYNC This SMA connector is the output Sync Out signal. The output level is switch selectable.

PULSE This SMA connector is the output Pulse signal. The high and low levels are programmable.

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3.5 IDENTIFICATION AND CONFIGURATION REGISTERS

3.5.1 I/O Registers

There are a variety of registers used to configure and control the MA209 module. These registers are located in the IOSpace. The address map of the registers is shown in Table I. Details of the registers are provided in Figure 6.

Table I. I/O Address Map/Command Summary

IO REG. (HEX)	REGISTER DESCRIPTION
00	Control/Status
02	Interrupt Control
04	Trigger/Gate Control
06	Version Info*
08	DDS Frequency – Low
0A	DDS Frequency – High
0C	Frequency Divider – Low
0E	Frequency Divider – High
10	Pulse Width – Low
12	Pulse Width – Mid
14	Pulse Width – High (7 bits)
16	Pulse Delay – Low
18	Pulse Delay – Mid
1A	Pulse Delay – High (7 bits)

IO REG. (HEX)	REGISTER DESCRIPTION
1C	Double Pulse Spacing – Low
1E	Double Pulse Spacing – Mid
20	Double Pulse Spacing – High (7 bits)
22	Burst Count – Low
24	Burst Count – High
26	Amplitude – Low
28	Amplitude – High
2A	Slew Rate
2C	Input Threshold Level
2E	Reserved
30	Calibration Control
32 – 76	Calibration Registers – Factory Use Only
78-7A	Reference Count Low/High (read only)*

* Rev. C and higher

MA209
Reg. 00

Control/Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	SI	SOE	RFE1	-	REFSEL		RFE0	PI	POE	DP	SPW	RMODE		RUN
Read	RDY	LOK	SI	SOE	RFE1	DET	REFSEL		RFE0	PI	POE	DP	SPW	RMODE		RUN

RDY ⇨ Ready (1 = ready)
LOK ⇨ Internal VCXO Locked to External Reference Clock (0 = not locked, 1 = locked)
SI ⇨ Sync Out Inversion (0 = normal (active high) (default), 1 = inverted (active low))
SOE ⇨ Sync Out Enable (0 = disabled (default), 1 = enabled)
RFE1/0 ⇨ Reference Clock Enable (00 = default) [2]
- 00 Disabled
- 01 100PPS Input (Rev. C and higher)
- 10 10MHz Input
- 11 1PPS Input (Rev. C and higher)

DET ⇨ Reference Clock Detected (0 = not detected, 1 = detected)
REFSEL ⇨ Reference Clock Source Select (if enabled)
- 00 Front Panel Signal A
- 01 Front Panel Signal B
- 10 Backplane Trigger A
- 11 Backplane Trigger B

PI ⇨ Pulse Inversion (0 = normal (active high) (default), 1 = inverted (active low))
POE ⇨ Pulse Output Enable (0 = disabled (default), 1 = enabled front panel output)
DP ⇨ Double Pulse Mode (0 = single pulse (default), 1 = double pulse)
SPW ⇨ Sync Out Pulse Width (0 = 5ns (default), 1 = 50ns)
RMODE ⇨ Run Mode
- 00 Single pulse or double pulse (default)
- 01 Continuously cycle
- 10 Burst count
- 11 Follow Trigger Input

RUN ⇨ Run (0 = enable (default), 1 = disable)

Notes:
1. Always set the RUN bit to 0 before changing the RMODE. Do not change the RMODE at the same time the RUN bit is changed (use separate write operations).
2. RFE1/0 bits are separated to maintain backwards compatibility with MA209 versions that do not support 1PPS and 100PPS input reference clocks.

Figure 6. MA209 I/O Registers

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MA209
Reg. 02

Interrupt Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	MIEN	-	-	-	-	-	-	IT	-	-	-	-	-	-	BIEN	RIEN
Read	MIEN	0	VL4X	VL2X	DL4X	DL2X	0	IT	0	0	EOB	RDI	0	0	BIEN	RIEN

MIEN ⇨ Master Interrupt Enable (0 = disabled (default), 1 = enable)
VL4X ⇨ Internal VCXO 4X DLL Lock (0 = locked, 1 = not locked) [1]
VL2X ⇨ Internal VCXO 2X DLL Lock (0 = locked, 1 = not locked) [1]
DL4X ⇨ Internal DDS 4X DLL Lock (0 = locked, 1 = not locked) [1]
DL2X ⇨ Internal DDS 2X DLL Lock (0 = locked, 1 = not locked) [1]
IT ⇨ Interrupt Type (0 = Type A, software-end-of-interrupt (default), 1 = Type C, hardware-end-of-interrupt)
EOB ⇨ End of Burst (1 = EOB occurred (write a 1 to this bit to clear))
RDI ⇨ Ready Interrupt (1 = Ready bit went high (write a 1 to this bit to clear))
BIEN ⇨ End of Burst Interrupt Enable (0 = disabled (default), 1 = enabled)
RIEN ⇨ Ready Interrupt Enable (0 = disabled (default), 1 = enabled)

Notes:
1. These bits are for diagnostic purposes only. They indicate proper locking of the internal DLL clocks. DDS locking (DL2X & DL4X) will not occur when FGM = 0 (direct DDS mode). These bits are only valid on Rev. C and higher assemblies.
2. When using Type C interrupts (IT = 1), the interrupt pending bits 7-0 are presented as the interrupt vector during the interrupt acknowledge cycle. The interrupt is also disabled and must be re-enabled during the interrupt service routine.

Figure 6. MA209 I/O Registers (continued)

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MA209
Reg. 04

Trigger/Gate Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	SG	GM	-	DSMS	GATESEL				MTRGSELB		MTRGSELA		TRGSEL			
Read	SG	GM	0	DSMS	GATESEL				MTRGSELB		MTRGSELA		TRGSEL			

SG ⇨ Synchronous Gating (0 = asynchronous gating, 1 = synchronous gating)
GM ⇨ Gated Mode (0 = disabled, 1 = enabled)
DSMS ⇨ DDS Sync Master/Slave (0 = use this DDS SYNC_CLK as master synchronization signal, 1 = this DDS accepts synchronization from other unit) [3]
GATESEL ⇨ Gate Source Select

	High Level		Low Level
0000	Ignore Gate (default)	1000	(reserved)
0001	Front Panel Signal A	1001	Front Panel Signal A
0010	Front Panel Signal B	1010	Front Panel Signal B
0011	(reserved)	1011	(reserved)
0100	Backplane M-Trigger A	1100	Backplane M-Trigger A
0101	Backplane M-Trigger B	1101	Backplane M-Trigger B
0110	(reserved)	1110	(reserved)
0111	(reserved)	1111	(reserved)

MTRGSELx ⇨ M-Trigger A and M-Trigger B Control

00	Trigger Input (default)
01	Output Pulse
10	Output Sync
11	DDS SYNC_IN or DDS SYNC_OUT [3]

TRGSEL ⇨ Trigger Source Select

	Rising Edge		Falling Edge
0000	Software RUN bit (default)[1]	1000	(reserved)
0001	Front Panel Signal A	1001	Front Panel Signal A
0010	Front Panel Signal B	1010	Front Panel Signal B
0011	(reserved)	1011	(reserved)
0100	Backplane M-Trigger A	1100	Backplane M-Trigger A
0101	Backplane M-Trigger B	1101	Backplane M-Trigger B
0110	(reserved)	1110	(reserved)
0111	(reserved)	1111	(reserved)

Notes:
1. Setting the RUN bit will cause a pulse or pulse train to occur.
2. All unused bits should be written as 0's to ensure future revision compatibility.
3. The DSMS bit sets the direction and usage of the signals. When DSMS = 0, DDS SYNC_OUT is output to the selected M-Trigger. When DSMS = 1, DDS SYNC_IN is input from the selected M-Trigger.

MA209
Reg. 06

Version Info*

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(read only)								(read only)							
Read	FWMAJ				FWMIN				LGMAJ				LGMIN			

FWMAJ ⇨ Firmware Major Version (first major release is 1, prerelease is 0)
FWMIN ⇨ Firmware Minor Version (minor releases involve insignificant changes or corrections)
LGMAJ ⇨ Logic Major Version (first major release is 1, prototype is 0)
LGMIN ⇨ Logic Minor Version (minor releases involve insignificant changes or corrections)

*Rev. C and higher

Figure 6. MA209 I/O Registers (continued)

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MA209 Reg.08

DDS Frequency – Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15							Low Order Bits								0
Read	15							Low Order Bits								0

MA209 Reg.0A

DDS Frequency – High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31							High Order Bits								16
Read	31							High Order Bits								16

Notes:

1. Each bit represents ~0.093Hz (use 400MHz ÷ (2^{32} – 1) for programming).
2. When FGM = 1 (frequency divider mode), the frequency must be set to a value >25MHz and ≤50MHz.
3. The registers must be written in the order low then high. The new frequency divider value does not take effect until the high order register is written.

MA209 Reg.0C

Frequency Divider – Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15							Low Order Bits								0
Read	15							Low Order Bits								0

MA209 Reg.0E

Frequency Divider – High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	FGM	-	29						High Order Bits							16
Read	FGM	0	29						High Order Bits							16

FGM ⇨ Frequency Generation Mode (0 = DDS output directly controls the pulse frequency (default), 1 = pulse frequency is controlled by a combination of the DDS output and a divider value)

Notes:

1. These registers are only used when the FGM bit the Frequency Mode Control register is set.
2. The pulse frequency is equal to (DDS Frequency × 4) ÷ Frequency Divider value.
3. The minimum divider value is two (2).
4. The registers must be written in the order low then high. The new frequency divider value does not take effect until the high order register is written.

Figure 6. MA209 I/O Registers (continued)

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MA209 Reg. 10

Pulse Width – Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15	Low Order Bits														0
Read	15	Low Order Bits														0

MA209 Reg. 12

Pulse Width – Mid

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31	Middle Order Bits														16
Read	31	Middle Order Bits														16

MA209 Reg. 14

Pulse Width – High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								39	High Order Bits						32
Read	0								39	High Order Bits						32

Notes:

1. Each bit represents 10ps with 0 equal to the minimum delay (see note 3).
2. The value must be greater than 4ns and less that 99% of the pulse period.
3. The registers must be written in the order low, mid., and then high. The new pulse delay does not take effect until the high order register is written.

MA209 Reg. 16

Pulse Delay - Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15	Low Order Bits														0
Read	15	Low Order Bits														0

MA209 Reg. 18

Pulse Delay - Mid

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31	Middle Order Bits														16
Read	31	Middle Order Bits														16

MA209 Reg. 1A

Pulse Delay – High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								39	High Order Bits						32
Read	0								39	High Order Bits						32

Notes:

1. Each bit represents 10ps with 0 equal to the minimum delay (see note 3).
2. The registers must be written in the order low, mid., and then high. The new pulse delay does not take effect until the high order register is written.
3. The time to an un-delayed output pulse as specified in Section 1.2.2, Sync Out Characteristics, must be taken into account when programming the desired pulse delay time.

Figure 6. MA209 I/O Registers (continued)

MA209
Reg.1C

Double Pulse Spacing – Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15							Low Order Bits								0
Read	15							Low Order Bits								0

MA209
Reg.1E

Double Pulse Spacing – Mid

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31							Middle Order Bits								16
Read	31							Middle Order Bits								16

MA209
Reg. 20

Double Pulse Spacing – High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								39			High Order Bits				32
Read	0								39			High Order Bits				32

Notes:

1. Each bit represents 10ps with 0 equal to 0ns.
2. The value must be greater than the Pulse Width + 1ns and less than the pulse period – the pulse width – 1ns.
3. The registers must be written in the order low, mid., and then high. The new pulse delay does not take effect until the high order register is written.

MA209
Reg.22

Burst Count – Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15							Low Order Bits								0
Read	15							Low Order Bits								0

MA209
Reg.24

Burst Count - High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31							High Order Bits								16
Read	31							High Order Bits								16

Notes:

1. The minimum burst count is one.
2. The registers must be written in the order low then high. The new burst count does not take effect until the high order register is written.

Figure 6. MA209 I/O Registers (continued)

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MA209 Reg. 26

Output Amplitude - Low Level

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	See Note											
Read	0	0	0	0	See Note											

Note: Each bit represents ~2mV (use 8V ÷ (2^{12} -1) for programming) with zero representing -1.5V (default = 0, -1.5V).

MA209 Reg. 28

Output Amplitude - High Level

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	See Note											
Read	0	0	0	0	See Note											

Note: Each bit represents ~2mV (use 8V ÷ (2^{12} -1) for programming) with zero representing -1.5V (default = 0, -1.5V).

MA209 Reg. 2A

Slew Rate

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SR	
Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SR	

SR ⇨ Output Pulse Slew Rate

- 00 100% of specified slew rate (default)
- 01 75% of specified slew rate
- 10 50% of specified slew rate
- 11 25% of specified slew rate

MA209 Reg. 2C

Input Threshold Level

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Signal B Level (see note)								Signal A Level (see note)							
Read	Signal B Level (see note)								Signal A Level (see note)							

Note: Each bit represents ~39 mV (use 10V ÷ (2^{8} – 1) for programming) with zero representing -5.0V (default = 0, -5.0V).

Figure 6. MA209 I/O Registers (continued)

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MA209
Reg. 30

Calibration Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	CRST	ECAL	-	-	Factory Use Only											
Read	0	ECAL	CFGMD		Factory Use Only											

CRST ⇨ Calibration Reset (1 = Resets all calibration values to factory default) [1, 2]
ECAL ⇨ Enable Calibration (1 = enable writing of calibration values (default = 0)) [3]
CFGMD ⇨ Configuration Mode* (indicates status of Mode configuration switches, OFF = 0, ON = 1)
00 Normal Operation (default)
01 Factory Debug Mode
10 unspecified
11 unspecified
*Rev. C and higher

Notes:
1. CRST must be set to zero in order to write any of the calibration values.
2. Writing a one to CRST will reset all calibrations values to the factory default values.
3. This bit is not implemented in Revision 1 firmware. The firmware revision can be found in Word 2 of the IDENT PROM (see Table II for details). In Revision 1 firmware, the "Factory Use Only" bits can be easily written to value that may effect the accuracy of the pulse width. If this occurs, use the CRST bit to reset the calibration values to factory default values.

MA209
Reg.78

Reference Count – Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15	(read only)														0
Read	15	Low Order Bits														0

MA209
Reg.7A

Reference Count – High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31	(read only)														16
Read	31	High Order Bits														16

Notes:
1. The count is a 2's complement integer value. Each count represents a difference of approximately 0.0025ppm. A positive value indicates that the internal VCXO is slower than the external reference.
2. The registers must be read in the order low then high.
3. This register is only available Rev. C and higher assemblies.

Figure 6. MA209 I/O Registers (continued)

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3.5.2 Module Identification

The MA209 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial PROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time. Instructions for reading the IDENT PROM are given in section 4.5. Data can not be written to the PROM.

The module also supports the VXI-IDENT function. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the PROM to 64 words and includes VXI compatible ID and Device Type Registers. Details are shown in Table II.

Table II. M-Module PROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00D1 (209 dec.)
2	Revision Number [1]	0003
3	Module Characteristics [2]	1E68
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (C&H)
18	VXI Device Type [3]	FFE2 (MA209)
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the functional revision level of the module (1 = A, 2 = B, etc.). It does not necessarily correspond to the hardware assembly level.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = needs ±12V
11	1 = needs +5V
10	1 = trigger outputs
9	1 = trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type C
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	$FE2_{16}$ = C&H specified VXI model code for MA209

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4.0 OPERATION

The MA209 is a register-based instrument that is controlled through a series of I/O registers described in Section 3.5.1. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access.

4.1 PROGRAMMING

4.1.1 Writing Register Values

Normal 16-bit wide register values can be written in one write operation using 16-bit register access. However, some pulse parameters, such as the pulse period, pulse width, and pulse delay, require more than 16-bits. Special attention must be given when programming these values. To prevent a pulse parameter from changing until the entire value is written, the order of the write operations are important. The internal logic is configured to only accept the change when the high-order bits are written. Therefore, the application software must write the low bits first, then the middle bits, and lastly the high bits.

4.1.2 Pulse Programming

With the RUN bit disabled (0) in the Control/Status register, set the desired pulse frequency, pulse width, pulse delays, high/low amplitude, desired trigger control mode, pulse mode (single or double pulse), and run mode (single, continuous, burst, or follow trigger). After setting the desired pulse parameters, a finite amount of time (<20ms) is required for configuration of the internal logic. The module will signal that it is ready to run by setting the RDY bit. Application software should verify the module is ready by reading the RDY bit. If desired, an interrupt can be generated to signal this event. Once the RDY bit is verified, enable the RUN bit (1). Modifications can be made to all settings except for RMODE without clearing the RUN bit; however, the RDY bit will go low momentarily and there may be a pulse glitch while the configuration is being adjusted.

4.1.2.1 Pulse Delay

The pulse delay is defined as the amount of time from the leading edge of Sync Out to the leading edge of the output pulse. Pulse delay is user programmable from 5ns to 5 seconds.

4.1.2.2 Sync Out

Sync Out marks the beginning of a single or double pulse sequence. The time from Sync Out to Pulse Out is user programmable from 5ns to 5 seconds. The width of Sync Out is programmable as short (~5ns) or long (~50ns). The short width should be used when pulsing at frequencies above 20MHz. For frequencies less than 20MHz, the short or long width can be used.

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In addition, when using external triggering, it is important to keep in mind the time from external trigger to Sync Out time as specified in Section 1.2.2, Sync Out Characteristics. This time is due to intrinsic propagation delays of the input circuitry and pulse generation logic. The time may vary from board to board, but will not vary significantly for a particular board.

In burst mode and when using synchronous gating, the time from the external trigger to Sync Out will jitter 5-10ns from trigger to trigger, if the DDS/Divider Mode (FGM = 1) is being used (see 4.1.2.3 for more details). This is due to the required synchronization of the asynchronous external trigger to the internal clock on the MA209. Synchronization is not required when producing a Single or Double pulse sequence, so this jitter does not occur.

4.1.2.3 Frequency (Internal Pulse Repetition Rate)

The internal pulse repetition rate can derived directly from the DDS output or controlled by a combination of the DDS output and a divider value. The direct DDS output should be used when producing continuous fixed frequency pulses, software initiated pulse burst, or asynchronous gating operations. This method allows the most flexible control and highest resolution of the frequency.

The combination of the DDS output and a divider value should be used when doing externally triggered pulse burst or synchronous gating operations. When using the divider, the DDS must be set to a frequency between 25 and 50MHz. This clock is multiplied by four internally to provide a 100 to 200MHz base clock for the input to the divider. The first pulse after an incoming external trigger or gate signal will occur synchronous to this base clock, which varies in period from 5 to 10ns, depending on the x4 internal clock frequency. If the direct DDS output were used, the pulse would be synchronous to that output clock, which may have a much longer period than 10ns.

4.1.3 Single Pulse vs. Double Pulse

The DP bit in the Control/Status Register selects whether a single pulse (or double pulse) occurs when triggered. It is important to remember that the Double Pulse Spacing is the time from the rising edge of the first pulse to the rising edge of the second pulse; therefore, the Double Pulse Spacing must be set to a value greater than the Pulse Width.

4.1.4 Single, Continuous, and Burst Modes

The RMODE bits in the Control/Status Register select whether a single pulse (or double pulse) or a series of pulses is output for each software run or external trigger. To output a continuous stream of pulses, set the RMODE to Continuous Cycle mode, then the RUN bit to 1. If the Trigger Source in the Trigger/Gate Control register is set to "Software RUN bit," the pulses will start immediately. Otherwise, the pulse will start when the selected trigger becomes active. To stop the stream of pulses, set the RUN bit to 0. To output a specific number of pulses, set the Burst Count registers to the desired number, then set the RMODE to Burst mode. Use the software RUN bit or an external trigger to initiate the output of the desired number of pulses.

The burst of pulses are output each time the RUN bit or external trigger go from inactive (0) to active (1). If desired, an interrupt can be generated at the end of the burst (see 4.4 for details).

> **NOTE: Always set the RUN bit to 0 before changing the RMODE. Do not change the RMODE at the same time the RUN bit is changed (use separate write operations).**

4.1.5 Follow Trigger Mode

Setting the RMODE bits in the Control/Status Register to "Follow Trigger Input" causes the output pulse to follow both the pulse width and period of the selected Trigger Source specified in the Trigger/Gate Control register. This feature can be used to provide level shifting of an input signal.

4.1.6 Pulse Gating

The pulse output can be gated to be present only during the active level of an external signal. To use this function, set the Gate Mode (GM) bit to a 1 in the Trigger/Gate Control register, the desired type of gating to synchronous or asynchronous using the SG bit, and select the gate source with the GATESEL bits.

With synchronous gating, the first pulse is synchronized with the rising edge of the gate signal. A pulse (or double pulse) will continue to be output as long as the gate signal is active when the **Sync Out** signal occurs.

With asynchronous gating, the pulse runs free internally, but will be low when the gate signal is inactive. The pulse output is **not** synchronized to the gate signal. Active pulses will only be present when the gate signal is active.

4.2 CALIBRATION

Calibration values are used to adjust the timing accuracy for each of the delay elements, the pulse width, pulse delay, and double pulse spacing. These values should only be modified by trained factory personnel. The values can always be reset to Factory Default Values by setting the CRST bit in the first Calibration register. This bit resets all calibration values to their factory default values. Calibration is recommended every 12 months.

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4.3 REFERENCE DISCIPLINING

The MA209's internal oscillator can be disciplined to an external clock by selecting the reference clock source (REFSEL bits) in the control/status register. Enable disciplining and select the frequency of the input reference by setting the RFE bits (RFE1 and RFE0) in the control/status register. If a reference clock is detected, the DET bit in the control/status will be a one.

When the internal clock is disciplined to within approximately one decade of the reference clock, the LOK bit will transition high. If the module has warmed to a stable operating temperature, this typically requires around 30 seconds. The disciplining logic checks the internal clock frequency against the external reference clock every three seconds. If the module temperature is not stable, the disciplining logic may require longer to achieve lock and may transition out of lock. Since the purpose of reference disciplining is to achieve long term stability, occasional out of lock conditions are typically not detrimental. The disciplining status can be monitored by reading the Reference Count register. This register indicates the difference between the internal VCXO frequency and the external reference clock. The MA209 will continue to discipline itself to the reference clock as long as the reference clock is present. If the reference clock is removed, the MA209 will hold its internal clock at the disciplined frequency; however, normal drift will occur.

Reference Disciplining only affects the output frequency of the pulses. It does not affect the pulse width, pulse delay, or double pulse spacing accuracy.

On Rev. C of the MA209, the reference disciplining logic was upgraded to include support for a reference input frequency of 1PPS and 100PPS. Prior versions only supported a 10MHZ input frequency. In addition, the disciplining logic was improved to achieve better stability and faster reaction times. Contact the factory if you have an older version and require this upgrade.

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4.4 INTERRUPTS

The MA209 supports Type A and Type C interrupts as specified in the M-module specification. A Type A interrupt releases the interrupt request only after the pending interrupt is cleared by software (software-end-of-interrupt (i.e., RORA)). A Type C interrupt releases the interrupt request during the interrupt acknowledge cycle (hardware-end-of-interrupt with vector (i.e., ROAK)) Type C interrupts provide an interrupt vector during an interrupt acknowledge cycle. Use the IT bit in the Interrupt Control Register to configure the desired type of interrupt.

For an interrupt to occur, the desired interrupt source must be enabled (RIEN or BIEN) and the master interrupt enable (MIEN) must be enabled in the Interrupt Control Register. For Type C interrupts, the interrupt vector is equal to the lower byte of the interrupt control register.

NOTE: For any interrupt to occur, the MIEN bit in the Interrupt Control Register must be set to a one.

NOTE: When using Type C interrupts, the MIEN bit is cleared during the interrupt acknowledge cycle. It must be re-enabled to receive another interrupt.

End of Burst The End of Burst bit (EOB bit) is set to a one when the burst of pulses is complete. It remains a one until a 1 is written to the bit to clear it. Enable an interrupt on this condition by writing a one to the BIEN and MIEN bit in the Interrupt Control Register.

Ready The Ready Interrupt (RDI bit) is set to a one when the module becomes ready for operation following a change in the pulse period, width, delay, or other operational mode. It remains a one until a 1 is written to the bit to clear it. Enable an interrupt on this condition by writing a one to the RIEN and MIEN bit in the Interrupt Control Register.

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4.5 ID PROM

Refer to 3.5.2 for a description of the ID PROM's function and contents. Reading data from the ID PROM involves writing and reading a register in a sequential manner. Data can not be written to the PROM. Figure 7 provides a general description of the code sequence necessary to read the information from the PROM. The PROM is compatible with a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*-------------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
  addr = 0xFE;                          /* address for IDPROM */
  id_addr = 0x80 | id_addr;             /* 80 is the read opcode for the PROM */
  write_prbyte (addr, id_addr);
  read_prbyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = rdval << 8;                  /* upper byte of sync code word */
  read_prbyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = tmpval | rdval;              /* combine bytes of sync code   */
  *value = tmpval;
  write_word(addr, 0x0000);             /* lower cs */
  return;
}
/*-------------------------------------------------------------------------*/
int write_prbyte (unsigned long addr, unsigned short value){
  write_word(addr, 0x0000);             /* insure cs is initially low */
  write_word(addr, 0x0004);             /* initialize */
  write_prbit(addr, 0x0001);            /* start bit */
  temp = value;
  for (i=0;i<=7;i++){
    write_prbit(addr, ((temp & 0x80)>>7));
    temp = (temp << 1);
  }
return;
}
/*-------------------------------------------------------------------------*/
int write_prbit (unsigned long addr, unsigned short value){
  temp = (0x0004 | (value & 0x0001));   /*  set data bit before clock */
  write_word(addr, temp);
  Delay(.000005);
  temp = (0x0006 | (value & 0x0001));   /*  set data bit & clock */
  write_word(addr, temp);
  Delay(.000005);
  return;
}
/*-------------------------------------------------------------------------*/
int read_prbyte (unsigned short addr, unsigned short *value){
  for (i=7;i>=0;i=i-1){
    read_prbit (addr, &rdval);
    temp = temp | ((rdval&0x01) << i);
  }
  *value = temp;
  return;
}
/*-------------------------------------------------------------------------*/
int read_prbit (unsigned short addr, unsigned short *value){
  write_word(addr, 0x4);                /* lower clock bit */
  Delay(.000005);
  write_word(addr, 0x6);                /* raise clock bit */
  Delay(.000005);
  read_word (addr, value);
  return;
}
/*-------------------------------------------------------------------------*/
```

NOTE: 1. write_word and read_word are low level memory access routines.
*2. **NOT** actual code and should be treated as a modeling tool only.*

Figure 7. ID PROM Access Routine

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APPENDIX A: CONNECTORS

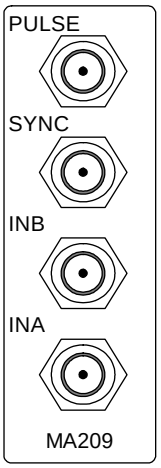


Figure A-1. Front Panel I/O Signals

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
A14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

Figure A-1. M-Module Interface Connector Configuration

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