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U S E R ' S M A N U A L

VXI
COUNTER/CLOCK
MODULE

MODEL
VX491C

Manual Part No: 11026849B

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INTRODUCTION

This manual describes the operation and use of the C&H Model VX491C VXI Counter/Clock (Part Number 11026855 Rev. B or higher). This module is one of a number of test and data acquisition/control modules in the VME and VXI format provided by C&H.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

The part numbers covered by this manual are:

Part Number	Description
11026845-0001	VX491C (with ovenized crystal oscillator)
11026845-0002	VX491C (no ovenized oscillator, uses VXI CLK10)

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1.0 GENERAL DESCRIPTION

The VX491C is a single slot register-based C-size VXIbus compatible special purpose counter/clock module. The module provides a variety of clock and counter functions, including a stable 10 MHz clock source, a number of derived clock outputs, six 32-bit counters, and a time-of-day clock.

1.1 PURPOSE OF EQUIPMENT

This instrument is designed for precise timing and clock applications required in data acquisition and test applications. The instrument can provide precise triggering signals to data acquisition equipment, produce a variety of pulse stimuli, and perform pulse count and time period measurement functions.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Specifications

- On-board oven controlled 10 MHz oscillator with drop-out detection and automatic switch-over to VXIbus CLK10 signal
- Four clock outputs derived from 10 MHz master clock (100 KHz, 10 KHz, and two frequencies derived from programmable 32-bit dividers)
- Flexible synchronous gating of clocks
- Six pre-loadable 32-bit up/down binary counters with programmable input sources and match registers
- Synchronous (on-the-fly) latching of 32-bit count values
- Time period measurement of signal events
- Time-of-day clock with periodic and set time interrupts
- Programmable interrupts on master clock drop-out, on counter roll-over and match conditions, at periodic times, and at a set time-of-day

1.2.2 Electrical

The module requires the +5V, +12V, and −12V power from the VXI backplane. The peak module current (I_{PM}) for the +5 volt supply is 1.5 amps, for the +12 volt supply it is 0.70 amps, and for the −12V supply it is 0.15 amps. Other electrical and timing characteristics are shown in Figure 1.

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1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with the VXIbus specification Rev 1.4 for single slot size 'C' modules. The nominal dimensions are 233.35 (9.187 in) high x 340 mm (13.386 in) deep.

10MHz Stable Clock (option -0001 only)

Accuracy:	≤ 1 x 10^{-8} (frequency stability)
Stability:	≤ 1 x 10^{-8}/day (short term aging)
Trim Range:	± 1 x 10^{-7} minimum
Auto Drop-out Detect and Switch-over:	≤ 500 ns
Output Level:	0-2.5 or 0-5V into 50 ohms (selectable)
Output Impedance:	7, 50, or 70 ohms (selectable)
Duty Cycle:	50 ±10%

Derived Clock Outputs (100Khz, 10Khz, Fx, Fy)

Output Level:	0-2.5V into 50 ohms, 0-5V TTL
Output Impedance:	50 ohm
Duty Cycle:	50 ±10%
Carry/Borrow PW:	125-275ns (225ns typical)
Gate to Clock Start:	≤ 50ns (clock starts on low side of wave)

Counters

Frequency Range:	DC to 10 MHz
Input Source:	Programmable
Event Measurement:	50ns resolution

Time-of-Day

Stability:	5±50 ppm
Aging:	±5 ppm/year (max)
Resolution:	1 ms
Power Loss Protection:	1 year

Note: The time-of-day function only uses the stable 10 MHz clock for the millisecond function. The remaining seconds-minutes-hours use a less stable internal oscillator.

Figure 1. Electrical Timing and Output Characteristics

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1.2.4 Environmental

The environmental specifications of the module are:

Operating Temperature:	10°C to +40°C
Storage Temperature:	-40°C to +75°C
Humidity:	<95% without condensation

1.2.5 Bus Compliance

The module complies with the VXIbus Specification Revision 1.4 for C-size register based modules and with VMEbus Specification ANSI/IEEE STD 1014-1987, IEC 821 and IEC 822.

Manufacturer ID:	$FC1_{16}$
Model Code:	$FFF0_{16}$
Access Type:	Register Based
Addressing:	A16
Data Transfer:	D16
Sysfail:	Supported
Interrupts:	RORA, programmable level
Bus Arbitration:	BRx tied to BGx
TTLTRGx lines:	Synchronous (SYNC) Trigger Protocol
Local Bus:	not used

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2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

In most cases the VX491C is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the carrier immediately as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The module contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION

CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.

Set the module's logical address and configure all jumpers as described in Section 3.2. Insert the module into the appropriate slot according to the desired priority. Apply power. If no obvious problems exist, proceed to communicate with the module as outlined in Section 4.0 (Operating Instructions).

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

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3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

The VX491C is configured, controlled, and statused through on-board registers accessible through the VXI backplane. These registers are used to configure, control, and status the instrument. A simplified block diagram of the module is shown in Figure 2.

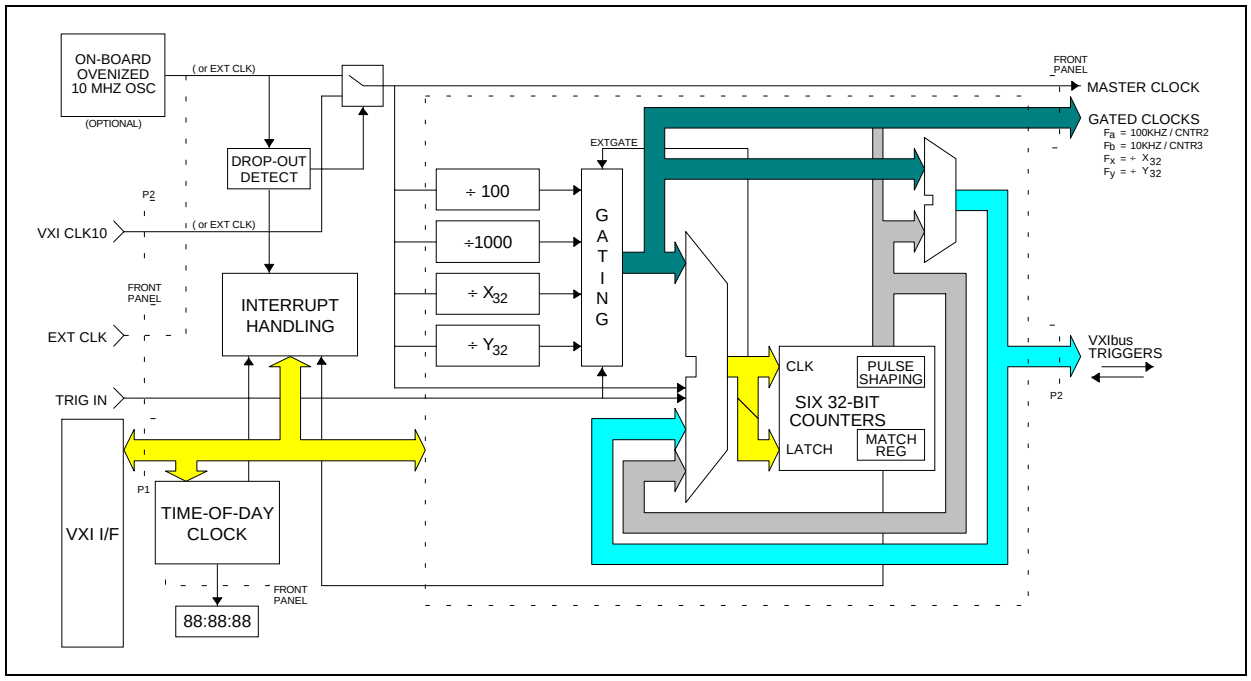


Figure 2. Functional Block Diagram

3.1.1 10 MHz Stable Oscillator

The heart of the 10 MHz stable clock source is an oven controlled crystal oscillator (OCXO). The OCXO provides an extremely accurate and stable clock source that is available at the front panel and is used to derive other frequencies. If the stable clock fails, the 10 MHz clock automatically switches over to the backup signal, which can be either the VXI CLK10 signal or an external clock.

3.1.2 Dividers

Four 32-bit modulo-N dividers derive four different clocks from the 10 MHz stable clock. These clocks are available at the front panel, VXIbus trigger lines, and at the inputs of the counters. Two are fixed at 100 KHz and 10 KHz and the other two are programmable.

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3.1.3 Clock Gating

Clock gating provides synchronous gating of the four derived clocks. Clocks can be enabled/disabled by software or by a combination of the front panel Trigger Input and a programmable external gating signal. The external gating signal can be mapped to any of the VXIbus trigger lines, the derived clocks, and other signals.

3.1.4 Counters

There are six 32-bit binary counters available for general counting/timing functions as shown in Figure 3. The inputs to each counter can be selected from the main stable clock, any of the derived frequencies, the VXIbus trigger lines, the front panel trigger input, or from the carry/borrow of the adjacent counter. The counters can count up or down and can either free run or stop on carry/borrow. The carry/borrow output of each counter is programmable as a square wave or a pulse and it may be directed to any of the VXIbus trigger lines. An interrupt can be generated upon carry/borrow or when the count value equals a match register value. The 32-bit count value can be read on-the-fly or it can be latched upon a signal event for event time measurement applications.

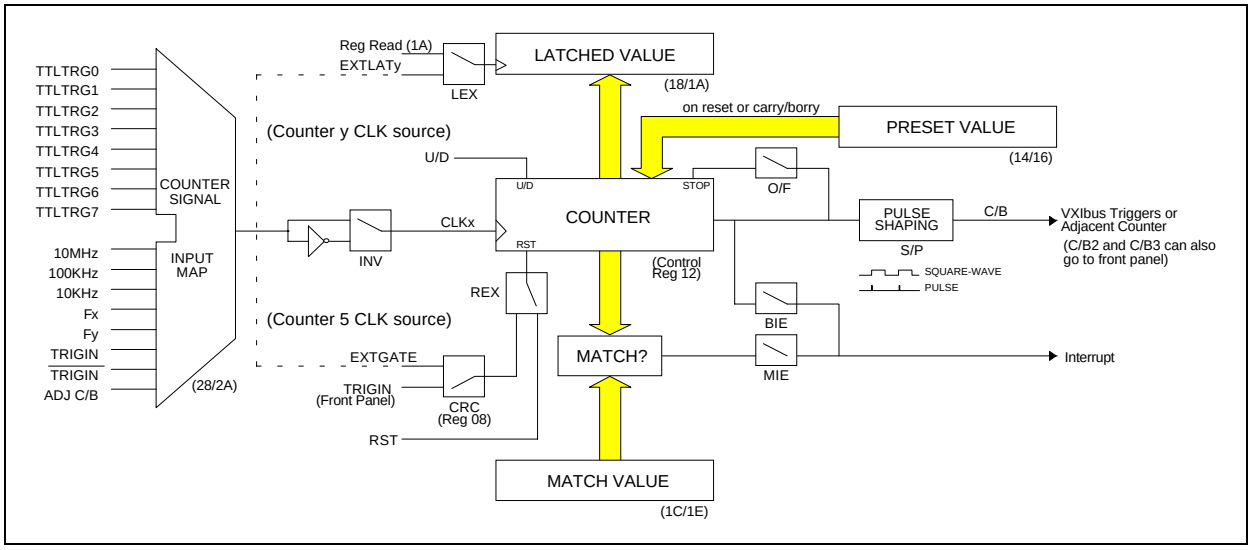


Figure 3. Counter Functional Diagram

3.1.5 Time-of-Day Clock

A real time clock is incorporated that provides date and time functions including periodic and time-of-day interrupts. The current time in a hours:minutes:seconds format is provided on the front panel.

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3.1.6 Interrupts

Interrupts from a variety of sources can be generated. Each source has a programmable interrupt status/ID. Interrupts are released on register access of a register associated with the interrupting source.

3.1.7 Reset

A VXIbus SYSRESET or a write to the RST bit in the VXI Status/Control register (base + 08_{16}) will reset the module to a default state.

3.1.8 Time-of-Day Battery Backup

The time-of-day maintained during power off conditions using a lithium battery. The battery can maintain operation for a minimum of one year. For long term storage, a means is provided to disable battery backup.

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3.2 HARDWARE CONFIGURATION

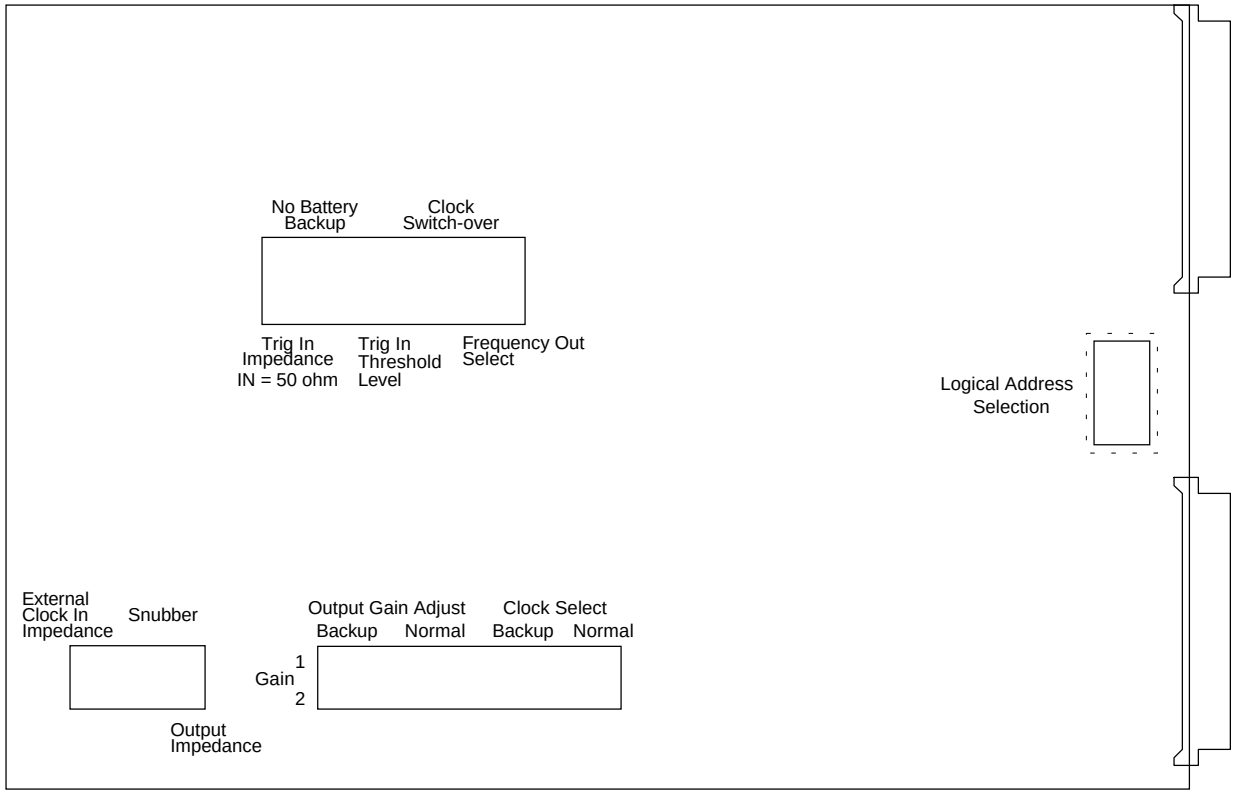


Figure 4. Hardware Configurable Controls

Logical Address An 8-bit logical address switch is provided to uniquely identify the module in the system. The switch location is shown in Figure 4.

Trig In Impedance This jumper selects the input impedance of the Trig In front panel signal. With the jumper installed (default) the input impedance is 50Ω. Without the jumper installed, the impedance is >100KΩ.

Trig In Level These jumpers select the threshold level of the Trig In front panel signal. The level can be set to 0V (zero crossing), TTL (0.8V), or CMOS (2.5V).

Threshold	Jumpers	
0V	OUT	OUT
TTL	IN	IN
CMOS	IN	OUT

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No Battery Backup This jumper allows the battery backup feature to be disabled. With power applied to the module, momentarily short the pins together. When module power is then removed, battery backup will not occur. The time-of-day clock will require reinitialization when power is re-applied. A software method of disabling the battery backup is also available for cases where this jumper is not accessible (see 4.8).

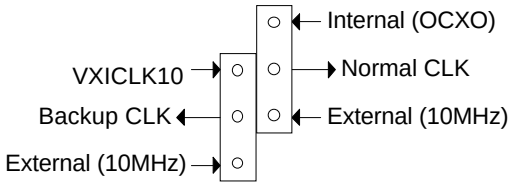
Autoswitch Test This jumper allows a test of the 10MHZ automatic switch-over circuit. Removing the jumper disables the normal clock and should cause the backup clock to take over. The CLK LED on the front panel should illuminate indicating that the instrument is running on the backup clock. A module reset or write to the clock control register is required to switch the ovenized oscillator back into operation.

100KHz/Fa Select This jumper allows the front panel output connector (100KHz/Fa) to be either the gated 100KHz derived clock or the inverted (active low) carry/borrow of Counter 2. Note that when Fa is selected, the gate indicator lamp is not necessarily applicable.

10KHz/Fb Select This jumper allows the front panel output connector (10KHz/Fb) to be either the gated 100KHz derived clock or the inverted (active low) carry/borrow of Counter 3. Note that when Fa is selected, the gate indicator lamp is not necessarily applicable.

External 10MHz Impedance This jumper selects the input impedance of the EXT10MHz front panel signal. With the jumper installed (default) the input impedance is 50Ω. Without the jumper installed, the impedance is >100KΩ.

Clock Select These jumpers selects the source of the normal and backup clocks. The Normal clock can be the internal ovenized oscillator, the clock present at the front panel EXT10MHz input connector, or the VXIbus CLK10 signal. The Backup clock can be either the VXIbus CLK10 signal or the clock present at the front panel EXT10MHz input connector. The jumpers should be configured to connected the clocks to the desired input signal as depicted below:



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10MHz Output Options Several jumpers and a potentiometer allow configuration output voltage level, impedance, quality, and frequency drift adjustment of the front panel 10MHz signal.

Output Gain Adjust These jumpers, one for the normal clock and one for the backup signal allow adjustment of the output voltage level of the signals. The voltage gain is a function of the output voltage with a 50Ω output impedance and a 50Ω load versus the input voltage. The internal input voltage of the OCXO is approximately 5.0V and the VXI CLK10 signal is approximately 3.8V. With the jumper in the Gain=1 position, the output voltage level will equal the internal or external clock input voltage. In the Gain=2 position, the output voltage level will be approximately twice the input voltage. With no jumper in place, the Gain=0.5. Note that with Gain=2 some signal distortion and clipping may occur.

Output Impedance This jumper controls the output impedance of the 10MHz signal. The default is 50Ω.

Pins Connected	Output Impedance (ohms)
1-2	7
2-3	50
None	70

Optional Snubber This jumper connects/disconnects a resistor (10Ω)/capacitor(100pF) circuit to the output signal. Use of the snubber circuit (jumper in) reduces high frequency ringing that commonly occurs.

Frequency Trim This potentiometer allows the frequency of the ovenized 10MHz oscillator to be adjusted.

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3.3 INDICATORS

Several LED indicators are provided on the front panel. Their functions are described below:

ACCESS This LED illuminates when the module is properly accessed by the host processor.

MODID This LED illuminates when the host processor applies the MODID signal to the slot the module is occupying.

SYSRST This LED illuminates when the SYSRST* signal is applied.

SYSFAIL This LED illuminates during module initialization and remains illuminated if the module fails to initialize correctly.

CLK This LED illuminates when the backup clock signal is being used. It indicates a failure of the normal clock or a manual switch-over to the backup clock.

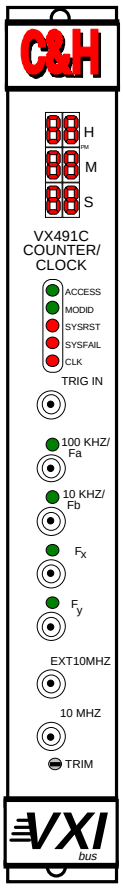


Figure 5. Front Panel

H:M:S These six seven-segment LEDs indicate the time-of-day (or alarm time when in the set alarm mode) in a hours:minutes:seconds format.

PM This LED illuminates when in the 12 hour clock mode and the time is PM.

GATE Each gated output connector has an associated LED that illuminates when the gate is ON (i.e., a signal is being output). Note that when gating with short duty cycle signals, the indicator may dim or not appear to be lit. Additionally, if the carry/borrow outputs are selected for the 100KHZ/F_a and 10KHZ/F_b outputs, the gate indicator is not necessarily applicable.

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3.4 CONNECTORS

3.4.1 Front Panel Connector

The front panel connectors are SMB-F type.

TRIG IN This input allows external trigger, gating, and clocking stimulus. The input impedance is selectable for 50Ω or high impedance and the input threshold is selectable for 0V, TTL, or CMOS. (+5V max.)

100KHZ/Fa This output is selectable to provide either a gated 100KHz square-wave signal or a programmable active-low carry/borrow signal from counter 2. The output can drive 0-2.5V into a 50Ω load or 0-5V into a high-impedance load.

10KHZ/Fb This output is selectable to provide either a gated 10KHz square-wave signal or a programmable active-low carry/borrow signal from counter 3. The output can drive 0-2.5V into a 50Ω load or 0-5V into a high-impedance load.

Fx This output provides a programmable gated square-wave signal. The frequency of the signal is 10MHz divided by the programmed Fx Divider Value (see register 20_{16} and 22_{16}) The output can drive 0-2.5V into a 50Ω load or 0-5V into a high-impedance load.

Fy This output provides a programmable gated square-wave signal. The frequency of the signal is 10MHz divided by the programmed Fy Divider Value (see register 24_{16} and 26_{16}) The output can drive 0-2.5V into a 50Ω load or 0-5V into a high-impedance load.

EXT 10MHZ INPUT This input allows an external reference clock to be used. The clock input is AC coupled and the input impedance is selectable for 50Ω or high impedance. This input clock can be either the normal clock or the backup clock. (+5Vpk-pk max.).

10MHZ OUTPUT This output provides the current 10MHz reference clock. The source of the signal is either the internal 10MHz ovenized oscillator (option -0001), the VXICLK10 from the VXI backplane, or the external 10MHz input signal. All internal clocks (with exception of the time-of-day clock) are based on this clock. The output impedance is selectable as 7, 50, or 70 ohms. The amplifier gain is selectable for gain=1 or gain=2. The gain refers to the output level with a 50Ω load versus the input voltage level. The internal 10MHz oscillator (option -0001) and the VXICLK10 both have an internal voltage level of 0-4.5.

3.4.2 Rear Connectors

The P1 and P2 connectors are configured in accordance with the VXI specification. (See Appendix A)

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3.5 CONFIGURATION REGISTERS

There are several types of registers used to configure and control the VX491C module. The VXI configuration registers provide for control and status as required by the VXIbus specification. The other registers provide special function control of the clocks, counters, interrupts, and time-of-day functions. An address map of the registers is shown in Table I.

Table I. VXI Register Address Map

A16 Address	Register Description
Base + 00	VXI ID
Base + 02	VXI Device Type
Base + 04	VXI Status/Control
Base + 06	VXI Unused Register
Base + 08	Clock Control/Status
Base + 0A	Gate Control/Status
Base + 0C	Time-of-Day Clock Interrupt ID/Port
Base + 0E	TOD Control/Millisecond Register
Base + 10	Interrupt/Counter Select
Base + 12	Counter X Control/Status (x 6)
Base + 14	Counter X Preset Value - High (x 6)
Base + 16	Counter X Preset Value - Low (x 6)
Base + 18	Counter X Count Latch - High (x 6)
Base + 1A	Counter X Count Latch - Low (x 6)
Base + 1C	Counter X Match Value - High (x 6)
Base + 1E	Counter X Match Value - Low (x 6)
Base + 20	Fx Divider Value (High)
Base + 22	Fx Divider Value (Low)
Base + 24	Fy Divider Value (High)
Base + 26	Fy Divider Value (Low)
Base + 28	Counter 0-3 Signal Input Map
Base + 2A	Counter 4-5 Signal Input Map
Base + 2C	Trigger 0-3 Output Map
Base + 2E	Trigger 4-7 Output Map

3.5.1 VXI Configuration Registers

The VXI configuration registers contain basic information needed to configure a VXIbus system. The configuration information includes: manufacturer identification, product model code, device type, memory requirements, device status, and device control. The registers are briefly described below and are detailed in Figure 6.

VXI Identification (ID) Register (00_{16}) A read of this register provides manufacturer identification, device classification (i.e., register based), and the addressing mode (A16). A write to this register has no effect.

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VXI Device Type Register (02_{16}) A read of this register provides the model code identifier. A write to this register has no effect.

VXI Status/Control Register (04_{16}) A read of this register provides the state of P2 MODID* line, the interrupt level, and the Ready and self-test Passed status. A write to this register controls inhibiting the SYSFAIL line and resetting of the module.

VXI ID

00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Only	Device Class		Address Space		Manufacturer ID											

Device Class ⇨ Device Class (11 = Register Based)
Address Space ⇨ Address Space (11 = A16 only)
Manuf. ID ⇨ Manufacturer Identification (C&H Technologies = $FC1_{16}$)

VXI Device Type

02

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Only	Model Code															

Model Code ⇨ Model code (VX491C = $FFF0_{16}$)

VXI Status/Control

04

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used														SI	RST
Read	AAA	MID	1	1	1	1	1	1	0	0	0	0	RDY	PASS	SI	1

AAA ⇨ A24/A32 Access (0 = disabled)
RST ⇨ Reset (A 1 written to this bit resets the module)
MID ⇨ Module ID Status (0 = P2 MODID* line is selected (active-high))
RDY ⇨ Ready (1 = ready)
PASS ⇨ Pass/fail indicator (0 = executing or failed, 1 = passed)
SI ⇨ Sysfail Inhibit (1 = disable SYSFAIL line)

Figure 6. VXI Configuration Registers

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3.5.2 Special Function Registers

Clock Control/Status Register (08_{16}) This read/write register controls the normal/backup clock switch-over, the enabling and interrupt status/ID for a clock switch-over interrupt, the source of the external reset signal for the counters, and the inversion of clock gate control signals. The CLK bit provides manual control during a write to the register and current status on read. A read of the register clears a pending clock switch-over interrupt.

Gate Control/Status Register ($0A_{16}$) This read/write register controls the gating of the fixed and programmable clocks. The clocks may be enabled/disabled by software or be controlled by internal module generated signals (EXTGATE) or an external signal (Trig In).

TOD Clock Interrupt ID/Port ($0C_{16}$) This read/write register provides control of the interrupt status/ID for time-of-day interrupts and provides a window (port) into the time-of-day clock functions. The design implementation uses an integrated circuit that provides extensive real-time clock functions. This implementation uses a 4-bit wide data bus for communication to this device. All registers (two banks of 16 4-bit words) are accessible through this port. The specific internal register accessed is controlled by data written to the TOD Control/Millisecond register. A specific register can be specified and automatic incrementing of the address may be selected. See the separate device data sheet for details of the internal time-of-day clock registers.

TOD Control/Millisecond Register ($0E_{16}$) This register provides various controls and statuses of the TOD clock function along with a millisecond counter value that is synchronized with the time-of-day clock. The counter is reset to zero at the beginning of each second.

Interrupt/Counter Select Register (10_{16}) This read/write register sets the interrupt level for all interrupts, provides a status summary of pending interrupts, and selects the active counter for registers accesses. Upon receiving an interrupt, this register should be the first read to determine the source or sources of an interrupt. Interrupts can then be serviced and cleared individually by reading the appropriate register for the interrupt source. Interrupts are not cleared by reading this register. This allows one or all interrupts to be serviced during an interrupt service routine. The other function of this register is to select the active counter for subsequent accesses to the Counter X registers.

Counter X Control Register (12_{16}) This read/write register controls the selected counter's interrupts, run modes, and other reset and enabling functions. Interrupts can be enabled to occur when the counter equals the value in the Counter Match Value register and/or upon a borrow/carry (or if external latching is enabled, when an external latch occurs), however, only one interrupt status/ID is provided per counter. Only one type of interrupt should be enabled at a given time, since the source of an interrupt may be impossible to determine if both types of interrupts are enabled. A pending counter interrupt is released after a read of this register. The mode control bits (Square/Pulse, Once-Through/Free Run, Clock Invert, Up/Down, Latch on External Signal, and Reset on External Signal) can be individually set to select the desired operational mode.

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Counter X Preset Value ($14_{16}/16_{16}$) This read/write register controls the value that is loaded into the selected counter when a roll-over or reset occurs.

Counter X Count Latch ($18_{16}/1A_{16}$) This register provides an on-the-fly snap-shot of the selected counter's current count value. The entire 32-bit count value is latched when the lower word ($1A_{16}$) is read, if external latching is not enabled, or on the rising edge of an external latch signal, if external latching is enabled. In external latch mode, two rising edges of the external latch are required to properly count (measure) the time between events. The first edge clears the count and the second latches the count value. Latching is disabled after the second latch occurs.

Counter X Match Value ($1C_{16}/1E_{16}$) This read/write register controls the value that will cause an interrupt (if enabled) to occur when the counter equals that value.

Fx Divider Value (20_{16}) This read/write register controls the modulo-N divide value (X_{32}) for the (F_x) frequency output.

Fy Divider Value (22_{16}) This read/write register controls the modulo-N divide value (Y_{32}) for the (F_y) frequency output.

Counter Signal Input Map ($28_{16}/2A_{16}$) These read/write registers control the clock and external source for each of the six counters. Counter 5's clock source also defines the source of the external gate (EXTGATE) signal used by the Gate Control logic.

VXI Trigger Output Source Map ($2C_{16}/2E_{16}$) These read/write registers control the signal output to each of the eight VXI TTLTRGx lines. If none is selected, the open collector TTLTRGx line is not driven.

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08	Clock Control/Status Register															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Interrupt Status/ID								-	-	IEG	ITI	CRC	CLK	SIE	-
Read	Interrupt Status/ID								-	-	IEG	ITI	CRC	CLK	SIE	SIP

Interrupt Status/ID ⇒ High byte of interrupt vector for a clock switch-over
IEG ⇒ Invert EXTGATE signal (1=invert polarity)
ITI ⇒ Invert Trig In signal (1=invert polarity)
CRC ⇒ Counter Reset Control (0 = Trig In Resets, 1 = EXTGATE[1] signal Resets)
CLK ⇒ Clock Status/Control (0 = normal clock, 1 = backup)
SIE ⇒ Clock Switch-Over Interrupt Enable (1 = enable)
SIP ⇒ Clock Switch-Over Interrupt Pending[2] (1 = pending)

Notes:
1) See Counter Signal Input Map (4-5) Register ($2A_{16}$) for programming EXTGATE.
2) A read of this register clears a pending clock switch-over interrupt.

0A	Gate Control/Status Register															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	Fy Gate Mode			-	Fx Gate Mode			-	10KHz Gate Mode			-	100KHz Gate Mode		
Read	-	Fy Gate Mode			-	Fx Gate Mode			-	10KHz Gate Mode			-	100KHz Gate Mode		

Gate Mode ⇒ Mode of gating for each of the clock signals
000 (0) - Disabled
001 (1) - EXTGATE high enables
010 (2) - Trig In high enables
011 (3) - Trig In ↓ enables, EXTGATE ↑ disables
100 (4) - EXTGATE ↑ enables, Trig In ↓ disables
101 (5) - (reserved for future use)
110 (6) - (reserved for future use)
111 (7) - Enabled

Note: See Counter Signal Input Map (4-5) Register ($2A_{16}$) for programming EXTGATE.

0C	Time-of-Day Clock Interrupt ID/Port															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Interrupt Status/ID								(ignored)				Data Port			
Read	Interrupt Status/ID								Register Address				Data Port			

Interrupt Status/ID ⇒ High byte of interrupt vector for a time-of-day interrupt
Register Address[1] ⇒ Feedback of the TOD clock register read
Data Port[2] ⇒ Data value read from or written to specified register address

Notes:
1) The register address is selected in the TOD Control/Millisecond Register ($0E_{16}$). The selected address may remain steady or automatically increment by controlling the Auto Increment bit in the same register.
2) See Figure 8 for details of the internal time-of-day registers.

Figure 7. Special Function Registers

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0E	TOD Control/Millisecond Register															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	AI	LT	NB	-	-	-	-	-	-	-	-	Register Address			
Read	BF	AI	LT	NB	-	MR	Millisecond Time Value									

BF ⇒ Battery Fail (1 = battery failure)
AI ⇒ Auto Increment register address after read or write (1 = auto increment)
LT ⇒ Lamp Test H:M:S display (1 = test)
MR ⇒ Milliseconds rolled over to 0 since last read (1 = rollover occurred)
NB ⇒ No Battery Backup (1 = no battery backup) - See text for details
Milliseconds ⇒ Number of elapsed milliseconds from last second increment

10	Interrupt/Counter Select Register															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	-	-	-	-	-	ILVL			-	SEL		
Read	PIP	AIP	SIP	CIP5	CIP4	CIP3	CIP2	CIP1	CIP0	ILVL			-	SEL		

PIP ⇒ Time-of-day Periodic Interrupt Pending (1 = pending)
AIP ⇒ Time-of-day Alarm Interrupt Pending (1 = pending)
SIP ⇒ Clock Switch-Over Interrupt Pending (1 = pending)
CIP0-5 ⇒ Counter 0-5 Interrupt Pending (1 = pending)
ILVL ⇒ Interrupt Level (000 = disabled)
SEL ⇒ Selects active counter for register accesses (0-5 are valid)

12	Counter X Control Register															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	BIE	MIE	Interrupt Status/ID						EC	S/P	O/F	U/D	INV	LEX	REX	RST
Read	BIE	MIE	Interrupt Status/ID						EC	S/P	O/F	U/D	INV	LTD	REX	CIP

BIE ⇒ Borrow/Carry or External Latch Interrupt Enable[1] (1 = enable)
MIE ⇒ Match Interrupt Enable (1 = enable)
Interrupt Status/ID[2] ⇒ High byte of interrupt vector
EC ⇒ Enable Counter (1 = enable)
S/P ⇒ Square wave/Pulse Select (0 = square wave[3], 1 = pulse)
O/F ⇒ Once-through/Free Run Select (0 = once-through, 1 = Free run)
U/D ⇒ Up/Down Select (0 = count down, 1 = count up)
INV ⇒ Invert Input Clock (0 = no inversion, 1 = invert)
LEX ⇒ Latch On External Latch Signal[4] (0 = count latched on register read, 1 = count latched on programmed EXTLAT signal)
LTD ⇒ Latched (1=two EXTLAT signals have been received)
REX ⇒ Reset On External Reset Signal (1 = enable)
RST ⇒ Reset Counter (1 = reset pulse that loads the preset value, write only)
CIP ⇒ Counter Interrupt Pending[5] (1 = pending)

Notes:
1) When LEX = 1, an interrupt is generated by an EXTLAT signal, not a borrow/carry.
2) BIE and MIE will appear in the Interrupt Status/ID during an interrupt acknowledge cycle. The low byte is always the logical address of the module.
3) In square wave mode the input clock to the counter is doubled in frequency. Use pulse mode when using the counter for counting functions.
4) When LEX=1 and REX=0, the counter is automatically reset to 0 after latching.
5) A read of this register clears a pending counter interrupt.

Figure 7. Special Function Registers (continued)

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14	Counter X Preset Value															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31-D24								D23-D16							
Read	D31-D24								D23-D16							

16																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15-D8								D7-D0							
Read	D15-D8								D7-D0							

D0-D31 ⇒ Preset counter value

18	Counter X Count Latch															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Only	D31-D24								D23-D16							

1A																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Only	D15-D8								D7-D0							

D0-D31 ⇒ On-the-fly latched count value

Note: When external signal latching is disabled (LEX=0), the entire 32-bits of data are latched when the lower word ($1A_{16}$) is read. When external signal latching is enabled (LEX=1), the 32-bit latching occurs the first two times EXTLAT signal goes high. Subsequent latching is disabled until LEX is written high again.

1C	Counter X Match Value															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31-D24								D23-D16							
Read	D31-D24								D23-D16							

1E																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15-D8								D7-D0							
Read	D15-D8								D7-D0							

D0-D31 ⇒ Match value

Figure 7. Special Function Registers (continued)

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20	Fx Divider Value															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31-D24								D23-D16							
Read	D31-D24								D23-D16							

22																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15-D8								D7-D0							
Read	D15-D8								D7-D0							

D0-D31 $\Rightarrow$ Fx divide-by value

24	Fy Divider Value															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31-D24								D23-D16							
Read	D31-D24								D23-D16							

26																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15-D8								D7-D0							
Read	D15-D8								D7-D0							

D0-D31 $\Rightarrow$ Fy divide-by value

Figure 7. Special Function Registers (continued)

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28	Counter Signal Input Map (0-3) Register															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	CLK3/EXTLAT2				CLK2/EXTLAT3				CLK1/EXTLAT0				CLK0/EXTLAT1			
Read	CLK3/EXTLAT2				CLK2/EXTLAT3				CLK1/EXTLAT0				CLK0/EXTLAT1			

2A	Counter Signal Input Map (4-5)Register															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								CLK5/EXTLAT4[1]				CLK4/EXTLAT5			
Read	FF								CLK5/EXTLAT4[1]				CLK4/EXTLAT5			

CLKx/EXTLATy ⇒ Counter x Clock Input Source/Counter y External Latch[2] Source

0	TTLTRG0	8	10 MHz
1	TTLTRG1	9	100 KHz
2	TTLTRG2	A	10 KHz
3	TTLTRG3	B	Fx
4	TTLTRG4	C	Fy
5	TTLTRG5	D	Trig In (rising edge clock)
6	TTLTRG6	E	Trig In (falling edge clock)
7	TTLTRG7	F	Adjacent Carry/Borrow[3]

Notes:

1) This register location also defines the External Gate Control signal (EXTGATE) used by the clock gating logic (see the Gate Control/Status Register (0A) for details).
2) External latch mapping only applies when LEX = 1 (see the Counter X Control Register (12) for details).
3) Counter 0 receives Counter 5's carry/borrow output, Counter 1 receives Counter 0's carry/borrow output, etc.

2C	VXI Trigger Output Source Map (0-3) Register															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Trigger 3				Trigger 2				Trigger 1				Trigger 0			
Read	Trigger 3				Trigger 2				Trigger 1				Trigger 0			

2E	VXI Trigger Output Source Map (4-7) Register															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Trigger 7				Trigger 6				Trigger 5				Trigger 4			
Read	Trigger 7				Trigger 6				Trigger 5				Trigger 4			

Trigger X ⇒ VXI Trigger Output Source

0	None	8	10 MHz
1	Counter 0 Carry/Borrow	9	100 KHz
2	Counter 1 Carry/Borrow	A	10 KHz
3	Counter 2 Carry/Borrow	B	Fx
4	Counter 3 Carry/Borrow	C	Fy
5	Counter 4 Carry/Borrow	D	Trig In (True)
6	Counter 5 Carry/Borrow	E	Trig In (Inverted)
7	Adjacent Trigger (true)	F	Adjacent Trigger (Inverted)

Figure 7. Special Function Registers (continued)

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Addr	A_3	A_2	A_1	A_0	BANK 0 D_3	BANK 0 D_2	BANK 0 D_1	BANK 0 D_0	Real-Time Register Name	BANK 1 D_3	BANK 1 D_2	BANK 1 D_1	BANK 1 D_0	Alarm Register Name
0	0	0	0	0	r-s_8	r-s_4	r-s_2	r-s_1	1 second digit	a-s_8	a-s_4	a-s_2	a-s_1	1 second digit
1	0	0	0	1	*	r-s_{40}	r-s_{20}	r-s_{10}	10 seconds digit	*	a-s_{40}	a-s_{20}	a-s_{10}	10 seconds digit
2	0	0	1	0	r-mi_8	r-mi_4	r-mi_2	r-mi1	1 minute digit	a-mi_8	a-mi_4	a-mi_2	a-mi_1	1 minute digit
3	0	0	1	1	*	r-mi_{40}	r-mi_{20}	r-mi_{10}	10 minutes digit	*	a-mi_{40}	a-mi_{20}	a-mi_{10}	10 minutes digit
4	0	1	0	0	r-h_8	r-h_4	r-h_2	r-h_1	1 hour digit	a-h_8	a-h_4	a-h_2	a-h_1	1 hour digit
5	0	1	0	1	*	r - PM / $\overline{\text{AM}}$	r-h_{20}	r-h_{10}	10 hours digit	*	a - PM / $\overline{\text{AM}}$	a-h_{20}	a-h_{10}	10 hours digit
6	0	1	1	0	r-d_8	r-d_4	r-d_2	r-d_1	1 day digit	a-d_8	a-d_4	a-d_2	a-d_1	1 day digit
7	0	1	1	1	*	*	r-d_{20}	r-d_{10}	10 days digit	*	*	a-d_{20}	a-d_{10}	10 days digit
8	1	0	0	0	r-mo_8	r-mo_4	r-mo_2	r-mo_1	1 month digit	a-mo_8	a-mo_4	a-mo_2	a-mo_1	1 month digit
9	1	0	0	1	*	*	*	r-mo_{10}	10 months digit	*	*	*	a-mo_{10}	10 months digit
A	1	0	1	0	r-y_8	r-y_4	r-y_2	r-y_1	1 year digit	*	a-w_4	a-w_2	a-w_1	Day of week
B	1	0	1	1	r-y_{80}	r-y_{40}	r-y_{20}	r-y_{10}	10 years digit	a-e_8	a-e_4	a-e_2	a-e_1	Area Enable register
C	1	1	0	0	*	r-w_4	r-w_2	r-w_1	Day of week digit	*	*	$TEST_2$	$TEST_1$	Test Register
D	1	1	0	1	IT / $\overline{\text{PLS}_2}$	IT / $\overline{\text{PLS}_1}$	$MASK_2$	$MASK_1$	Control register D	*	CY_2	CY_1	CY_0	Control register D'
E	1	1	1	0	IRQ FLAG 0	RESET	IRQ $FLAG_2$	IRQ $FLAG_1$	Control register E	H/S	24 / $\overline{12}$	CAL	D.P.	Control register E'
F	1	1	1	1	$\overline{\text{BANK}_1}$ / $\overline{\text{BANK}_0}$	STOP	30 sec ADJ	READ FLAG	Control register F	Same as Bank 0				Control register F'

PM / $\overline{\text{AM}}$ $\Rightarrow$ PM / $\overline{\text{AM}}$ (0 = AM, 1 = PM)
IT / $\overline{\text{PLS}_2}$ $\Rightarrow$ Alarm interrupt mode (0 = pulse mode, 1 = interrupt mode)
IT / $\overline{\text{PLS}_1}$ $\Rightarrow$ Periodic interrupt mode (0 = pulse mode, 1 = interrupt mode)
$MASK_2$ $\Rightarrow$ Alarm interrupt mask (1 = inhibit)
$MASK_1$ $\Rightarrow$ Periodic interrupt mask (1 = inhibit)
IRQ $FLAG_0$ $\Rightarrow$ Interrupt clear disable period. (stays high (1) for 122µs after the interrupt occurrence)
RESET $\Rightarrow$ One second counter reset (1 = reset)
IRQ $FLAG_2$ $\Rightarrow$ Alarm interrupt pending (1 = pending)
IRQ $FLAG_1$ $\Rightarrow$ Periodic interrupt pending (1 = pending)
$BANK_1$ / $\overline{\text{BANK}_0}$ $\Rightarrow$ Bank Select (0 = bank0, 1 = bank1)
STOP $\Rightarrow$ Stop counting (1 = stop)
30 sec ADJ $\Rightarrow$ 30-second adjustment (1 = enabled)
READ FLAG $\Rightarrow$ One-second digit rollover (1 = rollover occurred since last read)
$TEST_{1,2}$ $\Rightarrow$ Factory Test (0 = normal)
CY_1 to CY_2 $\Rightarrow$ Periodic pulse period (0 = 1/1024 sec., 1 = 1/128 sec., 2 = 1/64 sec., 3 = 1/16 sec., 4 = 1/2 sec., 5 = 1 sec., 6 = 1 minute, 7 = 10 minutes)
H/S $\Rightarrow$ Hardware/Software STOP (0 = software (normal))
24 / $\overline{12}$ $\Rightarrow$ 12/24 hour system select (0 = 12 hour, 1 = 24 hour)
CAL $\Rightarrow$ Calendar (1 = calendar mode (R-S_1 to R-Y_{10} and R-W used), 0 = RAM mode (* bits, calendar registers, and alarm registers can be used as read/write memory))
D.P. $\Rightarrow$ Data Protect (1 = protected)

NOTES:
1) A counting error may occur if the clock is set out of range.
2) A module reset does not affect the value of the time-of-day registers.
3) The real-time and alarm registers are in BCD code.
4) Week digit (0 = Sunday, 1 = Monday, 2 = Tuesday, 3 = Wednesday, 4 = Thursday, 5 = Friday, 6 = Saturday)

Figure 8. Time-of-Day Registers

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4.0 OPERATING INSTRUCTIONS

4.1 GENERAL

The VX491C is configured and controlled through a series of hardware switches and jumpers and software controlled registers as described in Section 3. The switches and jumpers configure the logical address of the module, the input/output impedance of some of the signals, provide test functions, and allow disabling of the time-of-day battery backup. The software controlled registers provide configuration, control, and status of the majority of the features of the module.

4.2 CONFIGURATION

4.2.1 Hardware Configuration

Logical Address The logical address has a range of 0 to 255. Any value within this range is valid, but care should be taken not to set the logical address the same as another module in the system. Position 1 on the switch is the most significant bit and has a weighted value of 128 when the switch is in the off position. Position 8 on the switch is the least significant bit and has a weighted value of 1 when the switch is in the off position. The sum of the weighted values of all the switches in the off position is the module address. The VXI secondary address is the Logical Address divided by 8.

Trig In and External 10MHz Input Impedance The input impedance of the Trig In and External 10MHz front panel signals are separately configurable. With the jumper installed (default) the input impedance is 50Ω. Without the jumper installed, the impedance is >100KΩ. The maximum input voltage in either case is +5V.

Trig In Level The input threshold of the Trig In signal is selectable for 0V, TTL (default), or CMOS levels. Configure the jumpers as shown on the shield to the desired input threshold.

10MHz Output Options The output voltage level, impedance, quality, and frequency drift adjustment of the front panel 10MHz signal are configured using several jumpers and a potentiometer. The output impedance should be selected to closely match the load impedance. Overshoot and undershoot can be minimized by using the Optional Snubber circuit. The output voltage level can then be selected for your particular application using the Output Gain Adjust jumpers. See 3.2 for details.

Output Clock Select The standard 100KHz and 10KHz front panel output signals can be changed to programmable frequencies by changing the jumpers to the Fa and Fb positions. In these positions, the carry/borrow signal from counters 2 and 3, respectively, appear at the output connector. These counters can then be configured to output a pulse or square wave at the desired frequency. Note that in this configuration, the clock gate indicator still reflects the gating status of the 100KHz and 10KHz clocks, which may still be used internally.

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4.2.2 Software Configuration

All software controlled registers are 16-bits wide and may be accessed as D8(Even/Odd) or D16. However, special precautions must be followed if D8(EO) access is used. For instance, when processing interrupts, a pending interrupt is cleared when either the odd or even byte of an interrupt status word is accessed. This may cause some confusion when the even byte is accessed, since the interrupt pending bit is in the odd byte. Also, the Counter Count Latch latches the entire 32-bits of data when either the odd or even byte of the lower word is read; therefore, the count value would be re-latched when the second byte is read.

4.3 CLOCKS

Five clocks signals (10MHz, 100KHz/Fa, 10KHz/Fb, Fx, and Fy) are available for usage at the front panel of the module, as input to any of the six counters, or as output to any of the seven VXIbus TTL Trigger lines. The clocks are derived from either the on-board highly-stable oven controlled 10MHz oscillator, the VXI CLK10 signal, or an external clock input. The normal clock can be either the on-board ovenized oscillator (option -0001) or an external clock input. The backup clock can be either the VXI CLK10 signal or an external clock input The module switches over to the backup signal automatically, if the normal clock fails. It can also be switched manually using the Clock Control/Status register (08_{16}). Fx and Fy are derived by dividing the 10MHz signal by the values in the 32-bit Fx and Fy Divider registers ($20_{16}/22_{16}$ and $24_{16}/26_{16}$ respectfully). All clock signals, except for the 10MHz signal, are gated on or off using the Gate Control/Status register ($0A_{16}$). This gating applies to the signal available at the front panel and to the internal signal that can be channeled to the counters and VXIbus TTL Trigger lines.

4.4 COUNTERS

Six 32-bit binary up/down counters are available for general counting and timing functions. A specific counter is selected through the SEL bits in the Interrupt/Counter Select register (10_{16}). Each counter has a set of registers (12_{16}-$1E_{16}$) for general control, the preset value (the value loaded upon reset or roll-over), and the match value (the compare value used for interrupt generation). A read-only count latch register ($18_{16}/1A_{16}$) is provides on-the-fly reading of the count value.

4.4.1 Counting Functions

For general pulse counting functions, the counter should be configured in the count up mode with a pulse output and a preset value of zero. The pulse output mode should be used so that the counter will increments by one for positive transition of the input clock. In square-wave mode, the counter increments on each clock transition (positive and negative). Depending on the application, the counter can be configured to stop on carry (once-through mode) or continuing counting after a roll-over (free run mode). The count value can either be monitored using the Count Latch register ($18_{16}/1A_{16}$) or a Match Value ($1C_{16}/1E_{16}$) can be set and an interrupt generated when that value is reached. The input source of the counter is controlled using the

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Counter Input Map register ($28_{16}/2A_{16}$). The counter clocks on the leading edge of the input signal. For the active-low TTLTRG signals, this would be the falling edge.

To configure the counter, first disable the counter by setting the EC bit low in the Counter Control register (12_{16}). Set the desired preset value (normally 0 for counting functions) and the match value, then enable, reset, and configure the mode with a single write to the Control register.

4.4.2 Event Time Measurement

A special configuration of the counters allows a pair of counters to be used for event time measurement. Using the counter pair 0 and 1, configure the clock source of counter 0 to be the 10MHz clock for the highest resolution. Configure the external latch for counter 0 (the same bits that define the clock source for counter 1) to be the event to be measured. Configure counter 0 for square-wave output, to count up and latch on an external signal (EXTLAT). The EXTGATE signal is defined in bits 7-4 of the Counter Signal Input Map register ($2A_{16}$). Counter 0 will count up at a rate of 20Mhz (square-wave mode doubles the input clock frequency) providing a event time measurement resolution of 50ns. When two positive transitions of the external latch signal occur, the 32-bit count value is latched, the counter is reset, and subsequent latching is disabled. The LTD bit in the Counter Control/Status register (12_{16}) will go high after the two latches have occur, indicating that the measurement has completed. The latched value is then read by reading the lower word ($1A_{16}$) then the upper word (18_{16}) of the Count Latch registers. Latching is re-enabled by writing the LEX bit again. Counter pairs 2/3 and 4/5 can be used in the same way.

4.4.3 Timing Functions

For general timed pulse functions, the counter is configured in the count down mode with either a square wave or pulse output. With the counter in a free run mode, the carry/borrow output pulse at the input clock frequency divided by the preset value. The counter will yield the same frequency in square wave or pulse mode. The input source of the counter is controlled using the Counter Input Map register ($28_{16}/2A_{16}$). With the counter in once-through mode, a single delayed pulse can be created by enabling the to reset on an external signal. The external signal can be defined as the Trig In signal or the external gate signal (EXTGATE) with the counter reset control (CRC) bit in the Clock Control/Status register (08_{16}). The EXTGATE signal is defined in bits 7-4 of the Counter Signal Input Map register ($2A_{16}$).

To configure the counter, first disable the counter by setting the EC bit in the Control register low. Set the desired preset value and the match value (if an interrupt is desired on a specific value), then enable, reset, and configure the mode with a single write to the Control register.

4.5 VXI TTL TRIGGERS

Any of the carry/borrow outputs from the counters, any of the clocks, the front panel Trig In signal, or the adjacent TTL Trigger line can be output to a VXI TTL Trigger line. The VXI Trigger Output Source Map register ($2C_{16}/2E_{16}$) allows mapping of the various sources to the trigger lines.

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4.6 TIME-OF-DAY CLOCK

The time-of-day clock function is provided by a real-time clock module that incorporates a built-in crystal resonator. The internal registers of the module are accessed through the Time-of-Day Clock Interrupt ID/Port (TCIP) register ($0C_{16}$) and auxiliary functions are available in the TOD Control/Millisecond (TCM) register ($0E_{16}$). To read or write a specific register set the register address in the TCM register, then read/write the data in bits 0-3 of the TCIP register. If all registers require reading or writing, set the register address to 0 and set the auto increment (AI) bit to 1. The TOD register address will then increment automatically after each read or write. To protect the real-time clock from data corruption during power-on and power-off, the Data Protect bit in the time-of-day registers should always be set, except when configuring or setting the time or alarm. See Figure 8 for details of the time-of-day registers.

4.7 INTERRUPTS

An interrupt to the VXI host can be generated if the OCXO fails (clock switch-over interrupt), when a counter borrow/carry or match occurs, at a periodic time, and at a preset alarm time. The interrupt level is set using the Interrupt Level Select (ILVL) bits in the Interrupt/Counter Select register (10_{16}). All zeros in these bits will disable all interrupts. The interrupt level is common for all interrupts, however, the interrupt status/ID returned during an interrupt acknowledge cycle can be unique for clock switch-over interrupts, time-of-day (periodic/alarm) interrupts, and for each of counter (carry/borrow and match) interrupts. The interrupt vector returned during an interrupt acknowledge cycle consist of the modules logical address in the low byte and the programmed interrupt status/ID for the source of interrupt in the high byte.

Interrupts are released on register access (RORA). Each source of interrupt requires a specific register to be read to clear the pending interrupt. Additionally, a summary of all pending interrupts is provided in the Interrupt/Counter Select register (10_{16}). This is useful for servicing multiple interrupts during the same interrupt service routine.

Servicing alarm and periodic interrupt requires special attention to the IRQ FLAG bits as defined in Figure 8. The time-of-day function requires 122µs after an interrupt occurs before the interrupt can be cleared. The proper sequencing is to continuously read the IRQ $FLAG_0$ until it goes low. The interrupt pending flag should then be clear.

If both counter type interrupts (Match and Carry/Borrow (or Latch)) are enabled, it is difficult or impossible to determine which event caused the interrupt. Therefore, only one type of interrupt should be enabled for a given counter. Multiple counters with the same clock source may be used if both types of interrupts are required.

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4.8 BATTERY BACKUP

The battery backup function automatically occurs unless it is disabled before power is removed from the module. There are two methods available to disable battery backup. If the No Battery Backup jumper is accessible, simply short the pins together momentarily before removing power. If the jumper is not accessible, a software procedure is provided to perform the same disable function. To prevent accidental disabling, a timed sequence of operations is required as described below: All operation are performed to the TOD Control/Millisecond register (OE_{16}).

1. Read register to clear the MR bit
2. Poll register until MR = 1
3. Wait 0.5 seconds, then write NB = 1
4. Wait 1.0 seconds, then write NB = 0
5. Wait 1.0 seconds, then write NB = 1
6. Read register, if NB = 1 then no battery backup was successful.

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5.0 TROUBLE ANALYSIS

5.1 BUILT IN TEST AND DIAGNOSTICS

During power-up initialization, many of the on-board devices perform basic built-in test functions. If an initialization failure is detected, the SYSFAIL lamp will light indicating a failure. Additionally, all registers have a read-back capability that can be used to perform many test and diagnostic functions.

5.2 TROUBLE ANALYSIS GUIDE

The following is a general guide of the most common problems that may be encountered during programming of the module along with a suggestion of the possible causes.

SYMPTOMS	POSSIBLE CAUSES
Bus time out on A16 Access	1. Logical address incorrectly set. 2. Card incorrectly installed. 3. Faulty card.
Incorrect VXI ID or Device Type	1. Incorrectly addressed. 2. Faulty card.
Incorrect Time-of-Day	1. TOD clock module not initialized properly 2. TOD clock register is in alarm mode (bank 1) 3. Backup battery has expired (see reg. $0E_{16}$) 4. Data Protect not being used (see TOD bank 1 reg E)
Derived Frequencies (100KHz, 10KHz, Fx, Fy) not outputting correctly	1. Clock gate not enabled (see reg. $0A_{16}$) 2. Fx/Fy Dividers not set correctly (see reg. 20_{16} through 26_{16})
Counters not operating properly	1. Counter not properly selected (see reg. 10_{16}) 2. Counter not enabled or configured correctly (see reg. 12_{16})

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APPENDIX A - CONNECTORS

PIN	C	B	A
1	D08	-	D00
2	D09	-	D01
3	D10	-	D02
4	D11	BG0IN*	D03
5	D12	BG0OUT*	D04
6	D13	BG1IN*	D05
7	D14	BG10UT*	D06
8	D15	BG2IN*	D07
9	GND	BG20UT*	GND
10	-	BG3IN*	-
11	-	BG3OUT*	-
12	SYSRESET*	-	DS1*
13	LWORD*	-	DS0*
14	AM5	-	WRITE*
15	A23	-	-
16	A22	AM0	DTACK*
17	A21	AM1	_
18	A20	AM2	_
19	A19	AM3	_
20	A18	GND	IACK*
21	A17	-	IACKIN*
22	A16	-	IACKOUT*
23	A15	GND	AM4
24	A14	IRQ7*	A07
25	A13	IRQ6*	A06
26	A12	IRQ5*	A05
27	A11	IRQ4*	A04
28	A10	IRQ3*	A03
29	A09	IRQ2*	A02
30	A08	IRQ1*	A01
31	+12 V	-	-12 V
32	+5 V	+5 V	+5 V

Figure A-1. P1 Pin Configuration

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PIN	C	B	A
1	CLK10+	+5V	-
2	CLK10-	GND	-2V
3	GND	-	-
4	-5.2V	-	GND
5	-	-	-
6	-	-	-
7	GND	-	-
8	-	-	-
9	-	-	-
10	GND	-	GND
11	-	-	-
12	-	GND	-
13	-	+5V	-
14	-	-	-
15	-	-	-
16	GND	-	GND
17	-	-	-
18	-	-	-
19	-5.2V	-	-
20	-	-	-
21	-	-	-
22	GND	GND	GND
23	TTLTRG1*	-	TTLTRG0*
24	TTLTRG3*	-	TTLTRG2*
25	GND	-	+5
26	TTLTRG5*	-	TTLTRG4*
27	TTLTRG7*	-	TTLTRG6*
28	GND	-	GND
29	-	-	-
30	GND	-	MODID
31	-	GND	GND
32	-	+5V	-

Figure A-2. P2 Pin Configuration

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N O T E S

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