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Chrislin Industries, Inc.

CI-VME80
CI-VME64
CI-VME32

TECHNICAL MANUAL

HIGH-SPEED
VME64
VMEbus/VSB
DUAL-PORTED
DYNAMIC MEMORY

Release 2.4
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Chrislin Industries, Inc.
31312 Via Colinas, #108
Westlake Village, CA 91362

Tel: (818) 991-2254
Fax: (818) 991-3490
Sales: (800) 468-0736

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1. GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation and installation of the CI-VME80 dynamic memory module for the VSB and VMEbus.

1.2 THE MEMORY MODULE

The CI-VME80 is available in five option sizes as follows:

OPTION	MEMORY CAPACITY	MODULE
32 MEG	8,192Kx32 bits with parity	CI-VME80/32
64 MEG	16,384Kx32 bits with parity	CI-VME80/64
128 MEG	32,768Kx32 bits with parity	CI-VME80/128
256 MEG	65,536Kx32 bits with parity	CI-VME80/256
512 MEG	131,072Kx32 bits with parity	CI-VME80/512

1.3 CI-VME80 MEMORY DESCRIPTION

The CI-VME80 is a high-density, high-speed Block Transfer DRAM Memory board with a Dual-Port interface that allows memory cycles to be performed to both the VSB and VMEbus simultaneously. A VME64 databus allows data transfer rates up to 80 Megabytes/Second.

The CI-VME80 uses a Custom Chip Set developed by Chrislin. This Chip Set includes two 64 bit ALU's which can perform any of 32 different Arithmetic or Logical functions during VMEbus write cycles.

Byte Parity Error Detection circuitry is provided for data integrity. VME64, ANSI/VITA 1-1994 functionality is also provided.

The CI-VME64 has the same VMEbus features but lacks the VSB interface. The sections in this manual regarding the VSB should be ignored for this version of the board.

The CI-VME32 does not have a VSB interface and only has a D32 interface on the VMEbus.

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1.4 OPERATIONAL FEATURES

The CI-VME80 performs all memory functions according to VMEbus ANSI/VITA 1-1994 and the VSB REV C protocols for byte, word, and long word operations (8, 16, 24 and 32 bit data transfers). VME64 functionality is provided according to ANSI/VITA 1-1994 specifications.

Read-Modify Write cycles, Unaligned transfers, Block transfers, Address Pipelining, Locked Bus cycles and Address Only cycles are all supported.

Starting and Ending Address selection may be selected for each port (VMEbus and VSB) on One Megabyte boundaries.

A Control Status Register (CSR) is provided, and responds to 16bit SHORT IO Address modifiers. CSR functions include ERROR ENABLE, ERROR DETECT, and ENHANCED ACCESS MODE.

Block transfer cycles are highlighted as the CI-VME80's strongest feature. Block Cycles can be performed on 32 or 64 bit wide locations. Chrislin uses a proprietary cycle management system that delivers access and cycle times that are not available elsewhere in the industry.

Block Transfer lengths of up to 4 Kbytes may be performed on either bus. Transfers may not cross 4 Kbyte boundaries. The VMEbus master is responsible for ending a Block Transfer. The VSB master will be notified by the deassertion of AC during the last cycle.

Up to 512 Refresh Requests can be queued for extended or delayed Block Transfers. To provide the fastest possible Block Transfers, Refresh Requests are queued until the burst is complete. This allows burst durations of up to 8 milliseconds. All pending Refresh Requests will be executed in burst mode.

The On-Board ALU performs all of the 74LS181 type of ALU functions. The master writes a value to the memory board using one of the User Defined Address Modifiers to select an operation. The CI-VME80 then performs the operation to the selected address.

VSB Cycles are initiated on PAS to absorb the delay between PAS and DS. Refresh cycles are performed for PAS only cycles.

LED indicators for VMEbus CYCLE, VSB CYCLE, D64 CYCLE, ALU CYCLE (green) and Parity Error status (red) are mounted on the front panel.

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1.5 POWER REQUIREMENTS

The CI-VME80 memory module requires only the +5 volt supply from the VMEbus/VSB backplane. (See the general specifications for current requirements.)

1.6 GENERAL SPECIFICATIONS

CAPACITY:	32, 64, 128, 256, or 512 Megabytes		
CYCLE TIME:	95ns BLOCK CYCLE, 195ns SINGLE CYCLE		
ACCESS TIME WRITE/READ:	30/30ns BLOCK CYCLE, 90/140ns SINGLE CYCLE		
WORD SIZE:	8, 16, 24, 32 or 64 bits		
MEMORY ADDRESSING:	A32, 4 GB maximum. Selectable on 1MB boundaries		
CSR Addressing:	A16, selectable on 256 byte boundaries using VMEbus SHORT I/O		
Modes of Operation:	READ, WRITE, READ-MODIFY-WRITE,		
MEMORY	BLOCK TRANSFERS, UNALIGNED TRANSFERS		
CSR	READ, WRITE		
ANSI/VITA Compatibility:	SLAVE, A16, A32, D8, D16, D24, D32, D64, RMW, BLT, MLBT, UAT, AD0		
VSB Rev C Compatibility:	SLAVE, D32, A32, SAS, ATLAS, AD0, BLT(32)		
Address Modifiers:	Responds to AM Codes 3F, 3E, 3D, 3B, 3A, 39, 0F, 0E, 0D, 0B, 0A, 09, 2D, & AM Codes are programmable, ALU Cycles are selected with AM Codes 10-1F		
Refresh:	Internal, Distributed		
Parity/Error Handling:	Byte Parity		
Indicators:	RED - Parity Error, GREEN - VME, VSB, D64 & ALU cycles		
Designed Temperature Range:	Operating: 0deg. C to +70deg. C non-condensing		
Power Requirements:	TYPICAL	MAXIMUM	
+5 Volts	1.5A	2.6A	64MB Option
Dimensions:	160mm x 233.35mm, 6U form factor		

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1.7 SWITCHING CHARACTERISTICS

VMEbus Switching Characteristics

Parameter	Description	Min	Notes
SCRA	Single Cycle Read Access Time	180ns	1
SCWA	Single Cycle Write Access Time	90ns	1
SCDV	Single Cycle Data Valid Setup 10ns		
SCCT	Single Cycle Time	195ns	
AOT	Access Turn Off Time	30ns	
BCAT	Block Cycle Access Time	20ns	Enhanced Access Enable
BCAT	Block Cycle Access Time	>30ns	Enhanced Access Disabled
BCCT	Block Cycle Time	95ns	
BCDV	Block Cycle Data Valid Setup	10ns	

VSB Switching Characteristics

Parameter	Description	Min	Notes
SCRA	Single Cycle Read Access Time	20ns	2
SCWA	Single Cycle Write Access Time	50ns	2
SCDV	Single Cycle Data Valid setup	10ns	
SCCT	Single Cycle Time	195ns	
AOT	Access Turn Off Time	30ns	
BCAT	Block Cycle Access Time	30ns	
BCCT	Block Cycle Time	95ns	
BCDV	Block cycle Data Valid Setup	10ns	

Notes:

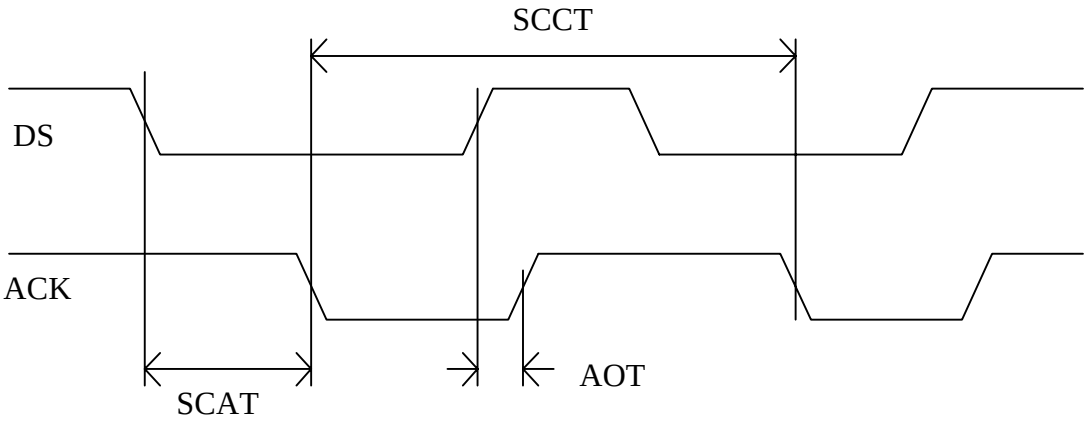
1. Access times are measured from data strobes and inside bus drivers and receivers.

2. VSB access times measured from data strobe given a PAS to DS delay of 130ns. Minimum access time from PAS is the same as that of the VMEbus.

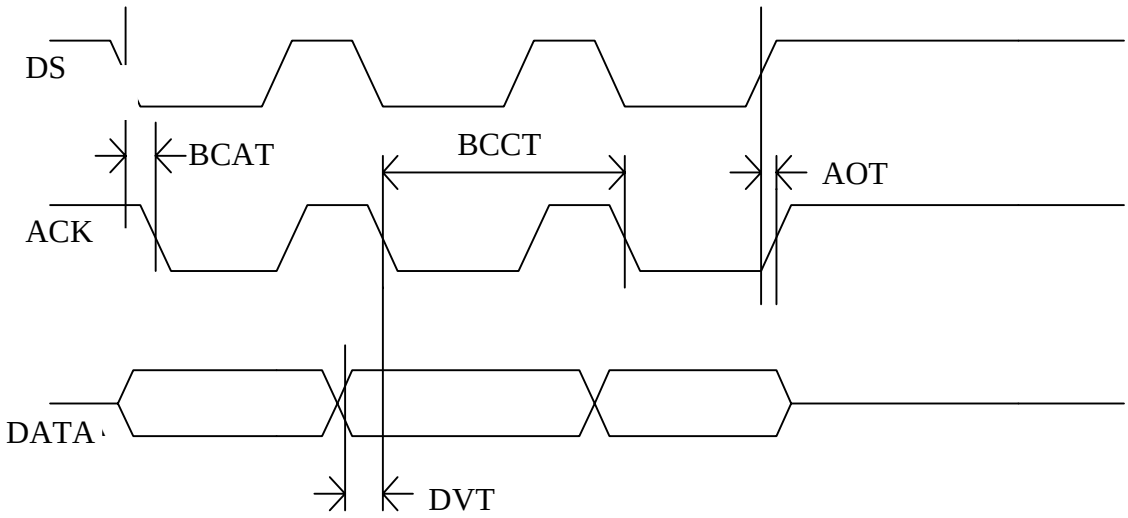
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ACCESS CYCLE TIMING

SINGLE TRANSFER CYCLE



BLOCK TRANSFER CYCLE



CHRISLIN

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2. HANDLING AND INSTALLATION

2.1 INTRODUCTION

This section describes the handling precautions and the procedure of installation of the CI-VME80 memory modules.

2.2 HANDLING PRECAUTIONS

The memory IC's on the CI-VME80 module are MOS devices. They are damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC's. Avoid unnecessary handling. When handling IC's wear cotton rather than synthetic clothing.

The CI-VME80 uses a Mezzanine Memory Array for added density. The Array does not need to be removed for board configuration. If the Array needs to be removed or installed, care needs to be taken not to damage the mating connector. Before applying pressure to seat the connector, examine that all pins are aligned.

2.3 MEMORY ADDRESS SELECTION

The CI-VME80 has an individually selectable START and END address with 1 mega-byte granularity. The VMEbus addresses may be selected independent from the VSB addresses. Refer to drawing 74052 for jumper positions.

Address sections are configured by representing the desired binary address in jumper selections. An installed jumper represents a '1' or HI on the bus where a removed jumper represents a "0" or LOW on the bus..

The address range for each bus is selected with a starting and ending address. Significant address bits used in the selection are A20 through A31 for each bus.

S20 - S31 VMEbus Start Address
E20 - E31 VMEbus End Address
J20 - J31 VSB Start Address
K20 - K31 VSB End Address

Refer to Table 2.3.1 for examples..

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2.3.1 STARTING AND ENDING ADDRESS EXAMPLES

S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	VME START ADDRESS
J31	J30	J29	J28	K27	J26	J25	J24	J23	J22	J21	J20	VSB START ADDRESS
O	O	O	O	O	O	O	O	O	O	O	O	00000000 (HEX)
O	O	O	O	O	O	O	O	O	O	O	O	00040000
O	O	O	O	O	O	O	O	O	O	O	O	00080000
O	O	O	O	O	O	O	O	O	O	O	I	00100000
O	O	O	O	O	O	O	O	O	O	I	O	00200000
O	O	O	O	O	O	O	O	O	I	O	O	00400000
O	O	O	O	O	O	O	O	I	O	O	O	00800000
O	O	O	O	O	O	O	I	O	O	O	O	01000000
O	O	O	O	O	O	I	O	O	O	O	O	02000000
O	O	O	O	O	O	I	I	O	O	O	O	03000000
O	O	O	O	O	O	O	O	O	O	O	O	START DEFAULT

E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	VME END ADDRESS
K31	K30	K29	K28	K27	K26	K25	K24	K23	K22	K21	K20	VSB END ADDRESS
O	O	O	O	O	O	O	O	O	O	O	O	0003FFFF (HEX)
O	O	O	O	O	O	O	O	O	O	O	O	0007FFFF
O	O	O	O	O	O	O	O	O	O	O	O	000FFFFF
O	O	O	O	O	O	O	O	O	O	O	I	001FFFFF
O	O	O	O	O	O	O	O	O	O	I	I	003FFFFF
O	O	O	O	O	O	O	O	O	I	I	I	007FFFFF
O	O	O	O	O	O	O	O	I	I	I	I	00FFFFFF
O	O	O	O	O	O	O	I	I	I	I	I	01FFFFFF
O	O	O	O	O	O	O	I	I	I	I	I	32MB END DEFAULT
O	O	O	O	O	O	I	I	I	I	I	I	64MB END DEFAULT

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2.4 24-BIT ADDRESS SYSTEMS

24 Bit address decoding is not supported with the CI-VME80. The board will respond to 24-Bit Address modifiers, but will decode address bits A20 through A31 for selection.

2.5 VMEbus ADDRESS MODIFIERS

The CI-VME80 may respond to different combinations of address widths and VMEbus address modifier codes. Shunt area D selects whether 32 bit only modifiers are to be responded to, or 32 or 24 bit modifiers will be responded to. See User Option Section.

The following table summarizes the AM codes that the CI-VME80 responds to:

3E, 3D 3A, 39, 0E, 0D, 0A, 09	Single Cycle Transfers
3F, 3B, 0F, 0B	32 Bit Block Transfers
3C, 38, 0C, 08	64 Bit MBLT Block Transfers
10, 11, 12, 13 14, 15, 16, 17 18, 19, 1A, 1B 1C, 1D, 1E, 1F	ALU Functions
2D, 29	16 Bit CSR Cycles

2.6 VSB ADDRESS SPACES

The CI-VME80 is configured to respond to VSB SYSTEMS ADDRESS SPACE. VSB ALTERNATE ADDRESS cycles can be configured by the factory.

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2.7 DUAL-PORT ADDRESS OVERLAPPING

Although each bus can be configured independently, the lower Bus addresses are used to address the memory array. This will cause certain addresses on one bus to access other addresses on another bus. Care must be taken when choosing bus addresses. For example a 4MB memory board is configured to respond to VMEbus addresses 100000h to 500000h and VSB address 0h to 400000h, the following overlap will exist:

VMEbus	VSB
400000 - 500000	000000 - 100000
100000 - 200000	100000 - 200000
200000 - 300000	200000 - 300000
300000 - 400000	300000 - 400000

Notice that the memory board has a 4MB redundancy. An 8MB board would similarly have an 8MB redundancy.

2.8 BUS INTERFACE DISABLE

If either the VMEbus or VSB Bus interface is to be disabled, simply set the starting address greater than the ending address.

2.9 CSR ADDRESS SELECTION

The CI-VME80 CSR is an 8 bit read/write register. The CSR is selected by a VMEbus 16 bit SHORT SUPERVISORY (2D) or SHORT NON-PRIVILEGED ACCESS (29) Address Modifier code. Address selection uses shunt areas I8 through I15 which places the CSR on 256 byte boundaries. Note that shunt labels correspond to address bits. An installed shunt represents a "0" or LOW on the bus where a removed shunt represents a "1" or HIGH on the bus. Refer to Table 2.9.1 for examples.

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2.9.1 CSR ADDRESS SELECTION EXAMPLES

I15	I14	I13	I12	I11	I10	I9	I8	ADDRESS
I	I	I	I	I	I	I	I	0000 - 00FF
I	I	I	I	I	I	I	O	0100 - 01FF
I	I	I	I	I	I	O	I	0200 - 02FF
I	I	I	I	I	O	I	I	0400 - 04FF
I	I	I	I	O	I	I	I	0800 - 08FF
I	I	I	O	I	I	I	I	1000 - 10FF
I	I	O	I	I	I	I	I	2000 - 20FF
I	O	I	I	I	I	I	I	4000 - 40FF
O	I	I	I	I	I	I	I	8000 - 80FF
O	O	O	O	O	O	O	O	FF00 - FFFF
I	I	I	I	I	I	I	I	DEFAULT CONFIGURATION

2.10 USER OPTIONS

The following USER OPTIONS are shunt selectable. Refer to drawing 74052 for shunt positions. The CSR (Control Status Register) is initialized to the shunt selections during /SYSRESET. The CSR configuration may then be changed by program control by writing to CSR bits D0-D3.

2.10.1 USER CONFIGURED SHUNT LOCATIONS

SHUNT AREA	POSITION	DESCRIPTION
A	IN	Error Disabled
A	OUT	Error Enabled
B	IN	Board Enable
B	OUT	Board Disable
C	IN	Standard ACK Time
C	OUT	Enhanced ACK Time
D	IN	Decode 24 bit AM Codes
D	OUT	Ignore 24 bit AM Codes
EE	IN	Standard ACK Drivers
EE	OUT	Receinding ACK

All other jumpers are Factory set and must not be modified by the user.

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2.11 ERROR ENABLE

Parity errors are always checked on any type of read cycle. The ERROR LED will light and stay lit whenever an error occurs. Error trapping is controlled by the user. Shunt area A is used to enable/disable error trapping. By installing the shunt at area A, DTACK/ACK will always be asserted in response to a valid memory cycle. Removing the shunt will allow BERR/ERR to be asserted whenever a parity error occurs.

Error trapping is set at /SYSRESET time according to shunt area A. The CSR can be used to change the initial setting. When CSR bit D2 of the first CSR is set to a '1' error trapping is enabled. Clearing this bit disables error trapping.

2.12 BOARD ENABLE

The memory board can be configured to be enabled or disabled at power up. Installing a shunt at area B enables the board, removing the shunt disables it. The board also can be enabled or disabled through software. By writing a '1' to D1 the board is enabled. Writing a '0' to this bit disables the board. This allows multiple boards to be placed at the same VME address and be individually enabled thus allowing more than 4 gigabytes to be placed in the system. Note that this feature does not effect the VSB selection of the board.

2.13 24/32 BIT VME ADDRESS SELECT

Area D selects whether the CI-VME80 will respond to only 32 bit Address modifiers or 24 bit and 32 bit modifiers. Note that the CI-VME80 decodes address bit A20-A31. If the CI-VME80 will be accessed by a 32 address bit master use the 32 bit configuration. If a 24 bit master will access the board, the 24/32 bit setting should be used. During an A24 cycle the upper address lines are decoded by the board. They must either be driven or pulled to some known state.

Some problems that have been noticed over the years is that some controller boards place buffer space in the 24 bit address modifier space. If the memory board is configured to respond to both 24 and 32, it may redundantly respond to the controllers address space.

If you need to place the CI-VME80 into 24 bit address space take care in setting up your bus addresses for all boards. If you are going to access the board with 32 bit address modifiers leave the shunt removed at area D.

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2.14 RESCINDING ACK

The CI-VME80 can be configured to drive the VSB ACK and VMEbus DTACK signals with either Open Collector or Tri-State drivers. The current Bus specifications define these drivers to be Open Collector. To optimize on MASTER/SLAVE hand-shaking, faster data rates can be obtained by having the SLAVE (CI-VME80) drive the ACK lines high instead of allowing bus terminators to pull the lines inactive from a Open Collector device. Installing a shunt at area EE selects the Open Collector Drivers. Removing the shunt selects the Rescinding ACK drivers. In the Rescinding mode, the first acknowledge is driven by the open collector device while the remaining cycles are driven by the tri-state device with the outputs enabled during the rest of the cycle.

The CSR can be used to change the initial setting. When CSR bit D3 of the first CSR is set to a '1' the Rescinding Drivers are selected. A '0" selects the Open Collector Drivers.

2.15 CONTROL / STATUS REGISTER

The CSR is accessible from the VMEbus side using Short IO Space Modifiers 29 and 2D hex with D16 cycles. The CSR can be used to control user selectable options and to check the status of the Error LED. When /SYSRESET is applied to the board, the CSR register is loaded with the configuration of the USER selectable jumpers.

Data Bit D4 selects one of two control registers. When writing data to the CSR, set bit D4 to '0' to select the first four controls. Setting to a '1' selects the remainder of the controls.

WRITE

D4	D3	D2	D1	D0
0	ACK TYPE	ERROR ENABLE	BOARD ENABLE	CARRY IN
1	S3	S2	S1	S0

READ

D4	D3	D2	D1	D0
0	ACK TYPE	ERROR ENABLE	BOARD ENABLE	ERROR DETECT

2.16 ERROR DETECT CSR BIT

The red LED will be lit and D0 of the CSR will be a '1' when a parity error has occurred. This bit is cleared when /SYSRESET is asserted or a write cycle to the CSR is performed. This is a read-only bit.

2.17 ACKNOWLEDGE TIME

With Shunt C removed, the board will return DTACK within 20ns. This is faster than the VMEbus Specification and may cause problems with some masters. Installing Shunt C will allow the board to return DTACK greater than 30ns.

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2.18 POWER-UP SELF INITIALIZATION.

Installing shunt "INIT" will configure the Memory Card to perform an initialization procedure each time power is applied to the board. This will clear all memory locations and initialize parity for each byte.

Power-Up Self Initialization takes approximately 6 seconds for any size board. The board will drive SYSFAIL during the power-up sequence to hold off bus activity. No memory accesses should be attempted until this sequence is complete. Please note that this is a special option and is installed at the factory.

3. OPERATION

3.1 THEORY OF OPERATION

The CI-VME80 performs 8, 16, 24, 32 or 64 bit data transfers as described in the VMEbus and VSB specifications. VMEbus Address selection for memory cycles is either 24 or 32 bits depending on the Address Modifiers presented. Address bits A20-A31 are decoded for each type of cycle. If A24 Address Modifiers are used, the user must insure that the upper address lines are terminated in a state that will select the board. User definable AM Codes are used to select ALU functions. Cycle types include READ, WRITE, READ-MODIFY-WRITE, BLOCK TRANSFERS, UN-ALIGNED TRANSFERS, ADDRESS ONLY and ADDRESS PIPELINING.

VSB address selections always uses 32 address bits and responds to the SYSTEM or ALTERNATE ADDRESS SPACE. Cycle types include READ, WRITE, LOCKED, BLOCK TRANSFERS, AND ADDRESS ONLY.

Refresh is internal and distributed. Refresh requests occur every 15 microseconds. PAS only cycles perform refresh cycles and could be used to control refresh cycles in special applications. Refresh Cycles have the highest priority in the arbitrator but are postponed during BLOCK TRANSFERS. This allows uninterrupted BLOCK TRANSFERS. Up to 512 Refresh cycles are queued during long Block Transfers. CAS before RAS Refresh cycles are implemented.

Since Block Transfers (BLT) are used for maximum data throughput, only 32 and 64 bit wide BLT transfers are supported.

BLT cycles use a proprietary Memory Management Scheme that allows the fastest possible cycle times on the VME and VSB busses. Data is available for the Master to read before the Master requests the data. DTACK/ACK is driven within 30 ns allowing the Master to digest the data and prepare for the next cycle. Note that this access time is the same for all cycles within a Block Burst. This allows synchronous cycles after the master receives the first acknowledge from the Memory. The Memory can keep up to a 10 MHZ rate at that point.

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The CI-VME80 does not use caching or interleaving methods that usually result in two different access times. Typically boards that use this method have a long access time for a normal cycle and a short access time for the cached or interleaved cycle. The CI-VME80 can perform back-to-back BLT cycles every 95ns.

Data is latched for both read and write cycles. The Chrislin Chip Set includes SWAP buffers that align 8, 16, and 32 bit data to the internal 64 bit data word. A synchronized four grant arbitration system is used. Arbitration priorities rank as follows: Refresh requests, VMEbus request (includes D64 cycles), VSB Requests and CSR requests. The VMEbus may lock out the VSB by performing READ-MODIFY-WRITE or BLOCK TRANSFER cycles. The VSB may lock out the VMEbus by asserting the LOCK signal and then perform any number of various VSB cycles or by performing BLOCK TRANSFER cycles.

Because of the programmable nature of the internal state machines, the CI-VME80 could easily be modified to respond in various MASTER/SLAVE environments. Chrislin supplies custom configurations for many customers. For example a synchronous block transfer protocol can be implemented.

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3.2 ALU Functions

A new concept in Memory design is the ability to perform various ALU functions during a VMEbus write cycle. This functionality has been implemented in the Chrislin ASIC Chip Set. A typical ALU cycle is where the master writes one of the operands to the memory. The previously stored data is used as the second operand. The result is stored back into the same memory location.

To access one of these functions one of two methods may be used. The first method determines the function to be executed by placing the User Defined Address Modifiers (as shown in the table below) during the write cycle. The second method allows the user to program the function via the Control Status Register. The second method allows the ALU to be used with standard off the shelf VMEbus masters. A CSR bit 'M' is used to select either Logical or Arithmetic Functions. A Carry-In bit 'C' is also set in the CSR and selects a second column in the function table. Carry-Outs are ignored and not stored. . The master must first set up the 'M' and 'C' bits in the CSR.

The following table summarizes the available functions. Note that BUS data is represented as A and previously stored MEMORY data is represented as B.

AM Code	M = H LOGIC Functions	M = L; ARITHMETIC OPERATIONS	
		Cn'=H (no Carry)	Cn'=L (with carry)
10	F=!A	F=A	F=A PLUS 1
11	F=!(A+B)	F=A+B	F=(A + B) PLUS 1
12	F=!AB	F=A+!B	F=(A + !B) PLUS 1
13	F = 0	F = MINUS 1(2's COMPL)	F = ZERO
14	F = !(AB)	F = A PLUS A!B	F = A PLUS A!B PLUS 1
15	F = !B	F = (A + B) PLUS A!B	F = (A + B) PLUS A!B PLUS 1
16	F=A@B	F=A MINUS B MINUS 1	F=A MINUS B
17	F = A!B	F = A!B MINUS 1	F = A!B
18	F=!A+B	F=A PLUS AB	F=A PLUS AB PLUS 1
19	F=!(A@B)	F=A PLUS B	F=A PLUS B PLUS 1
1A	F = B	F = (A + !B) PLUS AB	F = (A + !B) PLUS AB PLUS 1
1B	F = AB	F = AB MINUS 1	F = AB
1C	F=1	F = A PLUS A <	F=A PLUS A PLUS 1
1D	F=A + !B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
1E	F = A + B	F = (A + !B) PLUS A	F' = (A + !B) PLUS A PLUS 1
1F	F=A	F=A MINUS 1	F=A

< Shifted Left to the next most Significant position - M = M bit in the CSR register.

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3.3 Synchronous Block Transfers

The nature of the CI-VME80 allows synchronous block transfers. After the first handshake of a transfer is complete, the master may synchronously burst to or from the memory. This is an unsupported feature and is up to the user to insure proper operation.

A block transfer is normally initiated. A Data Strobe is issued and the master waits for the first Acknowledge is occur. This initial handshake must complete. The memory may be servicing the other DTB or may be performing a refresh cycle. This first Handshake indicates that the memory is now allocated to the transfer and no other event may interrupt it.

Data Strobe and Acknowledge are removed and at this point the synchronous transfer may begin. The master can then strobe the memory with Data Strobes without monitoring the Acknowledge line. A 100 ns maximum cycle rate must not be exceeded. A 60 ns DS time is suggested.

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4. INTERFACE PINOUTS

4.1 CI-VME80 P1 PIN ASSIGNMENTS

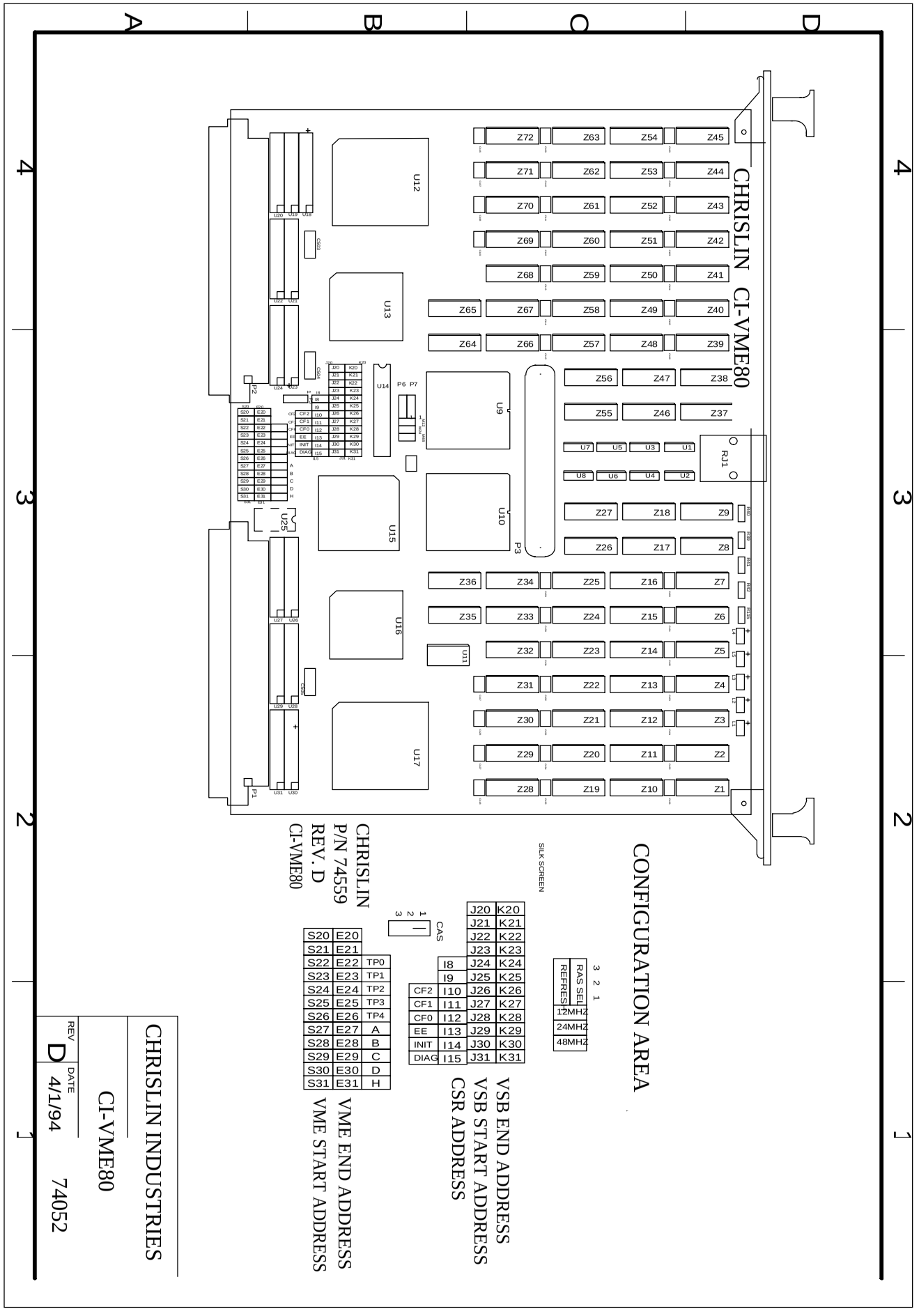
PIN	ROW A	ROW B	ROW C
1	D00	--	D08
2	D01	--	D09
3	D02	--	D10
4	D03	/BG0IN	D11
5	D04	/BG0OUT	D12
6	D05	/BG1IN	D13
7	D06	/BG1OUT	D14
8	D07	/BG2IN	D15
9	GND	/BG2OUT	GND
10	--	/BG3IN	--
11	GND	/BG3OUT	/BERR
12	/DS1	--	/SYSRESET
13	/DS0	--	/LWORD
14	/WRITE	--	AM5
15	GND	--	A23
16	/DTACKAM0	A22	
17	GND	AM1	A21
18	/AS	AM2	A20
19	GND	AM3	A19
20	/IACK	GND	A18
21	/IACKIN	--	A17
22	/IACKOUT	--	A16
23	AM4	GND	A15
24	A07	--	A14
25	A06	--	A13
26	A05	--	A12
27	A04	--	A11
28	A03	--	A10
29	A02	--	A09
30	A01	--	A08
31	--	+5VSTBY	--
32	+5V	+5V	+5V

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4.2 CI-VME80 P2 PIN ASSIGNMENTS

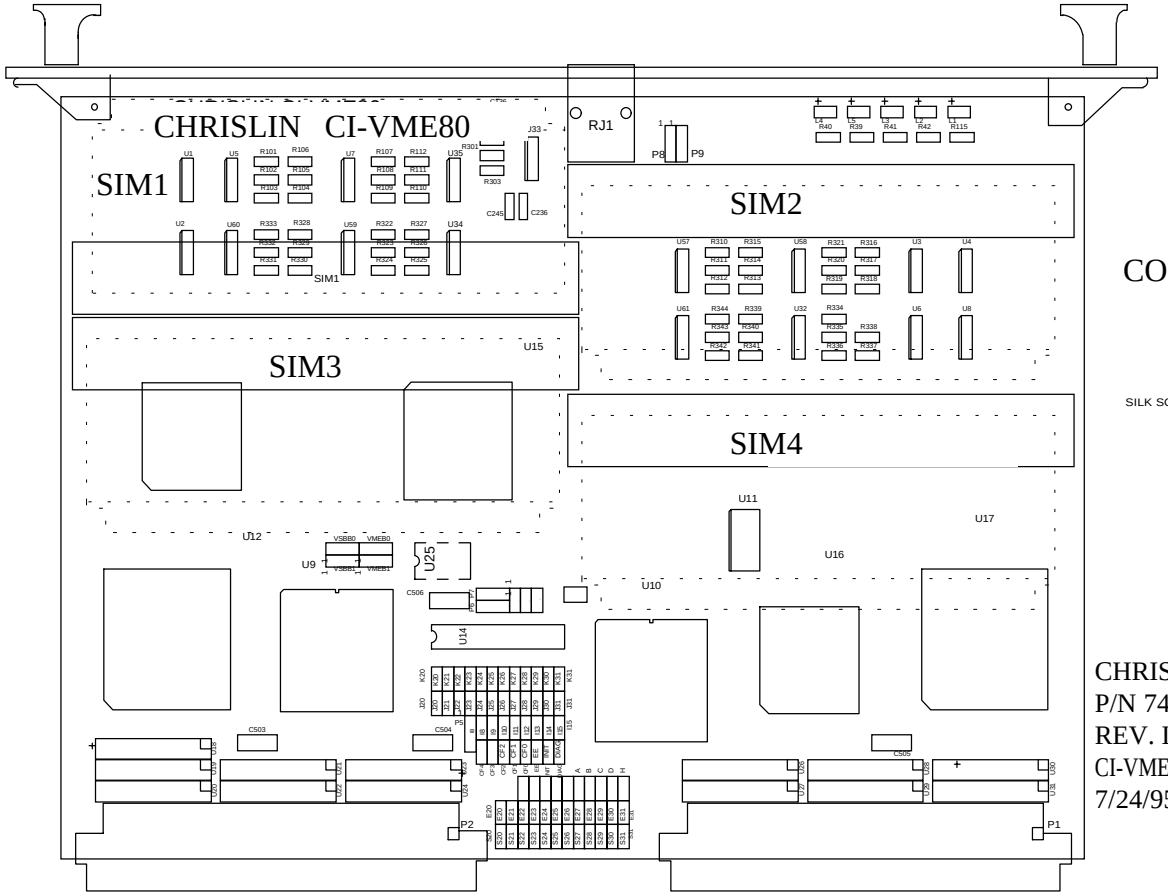
PIN	ROW A	ROW B	ROW C
1	VSBAD0	+5V	VSBAD1
2	VSBAD2	GND	VSBAD3
3	VSBAD4	--	VSBAD5
4	VSBAD6	A24	VSBAD7
5	VSBAD8	A25	VSBAD9
6	VSBAD10	A26	VSBAD11
7	VSBAD12	A27	VSBAD13
8	VSBAD14	A28	VSBD15
9	VSBAD16	A29	VSBAD17
10	VSBAD18	A30	VSBAD19
11	VSBAD20	A31	VSBAD21
12	VSBAD22	GND	VSBAD23
13	VSBAD24	+5V	VSBAD25
14	VSBAD26	D16	VSBAD27
15	VSBAD28	D17	VSBAD29
16	VSBAD30	D18	VSBAD31
17	GND	D19	GND
18	-	D20	GND
19	/DS	D21	GND
20	/WR	D22	GND
21	SPACE0	D23	SIZE0
22	SPACE1	GND	/PAS
23	/LOCK	D24	SIZE1
24	/ERR	D25	GND
25	GND	D26	/ACK
26	GND	D27	AC
27	GND	D28	/ASACK1
28	GA0	D29	/ASACK0
29	GA1	D30	/CACHE
30	GA2	D31	/WAIT
31	/BGIN	GND	-
32	-	+5V	/BGOUT

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CONFIGURATION AREA

3 2 1

RAS SEL	12MHz	24MHz	48MHz
REFRES			

SILK SCREEN

J20	J21	J22	J23	J24	J25	J26	J27	J28	J29	J30	J31
K20	K21	K22	K23	K24	K25	K26	K27	K28	K29	K30	K31

VSB END ADDRESS
VSB START ADDRESS
CSR ADDRESS

CAS

1
2
3

I8	I9	I10	I11	I12	I13	I14	I15	CF4	CF3	CF2	CF1	CF0	EE	INIT	DIAG

TP0	TP1	TP2	TP3	TP4	A	B	C	D	H		
E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30	E31
S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31

VME END ADDRESS
VME START ADDRESS

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CI-VME80

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